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Roll no.

II SEMESTER - B.Tech. (CSE/CSDS/CSA/IT/ITNS)

MID-SEMESTER EXAMINATION, May- 2023

Course Code- CAECC03/COECC03/CDECC03/ITECC01/INECC01
Course Title- Digital logic design/ Digital circuits and systems

Time- 1.5 Hours

Note: - All questions are compulsory.

Q. No.	Question.	Ma rks	CO
1	Convert the following: a. $(94CDE)_{16}$ to $(?)_2$ b. $(101010)_2$ to gray code c. 10110110 given signed 2's complement form into decimal form	3	CO ₁
2	a. If A and B are two binary nos. containing 2 bits each ($A = A_1A_0$, $B = B_1B_0$). Implement a 2 bit multiplier ($Y = A \cdot B$) using a 4 X 1 multiplexer. b. Realize a J K flip flop using a S-R flip flop.	1.5	CO ₂
3	a. Implement a full adder using a 3 X 8 complementary output decoder. b. Find a minimum product-of-sums expression for given function: $f(X, Y, W, Z) = \prod M(0, 2, 10, 11, 12, 14, 15) + \prod D(5, 7)$	1.5	CO ₂
4	a. The decimal digits 0 through 9 are represented using four bits A, B, C, D. The bits A, B, C, and D are the BCD representation of the decimal digit. The function $F(A, B, C, D)$ has value 1 if the decimal digit represented by A, B, C, D is divisible by either 2 or 3. (Zero is divisible by 2 and 3) Find all minimum sum of products for f using K-map. b. Implement the following function using universal gates only- $F(A, B, C) = \sum m(2, 4, 6, 7)$	1.5	CO ₂

5. a. What is race-round condition. How is it eliminated using a master-slave flip flop. Explain with help of suitable diagrams.

b. Solve using 2's complement (show all steps):

$$\begin{array}{r}
 (10101.101)_2 \\
 -(11000.011)_2 \\
 \hline
 (?)_2
 \end{array}$$

1

CO₃

3.	a. Write VHDL code of a J K flip flop using all three styles of coding. b. Write VHDL code of a 4 X 1 Multiplexer using behavioral style with conditional statements. c. Realize a 2-bit Magnitude comparator using any combinational circuit. Given that A and B are two binary nos. containing 2 bits each ($A=A_1A_0$, $B=B_1B_0$), Outputs are G= $A>B$, L= $A<B$, E= $A=B$.	4	CO ₂															
4	a. Design a MOD-5 counter using T flipflop which goes through the sequence as $000 \rightarrow 010 \rightarrow 011 \rightarrow 101 \rightarrow 111$. b. Implement a 4-bit Universal shift register using D flipflop which performs following action:	4	CO ₃															
	<table border="1"> <thead> <tr> <th>s0</th> <th>s1</th> <th>function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>hold state</td> </tr> <tr> <td>0</td> <td>1</td> <td>shift right</td> </tr> <tr> <td>1</td> <td>0</td> <td>shift left</td> </tr> <tr> <td>1</td> <td>1</td> <td>load new input</td> </tr> </tbody> </table> c. If there are 6 states a, b, c, d, e and f in an FSM. Show state assignment in binary code, gray code and one-hot encoding method.	s0	s1	function	0	0	hold state	0	1	shift right	1	0	shift left	1	1	load new input	4	
s0	s1	function																
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5.	a. Design a Mealy and Moore FSM to detect a sequence of '110'. Also mention present state, next state and output in each case. b. Realize a BCD to seven segment display using a suitable size of decoder. c. Briefly explain (any two): <ul style="list-style-type: none"> i) <u>A/D and D/A converter</u> ii) <u>Datapath in computers</u> iii) RAM and ROM 	4	CO ₅															

END-SEMESTER EXAMINATION, July- 2023

Course Code- CAECC03/COECC03/CDECC03/ITECC01/INECC01

Course Title- Digital logic design/ Digital circuits and systems

Time- 3 Hours

Max. Marks- 40

Q. No	Question	M ar ks	CO
Attempt any two parts of each question. Each question has equal marks.			
1	<p>a. Implement the following function using most suitable size of PLA.</p> $F_1(A, B, C) = \sum m(1, 2, 3, 7)$ $F_2(A, B, C) = \sum m(0, 1, 2, 6)$	4	CO ₁
	<p>b. Design a three-input, one-output minimal two-level gate combinational circuit that has a logic-1 output 1 when the majority of its inputs are logic-1 and has a logic-0 output when the majority of its inputs are logic-0.</p>	4	
	<p>c. Using the Quine-McCluskey method, obtain all the prime implicants.</p> $f_1(w, x, y, z) = \sum m(0, 2, 3, 4, 8, 10, 12, 13, 14)$	4	
2	<p>a. Implement NAND and NOR logic operation using CMOS logic family. Briefly Explain.</p>	4	CO ₄
	<p>b. A standard TTL NAND gate uses supply voltage V_{CC} of <u>5V</u> with average rising and falling propagation delay of <u>10 n sec</u> each and has current drains $I_{CH} = 2$ mA and $I_{CL} = 5$ mA. Find average power dissipation and find figure of merit.</p>	4	
	<p>c. Convert each of the following binary number into its equivalent in the octal and hexadecimal number systems.</p> <ol style="list-style-type: none"> 101001.010 111001011 	4	