List of publications

1. Aneesh, Y.M. and Bindu, B., 2020. A Physics-based Single Event Transient Pulse Width Model for CMOS VLSI Circuits. *IEEE Transactions on Device and Materials Reliability*.
2. Pappiah, M. and Boby, B., 2020. Capacitor-less FVF low drop-out regulator with active feed-forward compensation and efficient slew-rate enhancer circuit. *IET Circuits, Devices & Systems*, *14*(6), pp.853-859.
3. Manikandan, P. and Bindu, B., 2020. Dual-summed flipped voltage follower LDO regulator with active feed-forward compensation. *AEU-International Journal of Electronics and Communications*, *123*, p.153314.
4. Pasupathy, K.R. and Bindu, B., 2020. Sensitivity of SET Pulse-Width and Propagation to Radiation Track Parameters in CMOS Inverter Chain. *IETE Journal of Research*, pp.1-9.
5. Manikandan, P. and Bindu, B., 2020. A Cap-less Voltage Spike Detection and Correction Circuit for Low Dropout Regulator. *Journal of Circuits, Systems and Computers*, p.2020009.
6. Sriram, S.R. and Bindu, B., 2020. A physics-based model for LER-induced threshold voltage variations in double-gate MOSFET. *Journal of Computational Electronics*, pp.1-9.
7. Manikandan, P. and Bindu, B., 2020. High-PSR Capacitorless LDO with Adaptive Circuit for Varying Loads. *Journal of Circuits, Systems and Computers*, p.2050178.
8. Aneesh, Y.M., Sriram, S.R., Pasupathy, K.R. and Bindu, B., 2019. An Analytical Model of Single-Event Transients in Double-Gate MOSFET for Circuit Simulation. *IEEE Transactions on Electron Devices*, *66*(9), pp.3710-3717.
9. Sriram, S.R. and Bindu, B., 2019. Analytical modeling of random discrete traps induced threshold voltage fluctuations in double-gate MOSFET with HfO2/SiO2 gate dielectric stack. *Microelectronics Reliability*, *99*, pp.87-95.
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11. Sriram, S.R. and Bindu, B., 2019. Analytical Model for RDF-Induced Threshold Voltage Fluctuations in Double-Gate MOSFET. *IEEE Transactions on Device and Materials Reliability*, *19*(2), pp.370-377.

12. Sriram, S.R. and Bindu, B., 2019. A physics-based 3-D potential and threshold voltage model for undoped triple-gate FinFET with interface trapped charges. *Journal of Computational Electronics*, *18*(1), pp.37-45.

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15. Sriram, S.R. and Bindu, B., 2018, December. Study of Line Edge Roughness Induced Threshold Voltage Fluctuations in Double-Gate MOSFET. In *2018 15th IEEE India Council International Conference (INDICON)* (pp. 1-5). IEEE.

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