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Area of Interest : VLSI design and testing, Low power VLSI and VLSI architectures.

Publications

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2. Kumar, P.A., Anita, J.P., “Implementation of hybrid LBIST mechanism in digital circuits for test pattern generation and test time reduction”, Proceedings of the International Conference on Communication and Electronics Systems, pp. 243-248, 2020.
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7. Madhumitha, S., Sudheesh, P., Anita, J.P, “ Online state and parameter estimation of ultra capacitor using marginalized kalman filter”, Proceedings of the International Conference on Intelligent Computing and Control Systems, pp. 167-174, 2019.
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15. Abhiram, T., Ashwin, T., Sivaprasad, B., Aakash, S., Anita, J.P “Modified carry select adder for power and area reduction”, Proc. International Conference on Circuit, Power and Computing Technologies, 2017.
16. Anju Asokan and J.P. Anita “Multistage test data compression technique for VLSI circuits” , Proc. International conference on Advanced Communication Control and Computing Technologies, pp. 65-68, 2016.
17. Annu Roy and J.P. Anita, “Pattern Generation and Test Compression using PRESTO Generator” in Communications in Computer and Information Science, Vol. 746, Springer- Verlag, Berlin Heidelberg, pp 276-285, 2017.
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19. Ramnarayan, J., Anita, J.P., Sudheesh, P.,”Estimation and Tracking of a Ballistic Target Using Sequential Importance Sampling Method”, Communications in Computer and Information Science, Vol. 746, pp. 387 -398, 2017.
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