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## Publication Details

1. Deepa, A., & Marimuthu, C. N. (2020, July). VLSI Design of a Squaring Architecture based on Yavadunam Sutra of Vedic Mathematics. In *2020 International Conference on Electronics and Sustainable Communication Systems (ICESC)* (pp. 1162-1167). IEEE.
2. Deepa, A., Marimuthu, C. N., & Murugesan, C. (2020, January). An efficient high speed squaring and multiplier architecture using yavadunam sutra and bit reduction technique. In *Journal of Physics: Conference Series* (Vol. 1432, No. 1, p. 012080). IOP Publishing.
3. C Murugesan & CN Marimuthu, (2019). Cost optimization of PV-diesel systems in nanogrid using LJ cuckoo search and its application in mobile towers. *Mobile Networks and Applications*, 24(2), 340-349.
4. L Vigneash & CN Marimuthu. (2019). Optimization of motion estimation hardware using charged system optimization with low power multipliers for H. 264 encoders. *Cluster Computing*, 22(5), 10669-10677.
5. Deepa, A., & Marimuthu, C. N. (2019). Design of high speed Vedic Multiplier and square architecture based on Yavadunam sutra. *Sadhana*, 44(9), 197.
6. Deepa, A., & Marimuthu, C. N. (2018). High speed VLSI architecture for squaring binary numbers using Yavadunam sutra and bit reduction technique. *International Journal of Applied Engineering Research*, 13(6), 4471-4474.
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8. Maheswari, R. U., & Marimuthu, C. N. (2018). A Hybrid Low Power Fast Full Adder Using XOR And XNOR Gates. *International Journal of Recent Advances in science and technology*, 5(3), 64-68.
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12. Kumar, N. S., Deepa, S., Marimuthu, C. N., Eswari, T., & Lavanya, S. (2016). Signature based vulnerability detection over wireless sensor network for reliable data transmission. *Wireless Personal Communications*, 87(2), 431-442.
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14. Vigneash, L., & Marimuthu, C. N. (2016). Implementation of Power Reduction Adder with High Recital Multiplier. *Asian Journal of Research in Social Sciences and Humanities*, 6(8), 898-907.

15. Devi, A. R., Scholar, P. G., Erode, T., & Marimuthu, I. D. C. (2016). Intelligent Vehicle Control System Using Shared Steering Control Mechanism. *Journal of Network Communications and Emerging Technologies (JNCET)* [www.jncet.org](http://www.jncet.org), 6(4).
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