Dr. R. Udaiyakumar, M.E, Ph.D.,
Professor & Head, Department of ECE
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Professional Summary

- Having 17+ years of Experience in the area of Microelectronics and VLSI design as Design Engineer and as Senior Faculty at PG level National and International Institutions across the country.
- Involved in various Project and IP core developments in the area of VLSI.
- Held responsibility as Technical Consultant for E-Saplings consultants, Pune.
- Trained at Cadence Design Systems India (P) Ltd., Bangalore with Cadence IUS and SOC Encounter
- Taught advanced job oriented VLSI courses like ASIC Design, Low Power VLSI Design, Analog CMOS IC Design to Post Graduate engineering students.
- Presented & Published 7 papers in refereed international journals and 14 Papers at various National & International Conferences.
- Completed PhD [Information and Communication Engineering] in Low Power VLSI Design area under Anna University, Chennai (March 2014)
- Passed M.E [First Class with Distinction-80%] Applied Electronics Specialization from BIT-Sathyamangalam, Anna University, Chennai (April 2006).
- Passed B.E [First Class-70%] Electrical and Electronics Engineering from Thiagarajar College of Engineering (Autonomous), Madurai Kamaraj University, Madurai (April 1997).

Professional Experience (17+ Years)

Duration - 04.06.2007 to till date

Name of Organization : Sri Krishna College of Technology, Coimbatore
Present Position : Professor & HoD
Department : Electronics and Communication Engineering
Additional Responsibilities

- working as HoD of Electronics and Communication Engineering from 12.06.2008 to till date
- Successfully carried out NBA accreditation works of Department of ECE for two times consecutively (2008 & 2013) as HoD
- Successfully carried out UGC autonomous status Preparation works of Department of ECE and acquired autonomous status during 2010 as HoD
- Successfully carried out Department level NAAC accreditation works and obtained 'A' grade as HoD

- Chairman, Board of Studies for ECE at SKCT
- Member, Academic Council of SKCT, Coimbatore
- Member, Governing Body of SKCT, Coimbatore

Duration - 26.07.2006 to 23.05.2007

Name of Organization : I2IT Pvt. Ltd., Pune (IIIT Pune)
Present Position : Senior Lecturer
Department : Microelectronics and VLSI
Additional Responsibilities
- worked as Technical consultant for E-saplings, Pune

Duration - 05.02.2003 to 18.08.2004

Name of Organization : Radha Govind Engineering College, Meerut
Present Position : Senior Lecturer
Department : Electronics and Communication Engineering

Duration - 11.08.2000 to 01.02.2003

Name of Organization : S.R.M Engineering College, Chennai
Present Position : Lecturer
Department : Computer Science and Engineering, Electronics and Communication Engineering
Additional Responsibilities
- Commissioned VLSI Lab in Computer Science and Engineering department and offered VDesign certified training Programme on "VLSI Design using VHDL".

Duration - 16.04.1997 to 10.08.2000

Name of Organization : VDesign Pvt. Ltd., Pondicherry
Present Position : Design Engineer (Front End)
Department : IP Cores development for FPGA design using VHDL

Professional Membership : IEEE, ISTE

Key Skills : Front End VLSI design using VHDL & Back End ASIC Design

Skill Set
Front End VLSI Design

Digital Domain — Simulation:
Modelsim 5.8C [Mentor Graphics] Active HDL [Aldec], Incisive Simulator, Native

	Compiler [Cadence] Synthesizing : Leonardo Spectrum Level3 [Mentor Graphics] FPGA Express [Synopsys], RTL Compiler [Cadence] Programmable ASIC: Xilinx Spartan and Virtex Series
Back End VLSI Design	Analog and Mixed: Tanner's S-Edit, L-Edit and T-SPICE PRO, LASI-6 Signal Design ICFB Platform with Virtuoso, Spectre and Assura[Cadence Design System]-Schematic to GDS-II Technology: CMOS 16 Nanometer - SOI
Area of Interest	Digital CMOS VLSI Design CMOS Analog Integrated Circuit Design Low Power VLSI Design ASIC Design Computer Aided Design of VLSI Circuits & Design for Testability Cryptography
Research Interests	Hardware architectures and implementations of cryptographic algorithms. Reconfigurable Computing for HPC Low Power Digital VLSI design

Publication in Journals

1. R.Udaiyakumar, K. Sankaranarayanan and M.Valarmathy," Study on Leakage Power Reduction Techniques and its Impact on 16nm CMOS Circuits", IJCRR Volume 4 Feb 2012.
2. R.Udaiyakumar, K. Sankaranarayanan, "Dual Threshold Transistor Stacking (DTTS) - A Novel Technique for Static Power Reduction in Nanoscale CMOS Circuits:, European Journal of scientific research, ISSN 1450-216X Vol.72 No.2 (2012), pp. 184-194
3. R. Udaiyakumar, K. Sankaranarayanan, Certain Investigations on Static Power Dissipation in various Nano-Scale CMOS D Flip-Flop Structures, International Journal of Engineering and Technology Volume 2 No. 4, April, 2012
4. R.Udaiyakumar, Y. Hamsavarthini and V. Kavitha, "Static power analysis of 32nm CMOS NAND gate using active and standby leakage current reduction

techniques", Bonfring International Journal of power systems and integrated circuits, vol2, special issue 1, part3, February 2012.

5. R.Udaiyakumar, K. Sankaranarayanan, "Stacked Sleepy Super Cutoff CMOS (SS-CMOS) – A novel power gating leakage reduction technique for nanoscale CMOS circuits", Archives Des Sciences, VOl.65, No.11, November 2012.
6. Shilpa. B, Udaiyakumar.R, and Sankaranarayanan K., "Area, Power, Delay performances of logic element using various architectures" International journal of Engineering science Invention. Volume 2, Issue 3, pp 36-44 march 2013.
7. Anbarasu W, Udaiyakumar.R, "Studying impact of leakage current reduction techniques on different D Flip-flop architectures", International Journal of Advancements in Research & Technology , Vol. 2 , Issue 5, pp, 5-9 ,May 2013

International Conference

1. R.Udaiyakumar, K. Sankaranarayanan, "Self-Clock-Gating scheme for Modified Basic Logic Element Architecture", 2014 International Conference on Computer Communication and Informatics (ICCCI -2014), Jan. 03 – 05, 2014, Coimbatore, India, 978-1-4799-2352-6/14/ 2014 IEEE (Paper accepted for publication)

National Conferences

1. R.Udaiyakumar and K. Rekha, "Advanced encryption standard implementation on FPGA", National conference on innovations in electrical, electronics and control systems", Kumaraguru college of Technology, Coimbatore, March 2011.
2. R.Udaiyakumar and Nasser Husain.R, "Transistor level design of low power floating point arithmetic unit", National conference on Emerging trends in computer communication and informatics", ETCCI, at Tamilnadu college of Engineering, co-sponsored by CIIT international Journal March 2011.
3. R.Udaiyakumar and M.Valarmathy, "Leakage current reduction in deep submicrometer CMOS circuits", National conference on Innovation in communication and computing", SNS college of Technology, March 2011.
4. R.Udaiyakumar and M. Nithyajeevi, "BIST architecture using orthogonal code convolution for device under test", National conference on Emerging trends in computer communication and informatics", ETCCI, at Tamilnadu college of Engineering, co-sponsored by CIIT international Journal March 2011