

Dr.S. Sivanantham,
Associate Professor,
Electronics and Communication Engineering,
VIT,Vellore
Mobile : 9894432359
Email ID : ssivanantham@vit.ac.in

1. S Sivanantham, N Nitin Paul, R Suraj Iyer,” Object tracking algorithm implementation for security applications”, Far East Journal of Electronics and Communications,Volume 16, Issue 1,2016.
2. J Jean Jenifer Nesam, Sivanantham Sathasivam, “An efficient single precision floating point multiplier architecture based on classical recoding algorithm” , Indian Journal of Science and Technology, Volume 9,Issue 5,Pages 1-7,2016.
3. Sivanantham Sathasivam, S Khaja Rahamathulla, Implementation of HDB3 Encoder Chip Design” , Indian Journal of Science and Technology, Volume 9, Issue 5, Pages 1-4,2016.
4. Philip C Jose, S Karthikeyan, K Batri, S Sivanantham, “ An Efficient Algorithm for Tracing Minimum Leakage Current Vector in Deep-Sub Micron Circuits”, Advanced Computing and Communication Technologies, Pages :59-69,2016.
5. Dipankar Narendra Arya, KLV Sivanji, Raghunadha Reddy, S Sivanantham, K Sivasankaran, “A face detection system implemented on FPGA based on RCT colour segmentation”, 2016 Online International Conference on Green Engineering and Technologies (IC-GET),Pages 1-5,2016.
6. K Thilagavathi, S Sivanantham, “An Efficient Technique to Reduce Average and Peak Power in Scan Based BIST”, Indian Journal of Science and Technology,Volume 9, Issue 38, 2016
7. C Prayline Rajabai, S Sivanantham, “A Study on Vision Based Fall Detection for Automated Geriatric Care”, RESEARCH JOURNAL OF PHARMACEUTICAL BIOLOGICAL AND CHEMICAL SCIENCES, volume 7,Issue 4, pages :439-445,2016

8. Sivanantham Sathasivam, G Venu Reddy, "ASIC Implementation of High throughput FFT Processor for Scientific Applications", Indian Journal of Science and Technology, volume 9, Pages 5,2016
9. Sivanantham Sathasivam, Shah Jay Dilipbhai, Bhatt Anand Jitendrabha, Subhajit Sinha, "Implementation of Distributed Arithmetic Based Reconfigurable FIR Digital Filter", Asian Journal of Scientific Research, Volume 9, Issue 1, Pages 34, 2016
10. Chukka Santosh, C Prayline Rajabai, S Sivanantham, "A SAD architecture for variable block size motion estimation in H. 264 video coding",Pages 1-5,2017.
11. S Sivanantham, T Tresa, "Built-in self-test methodology for system-on-a-chip testing" , IEEE, 2017
12. K Mohanaprasad, Arunprakash Jayaprakash, Sivanantham Sathasivam, "Optimized-Fuzzy-Logic-Based Bit Loading Algorithms", Handbook of Research on Fuzzy and Rough Set Theory in Organizational Decision Making, Pages 305-315,2017.
13. J Jean Jenifer Nesam, S Sivanantham, " An area-efficient 32-bit floating point multiplier using hybrid GPPs addition", 2017 International conference on Microelectronic Devices, Circuits and Systems (ICMDCS),2017.
14. Vajrala Anil Reddy, C Prayline Rajabai, S Sivanantham, "Hardware implementation for the 32×32 IDCT of High-Efficiency Video Coding", Asian Journal of Applied Science and Technology,Volume 1, Pages 127-130,2017.
15. K Thilagavathi, S Sivanantham, "Two-stage low power test data compression for digital VLSI circuits" , Computers & Electrical Engineering, Volume 71, Pages 309-320,2018.
16. E Renold Sam Vethamuthu, S Sivanantham, R Sakthivel, "Implementation of Hierarchical DFT Approach for Better Testability", 2018 International Conference on Emerging Trends and Innovations In Engineering And Technological Research (ICETIETR),Pages 1-4,2018.
17. C Prayline Rajabai, J Harish, S Sivanantham, " Hardware Implementation of Diamond Search Algorithm for Motion Estimation", International Journal of Engineering & Technology, Volume 7, Issue 4.10, Pages 1075-1078,2018.
18. S Sivanantham, "High-throughput deblocking filter architecture using quad parallel edge filter for H. 264 video coding systems ", IEEE Access,Volume 7,Pages: 99642-99650,2019

19. Prayline Rajabai Christopher, Sivanantham Sathasivam, "Five-stage pipelined dual-edge deblocking filter architecture for H. 265 video codec", IEICE Electronics Express, 2019
20. Thilagavathi Karunamurthy, Satyapriya Dey, Renuka Pooja, Sivanantham Sathasivam, "Accumulator based BIST using Approximate Adders", Journal of Electrical and Electronics Engineering, Volume 12, Issue 1, Pages 21-26, 2019
21. Thilagavathi KARUNAMURTHY, Sivanantham SATHASIVAM, "Temperature-Aware X-filling for Very Large Scale Integrated Circuits." Gazi University Journal of Science, Volume 32, Issue 2, 2019
22. Sivanantham S SATHASIVAM, Jean Jenifer Nesam JEYAKUMAR, "Low-Error Reconfigurable Fixed-Width Multiplier for Image Processing Applications" , Volume 33, Issue 1, Pages 90-104, 2019.
23. J Jean Jenifer Nesam, S Sivanantham, "Efficient half-precision floating point multiplier targeting color space conversion" , Multimedia Tools and Applications, Volume 79, issue 1-2, Pages 89-117, 2020
24. Manisha Vinta, S Sivanantham, "Modeling and Test Generation for Combinational Hardware Trojans" , 2020 IEEE International Test Conference India, Pages 1-4, 2020
25. Jean Jenifer Nesam JEYAKUMAR, Sivanantham SATHASIVAM, "Low-Error Reconfigurable Fixed-Width Multiplier for Image Processing Applications." , Gazi University Journal of Science, Volume 33, Issue 1, 2020.
26. V Thanikaiselvan, Sakshi Patel, S Sivanantham, "Secured Data Transmission through Dual Domain Reversible Data Hiding and Encryption in Images" , 2020 International Conference on Inventive Computation Technologies (ICICT), Pages 840-847, 2020.
27. C Prayline Rajabai, S Sivanantham, "Analysis of hardware implementations of deblocking filter for video codecs" , International Journal of Materials and Product Technology, Volume 60, Issue 2-4, pages 214-235, 2020
28. J Jean Jenifer Nesam, S Sivanantham, "Reconfigurable half-precision floating-point real/complex fused multiply and add unit", International Journal of Materials and Product Technology, Volume 60, Issue 1, Pages 58-72, 2020.