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# List of journals

1. Adaptation of counters redundant bits with the provision of dual supply and modified clock gating to favour of low power in VLSI, M Sulaiman, B Jaison, A Bennet, D Vaithiyanathan Indian Journal of Pure & Applied Physics (IJPAP) 58 (10), 750-757

2. A Review on Additive Manufactured Sensors, H Choudhary, D Vaithiyanathan, H Kumar, MAPAN, 1-18

3. Synchrosqueezing Transform Based Powerline Interference Reduction in ECG Recording, MS Kumar, G Krishnamoorthy, D Vaithiyanathan, Journal of Medical Imaging and Health Informatics 10 (10), 2259–2273

4. Decisive structures for multirate FIR filter incorporating retiming and pipelining schemes, K Mariammal, M Hajira Banu, J Britto Pari, D Vaithiyanathan, Circuit World

5. Multiple Bandwidth FIR Filter Design with Adaptive Algorithms for Hearing Aid Systems, K Mariammal, R Sherin Mary, J Brittopari, D Vaithiyanathan, Indian Journal of Pure & Applied Physics (IJPAP) 58 (8), 605-623

6. Performance analysis of multi-scaling voltage level shifter for low-power applications, D Vaithiyanathan, MS Kurmi, AK Mishra, B Pari J, World Journal of Engineering

7. Performance Analysis of Channel and Inner Gate Engineered GAA Nanowire FET, Ashima, D Vaithiyanathan, B Raj, Silicon, 1-7

8. Energy efficient decision fusion for differential space-time block codes in wireless sensor networks, M Kanthimathi, R Amutha, D Vaithiyanathan, S Somesh Sharma, Indian Journal of Pure & Applied Physics (IJPAP) 58 (3), 147-156

9. Relationship between qualitative physics and fuzzy logic in natural subsystems P Gunasekaran, D Vaithiyanathan, M Ganesan, Indian Journal of Pure & Applied Physics (IJPAP) 58 (1), 44-49

10. Performance analysis of dynamic CMOS circuit based on node-discharger and twist-connected transistors, D Vaithiyanathan, R Kumar, A Rai, K Sharma, IET Computers & Digital Techniques 14 (3), 107-113

11. Simulation of the process variation in negative capacitance virtual-source carbon nanotube FET devices and circuits, BR Muthu, EPP Solomon, V Dhandapani, NISCAIR-CSIR, India

12. An adaptive denoising approach to powerline interference reduction in ECG recording, MS Kumar, G Krishnamoorthy, D Vaithiyanathan,NISCAIR-CSIR, India

13. Design and development of an additive manufactured force transducer, H Choudhary, D Vaithiyanathan, AP Singh, AJ Sheoran, H Kumar, NISCAIR-CSIR, India

14. An optimized MAC based architecture for adaptive digital filter, BP James, V Dhandapani, K Mariammal, NISCAIR-CSIR, India

15. Brain wave classification for divergent hand movements, S Bagyaraj, S Apurva, R Asha, B Sangeetha, D Vaithiyanathan, NISCAIR-CSIR, India

16. Performance Analysis of Implicit Pulsed and Low-Glitch Power-Efficient Double-Edge-Triggered Flip-Flops Using C-Elements, D Vaithiyanathan, V Gupta, S Kumar, AK Mishra, JB Pari, International Conference on Communication, Computing and Electronics Systems

17. Acquisition of Jugular Venous Pulse Waveform by a Non-invasive Technique, S Bagyaraj, M Ragumathulla, D Vaithiyanathan, Recent Advances in Mechanical Engineering, 343-352

18. Cloud based Text extraction using Google Cloud Vison for Visually Impaired applications, D Vaithiyanathan, M Muniraj, 2019 11th International Conference on Advanced Computing (ICoAC), 90-96

19. An Optimized FPGA Implementation of DCT Architecture for Image and Video Processing Applications, JB Pari, D Vaithiyanathan, 2019 International Conference on Wireless Communications Signal Processing and Networking (WiSPNET)

20. Implementation of Floating Point Unit based on Booth Multiplier and Compressor Adder, D Vaithiyanathan, JB Pari, S Keerthana, K Bharathan, 2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)

21. Fuzzy decision support system for improving the crop productivity and efficient use of fertilizers, G Prabakaran, D Vaithiyanathan, M Ganesan, Computers and electronics in agriculture 150, 88-97

22. Performance analysis of FinFET and negative capacitance FET over 6T SRAM, D Vaithiyanathan, MB Raj, SEP Pushpa, R Seetharaman, 2017 IEEE International Conference on Circuits and Systems (ICCS), 196-201

23. An efficient architecture for carry select adder, V Dhandapani ,World Journal of Engineering

24. An efficient multichannel FIR filter architecture for FPGA and ASIC realizations, JB Pari, D Vaithiyanathan, International Journal of Applied Engineering Research 12 (10), 2209-2220