INTERNATIONAL JOURNALS

- 1. Shanthi Rekha, S & **Saravanan**, P 2020, 'Power Analysis Attack Resilient Block Cipher Implementation based on 1-of-4 Data Encoding', Wiley ETRI Journal. (Accepted for Publication) (Scopus Indexed)
- 2. **Saravanan, P** & Shanthi Rekha, S 2019, 'Time-Shared AES-128 Implementation with Extremely Low Cost for Smart Card Applications', International Journal of Information and Computer Security. (Article in Press) (Scopus Indexed)
- 3. Shanthi Rekha, S & **Saravanan**, P 2019, 'Low-Cost AES-128 Implementation for Edge Devices in IoT Applications', Journal of Circuits, Systems and Computers, vol. 28, no. 4. pp. 1950062-1 1950062-24. (Scopus Indexed)
- 4. Shanthi Rekha, S & **Saravanan**, P 2018, 'Survey on power analysis attacks and its impact on intelligent sensor networks', IET Wireless Sensor Systems, vol. 8, no. 6. pp. 295-304. (Scopus Indexed)
- 5. **Saravanan**, P & Kalpana, P 2018, 'Novel Reversible Design of Advanced Encryption Standard Cryptographic Algorithm for Wireless Sensor Networks', Springer Wireless Personal Communications, vol. 100, no. 4. pp. 1427-1458. (Scopus Indexed)
- 6. **Saravanan, P** & Kalpana, P 2017, 'A Novel Approach to Attack Smartcards Using Machine Learning Method', Journal of Scientific and Industrial Research, vol. 76, pp. 95-99. (Scopus Indexed)
- 7. **Saravanan, P** & Kalpana, P 2016, 'A Novel Approach To Design A5/1 Stream Cipher Using Power Analysis Attack Resistant Reversible Logic Gates', International Journal of Enterprise Network Management, Inderscience, vol. 7, no. 1. pp. 70-85. (Scopus Indexed)
- 8. **Saravanan, P** & Kalpana, P 2015, 'Performance Analysis of Reversible Finite Field Arithmetic Architectures Over GF(p) and GF(2^m) in Elliptic Curve Cryptography', Journal of Circuits, Systems and Computers, vol. 24, no. 8. pp. 1550122-1550150. (Scopus Indexed)
- 9. **Saravanan, P** & Kalpana, P 2015, 'A Novel Implementation of SRAM PUF for Secure Applications', International Journal of Applied Engineering Research, vol. 10, no. 55, pp. 658-662. (Scopus Indexed)
- Saravanan, P & Kalpana, P 2015, 'Design of SubBytes and InvSubBytes
 Transformations of AES Algorithm Using Power Analysis Attack Resistant
 Reversible Logic Gates', Australian Journal of Basic and Applied Sciences,
 vol. 9, no. 1, pp. 8-18.
- 11. **Saravanan, P** & Kalpana, P 2015, 'Performance analysis of energy efficient XOR gate implementation resistant to power analysis attacks', Journal of Engineering Science & Technology, vol. 10, no. 10, pp. 1275-1292. (Scopus Indexed)

NATIONAL JOURNALS

12. Dinesh, R & **Saravanan**, P 2017, 'A Countermeasure for Leakage Power Analysis Attacks on Cryptographic Processor', National Journal of Technology, vol.13, no. 2, pp. 1-6.

INTERNATIONAL CONFERENCES

- 13. Priyadharshini, M, **Saravanan, P** 2020, "An Efficient Hardware Trojan Detection Approach Adopting Testability based Features", Proceedings of 4th IEEE International Test Conference India, ITC India 2020, during 12-14, July 2020.
- 14. **Saravanan, P,** Shanthi Rekha, S, Subha Rani S & Jatana HS 2019, "An Efficient ASIC Implementation of CLEFIA Encryption/Decryption Algorithm with Novel S-Box Architectures", Proceedings of IEEE 1st International Conference on Energy, Systems and Information Processing (ICESIP 2019), held at Indian Institute of Information Technology Design & Manufacturing (IIITD&M) Kancheepuram, during 04-06, July 2019.
- 15. Shanthi Rekha, S & **Saravanan**, P 2019, 'Threshold Implementation of a Lowcost CLEFIA-128 Cipher for Power Analysis Attack Resistance', Proceedings of 23rd International Symposium on VLSI Design and Test (VDAT-2019), held at Indian Institute of Technology Indore, India, during 04-06, July 2019.
- 16. Saravanan, P & Mehtre, BM 2018, 'A Novel Approach to detect Hardware Malware using Hamming Weight Model and One Class Support Vector Machine', Proceedings of 22nd International Symposium on VLSI Design and Test (VDAT-2018), Thiagarajar College of Engineering, Madurai, India, in Springer Communications in Computer and Information Science Vol. 892, 28th June 30th June, 2018, pp. 159-172.
- 17. Shanthi Rekha, S & Saravanan, P 2017, 'Low cost circuit level implementation of PRESENT-80 S-BOX', Proceedings of 21st International Symposium on VLSI Design and Test (VDAT-2017), IIT Roorkee, Roorkee, India, in Springer Communications in Computer and Information Science Vol. 711, 29th June 2nd July, 2017.