

#### **Publication Type: Journal Article**

1. K. A. Radhika and Dr. Anita J. P., "Test volume reduction for logic circuits by sharing of test patterns", *International Journal of Pure and Applied Mathematics*, vol. 118, pp. 2935-2941, 2018
2. A. Roy and Dr. Anita J. P., "Pattern Generation and Test Compression Using PRESTO Generator", *Communications in Computer and Information Science*, vol. 746, pp. 276-285, 2017.
3. A. Asokan and Dr. Anita J. P., "Burrows Wheeler Transform Based Test Vector Compression for Digital Circuits", *Indian Journal of Science and Technology*, vol. 9, no. 30, 2016.
4. Dr. Anita J. P. and Sudheesh, P., "Test power reduction and test pattern generation for multiple faults using zero suppressed decision diagrams", *International Journal of High Performance Systems Architecture*, vol. 6, pp. 51-60, 2016.
5. N. Mohan and Dr. Anita J. P., "A zero suppressed binary decision diagram-based test set relaxation for single and multiple stuck-at faults", *International Journal of Mathematical Modelling and Numerical Optimisation*, vol. 7, pp. 83-96, 2016.
6. Dr. Anita J. P. and Rajan, D., "Static relaxation technique with test vector compression", *International Journal of Applied Engineering Research*, vol. 10, no. 11, pp. 28731-28739, 2015.

#### **Publication Type: Conference Paper**

1. S. Aakash, Anisha, A., Das, G. J., Abhiram, T., and Dr. Anita J. P., "Design of a Low Power, High Speed Double Tail Comparator", in *2017 International Conference on Circuit ,Power and Computing Technologies (ICCPCT)*, 2017.
2. T. Abhiram, Ashwin, T., Sivaprasad, B., Aakash, S., and Dr. Anita J. P., "Modified Carry Select Adder for Power and Area Reduction", in *2017 International Conference on Circuit ,Power and Computing Technologies (ICCPCT)*, 2017.
3. A. Asokan and Dr. Anita J. P., "Multistage test data compression technique for VLSI circuits", in *Proceedings of 2016 International Conference on Advanced Communication Control and Computing Technologies, ICACCCT 2016*, 2016, pp. 65-68.
4. G. V. Madhavi and Dr. Anita J. P., "A Compaction based MT Filling Technique for Low-Power Test Set Generation", in *2016 3rd International Conference on Devices, Circuits and Systems (ICDCS)*, 2016, pp. 124-127.
5. V. Sinduja, Raghav, S., and Dr. Anita J. P., "Efficient don't-care filling method to achieve reduction in test power", in *2015 International Conference on Advances in Computing, Communications and Informatics, ICACCI 2015*, 2015, pp. 478-482.