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(B) IEEE Transactions/Journals:

1. Prem P, Sivaraman, D. Almakhlles, P. Sanjeevikumar, Z. Leonowicz, Matheswaran, **M.A.J Sathik**, "A New Multilevel Inverter Topology with Reduced Power Components for Domestic Solar PV Applications," *IEEE Access*. (Accepted)
2. **M.A.J Sathik**, D. Almakhlles, S. Ahamed Ibrahim, S. Alyami, S. Sivakumar and M. S. Basker, "A Generalized Multilevel Inverter Topology with Reduction of Total Standing Voltage," *IEEE Access*, doi: 10.1109/ACCESS.2020.3022040 - (Online).
3. N. Sandeep, **M.A.J Sathik**, U. R. Yaragatti, K. Vijayakumar, A.K. Verma and Hemanshu Pota, "Common-Ground-Type Five-Level Transformerless Inverter Topology with Full DC-Bus Utilization," *IEEE Transactions on Industry Applications*, - (Online)
4. **M.A.J Sathik**, N. Sandeep, Dhafer Almakhlles, and F. Blaabjerg, "Cross Connected Compact Switched-Capacitor Multilevel Inverter (C³-SCMLI) Topology with Reduced Switch Count," *IEEE Transaction on Circuits and System Express II*- (Online)
5. Marif Daula Siddique, **M.A.J Sathik**, et.al, "Reduce Switch Count Based Single Source 7L Boost Inverter Topology," *IEEE Transaction on Circuits and System Express II*- (Online)
6. Dhafer Almakhlles, **M.A.J Sathik**, et.al, "An Original Hybrid Multilevel DC-AC Converter Using Single-Double Source Unit for Medium Voltage Applications: Hardware Implementation and Investigation," *IEEE Access*, (Online) (Q1-Indexed).
7. Marif Daula Siddique, Saad Mekhilef, Noraisyah Mohamed shah, **M.A.J Sathik**, et al, "A Single DC Source Nine-Level Switched-Capacitor Boost Inverter Topology with Reduced Switch Count," *IEEE Access* – vol. 8, pp. 5840-5851, 2020.
8. **M.A.J Sathik**, N. Sandeep, and F. Blaabjerg, "High Gain Active Neutral Point Clamped Seven-Level Self-Voltage Balancing Inverter," *IEEE Transaction on Circuits and System Express II*- (Online).
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10. Marif Daula Siddique, Saad Mekhilef, Noraisyah Mohamed Shah, **M.A.J Sathik** and F. Blaabjerg, "A New Switched Capacitor 7L Inverter with Triple Voltage Gain and Low Voltage Stress," *IEEE Transaction on Circuits and System Express II*, doi:10.1109/TCSII.2019.2932480, (Online).
11. **M.A.J Sathik**, K. Bhatnagar, N. Sandeep and F. Blaabjerg, "An Improved Seven-Level PUC Inverter Topology with Voltage Boosting," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 1, pp. 127-131, Jan. 2020.
12. N. Sandeep, **M.A.J Sathik**, U. R. Yaragatti and K. Vijayakumar, "Switched-Capacitor-Based Quadruple-Boost Nine-Level Inverter," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7147-7150, Aug. 2019.
13. N. Sandeep, **M.A.J Sathik**, U. R. Yaragatti and K. Vijayakumar, "A Self-Balancing Five-Level Boosting Inverter with Reduced Components," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6020-6024, July 2019.
14. **M.A.J Sathik**, et al, "A New Generalized Multilevel Converter Topology with Reduced Voltage on Switches, Power losses and Components," *IEEE Journal of Emerging Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1094-1106, June 2019.
15. **M.A.J Sathik** et al., "A New Generalized Multilevel Converter Topology Based on Cascaded Connection of Basic Units," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2498-2512, Dec. 2019.
16. **M.A.J Sathik**, K. Vijayakumar, "Compact Switched Capacitor Multilevel Inverter (CSCMLI) with Self-Voltage Balancing and Boosting Ability," *IEEE Transaction on Power Electronics*, vol. 34, no. 5, pp. 4009-4013, May 2019.

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1. Ponnusamy P, Velliangiri S, and **M.A.J Sathik**, "A Hybrid Switched Capacitor Multi-Level Inverter with High Voltage Gain and Self-Voltage Balancing Ability," *Electric Power Components and Systems*.: vol. 1, no. 4, Sep. 2020. doi.org/10.1080/15325008.2020.1821832.
2. P. Prem, Sivaraman, J. S. Sakthi Suriya Raj, **M.A.J Sathik** and Dhafer Almakhlles, "Fast charging converter and control algorithm for solar PV battery and electrical grid integrated electric vehicle charging station," *Automatika*- (Online) <https://doi.org/10.1080/00051144.2020.1810506>
3. Marif D S, Mekhilef Saad, Noraisyah M Shah, **M.A.J Sathik** et al., "A New Switched-Capacitor Based Boost Multilevel Inverter Topology with Higher Voltage Gain," *IET Power Electronics*, (Online).
4. Marif Daula Siddique, **M.A.J Sathik**, et.al, 'Design and Implementation of a New Unity Gain Nine-Level Active Neutral Point Clamped (UG-9L-ANPC) Multilevel Inverter Topology," *IET Power Electronics*, (Online)
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7. **M.A.J Sathik** et al, "A Seven-Level Boosting ANPC Inverter Using Cross-Connected Switched Capacitor Cells", *IET Power Electronics*, DOI: [10.1049/iet-pel.2020.0107](https://doi.org/10.1049/iet-pel.2020.0107) (Online).
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9. Prem. P, Vidyasagar, A. Ibrahim, **M.A.J Sathik** et al, 'A Novel Cross-Connected Multilevel Inverter Topology for Higher Number of Voltage Levels with Reduced Switch Count. *Int Trans Electr Energ Syst.*, (Online).
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11. S. Selvaraj, G. Kumaresan, **M.A.J Sathik**, "Modified 'K' Type Multilevel Inverter Topology with Reduced Switches, DC Sources and Power Loss." *Int Trans Electr Energ Syst.*, (Online)
12. **M.A.J Sathik**, Prabakaran, N, Ibrahim, SAA, Vijayakumar, K, Blaabjerg, F. A new generalized switched diode multilevel inverter topology with reduced switch count and voltage on switches. *Int J Circ Theor Appl*. 2019; 1– 19. <https://doi.org/10.1002/cta.2732>.
13. George F. Savari, Vijayakumar Krishnasamy, **M.A.J Sathik**, Ziad M. Ali, Shady H.E. Abdel Aleem, Internet of Things based real-time electric vehicle load forecasting and charging station recommendation, *ISA Transactions*, (Feb-2019) (Online).
14. Prem.K, Sivaraman, **M.A.J Sathik**, et al, "A new asymmetric dual source multilevel inverter topology with reduced power switches," *Journal of the Chinese Institute of Engineers*- 42:5, 460472, 2019.
15. Karthikeyan D, Vijayakumar K and **M.A.J Sathik**, "Generalized Cascaded Symmetric and Level Doubling Multilevel Converter Topology with Reduced THD for Photovoltaic Applications" *Electronics, MDPI publisher*, Vol.8. No 2, 2019. 2018.
16. Ahamed Ibrahim, Anbazghan and **M.A.J Sathik**, A New Asymmetric Cascaded Switched Diode Multilevel Inverter Structure with Minimized Switch Count" *Journal of Circuits, Systems and Computers*, Vol. 28, No. 4, pp.1950064 (1-30), 2019.
17. Palanisamy. R, Vijayakumar. K, **M.A.J Sathik**, Ziad M. Ali, Shady H. E. Abdel Aleem, "Three-Dimensional Space Vector Modulation Strategy for Capacitor Balancing in Split Inductor Neutral Point Clamped Multilevel Inverters"- *Journal of Circuits, Systems and Computers*, Vol. 27, No. 14, pp.1850232, 2018.
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19. D.Karthikeyan, K. Vijayakumar, **M.A.J Sathik**, "Development of a Switched Diode Asymmetric Multilevel Inverter Topology," *Journal of Power Electronics*, (Vol. 18, No. 2, March 2018).
20. **M.A.J Sathik**, Shady Abdel Aleem, K.Ramani and Ahmed Zobaa, A New Switched DC –Link Capacitor Based Multilevel Converter (SDC2MLC), *Electric Power Components and Systems, Taylor & Francis*, Vol.45, No.9, pp.1001-1015, June-2017.
21. Sivakumar.S, **M.A.J Sathik**, Manoj.S, Sundarajan.G," An Assessment of Performance of DC-DC Converters for Renewable Energy Applications", -*Renewable & Sustainable Energy Reviews, Elsevier*, Vol.58, pp- 1475–1485, May 2016.
22. **M.A.J Sathik** and Ramani.K, "A New Symmetric cascaded Multilevel Inverter Topology Using Single and Double Source Unit", *Journal of Power Electronics*, - Vol.15, No.4, pp.951-963, July 2015.

23. K. Ramani, **M.A.J Sathik**, and S. Sivakumar. "A New Symmetric Multilevel Inverter Topology Using Single and Double Source Sub-Multilevel Inverters", *Journal of Power Electronics*, Vol.15. No. 1, pp 96-105, Jan-2015.

(D) Scopus Indexed Journals (Total No-04):

1. Ahamed Ibrahim, Anbazghan and **M.A.J Sathik**, A New Symmetric Switched Diode Multilevel Inverter Structure with Minimized Switch Count" *IET Journal of Engineering*, Online June 22, 2017.(Web of Science Indexed)
2. Lakshmi khandhan, Andy Srinivasan and **M.A.J Sathik**, "Single DC Source-Based Multilevel Converter Topology with Reduced Power Switches and Conduction Losses", *Journal Of Electrical Engineering*, vol.17, no.4,2017.
3. S. Mohamed Yousuf, S. Latha and **M.A.J Sathik**, "Creative Structure of Symmetric and Asymmetric Multilevel Converter Topology Using Single-Double Source Unit," *Applied Mathematics & Information Sciences" An International Journal*. Vol. 11, No. 2, pp:1-12 (2017).
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5. **M.A.J Sathik** and Ramani.K, "Investigation of Novel Symmetric and Asymmetric Multilevel Converter Topology with Reduced Power Switches"- *International Journal of Power Electronics*, Vol.7, No.3-4, pp.226-242, 2015.

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2. **M.A.J Sathik** & Ramani, K. A, "Novel Approach of Multilevel Inverter with Reduced Power Electronics Devices", Published in *WASET* Vol.8, No.11, Dec-2014, (Google Scholar-Indexed).
3. Vinothini, K., **M.A.J Sathik**, & Ramani, K. "Modelling and Analysis Of Induction Motor Drive With Novel Multilevel Inverter", Published in *International Journal of Scientific & Engineering Research*, Vol.5, No.4, Nov-2014 ISSN 2229-5518, (Google Scholar-Indexed).

4. Yazhini, R., **M.A.J Sathik**, & Ramani, K. Analysis and Modelling of New Modified Multilevel Inverter with PMSM Applications, Published in International Journal of Scientific & Engineering Research, Vol.5, No.4, Nov-2014 ISSN 2229-5518, (Google Scholar-Indexed).
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6. G. Manoranjitha, **M.A.J Sathik**, R. Solairaj, "Automatic Control of Hydraulic Machine using PLC," Published in Coimbatore Institute of Information and Technology (CIIT) April 2011, ISSN 0974 – 9551.
7. K. Immanuel Arokia James, **M.A.J Sathik**, M. Praveen, "GSM Based Data Logger System," Published in International Journal of Scientific & Engineering Research, Vol.2, No.11, Nov-2011 ISSN 2229-5518. (Google Scholar-Indexed).

(F) International Conference (Total No-10):

1. N. Sandeep, **M.A.J Sathik**, A. Kumar Verma and U. R. Yaragatti, "Three-Phase Magnetic-Less Boosting Multilevel Inverter Topology with Reduced Components," 2019 *IEEE Transportation Electrification Conference (ITEC-India)*, Bengaluru, India, 2019, pp. 1-5.
2. N. Sandeep, **M.A.J.Sathik**, A. K. Verma and U. R. Yaragatti, "Reduced Component Boost Seven- Level Inverter (RCB7LI) with Self-Voltage Balancing," 2020 *IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, Cochin, India, 2020, pp. 1-5.
3. **M.A.J. Sathik**, Z. Tang, Y. Yang, K. Vijayakumar, and F. Blaabjerg, "A New 5-Level ANPC Switched Capacitor Inverter Topology for Photovoltaic Applications," *IEEE-IECON 2019-Portugal*.
4. **M.A.J. Sathik**, N. Sandeep, K. Vijayakumar, R. Yaganthi, Frede Blaabjerg, "Hybrid Multilevel Inverter Topology with Reduced Part Count", *IEEE conference PEDES-18*, Dec 2018.
5. Sandeep.N, **M.A.J. Sathik**, et.al, "Switched-Capacitor-Based Three-Phase Five-Level Inverter Topology with Reduced Components", *IEEE conference IICPE-18*, Dec-2018.
6. **M.A.J Sathik**, R.S. Alishah, K. Vijayakumar, "A New Symmetric Multilevel Converter Topology with Reduced Voltage on Switches and DC Source" – *IEEE conference, ICETEST Conference 2018*, Thrissur, Kerala. India.
7. **M.A.J Sathik**, Ramani Kannan, Mohd. Fakhizan Romlie, "New Cascaded Multilevel Converter Topology Based on Basic Unit with Reduction of DC Sources " - *IEEE Explore Digital Library*" *CENCON 2015*, Malaysia.
8. **M.A.J Sathik**, Abdullah, Yogesh Raj, "Modified new GSM Based Data Logger System with Two-Way Communication"-*"IEEE Explore Digital Library" - INCOSSET 12*, India.
9. V.Arun Kumar, **M.A.J Sathik**, "Input Power factor improvement of rectifier followed by two quadrant shunt active filter"-*SET 12 at Vellore Institute of Technology*, India.
10. R. Yazhini, **M.A.J Sathik** & Ramani, K., "Analyzing and Modelling of New Modified Multilevel Inverter using with PMSM applications"- *ICECC-2014*, India.

11. K. Vinothini, **M.A.J Sathik** & Ramani, K., “Analysis and modelling of induction motor drive with novel multilevel inverter” *ICECC-2014*, India.