

**Dr. M. Revathy,**  
Associate Professor,  
Department of ECE,  
PSNACET,  
Dindigul.

**List of Publications**

1. M.Revathy,PN.Sundararajan and M.Kasthuri,"Error detection and correction method for timing errors in registers",Indian journal of natural Sciences,Vol.10,Issue 27, Dec 2019.
2. M.Revathy,A.Kavitha and N.Ashokkumar,"Automatic identification of maritime alert system using GPS",International Journal of Engineering and Technology,Vol.3,Issue 1,July 2018.
3. 4.M.Revathy and A.Gokilavani, "An improved secure IC design using tunable delay gate", International Journal of Pure and Applied Mathematics,Vol.118.Issue 20, 2018.
- 4.M.Revathy and T.Evangeline Santhia,"An efficient error detection and correction method for timing errors, Journal of Advances in Chemistry,Vol.12,Issue 21,Dec 2016.
5. M. Revathy and S. Sudha," Design and Analysis of Area & Energy Efficient Approximate Multiplier", Asian Journal of Research in Social Sciences and Humanities ,Vol. 6, No. 10,October 2016, pp. 260-275. ISSN 2249-7315.
6. M. Revathy and R. Saravanan," A Low-Complexity Euclidean Orthogonal LDPC Architecture for Low Power Applications", The Scientific World Journal, 2015, Article ID 327357, 8 pages.
7. M.Revathy and R. Saravanan, " Hybrid LDPC Decoder For High Error Detection and Correction Applications" International Journal of Applied Engineering Research, Vol. 10 No. 9(2015) pp. 24201-24214.
- 8.M.Revathy and R. Saravanan, " LDPC Decoder Based on Superimposing of Bit Streams For Low Power Applications" International Journal of Applied Engineering Research, Vol. 10 No. 9(2015) pp. 24215-24225.
9. Revathy.M and Arockia Muthu.A , , "Measurement Of Nearby Obstacles Distance Using Multiple Sonar" International Journal of Applied Engineering Research, Vol. 10 No.5 (2015) pp. 4730-4733, ISSN 0973-4562.
- 10 M.Revathy and S.Devi, "FPGA Based Implementation Of Area-Delay-Power Efficient Reconfigurable LMS Adaptive Filter" International Journal of Applied Engineering Research, Vol. 10 No.5 (2015) pp. 4734-4738, ISSN 0973-4562(Scopus)

11. M.Revathi, Siva Subramanian R, Ms.Suganya Thevi.T and, "Design of LowPower 4:2 and 5:2 Compressors for High Speed Arithmetic Circuits",International Journal of Applied Engineering Research, Vol. 10 No.55 (2015),pg.no.394-399, ISSN 0973-4562.
12. M.Revathy and S.Sudha, ," Design of Low Power Approximate Compressor For Dadda Multiplier", International Journal of Advanced Research in Electronics and CommunicationEngineering (IJARECE) ,Volume 4, Issue 11, November 2015.
13. M. Revathy and G. Swathi, ,"Design of a Multi-Standard DUC Based FIR Filter Using VLSI Architecture", International Journal of Scientific Engineering and Research(IJSER), Volume 3 Issue 11, November 2015,pg.no.41-44, ISSN (Online): 2347-3878.
- 14.Revathy, M. and R. Saravanan, "Performance analysis of high efficiency low density parity-check code decoder for low power applications". American Journal of Applied Sciences., Vol. 11, Issue No.4, Jan 2014, 558-563.
15. Revathy.M and Arockia Muthu.A," A Survey on Automatic Vehicle Parking and Retrieval Using Android Smartphone" International Journal of Engineering Sciences and Research Technology,Vol. 11, Issue No. 3, Nov. 2014,418-421.
16. , Revathy.M and Devi," Survey of FPGA based implementation of area-delay-power efficient reconfigurable LMS Adaptive filter" Global Journal of Engineering Science and Researches, 1(9): Nov, 2014,81-84, ISSN 2348 – 8034.
- 17.Anu Jose and M.Revathy, "VLSI implementation of Euclidean Geometry LDPC codes using maximum likelihood decoding", International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 4, April 2014,pg.no.1103-1107, ISSN: 2278 – 7798.
18. Revathy M ,Siva Subramanian R, Suganya Thevi T, "A Review on Low Power Compressor for High Speed Arithmetic Circuits", International Journal of Innovative Research in Science,Engineering and Technology, Vol. 3, Issue 11, November 2014,pg.no.17517-17522, ISSN:2319-8753.