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1.	**P.Sakthivel** and A.Nirmal Kumar, LT-GLFSR Based Test pattern Generator architecture for Mixed-mode Build-in –Self- Test (BIST), European Journal of Scientific Research (SCI), Vol.52 Issue.1, April'2011, pp.6-15.
2.	**P.Sakthivel** and A.Nirmal Kumar, Low Transition Generalized Linear Feed Back Shift Register based Test Pattern Generator Architecture for Built-in-Self-Test, Journal of Computer Science (SCOPUS), Vol.8, Issue.6, pp.815-828, March'2012
3.	**P.Sakthivel** and A.Nirmal Kumar and and T.Mayilsamy, Low Transition Test Pattern Generator for Built-in-Self-Test, American Journal of Applied Science(SCOPUS), Vol.9, Issue.9,pp. 1396-1406, July'2012
4.	**P.Sakthivel** and A.Nirmal Kumar and T.Mayilsamy, Low Transition Test Pattern Generator Architecture for Mixed mode Built-in-Self-Test (BIST), International Journal of Advances in Engineering & Technology, Nov. 2012, Vol. 5, Issue 1, Nov' 2012.
5.	T.Kalavathi devi and **P.Sakthivel**, An Asynchronous Low Power and High Performance VLSI Architecture for Viterbi Decoder Implemented with Quasi Delay Insensitive Templates, The Scientific World Journal, Hindawi Publishing Corporation (SCOPUS), Vol.2015,Article ID:621012
6.	V.Vithya and **P. Sakthivel**, Reducing Redundant Bits and Enhanced Memory Reliability Using Decimal Matrix Code, International Journal of Electrical and Electronics Research, Vol. 3, Issue 3, pp: (48-54), July - September 2015
7.	T.Kalavathi devi and **P.Sakthivel**, Design and FPGA implementation of Bit level pipelined Digit Serial VLSI Architecture for a Viterbi Decoder, Asian Journal of Information technology (SCOPUS), Vol.15,Issue 7, pp:1232-1242, June-2016
8.	**P.Sakthivel** and T.Kalavathi devi, Efficient Low Power Design of 4-Tap and 6-Tap 2d Daubechies Wavelet Filters using Pipelined Direct Mapping Method, Asian Journal of Research in Social Sciences and Humanities, Vol. 6, No. 6, pp. 1453-1470., June 2016
9.	T.Kalavathi devi and **P.Sakthivel**, Pipelined Direct Mapping Method Based Low Power Vlsi Architecture For The 4-Tap Wavelet Filter, Asian Journal of applied science and Technolgy, Vol.1,Issue No.7, PP. 76-79, August 2017
10.	P.Tamilarasu , **P.Sakthivel** and T.Kalavathi Devi, Heart Rate Monitoring System Using IOT, International Journal of Scientific Development and Research (IJSDR), Volume 4 Issue 4, pp.186-191, April 2019
11.	T.Kalavathi devi, **P.Sakthivel**, Monitoring and Analysis of Water Quality Parameters for Diagnosis of Safe Drinking Purpose using Wireless Sensor Network, International Journal of Innovative Technology and Exploring Engineering, Vol.9, issue.2, pp.1478-1482, December2019.
12.	T.Kalavathi devi and **P.Sakthivel**, A Design of Phase Locked loop Based Frequency Synthesizer using 4/5 Prescalar circuit, International journal of Engineering and Advanced Technology, (Scopus), ISSN: 2249-8958 (Online), Vol.8, issue.4, pp.581-586, April 2019.
13.	T.Kalavathi devi, **P.Sakthivel**, V.G. Pratheep and E.B. Priyanka, 120 MHz, 2.2 mW Low Power Phase-Locked Loop using Dual Mode Logic and its Application as Frequency Divider, GEDRAG & ORGANISATIE REVIEW, ISSN:0921-5077, Vol. 33 : Issue.02 – 2020, pp.152-162, April-June 2019.
14.	T.Kalavathi devi and **P.Sakthivel** , Analysis of Overloading in Trucks using Embedded Controller, IEEE Conference ICESCS 2020-Scopus Indexed, IEEE Xplore.

15.	Kalavathi Devi Thangavel, Sakthivel Palaniappan, Sathish Kumar Shanmugam Performance Analysis of VLSI Architecture of Viterbi Decoder in WLAN Using the Sleepy Keeper Technique, Comptes rendus de l'Acade'mie bulgare des Sciences, Vol 73, No8, pp.1123-1131 (SCI)

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