Papers published in International Journals of

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1.Innovative localization algorithm using the line of intersection technique in wireless sensor networks, Journal of Internet technology, Volume 21, Year 2020, Pages 425-433.

2.Area-Efficient Dual-Mode Fused Floating-Point Three-Term Adder Thiruvenkadam by K.;Ramesh, J.;Pillai, Anjali S. Circuits, Systems, and Signal Processing, Volume 38, Year 2019, Pages 173-190.

3.Adaptive neuro fuzzy inference system-based power estimation method for CMOS VLSI circuits by Vellingiri, Govindaraj;Jayabalan, Ramesh, International Journal of Electronics, Volume 105, Year 2018, Pages 398-411.

4.An improved low transition test pattern generator for low power applications by Vellingiri, Govindaraj;Jayabalan, Ramesh,Article Design Automation for Embedded Systems, Volume 21, Year 2017, Pages 247-263.

5.An Improved Self Adaptive Min-Sum Decoding Algorithm for Flexible Low-Density Parity-Check Decoder by Roberts, Michaelraj Kingston;Jayabalan, Ramesh , National Academy Science Letters, Volume 40, Year 2017, Pages 121-125

6.Enhanced test zone search algorithm for high efficiency video coding encoders Madhuvappan, C. Arunkumar;Ramesh, J.,Journal of Computational and Theoretical Nanoscience, Volume 14, Year 2017, Pages 1245-1249.

7.An area efficient multi-mode quadruple precision floating point adder by Thiruvenkadam, K.;Ramesh, J.;Kalaiyarasi, V. Microprocessors and Microsystems, Volume 45, Year 2016, Pages 310-323.

8.A Power- and Area-Efficient Multirate Quasi-Cyclic LDPC Decoder by Roberts, Michaelraj Kingston;Jayabalan, Ramesh , Circuits, Systems, and Signal Processing, Volume 34, Year 2015, Pages 2015-2035

9.An Improved Low Complex Hybrid Weighted Bit-Flipping Algorithm for LDPC Codes ,by Roberts, Michaelraj Kingston;Jayabalan, Ramesh

Wireless Personal Communications, Volume 82, Year 2015, Pages 327-339

10.An improved low-complexity sum-product decoding algorithm for low-density parity-check codes by Roberts, Michaelraj Kingston;Jayabalan, Ramesh, Frontiers of Information Technology and Electronic Engineering, Volume 16, Year 2015, Pages 511-518

11.FPGA implementation of variable bit rate 16 Qam transceiver system by Dhanasekar, S.;Ramesh, J. International Journal of Applied Engineering Research, Volume 10, Year 2015, Pages 26497-26507

12.Low power test pattern generation for bist applications by Govindaraj, V.;Ramesh, J.;Kasthuri, N. International Journal of Applied Engineering Research, Volume 10, Year 2015,