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Present Position

Professor, Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai from August-2015.

Present Additional Responsibility

- Deputy Director, Centre for Distance Education, Anna University, Chennai from February-2015.
- Treasurer, Department of Electronics and Communication Engineering, Anna University, Chennai from January-2015.
- FACULTY IN CHARGE FOR PA SYSTEM, Department of Electronics and Communication Engineering, Anna University, Chennai from January-2003.

Previous Positions

- Associate professor, Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai during August-2012 and August-2015.
- Assistant Professor, Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai during August-2009 and August-2012.
- Lecturer, Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai during February-2005 and August-2009.
- Teaching Research Associate, Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai during February-2002 and February-2005.

Previous Additional Responsibility

- Additional Chief Superintendent For Pg, Department of Electronics and Communication Engineering, Anna University, Chennai during May-2003 and July-2006.
- Additional Chief Superintendent For Ug, Department of Electronics and Communication Engineering, Anna University, Chennai during May-2003 and July-2006.
- , , Anna University, Chennai.

Other Employment

- Lecturer, Saveetha Engg College for 1 year.

Degree

- ❖ M.E. in Applied Electronics, , Bharathiar (1999 - 2001).

Research Degree

- ❖ Ph.D. in VLSI from Faculty of ICE, ANNA University, ANNA - 0).
Title: .

Area of Specialisation

- Reconfigurable computing, VLSI for wireless Communication., VLSI Image Proc

Membership in Professional Organization

- IEICE

Research Guidance

Number of Ph.D Scholars Guided	: 6
Number of Ph.D Scholars Guiding	: 7
Number of M.E./ M.Tech. Projects Guided	: 100
Number of M.E./ M.Tech. Projects Guiding	: 10

Papers Published in Journals

Research Papers Published in International Journals	: 36
Research Papers Published in National Journals	: 0

1. P.Nirmal Kumar and J.Raja Paul Perinbam, "On suitability of FPGA based Evolvable Hardware systems to integrate reconfigurable circuits with host processing unit", Journal of Computer Science and Network Security, Vol. 6, Issue 9, pp. 216-221 (2006).
2. P.Nirmal Kumar and J.Raja Paul Perinbam, "Testing Virtual Reconfigurable Circuit Designed for a Fault Tolerant System", Journal of Computer Science, published by Science Publications. pp. 934-938 (2007).
3. B.Padhmavathi and P.Nirmal Kumar, "A Denoising Filter Design based on No-Reference Image Content Metric", International Journal of Computer Science & Engineering, published by Engg Journals Publications. Vol. 3, Issue 12, pp. 3780 - 3790 (2011).

4. P.Ezhilarasi and P.Nirmal Kumar, " An Efficient Image Compression Algorithm using Modified IWT and SPIHT for CMOS Image Sensor", International Review on Computers and Software, Vol. 8, Issue 9, pp. 2044-2050 (2012).
5. "Power consumption reduction in a SDR based wireless communication system using partial reconfigurable FPGA", International Journal of VLSI design & Communication Systems (VLSICS) , Vol. 3, Issue 2, pp. 203-210 (2012).
6. Neenu Joseph, Dr.P Nirmal kumar, "Realization of SDR in Partial Reconfigurable FPGA Using Different types of Modulation Techniques", NetCom2011 published in Springer LNCS., (2012).
7. P.Ezhilarasi and P.Nirmal Kumar, "An Efficient Image Compression By Overlapped Discrete Cosine Transform With Adaptive Thinning", International Journal of Engineering Research and Applications, Vol. 2, Issue 5, pp. 1675-1681 (2012).
8. B.Padhmavathi, P. Nirmal Kumar and M. A. Dorai Rangaswamy, "A Robust Three-Way Authentication System using Modified Random Grid based Reversible Style Visual Cryptography", International Journal of Computer Applications, Vol. 37, Issue 1, (2012).
9. Neenu Joseph & P Nirmal Kumar, ""Reduction of PAPR using PTS and SLM of OFDM Transceiver System",", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, pp. pp. 5640 - 5646 (2013).
10. Deepa Jose, P.Nirmal Kumar and P.Jaya Kumar, "Optimal and Power Aware BIST for Delay Testing of System-On-Chip", ACEEE International Journal on Control System and Instrumentation, Vol. 4, Issue 2, pp. 45-53 (2013).
11. R.Umamaheswari and P.Nirmal Kumar, "Optimized 512-point FFT with effective computational components for WLAN application", Information-International Information Institute, Vol. 17, Issue 6, pp. 2225-2238 (2014).
12. Neenu Joseph and P.Nirmal Kumar, "Reduction of PAPR in OFDM Transceiver system for Next Generation Communication systems", International Journal of Recent Trends in Engineering and technology, Vol. 11, pp. 513-522 (2014).
13. A.Arun and P.Nirmal Kumar, "Modified TACIT Algorithm Based on 4H-key Distribution for Secure Routing in NoC Architecture", IEICE Electronics Express, Vol. 11, Issue 13, pp. 1-8 (2014).
14. Deepa Jose, P.Nirmal Kumar, Arfath Hussain and Prabhu Shanker, "VLSI Circuit Partitioning using Ant Colony Optimization to yield Fault Tolerant Testable VLSI systems", Arabian Journal of Science and Engineering , published by Springer. Vol. 39, Issue 12, pp. 8709-8729 (2014).
15. Deepa Jose, P.Nirmal Kumar, J.Abanah Shirley and S.Ghayathrie, "Implementation of Genetic Algorithm framework for Fault Tolerant System on Chip", Information-International Information Institute, Vol. 17, Issue 8, pp. 3921-3946 (2014).
16. P.Ezhilarasi and P.Nirmal Kumar, " A combined approach for lossless image compression technique using curvelet transform", International Journal of Engineering and Technology, Vol. 6, Issue 3, pp. 1487-1494 (2014).

17. A.Arun and P.Nirmal Kumar, "SoPC based wireless remote patient monitoring using ultra lightweight cryptography", *Journal of Computer Science*, Vol. 10, Issue 10, pp. 1924-1928 (2014).
18. Neenu Joseph and P.Nirmal Kumar, "PAPR reduction using companding and PTS method in OFDM transceiver system", *WIT Transactions on Information and Communication Technologies*, Vol. 58, pp. 733-740 (2014).
19. N.Janakiraman and P.Nirmal Kumar, "Multi-objective hardware/software partitioning technique for dynamic and partial reconfigurable system-on-chip using genetic algorithm", *International Journal of Engineering and Technology*, Vol. 6, Issue 2, pp. 552-558 (2014).
20. Neenu Joseph and P.Nirmal Kumar, "FPGA Based Realization of Multi-Carrier Direct Sequence CDMA for SDR Application", *International Journal of Innovative Research in Science, Engineering and Technology*, Vol. 3, Issue 3, pp. 1479-1485 (2014).
21. N.Janakiraman, S.J.Udaya Kumar, K.J.Sabarish, S.Vimal Kandan, P.Nirmal Kumar and S.Selvakumar, "A Low Power and High Speed MPSOC Architecture for Reconfigurable Application", *International Journal of Innovative Research in Science, Engineering and Technology*, Vol. 3, Issue 3, pp. 1567-1571 (2014).
22. N.Janakiraman, P.Mano Arunika and P.Nirmal Kumar, "An optimized Mapping of IP Core onto NoC using Multi-Objective Evolutionary Algorithms", *International Journal of Innovative Research in Science, Engineering and Technology*, Vol. 3, Issue 3, pp. 1409-1414 (2014).
23. 1. N.Janakiraman and P.Nirmal Kumar, "Multi-objective module partitioning design for dynamic and partial reconfigurable system-on-chip using genetic algorithm", *Journal of System Architecture (Elsevier)*, pp. 119-139 (2014).
24. Neenu Joseph and P.Nirmal Kumar, "FPGA Based realisation of SDR with OFDM Transciever", *Defense Science Journal*, Vol. 65, Issue 3, pp. 233-239 (2015).
25. N.Janakiraman, P.Nirmal Kumar and Syed Mohsin Akram, "Coarse grained ADRES based MIMO-OFDM transceiver with new Radix-25 pipeline FFT/IFFT processor", *Circuits, Systems & Signal Processing*, published by SPRINGER. Vol. 34, Issue 3, pp. 851-873 (2015).
26. P.Ezhilarasi and P.Nirmal Kumar, "Algorithmic based VLSI architecture of Integrated Image Compression for CMOS Image Sensor", *National Academy Science Letters*, published by Springer. Vol. 38, Issue 1, pp. 49-59 (2015).
27. Neenu Joseph and P.Nirmal Kumar, "Realization of OFDM Transceiver system and PAPR Reduction Using Walsh Hadamard transform", *International Journal of Applied Engineering and Research*, Vol. 10, Issue 2, pp. 3391-3398 (2015).
28. Neenu Joseph and P.Nirmal Kumar, "Peak power and Crest Factor Reduction in OFDM Transceiver using Filtering method for SDR Application", *National Academy Science Letters*, Vol. 38, Issue 6, pp. 483-488 (2015).
29. Deepa Jose, P.Suganya and P.Nirmal Kumar, "Content Addressable Memory Using Automatic Charge Balancing with Self-Control Mechanism and Master-Slave Match Line Design", *Circuits and Systems*, Vol. 7, Issue 6, pp. 597-611 (2016).

30. R.Kalaivani, Deepa Jose and P.Nirmal Kumar, "An Area Efficient FFT Implementation for OFDM", International Journal of Advanced Research in Biology Engineering Science and Technology , Vol. 2, Issue 14, (2016).
31. N.Janakiraman, P.Nirmal Kumar, S.Rajeswari, C.Kumar Charlie Paul and S.Babu, "Dynamic Resource Allocation Scheme for MIMO-OFDMA Multicast System", National Academy of Sciences, India Section A: Physical Sciences, Vol. 86, Issue 2, pp. 187-199 (2016).
32. N.Janakiraman and P.Nirmal Kumar, " An experimental study of coarse grained reconfigurable system-on-chip based software defined radio", Turkish Journal of Electrical Engineering & Computer Sciences, Vol. 24, Issue 3, pp. 1176-1193 (2016).
33. R.UmaMaheswari and P.Nirmal Kumar, "An FPGA Implementation of Finite State Machine based 2-step interleaver for 3G-LTE turbo codes", Journal of computational and theoretical nanoscience, Vol. 14, Issue 3, pp. 1288-1293 (2017).
34. Deepa Jose, A.Noufal Chithara, P.Nirmal Kumar and H.Kareemulla, "Automatic Detection of Lung Cancer Nodules in Computerized Tomography Images", National Academy Science Letters-India , published by SPRINGER. Vol. 40, Issue 3, pp. 161-166 (2017).
35. H.Kareemullah, N.Janakiraman and P.Nirmal Kumar, "Massively Parallel ECoG Signal Processing using MPSoC for Real-time Brain-Computer Interface", Asian Journal of Research in Social Sciences and Humanities, Vol. 7, Issue 3, pp. 1017-1032 (2017).
36. Neelam Sanjeev Kumar ,P Nirmalkumar, "An Intelligent Decision-Support System For Telemedicine", Applied Mathematics & Information Sciences, published by 991. Vol. 5, Issue 12, pp. 981 (2018).

Papers Presented in Programmes

Research Papers Presented in International Programmes : 7
 Research Papers Presented in National Programmes : 1

1. B.Padhmavathi, Dr.P.Nirmal Kumar, Dr.DoraiRangaswamy, "" A Novel Mutual Authentication Scheme using Visual Cryptography in Reversible Style", " presented in a International level conference on " A Novel Mutual Authentication Scheme using Visual Cryptography in Reversible Style", , INDIA .
2. Ezhilarasi, P & Nirmalkumar, P, on 'An Enhanced Anti Artifacts Compressive Approach for CMOS Image Sensor', , organised by International Conference on communication and signal processing, ICCSP'13, INDIA .
3. Ezhilarasi, P & Nirmalkumar, P, on 'An Enhanced Anti Artifacts Compressive Approach for CMOS Image Sensor', , organised by International Conference on communication and signal processing, ICCSP'13 2013, INDIA .
4. S. Sathyabhama, P. Nirmal Kumar, on "Realization of multi-carrier direct sequence CDMA using viterbi decoder", organised by International Conference on Electronics and Communication Systems (ICECS), , INDIA .

5. N.Janakiraman, P Nirmal Kumar, " System-On-Chip implementation of MIMO-OFDM Transceiver for Software Defined Radio"" presented in a National level conference on IETE national conference on Expanding Horizon in Computer, Information Technology, Telecommunication & Electronics (EXCITE), INDIA .
6. P.Nirmal Kumar and Dr.J.Raja Paul Perinbam, "Digital Filter Design using Evolvable Hardware" presented in a International level conference on conference on Computer and Information Science, organised by IEEE ACIS - International Co, South Korea .
7. "Evolvable Fault Tolerant with Neural Estimator" presented in a International level conference on IEEE 1st International Conference on Industrial and Information system (ICIIS), organised by IEEE 1st International Conference on Industrial and Information system (ICIIS), Sri Lanka .
8. P.Nirmal Kumar and Dr.J.Raja Paul Perinbam, "Evolving Virtual Reconfigurable Circuit for a Fault Tolerant System" presented in a International level conference on IEEE Congress on Evolutionary Computation (CEC), Singapore .

Sponsored Projects Completed

1. "Aksharabhyasam – Aathichudi Slate" (January-2017 - December-2017). Project Cost: 1.50.

Programme Chaired

1. Co Chairman, International level conference titled "ICIDSET-18" conducted by KCG College of Technology from 17-Apr-2018 to 18-Apr-2018.

Programme Organized

1. co-ordinator, International level Short Course on "FDP on Electronic Circuit-I" from 15-Jun-2009 to 21-Jun-2009.
2. co-ordinator, International level Short Course on "EC6304-Electronic Circuit-I" from 23-Mar-2014 to 29-Nov-2014.
3. organizer, International level workshop on "Digital Custom IC Design using CADENCE EDA Tools" from 12-Mar-2015 to 14-Nov-2015.

Programme Attended

1. Participated in a International level conference on "A Novel Scheme for Mutual Authentication and Cheating Prevention in Visual Cryptography Using Image Processing" organized by Proceedings International Conference on Advances in Computer Science ACS 2010, INDIA.
2. Participated in a International level conference on "'Integrated Image Compression by Predictive Boundary Adaptation with QTD and Adaptive Thinning'," organized by Advances in computer and communication technology IETE conference, 2013, INDIA from 31-Dec-1969 to 31-Dec-1969.

3. Participated in a International level conference on "An Efficient Image Compression by Improved DCT with Adaptive Thinning'" organized by International Conference on Research and Development Prospectus on Engineering and technology 2013, INDIA from 31-Dec-1969 to 31-Dec-1969.
4. Participated in a International level conference on "Implementation of power optimized VLSI designs for reliable processing using majority circuit', " organized by Proceedings of IEEE Annual International Conference, IIT Bombay 2013, INDIA from 31-Dec-1969 to 31-Dec-1969.
5. Participated in a International level conference on "Reliability aware self-healing FFT system employing partial reconfiguration for reduced power consumption'" organized by Proceedings of IEEE Students Technology Symposium, IIT Kharagpur, 2013, INDIA from 31-Dec-1969 to 31-Dec-1969.
6. Participated in a International level conference on "'Fault tolerant adaptive-neuro-fuzzy based automated cruise controller on FPGA'," organized by Proceedings of IEEE Annual International Conference, IIT Bombay 2007, INDIA from 31-Dec-1969 to 31-Dec-1969.
7. Participated in a International level conference on "Computer aided partitioning for design of parallel testable VLSI systems'," organized by Proceedings of IEEE International Conference in Advances in Computing, Communications and Informatics , INDIA from 31-Dec-1969 to 31-Dec-1969.
8. Participated in a International level conference on "'Parallel Pseudo Exhaustive and Low Power Testing of VLSI Systems'," organized by Proceedings of International Conference on Advances in Information Technology and Engineering,, INDIA from 31-Dec-1969 to 31-Dec-1969.
9. Participated in a International level conference on "'FPGA based Realization of PAPR Reduction in OFDM and Optimization using RWBS Algorithm for SDR Application" organized by Proc. of Int.Conf. on Advances in Electrical & Electronics, , INDIA from 31-Dec-1969 to 31-Dec-1969.
10. Participated in a International level conference on "A Robust Blind & Invisible Watermarking Scheme for Share Authentication in Visual Cryptography to prevent Cheating Attacks'" organized by Proceedings Intl. Conference ICISA 2010, INDIA from 31-Dec-1969 to 31-Dec-1969.
11. Participated in a International level conference on "Implementation of Software Defined Radio on WARP using MATLAB", " organized by Organized by Department of ECE Anna University, Coimbatore Campus , INDIA from 31-Dec-1969 to 31-Dec-1969.
12. Participated in a International level conference on "'Secure Reliable Data Processing for Reconfigurable Platforms,'" organized by Proceedings of Fifth National Conference on Signal Processing, Communication and VLSI Design,, INDIA from 31-Dec-1969 to 31-Dec-1969.
13. Participated in a International level conference on "Evolvable Fault Tolerant with Neural Estimator", " organized by IEEE 1-st International Conference on Industrial and Information system (ICIIS), 2006,, INDIA from 31-Dec-1969 to 31-Dec-1969.

14. Participated in a International level conference on ""Evolvable Fault Tolerant system using Kalman Estimator", " organized by International conference on Emerging Trends in High Performance Architecture Algorithms and Computing (HiPAAC),, INDIA from 31-Dec-1969 to 31-Dec-1969.
15. Participated in a International level conference on ""A Novel Scheme for Mutual Authentication and Cheating Prevention in Visual Cryptography Using Image Processing" organized by Proceedings International Conference on Advances in Computer Science ACS 2010, , INDIA from 31-Dec-1969 to 31-Dec-1969.
16. Participated in a International level conference on ""Realization of SDR in Partial Reconfigurable FPGA Using Different types of Modulation Techniques" , INDIA from 31-Dec-1969 to 31-Dec-1969.
17. Participated in a International level conference on "" A Novel Reversible Style Visual Cryptography with Blind and Invisible Watermarking Scheme"" , INDIA from 31-Dec-1969 to 31-Dec-1969.
18. Participated in a International level conference on ""System-On-Chip implementation of MIMO-OFDM Transceiver for Software Defined Radio"," organized by IETE national conference on Expanding Horizon in Computer, Information Technology, Telecommunication & Electronics (EXCITE), INDIA from 31-Dec-1969 to 31-Dec-1969.
19. Participated in a International level conference on ""Secure Reliable Data Computing using TMR for FPGAs," " organized by Proceedings of 2nd National Conference on Frontiers in Applied Sciences and Computer Technology,National Institute of Technology(NIT), 2013, INDIA from 31-Dec-1969 to 31-Dec-1969.
20. Participated in a International level conference on "Realization of SDR in Partial Reconfigurable FPGA Using Different types of Modulation Techniques", 2012" organized by NetCom201, I from 31-Dec-1969 to 31-Dec-1969.
21. Participated in a International level conference on ""Design of Control System for MEMS based Nanoparticle Propulsion"," organized by Proceedings of Second International Conference on Futuristic Trends in Electronics Engineering 2013, INDIA from 31-Dec-1969 to 31-Dec-1969.
22. Participated in a International level conference on ""Pattern Generator for Pseudo Exhaustive Testing", " organized by International Conference on Computing and Control Engineering, INDIA from 31-Dec-1969 to 31-Dec-1969.
23. Participated in a International level conference on "Design of Control System for MEMS based Nanoparticle Propulsion"," organized by Proceedings of Second International Conference on Futuristic Trends in Electronics Engineering, INDIA.
24. Participated in a International level conference on "Secure Reliable Data Processing for Reconfigurable Platforms," Proceedings of Fifth National Conference on Signal Processing" organized by Communication and VLSI Design, Anna University Regional Centre,2013, INDIA.
25. Participated in a International level conference on "A Novel Mutual Authentication Scheme using Visual Cryptography in Reversible Style" organized by Proceedings International Conference on Advances in Electrical, Electronics, Information ,Communication and Bio-Informatics AEEICB 2013, INDIA.

26. Participated in a International level conference on "A Novel Cheating Prevention Technique for Reversible Style Visual Cryptography using Blind And Invisible Watermarking Scheme"" organized by Proceedings Intl. Conference ICFET'2010, INDIA.
27. Participated in a International level conference on "Implementation of Software Defined Radio on WARP using MATLAB" organized by proceedings 5th National Conference on Signal Processing Communications & VLSI Design, Organized by Department of ECE Anna University 2013., INDIA.

Invited Lectures

1. Delivered a Lecture on "ELECTRONICS CIRCUITS -1" in Faculty development Programme organized by AnnaUniversity, chennai (06-May-2008).
2. Delivered a Lecture on "electronic circuit" in invited lectures organized by veltech university, chennai (22-Aug-2017).
3. Delivered a Lecture on "PN DIODE,current equation and its characteristics,Energy Band " in Faculty Development programme organized by university collage of engineering, panruti (24-Nov-2017).
4. Delivered a Lecture on "CONTROL SYSTEM ENGINEERING" in FDTP organized by KALAIAGNARKARUNIDHI INSTITUTE OF TECHNOLOGY, COIMBATORE (11-Dec-2017).