Dr. Sakthivel Ramachandran

List of Publication

Design of Artificial Neuron Network with Synapse Utilizing Hybrid CMOS Transistors with Memristor for Low Power Applications — 2020
VK Rai, R Sakthivel
JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS 29 (12)

Superior Implementation of Accelerated QR Decomposition for Ultrasound Imaging — 2020
SG Sreejeesh, R Sakthivel, JU Kidav
IEEE Access 8, 156244-156260

Low power area optimized and high speed carry select adder using optimized half sum and carry generation unit for FIR filter — 2020
R Sakthivel, G Ragunath
JOURNAL OF AMBIENT INTELLIGENCE AND HUMANIZED COMPUTING

Implementation of D-flipflop using Hybrid Memristor with CMOS Transistor — 2020
R Sakthivel, VK Rai
Helix 10 (02), 143-146

Design of Artificial Neuron Network with Synapse Utilizing Hybrid CMOS Transistors with Memristor for Low Power Applications — 2020
V Keerthy Rai, R Sakthivel
Journal of Circuits, Systems and Computers, 2050187

Single Bit Fault Detecting ALU Design using Reversible Gates — 2020
M Bhusal, R Rohith, R Sakthivel
2020 International Conference on Emerging Trends in Information Technology …

Nonlinear System Modelling Using Programmable Hardware for Soft Computing Applications — 2020
M Vanitha, R Sakthivel, R Mangayarkarasi, S Sharma
Soft Computing for Problem Solving, 293-306

Long-Lifetime and Low Latency Data Aggregation Scheduling for Wireless Sensor Network — 2019
E Gayathri, M Vanitha, R Mangayarkarasi, R Sakthivel
Journal of Testing and Evaluation 47 (6), 3878-3892

A Review On Dynamic Comparator Topologies — 2019
PH Naikar, R Sakthivel
2019 International Conference on Vision Towards Emerging Trends in …

Delay Optimized Binary to BCD Converter for Multi-operand Parallel Decimal Adder — 2019
G Ragunath, V Sugandh, R Sakthivel
2019 International Conference on Vision Towards Emerging Trends in …

Radix-4 Interleaved Modular Multiplication for Cryptographic Applications — 2019
T Kudithi, M Potdar, R Sakthivel
2019 International Conference on Vision Towards Emerging Trends in …

High-performance ECC processor architecture design for IoT security applications 2019
T Kudithi, R Sakthivel
The Journal of Supercomputing 75 (1), 447-474

Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems 2019
K Sanapala, R Sakthivel
IET Circuits, Devices & Systems 13 (4), 465-470

Radix 8 Booth Encoded Interleaved Modular Multiplication 2019
J Gandhi, R Sakthivel

High Performance GCM Architecture for the Security of High Speed Network 2018
V Mohanraj, R Sakthivel, A Paul, S Rho
International Journal of Parallel Programming 46 (5), 904-922

Schmitt trigger-based single-ended 7T SRAM cell for Internet of Things (IoT) applications 2018
K Sanapala, R Sakthivel, SS Yeo
The Journal of Supercomputing 74 (9), 4613-4622

15–4 Approximate Compressor Based Multiplier for Image Processing 2018
TUS Krishna, KS Riyas, Y Premson, R Sakthivel
2018 2nd International Conference on Trends in Electronics and Informatics …

A Low Power 10 bit 50-MS/s Sample and Hold OTA Amplifier 2018
R Sakthivel, GN Jyothi, ND Kumar
Proceedings of the 2018 International Conference on Communication …

Design of ultralow voltage-hybrid full adder circuit using GLBB scheme for energy-efficient arithmetic applications 2018
K Sanapala, LR Shree, R Sakthivel
Microelectronics, Electromagnetics and Telecommunications, 217-223

Analysis of GDI logic for minimum energy optimal supply voltage 2017
K Sanapala, R Sakthivel
2017 International conference on Microelectronic Devices, Circuits and …

Low power XOR gate design and its applications 2017
K Ravali, NR Vijay, S Jaggavarapu, R Sakthivel
2017 Fourth International Conference on Signal Processing, Communication and …

DYNAMIC DATA PARTITIONING AND VIRTUAL CHUNKING FOR EFFECTIVE DATA RETRIEVAL 2017
M Vanitha, R Mangayarkarasi, J Norman, R Sakthivel, K Baranitharan
International Journal of Pure and Applied Mathematics 117 (17), 33-40

Two Novel Subthreshold Logic Families for Area and Ultra Low-Energy Efficient Applications: DTGDI & SBBGDI 2017
K Sanapala
Gazi University Journal of Science 30 (4), 283-294

VLSI Implementation of Lightweight Cryptography Algorithm 2016
R Sakthivel
Advances in Systems Science and Applications 16 (1), 95-101

A custom reconfigurable power efficient FIR filter 2016
R Sakthivel, I Mishra, V Jalke, A Wachaspati
2016 International Conference on Circuit, Power and Computing Technologies …

VLSI Architecture for Image Contrast Enhancement using Modified Adaptive Gamma Correction with Weighting Distribution 2016
Y Premson, R Sakthivel
Indian Journal of Science and Technology 9 (5), 1-7

Low power realization of subthreshold digital logic circuits using body bias technique 2016
K Sanapala, R Sakthivel
Indian Journal of Science and Technology 9 (5), 1-5

Low-Power and Area-Efficient Square–Root Carry Select Adders using Modified XOR Gate 2016
G Ragunath, R Sakthivel
Indian Journal of Science and Technology 9, 5

A Power Saving Multiplication Algorithm 2016
S Subha, R Sakthivel
International Journal of Applied Engineering Research 11 (9), 6200-6203

Comparison of Weibull parameters computation methods and analytical estimation of wind turbine capacity factor using polynomial power curve model: case study of a wind farm 2015
BK Saxena, KVS Rao
Renewables: Wind, Water, and Solar 2 (1), 3

Efficient VCO using FinFET 2015
S Saxena, M Srikanth, S Jawale, R Sakthivel
Indian Journal of Science and Technology 8 (S2), 262-270

Low Power Modulo 2n+ 1 Multiplier Using Data Aware Adder Tree 2015
R Sakthivel, M Vanitha, K Sanapala, K Thirumalesh
Procedia Computer Science 70, 355-361