Name of the faculty: Dr. D. S. Shylu
Designation: Associate Professor
Department: Electronics and Communication Engineering,
Institution: Karunya Institute of Technology and Sciences
Karunya Nagar, Coimbatore, Tamil Nadu 641114
Email ID: shylusam@karunya.edu
Mobile No: 94872 24478
Area of Interest: VLSI Design

Publications:

INTERNALTIONAL JOURNAL:

1. Vimukth John,D.S.Shylu,S.Radha,P.Sam Paul,Joel, (2020)Design of a power efficient Kogge-Stone Adder by exploring new OR gate in 45nm CMOS Process ,International Journal of Circuit World, Vol. 46 No. 4, pp. 257-269.

2. D. S. Shylu, P. Sam Paul, D. Jackuline Moni, J. Arolin Monica Helan,(2020) A Power efficient Delta-Sigma ADC with Series-Bilinear Switch Capacitor VCO,Telekomnika,Vol.18,No.5.
3. Radha S.,Shylu D.S, Nagabushanam P.(2019) "Power efficient low latency architecture for decoder: Breaking the ACS bottleneck" International Journal of Circuit Theory and Applications, John Wiley,Volume 47, Issue 9, 1513-1528.

4. Radha S. Shylu D.S,Nagabushanam,Mathew,Jisha. (2019) "Low Noise Amplifier with resistive and capacitive feedback for 2.4GHz RF receiver front end", Journal of High Speed Networks,vol.25,No.2,181-203.

5. Sam Paul, P., Shylu, D.S., Varadarajan, A.S., (2017) Prediction of fusion-based tool wear with signals from inbuilt sensor turning tool, International Journal of Advanced Mechatronic Systems, 7(6), pp. 368-377.Published online on April 2019.

6. D.S. Shylu Sam, S. Radha, D. Jackuline Moni, P. Sam Paul, J. Jecintha, (2019) "Design of 1-V, 12-Bit Low Power Incremental Delta Sigma ADC for CMOS Image Sensor Applications" , International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-7, Issue-5S3, February 2019 ,249-254.

7. D.S.Shylu, A.Christina Roseline(2018)" Performance Analysis of Array Multiplier Using Low Power 10T Full Adder" Springer SIST Series**.** 277-285.

8. Radha, S., Shylu, D.S., Nagabushanam, P., Sunitha Kumari, J(2018). Design of RF LNA with resistive feedback and gain peaking for multi-standard application,International Journal of Recent Engineering & Technology, 7(4), pp. 100-107.

9. Shylu D.S.,Jackuline Moni D.,Nivetha G.(2016) “Design and Power Optimization of High-Speed Pipelined ADC with Programmable Gain Amplifier for Wireless Receiver Applications”, Wireless Personal Communication, Springer,90,657-678.

10. Shylu D.S., Jackuline Moni D., (2016),“Design of low power dynamic comparator with reduced kick back noise using clocked PMOS technique”, Journal of Electrical Engineering (JEE), **16(3),1-10.**

11. Shylu D.S,Jackuline Moni D.,Divya M.,(2016) “ Post Layout Simulation and Analysis of 10-bit low power Pipelined ADC ”, International Journal of Science and Innovative Engineering & Technology.5(1).

INTERNATIONAL CONFERENCE:

1. Shylu D.S.,Jackuline Moni D. and Renita Pearlin T. (2016) “A 10-bit 40MS/s low power SHA-less pipelined ADC for System –On-Chip Digital TV Application”, ICDCS,305-309.

2. Shylu D.S.,Jackuline Moni D.,Jecintha J. (2017) “Design of low power CMOS circuits for high performance 12-bit Incremental delta–sigma ADC”, International Conference on Latest Trends in Science, Engineering and Technology(ICLTSET’17), 178-182.

3. D.S.Shylu Sam,J.Arolin,D.Jackuline Moni (2018) “ Design of 12 Bit 100MS/s Low Power Delta Sigma ADC Using Telescopic Amplifier, International Conference on Circuits,Devices and Systems (ICDCS’18),263-265.

4. D.S.Shylu,S.Jasmine,D.Jackuline Moni(2018)” A Low Power Dynamic Comparator for a 12-bit Pipelined Successive Approximation Register (SAR) ADC” International Conference on Circuits,Devices and Systems (ICDCS’18),339-342.

NATIONAL CONFERENCE:

1. Sushmita Selvadass Shylu Sam D.S.,(2017)”Design of a Digital code lock using VHDL” National Conference on Innovations in Future Communication Technologies (NCIFCT’17), Karunya University,Coimbatore,pp.177-181.

2. Benita Poul raju D.,Shylu Sam D.S.,Benita.B,Dharani,Gracy,(2017)”Low Power 4-bit full adder using GDI technique with sleep transistor” National Conference on Innovations in Future Communication Technologies (NCIFCT’17), Karunya University,Coimbatore,pp.137-140.

3. Shylu Sam D.S., Judson Princy Nesa Mary, Sherin Varghese, Soumya Mathew (2017)” Design of Low Power Fat Tree Encoder ” National Conference on Innovations in Future Communication Technologies (NCIFCT’17), Karunya University,Coimbatore,pp.74-77.

4. D.S Shylu, J.Murali Shankar, B.MarcelloSamprass, M.Harish Reddy ,Design and implementation of modified tollbooth system using FPGA, 2nd National Conference on Innovations in Future Communication Technologies ,NCIFCT’18,pp.7.