Dr.N.B.Balamurugan Publication List

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Publications in Books and Proceedings:

1. **N.B. Balamurugan** 2019. Analytical Modeling of High Electron Mobility Transistors in Handbook for III-V High Electron Mobility Transistor Technologies. CRC Press, https://doi.org/10.1201/9780429460043.
2. S. Rajaram, **N.B.Balamurugan**, D. G. N. Rani, and V. Singh, "VLSI Design and Test: 22nd International Symposium, VDAT 2018, Madurai, India, June 28-30, 2018, Revised Selected Papers," 2019.
3. **N.B.Balamurugan,** Laboratory manual of Signals and Systems for National Instruments Banglore, 2009.
4. **N.B.Balamurugan,** Laboratory manual of Digital Signal processing for National Instruments Banglore, 2009.

Publications in Journals:

1. M. Venkatesh, M. Suguna, and **N.B.Balamurugan**, "Influence of Germanium Source Dual Halo Dual Dielectric Triple Material Surrounding Gate Tunnel FET for Improved Analog/RF Performance," *Silicon*, pp. 1–9, 2020.
2. M. Venkatesh and **N.B.Balamurugan**, "Influence of Threshold Voltage Performance Analysis on Dual Halo Gate Stacked Triple Material Dual Gate TFET for Ultra Low Power Applications," *Silicon*, pp. 1–13, 2020.
3. I. S. Arafat, **N.B.Balamurugan**, and S. B. Khan, "Influence of Temperature in Scattered SiNW MOSFET," *Proceedings of the National Academy of Sciences, India Section A: Physical Sciences*, vol. 89, no. 1, pp. 35–40, 2019.
4. G. Lakshmi Priya and **N.B.Balamurugan**, "New dual material double gate junctionless tunnel FET: Subthreshold modeling and simulation," *AEU-International Journal of Electronics and Communications*, vol. 99, pp. 130–138, 2019.
5. B. Buvaneswari and **N.B.Balamurugan**, "2D analytical modeling and simulation of dual material DG MOSFET for biosensing application," *AEU-International Journal of Electronics and Communications*, vol. 99, pp. 193–200, 2019.
6. B. Buvaneswari and **N.B.Balamurugan**, "Sensitivity Analysis of Double Gate Metal Oxide Semiconductor Field Effect Transistor for Bio-Sensing Applications," *Journal of Nanoelectronics and Optoelectronics*, vol. 14, no. 1, pp. 136–145, 2019.
7. K. Sowmya, **N. B. Balamurugan**, and V. Parvathy, "A 2-D Modeling of Fe doped Dual Material Gate AlGaN/AlN/GaN High Electron Mobility Transistors for High Frequency

Applications," *AEU-International Journal of Electronics and Communications*, vol. 103, pp. 46–56, 2019.
8. V. Dharshana, **N. B. Balamurugan**, and T. S. Samuel, "An Analytical Modeling and Simulation of Surrounding Gate TFET with an Impact of Dual Material Gate and Stacked Oxide for Low Power Applications," *Journal of Nano Research*, vol. 57, pp. 68–76, 2019.
9. M. Venkatesh and **N. B. Balamurugan**, "New subthreshold performance analysis of germanium based dual halo gate stacked triple material surrounding gate tunnel field effect transistor," *Superlattices and Microstructures*, vol. 130, pp. 485–498, 2019.
10. M. Venkatesh, M. Suguna, and **N. B. Balamurugan**, "Subthreshold performance analysis of germanium source dual halo dual dielectric triple material surrounding gate tunnel field effect transistor for ultra low power applications," *Journal of Electronic Materials*, vol. 48, no. 10, pp. 6724–6734, 2019.
11. S. Manikandan, **N. B. Balamurugan**, and T. S. A. Samuel, "Impact of uniform and non-uniform doping variations for ultrathin body junctionless FinFETs," *Materials Science in Semiconductor Processing*, vol. 104, p. 104653, 2019.
12. S. Manikandan, **N. B. Balamurugan**, and D. Nirmal, "Analytical Model of Double Gate Stacked Oxide Junctionless Transistor Considering Source/Drain Depletion Effects for CMOS Low Power Applications," *Silicon*, pp. 1–11, 2019.
13. L. Priya, **N.B.Balamurugan** "Subthreshold Modeling of Triple Material Gate-All-Around Junctionless Tunnel FET with Germanium and High-K Gate Dielectric Material," *Informacije MIDEM*, vol. 48, no. 1, pp. 53–62, 2018.
14. T. V. Kumar and **N.B.Balamurugan**, "Analytical modeling of InSb/AlInSb heterostructure dual gate high electron mobility transistors," *AEU-International Journal of Electronics and Communications*, vol. 94, pp. 19–25, 2018.
15. B. Buvaneswari, **N.B.Balamurugan**, and others, "Comparative analytical analysis of various configurations of nanoscaled dielectric-modulated double gate MOSFET based biosensors," *Journal of Optoelectronics and Advanced Materials*, vol. 20, no. September-October 2018, pp. 526–536, 2018.
16. M. Jothi, **N.B.Balamurugan**, and R. H. Kumar, "Performance Analysis of Fuzzy processor for a Healthcare Application-Diabetic Epilepsy Risk Classifier," *Asian Journal of Research in Social Sciences and Humanities*, vol. 7, no. 2, pp. 124–140, 2017.
17. I. S. Arafat and **N.B.Balamurugan**, "Influence of scattering in near ballistic silicon nanowire metal-oxide-semiconductor field effect transistor," *Journal of nanoscience and nanotechnology*, vol. 16, no. 6, pp. 6032–6036, 2016.
18. P. Vanitha, G. L. Priya, **N.B.Balamurugan**, S. T. Chandra, and S. Manikandan, "Analytical Approach on the Scale Length Model for Tri-material Surrounding Gate Tunnel Field-Effect Transistors (TMSG-TFETs)," in *Intelligent Computing and Applications*, Springer, New Delhi, 2015, pp. 231–238.
19. D. Saraswathi, **N.B.Balamurugan**, G. L. Priya, and S. Manikandan, "A compact analytical model for 2D triple material surrounding gate nanowire tunnel field effect transistors," in *Intelligent Computing and Applications*, Springer, New Delhi, 2015, pp. 325–332.
20. Vimala Palanichamy and **N.B.Balamurugan**, "COMPARATIVE ANALYSIS OF QUANTUM EFFECTS IN NANO-SCALE MULTIGATE MOSFETS USING VARIATIONAL APPROACH," *Journal of Engineering Science and Technology*, vol. 10, no. 2, pp. 224–234, 2015.
21. S. Theodore Chandra, **N.B.Balamurugan**, G. L. Priya, V. Muralidharan, D. S. S. R. RANI, and others, "Compact modeling of gate engineered triple material gate (TMG) AlInSb/InSb high electron mobility transistors," *Journal of Optoelectronics and Advanced Materials*, vol. 17, no. January-February 2015, pp. 222–228, 2015.

22. S. Theodore Chandra, **N.B.Balamurugan**, M. Bhuvaneswari, N. Anbuselvan, and N. Mohankumar, "Analysis of charge density and Fermi level of AlInSb/InSb single-gate high electron mobility transistor," *Journal of Semiconductors*, vol. 36, no. 6, p. 64003, 2015.
23. S. Theodore Chandra, **N. B. Balamurugan**, G. L. Priya, and S. Manikandan, "Subthreshold behavior of AlInSb/InSb high electron mobility transistors," *Chinese Physics B*, vol. 24, no. 7, p. 76105, 2015.
24. G. L. Priya, **N. B. Balamurugan**, and D. Saraswathi, "Impact of Electricfield Distribution on the performance of Dual Material Gate Work function Engineered Surrounding Gate Nanowire Tunnel FETs," *International Journal of Applied Engineering Research*, vol. 10, no. 1, pp. 1018–1023, 2015.
25. P. Vanitha, **N. B. Balamurugan**, and G. L. Priya, "Triple material surrounding gate (TMSG) nanoscale tunnel FET-analytical modeling and simulation," *Journal of Semiconductor Technology and science*, vol. 15, no. 6, pp. 585–593, 2015.
26. T. S. Arun Samuel, **N. B. Balamurugan**, S. Bhuvaneswari, D. Sharmila, and K. Padmapriya, "Analytical modelling and simulation of single-gate SOI TFET for low-power applications," *International Journal of Electronics*, vol. 101, no. 6, pp. 779–788, Jun. 2014, doi: 10.1080/00207217.2013.796544.
27. P. S. Dhanaselvam and **N. B. Balamurugan**, "Performance analysis of fully depleted triple material surrounding gate (TMSG) SOI MOSFET," *Journal of Computational Electronics*, vol. 13, no. 2, pp. 449–455, 2014.
28. I. S. Arafat, **N. B. Balamurugan**, and C. Priya, "Effects of roughness scattering in carrier transport of near ballistic silicon nanowire MOSFET," in *Applied Mechanics and Materials*, 2014, vol. 573, pp. 201–208.
29. S. T. Chandra and **N. B. Balamurugan**, "Performance analysis of silicon nanowire transistors considering effective oxide thickness of high-k gate dielectric," *Journal of Semiconductors*, vol. 35, no. 4, p. 44001, 2014.
30. P. T. Mary and **N. B. Balamurugan**, "Performance Analysis of Silicon and Germanium Nanowire Transistor using Crystal Orientation and Oxide Thickness," *International Journal of Advanced Computer Research*, vol. 4, no. 3, p. 898, 2014.
31. P. S. Dhanaselvam and **N. B. Balamurugan**, "A 2D sub-threshold current model for single halo triple material surrounding gate (SHTMSG) MOSFETs," *Microelectronics Journal*, vol. 45, no. 6, pp. 574–577, 2014.
32. T. S. Arun Samuel and **N. B. Balamurugan**, "Analytical modeling and simulation of germanium single gate silicon on insulator TFET," *Journal of Semiconductors*, vol. 35, no. 3, p. 34002, 2014.
33. S. Theodore Chandra, **N. B. Balamurugan**, G. Subalakshmi, T. Shalini, and G. L. Priya, "Compact analytical model for single gate AlInSb/InSb high electron mobility transistors," *Journal of Semiconductors*, vol. 35, no. 11, p. 114003, 2014.
34. M. K. Pandian and **N. B. Balamurugan**, "Analytical threshold voltage modeling of surrounding gate silicon nanowire transistors with different geometries," *Journal of Electrical Engineering & Technology*, vol. 9, no. 6, pp. 2079–2088, 2014.
35. T. S. Arun Samuel, **N. B. Balamurugan**, T. Niranjana, and B. Samyuktha, "Analytical Surface potential model with TCAD simulation verification for evaluation of Surrounding Gate TFET," *Journal of Electrical Engineering and Technology*, vol. 9, no. 2, pp. 655–661, 2014.
36. P. S. Dhanaselvam, **N. B. Balamurugan**, G. C. V. Chakaravarthi, R. P. Ramesh, and B. R. S. Kumar, "A 2d analytical modeling of single halo triple material surrounding gate

(SHTMSG) mosfet," *Journal of Electrical Engineering & Technology*, vol. 9, no. 4, pp. 1355–1359, 2014.
37. P. Vimala and **N. B. Balamurugan**, "Modeling and simulation of nanoscale tri-gate MOSFETs including quantum effects," *Journal of Semiconductors*, vol. 35, no. 3, p. 34001, 2014.
38. **N. B. Balamurugan**, S. Sudha, J. Jasmine, and others, "Analysis of Tunnelling Rate Effect on Single Electron Transistor," *Journal of Electrical Engineering & Technology*, vol. 9, no. 5, pp. 1670–1676, 2014.
39. P. Vimala and **N. B. Balamurugan**, "Analytical modeling of quantization effects in surrounding-gate MOSFETs," *COMPEL: Int J for Computation and Maths. in Electrical and Electronic Eng.*, vol. 33, no. 1–2, pp. 630–644, 2014.
40. P. Vimala and **N. B. Balamurugan**, "A Compact Quantum Model for Cylindrical Surrounding Gate MOSFETs using High-k Dielectrics," *Journal of Electrical Engineering and Technology*, vol. 9, no. 2, pp. 649–654, 2014.
41. P. Vimala and **N. B. Balamurugan**, "New analytical model for nanoscale tri-gate SOI MOSFETs including quantum effects," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 1, pp. 1–7, 2014.
42. T. S. Arun Samuel and **N. B. Balamurugan**, "An analytical modeling and simulation of dual material double gate tunnel field effect transistor for low power applications," *Journal of Electrical Engineering and Technology*, vol. 9, no. 1, pp. 247–253, 2014.
43. M. K. Pandian, **N. B. Balamurugan**, and S. Manikandan, "Analytical Modeling of Junctionless Surrounding Gate Silicon Nanowire Transitors," *Journal of Nanoelectronics and Optoelectronics*, vol. 9, no. 4, pp. 468–473, 2014.
44. G. L. Priya and **N. B. Balamurugan**, "Triple Material Gate Work Function Engineering in Surrounding Gate Nanoscale MOSFETs for reduced Short Channel Effects (SCE's): Scale Length Model," *International Journal of ChemTech Research*, vol. 7, no. 2, pp. 1005–1013, 2014.
45. M. K. Pandian, **N. B. Balamurugan**, and S. Manikandan, "Analytical IV Modeling of Accumulation Mode Cylindrical Surrounding Gate Nanowire Mosfets," *International Journal of Applied Engineering Research*, vol. 9, no. 22, pp. 17745–17758, 2014.