

Dr.S.Sudha

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5. Ramesh, K & Sudha. S, 2017, ‘FPGA Implementation of High Speed and Low Power Viterbi Decoder Using Reverse Algorithm of Convolution Encoder’, Journal of Computational and Theoretical Nanoscience, vol.14, no 12, pp. 5957–5962 (Scopus) IF:1.66
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11. Dr.S.Sudha,S.Sridharan,” Real Time implementation of PID controller for Switched Reluctance Motor”,Pak.Journal of Biotechnology.Vol 13,PP.533-537(2016).(Scopus) Impact factor:0.25
12. Dr.S.Sudha,S.Sridharan,”High Frequency Charging Techniques-Grid connected powr generation using switched reluctance Generator”,Journal of Circuits and Systems,Volume-7,4308-4313,2016.(Scopus) IF: 0.595
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14. Dr. S. Sudha ,P.Meenakshividhya,” Realization of Flexible Multiband Divider with Integrated program and Swallow Counters, International Journal Of Applied Engineering Research, ISSN: 0973-4562, Vol.10, No. 38, pp.28811-28816, 2015.
15. Dr. S. Sudha ,P.Meenakshividhya,” Power Analysis of Spread Spectrum Clock Generation in Digital Devices, International Journal Of Applied Engineering Research, ISSN: 0973-4562, Vol.10, No.38, pp.. 28959 – 28964, 2015.
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