

Dr.D.Gracia Nirmala Rani, Assistant Professor/ECE

Journals Publication:

1. Andrew Roobert.A & D. Gracia Nirmala Rani,"Design and analysis of a sleep and wakeup CMOS low noise amplifier for 5G applications",Springer TeleCommunication Systems 2020, <https://doi.org/10.1007/s11235-020-00729-y>.
2. G. Giftha, D. Gracia Nirmala Rani, and D. Nirmal,"A 1-V, 5 μ W, Atto Current Bulk-Driven CMOS Based Operational Transconductance Amplifier for Biosensor Applications",ECS Journal of Solid State Science and Technology, 2020 9 115003.
3. Andrew Roobert and D. Gracia Nirmala Rani,"Design and analysis of 0.9 and 2.3-GHz concurrent dual-band CMOS LNA for mobile communication",International Journal of Circuit Theory and Applications, Wiley Publications 2019; pp 1–14.DOI: 10.1002/cta.2688.
4. A.Andrew Roobert, D.Gracia Nirmala Rani, S.Rajaram, "Design and Optimization of Feed Forward Noise Cancelling CMOS LNA for 2.4 GHz WLAN Applications" in IET Circuits, Devices and Systems, Impact Factor 1.395, May 2019. DOI: 10.1049/iet-cds.2018.5291.
5. A.Andrew Roobert, D.Gracia Nirmala Rani,"Survey on parameter optimization of mobile communication band low noise amplifier design",International Journal of RF and Microwave Computer-Aided Engineering (Wiley Publication)Vol. 29, Issue 7,pp 1-16,2019,DOI: <https://doi.org/10.1002/mmce.217>.
6. M.R.Sheeba, D.Gracia Nirmala Rani," PLACEMENT OF TSVS IN THREE DIMENSIONAL INTEGRATED CIRCUITS (3D IC)", International Journal of Pure and Applied Mathematics, Volume 117 No. 16 2017, 179-184 ISSN: 1311-8080 (printed version); ISSN: 1314-3395 (on-line version)
7. Gracia Nirmala Rani.D & Rajaram.S 2016 , 'Analysis and Design Of VLSI Floorplanning Algorithms For Nano-Circuits' International Journal of Advanced Engineering Technology, Vol. VII/Issue I/Jan.-March., 2016/527-532.
8. G. Rajakumar,A. Andrew Roobert,T. S. Arun Samuel, D. Gracia Nirmala Rani,"Low power VLSI architecture design of BMC, BPSC and PC schemes",Springer Analog Integrated Circuits and Signal Processing(2017),pp1-10. ISSN: 0925-1030 (Print) 1573-1979 (Online), <https://doi.org/10.1007/s10470-017-1025-0>.
9. Gracia Nirmala Rani, D & Rajaram, S, 'A Novel Differential Evolution based optimization algorithm for Non-Sliceable VLSI Floorplanning', Iranian Journal of Science and Technology Transaction A, Article 5, Volume 39, Issue 3.1, Autumn 2015, Page 375-382.
10. D.Gracia Nirmala Rani, Amalin Marina, V.Dharshana & s.Rajaram,"Testing of Reversible Logic Circuits using automatic Test pattern generation techniques", International journal of Applied Engineering Research, Vol.27, No.4,2015,pp 553 – 558.
11. G. Nallathambi, D. Gracia Nirmala Rani and S. Rajaram,"Thermal Aware Floor planning Technique for Nano Circuits",Research Journal of Applied Sciences, Engineering and Technology 8(10): 1279-1284, 2014.ISSN: 2040-7459; e-ISSN: 2040-7467
12. Nithya, A. G. Priyanka, B. Ajitha, D. Gracia Nirmala Rani, S. Rajaram, 'FPGA implementation of low power and area efficient carry select adder', International Journal of Enhanced Research in Science, Technology & Engineering, Vol. 3,Issue 6, June- 2014. (ISSN No: 2319-7463, Impact Factor : 1.252)

13. D.Gracia Nirmala Rani & S.Rajaram , "Temperature Driven Non-sliceable VLSI Floor Planning For 3D Integrated Circuits," Wulfenia Journal vol. 20, No.3, 2013
14. D.Gracia Nirmala Rani and S.Rajaram , " A Survey on B*tree based Evolutionary Algorithms for VLSI Floorplanning Optimizations", International Journal of Computer Application in Technology, Vol 48 N3, pp 1-10,2013
15. D.Gracia Nirmala Rani ,S.Rajaram, Athira Sudarsan , " A Novel 3D algorithm for VLSI Floorplanning," Proc. of SPIE, Vol. 8760 87601S-1-5,2013
16. D.GraciaNirmalaRaniPerformance Driven VLSI FloorPlanning With B*tree Representation using different Evolutionary Algorithm -JournalSpringerLink,Trends in Network and Communication, Communication in Computer and Information science, Vol 197,pp 445-456,2011
17. D.GraciaNirmalaRani,D.JaclulineMoniVLSI Floorplanning Relying on Differential Evolution Algorithm, ICGST,International Journal on Artificial Intelligence and Machine Learning AIML, Vol.7,Issue 1 pp62-67

Conferences

1. Dhanusa Sri Sudhagaram and D.Gracia Nirmala Rani," Thermal Energy Harvesting using CMOS Techniques for Internet of Medical Things", International Conference on Innovative Trends In Information Technology (ICITIIT- 20) on 13 & 14 February 2020, at Indian Institute of Information Technology (IIIT), Kottayam.
2. Shanthi J, Gracia Nirmala Rani D and Rajaram S,"A Novel Machine Learning Based MultiObjective Memetic Algorithm (ML-MOMA) for 3D IC Floorplanning", 2020 International Conference on VLSI Design, 4-8th 2020 held at Bengaluru.
3. Dhanusa Sri Sudhagaran and D. Gracia Nirmala Rani"Develop An Energy Harvesting Technique For Wearable Biomedical Devices", TEQIP - III sponsored International Conference on Instrumentation and Control Engineering ICECON-2019 held at Department of Instrumentation and Control EngineeringNational Institute of Technology Tiruchirappalli – 620015 during 19th - 21st December, 2019.
4. Dr.D.Gracia Nirmala Rani G.Gifta M.Meenakshi C.Gomathy and T.Gowsalaya, "Design and Analysis of CMOS Low Power OTA for Biomedical Applications", 4th IEEE International Conference on Recent Trends in Electronics, Information and Communication Technologies held at Sri Venkateshwara College of Engineering, Bangalore from 17th to 18th May, 2019.
5. A.Andrew Roobert, D.Gracia Nirmala Rani, M.Divya, S.Rajaram,"Design of CMOS based LNA for 5G Wireless Applications", ProceedingICCBN 2018 Proceedings of the 6th International Conference on Communications and Broadband Networking, Pages 43-47, Singapore, Singapore — February 24 - 26, 2018.
6. G. Gifta, D. Gracia Nirmala Rani, Nifasath Farhana, and R. Archana, "Design of CMOS Based Biosensor for Implantable Medical Devices", Proceedings of 22nd International Symposium, VDAT 2018, Published in Communications in Computer and Information Science, Springer, DOI:10.1007/978-981-13-5950-7.

7. M.R.sheeba, D.Gracia Nirmala Rani,"Placement of TSVs in Three Dimensional Integrated Circuits (3D-IC),2nd International Conference on Recent Trends in Engineering and Techhnology (ICRTET), St.Joseph's Institute of Technology, OMR, Chennai, 5-6th May,2017
8. M.Sarojini, D.Gracia Nirmala Rani, G. Divya Preethi,"3D-IC partitoning and TSV Sharing Optimization Algorithm"International Conference on Computing, Communication, Nanophotonics, Nanoscience, Nanomaterials and Nanotechnology (12C4N-2K16) held on Holy Grace Academy of Engineering, Ernakulam, Kerala, India, 7th-8th April, 2016.
9. D.Gracia Nirmala Rani¹,C.Mathumitha², R.Priyadharshini³ and S.Rajaram,"Design and Implementation Of Configurable Logic Block Of An Fpga Using Quantum Dot Cellular Automata " Third International IEEE Conference on Devices, Circuits and Systems (ICDCS'16),Karunya University3rd – 5th, Mar 2015.
10. D. Gracia Nirmala Rani¹,M. Saranya²,T. Sivashankari³,N.Meenakshi⁴,R.Meena⁵, S.Rajaram, " Design Of Static Random AccessMemory Using QCA Technology ",Third International IEEE Conference on Devices, Circuits and Systems (ICDCS'16),Karunya University, 3rd – 5th, Mar 2015.
11. Gracia Nirmala Rani.D ,Kavya.K, Kavitha.A, ,Keerthana.P , " ASIC Low Power Implementation Using Multi-Bit Flip Flops Techniques",National Conference on Wireless and Communication Systems, Thiagarajar College of Engineering,18 -19 April, 2014.
12. D.Gracia Nirmala Rani,Dr.S.Rajaram & Athira sudrasan," A Noval 3D algorithm For VLSI Floorplanning",Internationa Conference on Electronics and Communication System Design,Malaviya National Institute of Technology,Jaipur, India,2013
13. D.Gracia Nirmala Rani M.G.Mangala Meenakshi S.Amalin Marina,"Low Hardware Overhead implementation of 3-weight pattern generation technique for VLSI testing",Second IEEE International Conference on Devices, Circuits and Systems (ICDCS'14),Karunya University,6th -8th March, 2014
14. D.Gracia Nirmala Rani ,S.Rajaram, J.Prabha, " B* Tree Based Thermal Aware Non Sliceable Floorplanning, International Conference on System Engineering, Srinivasan Engineering College, Perambalur,TamilNadu,17th May,2013.
15. D.Gracia Nirmala Rani," Ph.D Forum on VLSI Physical Design Automation for Wireless communication systems" 16th VLSI Design Automation and Test (VDAT'12), Jadavpur University, Kolkata. ,01-07-2012 to 04-07-2012
16. D.Gracia Nirmala Rani ,S.Rajaram, Athira Sudarsan, Nivathitha," Thermal Aware Modern VLSI Floorplanning, IEEE Xplore, IEEE International Conference on Devices, Circuits and Systems(ICDCS),15-16 Mar,pp187-190, 2012.
17. D.Gracia Nirmala Rani and S.Rajaram Optimization in VLSI Floor planning using Differential Evolutionary, International Silver Jubilee Conference on Communications Technologies and VLSI Design, Oct8-10,2010,VIT Vellore, 2009
18. D.Gracia Nirmala Rani, S.Rajaram, Vimal Mohan," VLSI Floorplanning Area Optimization Using Genetic & Memetic Algorithm," National /Second National Conference on Explorations & iNnovations in Advanced Computing, Mar2-4, 2009, National Engineering College, Kovilpatti.

19. D.Gracia Nirmala Rani , S.Rajaram, Athira Sudarsan ,” A Novel 3D algorithm for VLSI Floorplanning,” IEEE International Conference on Communication and Electronics System Design, Malaviya National Institute of Technology, Jaipur, 28-29 Jan, 2013.

Books

1. Gracia Nirmala Rani D, Shanthi, J, & Rajaram S "Machine Learning Optimization Techniques for 3D IC Physical Design." Handbook of Research on Emerging Trends and Applications of Machine Learning, edited by Arun Solanki, et al., IGI Global, 2020, pp. 47-61. <http://doi:10.4018/978-1-5225-9643-1.ch003>
2. S. Rajaram,N. B. Balamurugan,D. Gracia Nirmala Rani,Virendra Singh (Eds.)Book Editor, VLSI Design and Test, Springer Communications in Computer and Information Science, ISSN 1865-0937 (electronic) ISBN 978-981-13-5950-7
3. G. Gifta, D. Gracia Nirmala Rani, Nifasath Farhana, and R. Archana, “Design of CMOS Based Biosensor for Implantable Medical Devices”, Proceedings of 22nd International Symposium, VDAT 2018, Published in Communications in Computer and Information Science, Springer, DOI:10.1007/978-981-13-5950-7.
4. Gracia Nirmala Rani D and Rajaram S(Book Chapter Author) "Performance Driven VLSI Floorplanning with B*tree representation using differential Evolutionary Algorithm"Springer Lecture Notes in Computer Science,2011 Springer, Berlin, Heidelberg,Print ISBN 978-3-642-22542-0DOI:https://doi.org/10.1007/978-3-642-22543-7_45

Industry Interactions

COMPANY NAME	NATURE OF WORK	PERIOD	DETAILS
1. MicroChip Technology Cooperation, Chennai	One credit course offered by them.	12-11-2019 to 02-01-2020	Curriculum Design
2. Cadence Design Systems Pvt.Ltd, Bangalore Company	Participated Contest instituted by Cadence Collaborative student Projects	01-06-2011 to 14-11-2019	