Faculty

Dr. Binsu J Kailath

Associate Professor

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Education

IIT Madras	**Chennai**
PhD in Ultra Thin Oxide MOS Devices, Dept. of Electrical Engineering	2003 - 2007
IIT Madras	**Chennai**
M.Tech. in MicroElectronics and VLSI Design, Dept. of Electrical Engineering	1999 - 2001
University of Calicut	**Kerala**
B.Tech. in Electronics and Communication Engineering	1988 - 1992

Specialization

- Micro Electronics and VLSI Design

- Mixed Signal IC Design
- Neuromorphic Circuits
- Microelectronics and MEMS

Honours + Awards + Recognitions

- Lower Secondary School Scholarship (1980)
- Upper Secondary School Scholarship (1983)
- National Merit Scholarship (1986)
- President's Guide Award from the President of India (1986)
- DAAD fellowship for post-doctoral research, 2011
- Best Paper Award in INDICON 2015 held in New Delhi in Dec. 2015
- Industry Ready Technology award in the '' IEEE TECHSYM 2016, IIT Kharagpur, 27/09/16 - 02/10/16
- Reviewer for IEEE Transactions on Circuits And Systems II (TCAS II)
- Reviewer for Microelectronics Journal by Elsevier
- Reviewer for Materials Science and Engineering B Journal by Elsevier
- Member, Board of Studies, IIITDM Kurnool

Work Experience

Teaching

- Faculty Member in Electronics Engineering in College of Engineering, Chengannur, Kerala, for 8 years
- Faculty Member in Electronics Engineering in IIITDM Kancheepuram from Oct 2008

Research

- Switch Capacitor circuit simulator Development (ongoing)
- Sigma Delta ADC (ongoing, fabrication is planned in SCL, Punjab under SMDP-C2SD sponsored
- by MeitY))

- Fabrication, characterization and extraction of conduction Mechanisms in SiC MIS Capacitors with High-k dielectrics of which fabrication and characterization was carried out in Centre for Nano Science and Engg, IISc Bangalore through INUP (completed)
- In the sponsored project ???Novel Oxidation Techniques for improvement in the Electrical properties of Ultra-thin SiO2 for VLSI technology??? coordinated by Prof. Nandita DasGupta in Microelectronics and MEMS Laboratory, Dept. of Electrical Engineering, IIT Madras (completed)
- Study of Novel gate oxidation techniques for future MOS devices (completed)
- Study of high-k gate dielectrics for future MOS devices (completed)
- Study of Laser Induced Oxidation as a viable technique to grow ultra thin SiO2 (completed)
- Study of Rapid thermal Oxidation technique to grow ultra thin SiO2 (completed)
- Optimization of HNO3 Vapour oxidation technique to grow ultra thin SiO2 (completed)
- Study of the effect of phosphorus doping on passivation of grain boundaries in poly Si TFTs (completed)

Professional Membership

- Member, IEEE
- Life Member, ISTE

Professional Service

- Member, Board of Studies, IIITDM Kurnool
- CURRICULUM DEVELOPMENT
- B Tech programme:
- Electronics Engg Design and Manufacturing curriculum adopted for 2008 to 2013 batches admissions
- Electronics and Communication Engineering Design and Manufacturing curriculum adopted from 2014 batch admissions
- Dual degree programme:

- M Des programme:
- Electronic Systems adopted for admissions from 2010 - 2016
- STREAM COORDINTAOR
- Electronics Engineering (2008-2013)
- M DES AND PHD ADMISSION COORDINATOR (2009 - 2014)
- DESIGNERS??? CLUB COORDINATOR (2011 - 2014)
- CHAIRPERSON, DISCIPLINARY COMMITTEE (2012- 2014)
- WOMEN???S FORUM COORDINATOR (2009 - 2015)
- GUIDANCE AND COUNSELING (2011 - 2015)

Teaching

- ELE 101, ELE 103T Basic Electrical and Electronics Engg (2008, 2014, 2015, 2016)
- ELE 106 Digital Logic Design (2011, 2012)
- ELE 203 Control Systems (2009)
- ELE 206 Networks and Systems (2009, 2010)
- ELE 213, ELE 223T Analog Circuits (2009, 2010, 2011, 2012, 2013, 2014, 2015, 2018)
- ELE 306 Analog IC Applications (2010, 2011, 2012)
- ELE 501 Design and Applications of Analog ICs (2011, 2012, 2013)
- MEMS (2012, 2014)
- ELE 302T Electronic Manufacturing and Prototyping (2016)
- ELE 311 VLSI Design (2015, 2016)
- ELE 318T Digtal IC Design (2017, 2019)
- ELE 522T Analog IC Design (2017, 2018, 2019)
- ELE 411T Digital Systems Engineering (2018, 2019)

Books

- Book Chapter
- Binsu J Kailath, Abdul Majeed K. K., ???Composite PFD based Low Power Low Noise Fast Lock-in PLL,??? in VLSI and Post-CMOS Devices, Circuits and

Journal Publications

- International Refereed Journals
- E. Papanasam, Binsu J Kailath (2019) “Extraction and Analysis of Gate Leakage Current Mechanism in Silicon Carbide (SiC) MIS Capacitors", Accepted for Publication in IETE Journal of Research
- Manne SaiSravan, SudhaNatarajan, Eswar SaiKrishna, Binsu JKailath (2018) “Fast and accurate on-road vehicle detection based on color intensity segregation”, Procedia Computer Science, Vol. 133, pp 594-603
- E. Papanasam, Binsu J Kailath (2018),”Effect of Post Deposition Annealing and Post Metallization Annealing on Electrical and Structural Characteristics of Pd/Al2O3/6H-SiC MIS Capacitors”, Microelectronics International, Vol. 35, Issue 2, pp 65-73.
- Abdul Majeed and Binsu Kailath (2018), “Novel PLL Architecture with a Composite PFD and variable Loop Filter” IET Circuits, Devices & Systems, Volume: 12 , Issue: 3 , 5 pp 256 - 262
- Abdul Majeed, K.K. Kailath, B.J. (2017) "Low power PLL with reduced reference spur realized with glitch-free linear PFD and current splitting CP", Analog Integrated Circuits and Signal Processing, Vol. 93, number 1, pp 29-39
- E.Papanasam and Binsu J Kailath (2017), “Improvement on the electrical characteristics of Pd/HfO2/6H-SiC MIS capacitors using post deposition annealing and post metallization annealing” Applied Surface Science, 413, 66–71

Conference Publications

- Amrutha Manoharan, Gadamsetty Muralidhar, Binsu J Kailath, ’A Novel Method to Implement STDP Learning Rule in Verilog’, IEEE Region 10 Symposium (TENSYMP), 5-7 June 2020, Dhaka, Bangladesh.
- Nithya K, Muralidhar Gadamsetty and Binsu J Kailath, “FPGA Implementation of Speech Recognizer for Isolated Words”, accepted for Lecture presentation at 2019 IEEE 5th International Symposium on Smart Electronic Systems (iSES), to be held in Rourkela, India from December 16-18, 2019.