

Name: Dr. P. Radhika

Designation: Assistant Professor (Sr.G)

Email ID: radhikap@srmist.edu.in

Area: VLSI Design

Affiliation: Department of Electronics and Communication Engineering, Kattankulathur Campus, SRM Institute of Science and Technology(SRMIST)

Selected Publications:

Journals:

- P.Radhika, T.Vigneswaran, J.Selvakumar,” Design of modified reconfigurable unsymmetrical six parallel FIR filter with retiming technique for low power & high speed applications”, International Journal of Recent Technology and Engineering , Volume-8, Issue-1, pp 759-767,May 2019.
- Tharun Chowdary.A, Radhika. P, Jannath A.S, Vinod Chandra M, Pruthvi Raj. M,” Remotely operated under water vehicle for monitoring and analyzing water quality “, International Journal of Recent Technology and Engineering, Volume-8, Issue-1, pp 311-314, May 2019.
- P.Radhika, T.Vigneswaran, J.Selvakumar, Design of high performance filter bank multi-carrier transmitter, cluster computing, pp.1-7, 2018, SNIP-0.981 (SCI Indexed)
- M.Anila, P.Radhika, Facial actions based aac device using morse code Journal of Advanced Research in Dynamical and Control Systems, vol 9(6),pp.702-715, 2017 ,SNIP-0.152 (Scopus Indexed).
- P.Radhika, B.Sathis,T.Vigneswaran,”Realization of Energy Efficient and High speed 64 bit Carry skip adder under a wide range of supply voltages,” International Journal of Control Theory and Applications,SNIP:1.466,Vol :9(13), pp-5911-5919,Sept 2016.
- P.Radhika, G. V. K. Chaitanya,T.Vigneswaran,”Constant multiplier architecture based on vertical-horizontal binary common subexpression elimination for FIR filter,” International Journal of Control Theory and Applications,SNIP:1.466,Vol :9(13), pp-501-509,Sept 2016.
- P.Radhika, A.V.Sunil,T.Vigneswaran,” Area and Delay optimization using various multiple constant multiplication techniques for FIR filter “,International Journal of Control Theory and Applications,SNIP:1.466,Vol :9(13), pp-5893-5899,Sept 2016.
- D. Vamshi Krishna,P.Radhika,T.Vigneswaran,” High Speed Han Carlson Adder Using modified SQRT CSLA”, International Journal of control Theory and Applications,SNIP:1.466,Vol:9(13),pp-7843-7849,sept-2016.
- P.Radhika,Dr.T.Vigneswaran,”Design of a novel high speed and low power MCM based FIR filter by using hybrid adder structure, retiming and pipelined techniques”, European journal of Scientific Research, Vol 135,No 3,ISSN-1450-216X/1450-202X,Nov 2015.

- P.Radhika, Dr.T.Vigneswaran,"Incorporation of optimized AND, OR and HA into carry select addressing CMOS technology",International Journal of Applied Engineering and research, Vol 22,PP-17083-17095,March 2014.
- P.Radhika,Dr.T.Vigneswaran,"Design of low power reduced Wallace tree multiplier with compact select adder ,half adder& full adder using CMOS technology", Journal of Applied Theoretical Information technology", Vol 74,no2 20th April 2014.

Papers Presented:

International Conference

- P.Radhika, "Design of reconfigurable block FIR filter architecture and implementation on hardware", International conference on modern research in engineering and technology,2018.
- P.Radhika , "cloud based smart parking system using IoT", International conference on recent trends & technology,2018.
- Anila, M., Radhika, P," Lip contour detection based AAC device using morse code ",Proceedings of the 2017 International Conference on Wireless Communications, Signal Processing and Networking, WiSPNET 2017.
- L. Bharani1 & P. Radhika2optimal Step Size Nlms Algorithm And Its Performance Analysis, International Conference on Computer Science and Information Technology, 10th, March 2013, Hyderabad, ISBN: 978-93-82208-70-9,PP-160-164.

National conference

- M.K.Tarun1, P.Radhika2,"Next Generation Auto Theft Prevention of A Vehicle"2nd National Conference recent advances in communication engineering, April 2014.
- L. BHARANI1 & P. RADHIKA , "Implementation of Optimal Step Size NLMS Algorithm and Its Performance Analysis", Proceedings of the National Conference-NCECT'2K13,2013.
- P. Radhika, Bhanu Chander.K, "FPGA implementation of UART architecture for better noise performance", National Conference on communication high performance Electrical &Electronics Technological applications [CHEETA'10], Angel College of Engineering and Technology, Tirupur, 2nd April 2010.