1. B. P. Bhuvana and B. V. S. Kanchana, "Positive Feedback Symmetric Adiabatic Logic Against Differential Power Attack," 2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID), Pune, 2018, pp. 149-154, doi: 10.1109/VLSID.2018.53.

2. C. Vinoth ,V. S. Kanchana,B.Brindha,et all, "A novel low power and high speed Wallace tree multiplier for RISC processor," 2011 3rd International Conference on Electronics Computer Technology, Kanyakumari, 2011, pp. 330-334, doi: 10.1109/ICECTECH.2011.5941617.

3. Thangarajan, Sreenath; Bhaaskaran, V S Kanchana "High Speed and Low Power Implementation of AES for Wireless Sensor Networks" published in Procedia computer science, Volume 143, Number 1, 2018, pp. 736-743(8),Publisher: Elsevier

4. Sasipriya, P.; Bhaaskaran, V.S. Kanchana" Design and Analysis of Clocked CMOS Differential Adiabatic Logic (CCDAL) for Low Power "published in Journal of Low Power Electronics, Volume 14, Number 4, December 2018, pp. 548-557(10),Publisher: American Scientific Publishers,DOI: https://doi.org/10.1166/jolpe.2018.1578

5. Bhuvana, B.P.; Kanchana Bhaaskaran, V.S "Performance Analysis of 2N-N-2P Adiabatic Logic Circuits for Low Power Applications using FinFET",Source: Procedia computer science, Volume 115, Number 1, 2017, pp. 166-173(8),Publisher: Elsevier

6. Bhaaskaran, V. S. Kanchana; Raina, J.P" Differential Cascode Adiabatic Logic Structure for Low Power",Source: Journal of Low Power Electronics, Volume 4, Number 2, August 2008, pp. 178-190(13) ,Publisher: American Scientific Publishers DOI: https://doi.org/10.1166/jolpe.2008.264

7. D. Anandani, A. Kumar and V. S. K. Bhaaskaran, "Gating techniques for 6T SRAM cell using different modes of FinFET," 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Kochi, 2015, pp. 483-487, doi: 10.1109/ICACCI.2015.7275655.

8. Savio Victor Gomes, P. Sasipriya and V. S. Kanchana Bhaaskaran" A Low Power Multiplier using a 24-Transistor Latch Adder" Indian Journal of Science and Technology, Vol 8(19), DOI: 10.17485/ijst/2015/v8i19/76866, August 2015, ISSN (Print) : 0974-6846 ISSN (Online) : 0974-5645

9. Appasaheb B.R., Kanchana Bhaaskaran V.S. (2013) "Design and Implementation of an Efficient Multiplier Using Vedic Mathematics and Charge Recovery Logic" In: Chakravarthi V., Shirur Y., Prasad R. (eds) Proceedings of International Conference on VLSI, Communication, Advanced Devices, Signals & Systems and Networking (VCASAN-2013). Lecture Notes in Electrical Engineering, vol 258. Springer, India. https://doi.org/10.1007/978-81-322-1524-0_15

10. N. Poornima, V. S. Kanchana Bhaaskaran"Area Efficient Hybrid Parallel Prefix Adders"Procedia Materials Science,Volume 10,2015,Pages 371-380,ISSN 2211-8128,https://doi.org/10.1016/j.mspro.2015.06.069.,(http://www.sciencedirect.com/science/article/pii/S2211812815003077)

11. Bhuvana B P,Manohar B R,Kanchana Bhaaskaran V S" Adiabatic Logic Circuits Using FinFETs and CMOS – A Review" International Journal of Engineering and Technology (IJET), 2016, Volume-8,Issue-2,Pages 1256-1270