## RESEARCH PUBLICATIONS IN INTERNATIONAL JOURNALS

**1. Encrypted Biography of Biomedical Image - a Penta layer Cryptosystem on FPGA**
*Journal of Signal Processing Systems*
2018 | journal-article
DOI: 10.1007/s11265-018-1337-z
EID: 2-s2.0-85042071091
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**2.Networked hardware assisted key image and chaotic attractors for secure RGB image communication**
*Multimedia Tools and Applications*
2018 | journal-article
DOI: 10.1007/s11042-017-5566-0
EID: 2-s2.0-85041233213
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**3.ON–Chip peripherals are ON for chaos – an image fusedencryption**
*Microprocessors and Microsystems*
2018 | journal-article
DOI: 10.1016/j.micpro.2018.06.011
EID: 2-s2.0-85049300954
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**4.YRBS coding with logistic map – a novel Sanskritaphorism and chaos for image encryption**
*Multimedia Tools and Applications*
2018 | journal-article
DOI: 10.1007/s11042-018-6574-4
EID: 2-s2.0-85053463335
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**5.A case study of fault-tolerant biological systems with mriimages.***Biomedical Research (India)*
2017 | journal-article
EID: 2-s2.0-85024884104
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**6.Area, delay and power comparison of fault-tolerant systems with TMR using different voter circuits**
*International Journal of Signal and Imaging Systems Engineering*
2017 | journal-article
DOI: 10.1504/IJSISE.2017.084572
EID: 2-s2.0-85021135109
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**7.A comparative study on CMOS majority voter circuitsusing microwind**
*International Journal of Pharmacy and Technology*
2016 | journal-article
EID: 2-s2.0-85018203544
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**8.Concurrent error detection with self-checking majority voting circuits**
*IIOAB Journal*
2016 | journal-article
EID: 2-s2.0-85006380379
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**9.Fault-tolerant system design using 7-modular redundancy configurations**
*International Journal of Pharmacy and Technology*
2016 | journal-article
EID: 2-s2.0-85018202161
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**10.FPGA implemenation of high speed and low power carrysave adder**
*IIOAB Journal*
2016 | journal-article
EID: 2-s2.0-85006341659
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**11.Reliability improvement by hardware redundancy usingaltera DSP builder**
*International Journal of Pharmacy and Technology*
2016 | journal-article
EID: 2-s2.0-85018213809
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**12.Review on recent developments in automation of Indian sign language**
*Far East Journal of Electronics and Communications*
2016 | journal-article
DOI: 10.17654/EC03010063
EID: 2-s2.0-84968835182
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**13.A case study of impulse noise reduction usingmorphological image processing with structuringelements**
*Asian Journal of Scientific Research*
2015 | journal-article
DOI: 10.3923/ajsr.2015.291.303
EID: 2-s2.0-84933498474
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**14.A case study on wavelet analysis and its applications**
*International Journal of Pharmacy and Technology*
2015 | journal-article
EID: 2-s2.0-84944454458
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**15.A comparative study of high-speed CMOS adders usingMicrowind and FPGA**
*Indian Journal of Science and Technology*
2015 | journal-article
DOI: 10.17485/ijst/2015/v8i22/79181
EID: 2-s2.0-84944450858
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**16.A handy approach for teaching and learning digital VLSIdesign using EDA tools***International Journal of Pharmacy and Technology*
2015 | journal-article
EID: 2-s2.0-84953233266
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**17. An implementation of area and power efficient digital FIRfilter for hearing aid applications**
*Optoelectronics and Advanced Materials, Rapid Communications*
2015 | journal-article
EID: 2-s2.0-84934936253
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**18.CMOS VLSI design of low power SRAM cell architectureswith new TMR: A layout approach**
*Asian Journal of Scientific Research*
2015 | journal-article
DOI: 10.3923/ajsr.2015.466.477
EID: 2-s2.0-84944888210
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**19.FPGA implementation of self-testing logic gates, addersand multipliers**
*Indian Journal of Science and Technology*
2015 | journal-article
DOI: 10.17485/ijst/2015/v8i22/79331
EID: 2-s2.0-84944448718
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**20.FPGA implementation of subband coding with multimediadata watermarking**
*International Journal of Pharmacy and Technology*
2015 | journal-article
EID: 2-s2.0-84944463627
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**21.Low power CMOS look-up tables using PROM**
*Indian Journal of Science and Technology*
2015 | journal-article
DOI: 10.17485/ijst/2015/v8i22/79164
EID: 2-s2.0-84944451795
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**22.Low power digital barrel shifter datapath circuits usingmicrowind layout editor with high reliability**
*Asian Journal of Scientific Research*
2015 | journal-article
DOI: 10.3923/ajsr.2015.478.489
EID: 2-s2.0-84944882969
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**23.Majority function computation using different votercircuits - A comparative study**
*International Journal of Pharmacy and Technology*
2015 | journal-article
EID: 2-s2.0-84953228261
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier

**24.Real time audio denoising using digital fir filters withFPGA implementation**
*International Journal of Pharmacy and Technology*
2015 | journal-article
EID: 2-s2.0-84953254824
**Source:**Har Narayan Upadhyay *via*Scopus - Elsevier