

LIST OF INTERNATIONAL JOURNAL PUBLICATIONS

1. P.Vimala, T.S.Arun Samuel, M. Karthigai Pandian, "Performance Investigation of Gate Engineered tri-Gate SOI TFETs with Different High-K Dielectric Materials for Low Power Applications", Silicon (Springer), Impact factor: 1.210, First Online: 04 November 2019.
- 2.S.Darwin, T.S.Arun Samuel and P.Vimala, "Impact of two gate oxide with no junction metal oxide semiconductor field effect transistor- an analytical model", Physica E: Low-dimensional Systems and Nanostructures (Elsevier publisher), impact factor: 3.17), Vol. 113803, Available online 31 October 2019.
- 3.P. Vimala, T.S. Arun Samuel, D. Nirmal, Ajit Kumar Panda, "Performance enhancement of triple material double gate TFET with heterojunction and heterodielectric", Solid State Electronics Letters (Elsevier publisher), vol. 1, pp. 64–72, Nov 2019.
- 4.S. Manikandana, N.B. Balamurugan and T.S. Arun Samuel, "Impact of uniform and non-uniform doping variations for ultrathin body junctionless FinFETs" Materials Science in Semiconductor Processing (Elsevier publisher, impact factor: 2.72), Vol.104, Dec 2019.
- 5.S. Komalavalli, T.S. Arun Samuel and P. Vimala, "Performance analysis of triple material tri gate TFET using 3D analytical modelling and TCAD simulation", AEÜ - International Journal of Electronics and Communications (Elsevier publisher, impact factor:2.115), Vol.110, Oct 2019.
- 6.Vimala Palanichamy, Netravathi Kulkarni and Arun Samuel T.S, "Improved drain current characteristics of tunnel field effect transistor with heterodielectric stacked structure", International Journal of Nano Dimension (Scopus Journal), Vol.10, No.4, pp.413-419, July 2019.
- 7.V.Dharshana, N.B.Balamurugan and T.S. Arun Samuel, "An Analytical Modeling and Simulation of Surrounding Gate TFET with an Impact of Dual Material Gate and Stacked Oxide for Low Power Applications", Journal of Nano Research, Impact Factor: 0.6, Vol. 57, pp 68-76, April 2019.
- 8.Darwin.S and Arun Samuel T.S, A Holistic Approach on Junctionless Dual Material Double Gate (DMDG) MOSFET with High k Gate Stack for Low Power Digital Applications, Silicon (Springer), Impact factor: 1.210, First Online: 27 March 2019.
- 9.P. Vanitha, T.S. Arun Samuel and D. Nirmal, "A new 2 D mathematical modeling of surrounding

gate triple material tunnel FET using halo engineering for enhanced drain current”, AEÜ - International Journal of Electronics and Communications (Elsevier publisher) impact factor:2.115, Vol.99, pp:34-39, Feb 2019.

10.Darwin.S and Arun Samuel T.S, “Mathematical Modeling of Junctionless Triple Material Double Gate MOSFET for Low Power Applications”, Journal of Nano Research, Impact Factor: 0.6 Vol. 56, pp 71-79, Feb 2019.

11.R. Solomon Roach, N.Nirmal Singh and T. S. Arun Samuel, “Resource minimization and power reduction of ESPFIR filter using unified adder/subtractor”, Analog Integrated Circuits and Signal Processing (Springer), Impact Factor: 0.8, Vol.98, No.1, Jan 2019.

12.D. David Neels Ponkumar, P. Jagatheeswari, T.S.Arun Samuel, “Implementation of VIP for bus interface logic of 32-bit processor using System Verilog, Journal of Microelectronics, Electronic Components and Materials Impact Factor: 0.476, Vol. 48, No. 4, pp.205 – 211, 2018.

13.G. Rajakumar, T.Ananth Kumar and T.S. Arun Samuel “IOT Based Milk Monitoring System For Detection Of Milk Adulteration”, International Journal of Pure and Applied Mathematics, Vol.118, No.9, pp.21-32, 2018.

14.T.S.Arun Samuel and S.Komalavalli, “Analytical Modelling and Simulation of Triple Material Quadruple Gate Tunnel Field Effect Transistors”, Journal of nano research, Impact Factor: 0.6, Vol. 54, pp 146-157, 2018.

15.T.S. Arun Samuel, S. Darwin and N. Arumugam, “Design of adiabatic logic based comparator for low power and high speed applications”, ICTACT Journal On Microelectronics, Vol.3, No.1, 365-369, 2017.

16.R. Anand, T.S. Arun Samuel and P. Melba Mary 2017, “Improved dynamic response of isolated full bridge DC to DC converter using BATA optimization tuned fuzzy sliding mode controller for solar applications”, International Journal of Hydrogen Energy-(Elsevier), Impact Factor: 4.084 Vol. 42, pp. 21648 -21658.

17.G. Rajakumar, A. Andrew Roobert, T. S. Arun Samuel & D. Gracia Nirmala, 2017 “Low power VLSI architecture design of BMC, BPSC and PC scheme” Analog Integrated Circuits and Signal Processing (Springer), Impact Factor: 0.8 Vol.93, pp.169-178.

18.T.S.Arun Samuel, N. Arumugam and S.Theodore Chandra, “Analytical Approach and Simulation of GaN Single Gate TFET and Gate All around TFET”, ECTI transactions on electrical eng.,

electronics, and communications, Vol.15, No.02, pp. 1-7, 2017.

19.T.S.Arun Samuel and M.Karthigai Pandian, "Comparative Performance Analysis of Multi Gate Tunnel Field Effect Transistors", Journal of Nano Research, Impact Factor: 0.6, Vol. 41, pp 1-8), 2016.

20.T.S. Arun Samuel, N. Arumugam and A. Shenbagavalli, "Drain Current Characteristics Of Silicon Nanowire Field Effect Transistor", ICTACT Journal On Microelectronics, Vol. 2, No.3, pp 284-287, 2016.

LIST OF INTERNATIONAL CONFERENCE PUBLICATIONS

1.T.S.Arun Samuel, Design of IOT node for smart cities, International Conference on Applied soft computing Techniques (ICASCT'18) on 23rd and 24th March 2018 at Kalasalingam University, Krishnankoil.

2.T.S.Arun Samuel, IOT Based Milk Monitoring System For Detection Of Milk Adulteration, International Conference on Data Security (INCODS 2017) at Kalasalingam Academy of research and education on 11-13th December 2017.

3.T.S.Arun Samuel, Methodology for distance measurement: A comparative study, 3rd International conference on Advancement in engineering, Applied science and management (ICAEASM 2017) at Centre for development of Advanced computing, Jahu, Mumbai on 20th August 2017.

4.Arun Samuel, TS and N. Arumugam, Drain Current Characteristics Of Silicon Nanowire Field Effect transistor, 3rd International Conference on Emerging Electronics, December 27-30, 2016, Indian Institute of Technology Bombay, Mumbai, India