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PUBLICATIONS:

TEXT BOOKS:

1. Fundamentals of DIGITAL DESIGN- Published by S.Chand publishers, ISBN: 978-93-84319-12-0.
2. Linear Integrated circuit -Published by S.Chand publishers, ISBN: 978-81-219-4113-6.

Publications :

1. **Senthil Sivakumar M**, Joy Vasantha Rani SP, & Gurumekala T, 2019, 'Built-In Self-Test of Analog to Digital Converter – Review', Australian Journal of Electrical and Electronics Engineering, Taylor & Francis Publication, (Minor Revision).
2. **Senthil Sivakumar M** & Joy Vasantha Rani SP, 2019, 'Time Domain Modelled ADC BIST with Ramp Noise Projection', International Journal of Electronics, Taylor & Francis Publication, Vol. 106 (8), pp. 1127-1140.
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4. **Senthil Sivakumar M**, Gurumekala T, Sruthi Pulya, 2019. Error Detection of Data Conversion in Flash ADC using Code Width Based Technique. Procedia Computer Science, Elsevier Publications, Vol.165, pp.270-277.
5. **Senthil Sivakumar M**, Sowmya Priya M, 2019, 'Design and Analysis of a Comparator for Flash ADC, International Journal of Recent Technology and Engineering (IJRTE), Vol.7, no.5S4, pp.368-372. ISSN: 2277-3878.

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10. Karpagam, **Senthil Sivakumar M** & Joy Vasantha Rani SP 2018, 'Effect of Ramp Slope Error in an On-Chip ADC BIST', Journal for Advanced Research in Applied Sciences, vol. 5 (4), pp. 249-254.
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12. **Senthil Sivakumar M**, Gurumekala T, Sundaram A, Banupriya M & Arputharaj T, 2015, 'Design of Novel AES processor for High Speed Next Generation Internet Security', International Journal of Applied Engineering Research, Vol.10 (55), pp.389-393.
13. Gurumekala T, **Senthil Sivakumar M**, Sundaram A & Arputharaj T, 2015, 'Enhanced Fuzzy Based Clustering Approach for Improving Reliability of WSNs, International Journal of Applied Engineering Research, Vol.10(55), pp.1314-1319.
14. Gurumekala T, **Senthil Sivakumar M**, Sundaram A & Arputharaj T, 2015, Identification of High Throughput Path in WMNs using Novel Routing Metric, International Journal of Applied Engineering Research, Vol.10 (55), pp.1278-1283.
15. **Senthil Sivakumar M**, Sundaram A, Gurumekala T & Banupriya M, 2015, 'Design of ALU using reversible logic based Low Power Vedic Multiplier', International Journal of Scientific & Engineering Research (Thomson Reuters), vol.6(2), pp.5-8.

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2. **Senthil Sivakumar M**, M. Sowmya Priya, S. Pulya, 2019. Comparative analysis of the CMOS 180nm technology-based flash ADC designs using dynamic comparator and TIQ comparator. Proceedings of IEEE 2nd International Conference on Power and Embedded Drive Control, pp. 111-115, doi: 10.1109/ICPEDC47771.2019.9036632.
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5. Ashwini S, **Senthil Sivakumar M**, & Joy Vasantha Rani SP 2017, 'Design of Linear Ramp Generator for ADC', proc.of IEEE 4th International Conference on Signal Processing (2017), Communications and Networking, MIT-Anna University, Chennai-600044.
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12. **Senthil Sivakumar M**, Thandaiah Prabu & Jayanandan, 2014, 'Design of Digital Clock Calendar Using FPGA', IETE 45th Mid-term Symposium on Broadband Technologies and Services for Rural India, 4th and 5th April, proceeding of CIIT'2014, Chennai.
13. **Senthil Sivakumar M**, Arockia Jayadhas S, Arputharaj T & Banupriya M 2013, '4-Bit Manchester Carry Look-Ahead Adder Design Using MT-CMOS Domino Logic', proc. of IEEE Pan African International conference on PACT, Zambia, Africa, July, pp.15-18.
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