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Last FIVE YEARS Publications

1	VLSI Design of a Squaring Architecture based on Yavadunam Sutra of Vedic Mathematics A Deepa, CN Marimuthu 2020 International Conference on Electronics and Sustainable Communication	2020
2	An efficient high speed squaring and multiplier architecture using yavadunam sutra and bit reduction technique A Deepa, CN Marimuthu, C Murugesan Journal of Physics: Conference Series 1432 (1), 012080	2020
3	Design of a high speed Vedic multiplier and square architecture based on Yavadunam Sutra A Deepa, CN Marimuthu Sādhana 44 (9), 197	2019
4	Optimization of motion estimation hardware using charged system optimization with low power multipliers for H. 264 encoders L Vigneash, CN Marimuthu Cluster Computing 22 (5), 10669-10677	2019
5	Cost optimization of PV-diesel systems in nanogrid using LJ cuckoo search and its application in mobile towers C Murugesan, CN Marimuthu Mobile Networks and Applications 24 (2), 340-349	2019
6	A novel center-tapped transformer based multilevel inverter with common DC source G Arthy, CN Marimuthu Journal of Vibroengineering 20 (8), 3040-3053	2018
7	A Hybrid Low Power Fast Full Adder Using XOR And XNOR Gates RKU Maheswari, CN Marimuthu International Journal of Recent Advances in science and technology 5 (3), 64-68	2018
8	High speed VLSI architecture for squaring binary numbers using Yavadunam sutra and bit reduction technique A Deepa, CN Marimuthu International Journal of Applied Engineering Research 13 (6), 4471-4474	2018
9	Modified RS encoder architecture with reduced critical path delay for high speed data communication A Deepa, CN Marimuthu 2017 International Conference on Intelligent Sustainable Systems (ICISS ...	2017

10	A survey on control algorithms for DSTATCOM G Arthy, CN Marimuthu 2017 International Conference on Computer Communication and Informatics ...	2017
11	A high speed VLSI architecture of a pipelined reed solomon encoder for data storage in communication systems A Deepa, CN Marimuthu Asian Journal of Research in Social Sciences and Humanities 7 (2), 228-238	2017
12	Implementation of Power Reduction Adder with High Recital Multiplier LV Dr. C. N. Marimuthu Asian Journal of Research in Social Sciences and Humanities , 6 (8), 898-907	2016
13	Intelligent Vehicle Control System Using Shared Steering Control Mechanism AR Devi, PG Scholar, TN Erode, IDCN Marimuthu Journal of Network Communications and Emerging Technologies (JNCET) www ...	2016
14	A New Multilevel Inverter Design with Reduced Power Electronic Components for Three Phase Grid Connected System AGDM C. N. Asian Journal of Research in Social Sciences and Humanities 6 (11), 642-658	2016
15	Immune RBF neural network algorithm for DSTATCOM GA C. N. Marimuthu 2016 International Conference on Computer Communication and Informatics ...	2016
16	Fast Multiplier for FIR Filters GR Babu, CN Marimuthu International Journal of Scientific and Technical Advancements 2 (1), 57-61	2016
17	Signature Based Vulnerability Detection Over Wireless Sensor Network for Reliable Data Transmission NMS Kumar, S Deepa, CN Marimuthu, T Eswari, S Lavanya Wireless Personal Communications, 1-12	2015
18	Shared Steering Control between a Driver and an Automation: Stability in the Presence of Driver Behavior Uncertainty C.N. MarimuthuA. Ranjittha devi International Journal of Recent Research in Electrical and Electronics ...	2015
19	Implementation of Han-Carlson Adder for Error Tolerent Applications MCN Sasireka.S International Journal of Electrical and Electronics Research 3 (4), 39-50	2015
20	Power optimization using body biasing method for dual voltage FPGA B Sankar, C Marimuthu Proceedings of International Research Journal of Engineering and Technology ...	2015
21	ENHANCED Q-LEACH ROUTING PROTOCOL FOR WIRELESS SENSOR NETWORKS D S Deepa, CN Marimuthu ARPN Journal of Engineering and Applied Sciences 10 (9), 4036-4041	2015
22	GAUSSIAN FILTER BASED BIOMETRIC SYSTEM SECURITY ENHANCEMENT M Selvi, MT Manickam, CN Marimuthu	2015