

1. S. Veeramani and Sk. Noor Mahammad, "\An Approach to Place Sink Node in a Wireless Sensor Network (WSN)", Wireless Personal Communications, pp 111, October 2019. [SCI Indexed]
2. S. M. Srinivasavarma Vegesna, Ashok Chakravarthy Nara and Noor Mahammad Sk, "\A Novel Rule Mapping on TCAM for Power E_cient Packet Classi_cation", ACM Transactions on Design Automation of Electronic Systems (ACM TODAES), Vol. 24, no. 5, pp. 48:1-48:23, 2019. [SCI Indexed]
3. Veeramani S and Noor Mahammad Sk, "\Controller Load Balancing using Graph Theoretic Approach for OpenFlow Network", Caribbean Journal of Science, Vol. 53, no. 2, pp. 823-833, 2019. [SCI Indexed]
4. S Veeramani and Noor Mahammad Sk, "\A Heuristic Approach for the CCLP Problem in Software De_fined Network (SDN)", Internetworking Indonesia Journal, Vol. 10, No. 1, pp. 3-8, 2018. [SCOPUS Indexed]
5. Mohamed Asan Basiri M and Noor Mahammad Sk, "\Discrete Orthogonal Multi-transform on Chip (DOMoC)" Journal of Signal Processing Systems, pp. 1-22, Available: ONLINE, 22 Jan 2018. [SCI Indexed]
6. Shanmugakumar Murugesan and Noor Mahammad Sk, "\A Novel Range Matching Architecture for Packet Classi_cation without Rule Expansion", ACM Transactions on Design Automation of Electronic Systems (ACM TODAES), Vol. 23, no. 1, pp. 8:1-8:15, September 2017. [SCI Indexed]
7. Mohamed Asan Basiri M and Noor Mahammad Sk, "\Quadruple Throughput Fixed Point Quarter Precision Multiply Accumulate Circuit", IET Computers and Digital Techniques, Vol. 11, no. 5, pp. 183-189, April 2017. [SCI Indexed]
8. Mohamed Asan Basiri M and Noor Mahammad Sk, "\An E_cient VLSI Architecture for Lifting based 1D/2D Discrete Wavelet Transform", Microprocessors and Microsystems, Vol.47, Part B, pp. 404-418, November 2016. [SCI Indexed]
9. Mohamed Asan Basiri M and Noor Mahammad Sk, "\High Speed Multiplexer Design using Tree based Decomposition Algorithm", Microelectronics Journal, Vol. 51, pp. 99-111, May 2016. [SCI Indexed]
10. Mohamed Asan Basiri M and Noor Mahammad Sk, "\Multi-mode Parallel and Folded VLSI Architectures for 1D-Fast Fourier Transform", Integration, the VLSI Journal, Vol. 55, pp. 43-56, September 2016. [SCI Indexed]