
Publications in scopus-indexed journals:

1. Y. M. Aneesh and **B. Bindu**, "A Physics-based Single Event Transient Pulse Width Model for CMOS VLSI Circuits," **IEEE Transactions on Device and Materials Reliability**, Sept. 2020 (early access - DOI: 10.1109/TDMR.2020.3023285).
2. P. Manikandan and **B. Bindu**, "Dual-summed flipped voltage follower LDO regulator with active feed-forward compensation," **AEU-International Journal of Electronics and Communications** (elsevier), vol. 123, pp. 153314, Aug. 2020.
3. P. Manikandan and **B. Bindu**, "A push-pulled capacitor-less FVF LDO with active feed-forward compensator," **International Journal of Electronics** (Taylor & Francis), 2020 (DOI: 10.1080/00207217.2020.1793413).
4. K.R Pasupathy and **B. Bindu**, "Sensitivity of SET pulse-width and propagation to radiation track parameters in CMOS inverter chain," **IETE Journal of Research**, 2020 (DOI: 10.1080/03772063.2020.1787875).
5. P. Manikandan and **B. Bindu**, "A capacitor-less FVF low drop-out regulator with active feed-forward compensation and efficient slew-rate enhancer circuit," **IET Circuits, Devices & Systems**, 2020 (DOI: 10.1049/iet-cds.2019.0495).
6. P. Manikandan and **B. Bindu**, "A cap-less voltage spike detection and correction circuit for low dropout regulator," **Journal of Circuits, Systems and Computers**, vol. 29, no. 16, pp. 2020009, 2020.
7. S. R. Sriram and **B. Bindu**, "A physics-based model for LER-induced threshold voltage variations in double-gate MOSFET," **Journal of Computational Electronics** (springer), vol. 19, pp. 622-630, 2020.
8. P. Manikandan, **B. Bindu**, "High PSR Capacitor-Less LDO with Adaptive Circuit for Varying Loads", **Journal of Circuits, Systems and Computers**, vol. 29, no. 11, pp. 2050178, 2020.
9. Y. M. Aneesh, S. R. Sriram, K. R. Pasupathy, and **B. Bindu**, "An Analytical Model of Single-Event Transients in Double-Gate MOSFET for Circuit Simulation," **IEEE Transactions on Electron Devices**, vol. 66, no. 9, pp. 3710–3717, 2019.
10. S. R. Sriram and **B. Bindu**, "Analytical Model for RDF-induced Threshold Voltage Fluctuations in Double-Gate MOSFET," **IEEE Transactions on Device and Materials Reliability**, vol. 19, no. 2, pp. 370–377, 2019.
11. K. R. Pasupathy and **B. Bindu**, "Analysis of bipolar amplification due to heavy-ion irradiation in 45 nm FDSOI MOSFET with thin BOX and ground plane," **Microelectronics Reliability** (elsevier), vol. 98, pp. 56–62, 2019.

12. S. R. Sriram and **B. Bindu**, "Analytical modeling of random discrete traps induced threshold voltage fluctuations in double-gate MOSFET with $\text{HfO}_2/\text{SiO}_2$ gate dielectric stack," *Microelectronics Reliability* (elsevier), vol. 99, pp. 87–95, 2019.
13. S. R. Sriram and **B. Bindu**, "A physics-based 3-D potential and threshold voltage model for undoped triple-gate FinFET with interface trapped charges," *Journal of Computational Electronics* (springer), vol. 18, no. 1, pp. 37–45, 2019.
14. S. R. Sriram and **B. Bindu**, "Analytical model of hot carrier degradation in uniaxial strained triple-gate FinFET for circuit simulation," *Journal of Computational Electronics* (springer), vol. 17, no. 1, pp. 163–171, 2018.
15. K. R Pasupathy and **B. Bindu**, "Widening and narrowing of time interval due to single-event transients in 45 nm vernier-type TDC," *IET Circuits, Devices & Systems*, vol. 11, no. 6, pp. 676–681, 2017.
16. K.R Pasupathy and **B Bindu**, "A review on circuit simulation techniques of single-event transients and their propagation in delay locked loop," *IETE Technical Review*, vol. 34, no. 3, pp. 276–285, 2017.
17. P Prabhu Thapaswini, R Padma, N Balaram, **B. Bindu**, and V. Rajagopal Reddy, "Modification of electrical properties of Au/n-type InP Schottky diode with a high-k $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ interlayer," *Superlattices and Microstructures* (elsevier), vol. 93, pp. 82–91, 2016.
18. S. R. Sriram and **B. Bindu**, "Impact of NBTI induced variations on delay locked loop multi-phase clock generator," *Microelectronics Reliability* (elsevier), vol. 60, pp. 33–40, 2016.
19. A. Narendiran, K. Akhila, and **B. Bindu**, "A physics-based model of double-gate tunnel FET for circuit simulation," *IETE Journal of Research*, vol. 62, no. 3, pp. 387–393, 2016.
20. K. R. Pasupathy and **B. Bindu**, "Low power, high speed carbon nanotube FET based level shifters for multi-vdd systems-on-chips," *Microelectronics Journal* (elsevier), vol. 46, no. 12, pp. 1269–1274, 2015.
21. **B. Bindu**, B. Cheng, G. Roy, X. Wang, S. Roy, and A. Asenov, "Parameter Set and Data Sampling Strategy for Accurate Yet Efficient Statistical MOSFET Compact Model Extraction," *Solid State Electronics* (slsevier), vol. 54, no. 3, pp. 307–315, 2010.
22. **B. Bindu**, Nandita DasGupta, and Amitava DasGupta, "A Unified Model for Gate Capacitance-Voltage Characteristics and Extraction of Parameters of Si/SiGe heterostructure PMOSFETs," *IEEE Trans. on Electron Devices*, vol. 54, no. 8, pp. 1889–1896, 2007.
23. **B. Bindu**, Nandita DasGupta, and Amitava DasGupta, "Analytical Model of Drain Current of Si/SiGe heterostructure p-channel MOSFETs for Circuit Simulation," *IEEE Trans. on*

Electron Devices, vol. 53, no. 6, pp. 1411–1419, 2006.

24. **B. Bindu**, N. Lakshmi, K. N. Bhat, and Amitava DasGupta, “Design of nMOS and pMOS transistors operating in Virtual Double-Gate mode in Conventional SOI CMOS Technology,” **Solid State Electronics** (elsevier), vol. 50, no. 7, pp. 1359–1367, 2006.
25. **B. Bindu**, N. DasGupta, and A. DasGupta, “Analytical Model of Drain Current of Strained-Si/Strained-Si_{1-y}Gey/Relaxed-Si_{1-x}Gex NMOSFETs and PMOSFETs for Circuit Simulation,” **Solid State Electronics** (elsevier), vol. 50, no. 3, pp. 448–455, 2006.

Publications in conference proceedings:

1. S. R. Sriram and B. Bindu, “Study of Line Edge Roughness Induced Threshold Voltage Fluctuations in Double-Gate MOSFET,” in **IEEE INDICON**, 2018, pp. 10-15.
2. S. R. Sriram and B. Bindu, “Hot Carrier Reliability in 45 nm Strained Si/relaxed Si_{1-x}Gex CMOS Based SRAM Cell,” in **IEEE INDICON**, 2018, pp. 1–5.
3. S.R Sriram and B. Bindu, “Impact of NBTI induced variations on FinFET based Vernier delay line time to digital converter,” in **International Conference on Nextgen Electronic Technologies: Silicon to Software** (ICNETS2), 2017, pp. 122-125.
4. P Manikandan and B. Bindu, “A capacitor-less low-dropout regulator (LDO) architecture for wireless application,” in **International Conference on Nextgen Electronic Technologies: Silicon to Software** (ICNETS2), 2017
16. Y. M. Aneesh, K. R. Pasupathy, and **B. Bindu**, “Design and Optimization of Double-Gate MOSFET to Reduce the Effects of Single Event Transients,” in **International Workshop on the Physics of Semiconductor and Devices** (IWPSD), 2017, pp. 583–588.
17. N.K Subramani, J.C Nallatamby, A.K Sahoo, R. Sommet, R. Quéré, and **B. Bindu**, “A physics based analytical model and numerical simulation for current-voltage characteristics of microwave power AlGaN/GaN HEMT,” in **IEEE MTT-S International Microwave and RF Conference** (IMaRC), 2016, pp. 1–4.
18. Keerthikumar, K.R Pasupathy, and **B. Bindu**, “Design of FinFET based All-Digital DLL for multiphase clock generation,” in **IEEE INDICON**, 2015, pp. 1–4.
19. Sobhana Tayenjam, S. R. Sriram, and **B. Bindu**, “Design of FinFET based frequency synthesizer,” in **IEEE INDICON**, 2015, pp. 1–5.
20. S. R. Sriram and B. Bindu, “NBTI Induced Variations in MCML and CMOS based Ring Oscillators,” in **International Workshop on Physics of Semiconductor Devices** (IWPSD), 2015, pp. 520–524.

21. Akhila Kamal and B Bindu, "Design of tunnel FET based low power digital circuits," in 18th *International Symposium on VLSI Design and Test*, 2014, pp. 1–2.
22. A. Narendiran and **B. Bindu**, "Simulation Studies of Negative Bias Temperature Instability in FinFETs using Two-Stage model," in *IEEE International Conference on Devices, Circuits and Systems* (ICDCS), 2012, pp. 555–557.
23. R. RamaPradeep Reddy and **B. Bindu**, "Random Dopant Induced Variability in SOI Trigate FINFET : A Simulation Study," in *IEEE International Conference on Devices, Circuits and Systems* (ICDCS), 2012, pp. 581–584.
24. S. Nandhakumar and **B. Bindu**, "Reliability Studies of AlGaIn/GaN High Electron Mobility Transistors (HEMT)," in *IEEE International Conference on Devices, Circuits and Systems* (ICDCS), 2012, pp. 558–562.
14. R. Rama Pradeep Reddy and **B. Bindu**, "Statistical Variability in Strained-Channel FinFET due to RDF and LER : A Comparative Analysis," in *International Conference on Nanoelectronics and Nanodevices*, 2013, pp. 1-4.
15. E. Priya and **B. Bindu**, "Design and Optimization of 22nm Trigate SOI FinFET for Digital Circuits," in *IEEE International Conference on Electronics Computer Technology*, 2012, pp. 84–88.
16. K. S. Nikhil and **B. Bindu**, "Performance Optimization of GAA Silicon Nanowire MOSFETs with Dual Gate Architecture," in *IEEE International Conference on Electronics Computer Technology*, 2012, pp. 30–34.
17. D. Dinesh Kumar and **B. Bindu**, "Performance Analysis of Double Gate Tunnel FET for Digital Circuits," in *IEEE International Conference on Electronics Computer Technology*, 2012, pp. 26–29.
18. K. S. Nikhil and **B. Bindu**, "Feasibility Study of Conical Channel Nanowire MOSFETs for Improved Performance," in *International Conference of Modeling, Optimization and Computing*, 2012, pp. 2364–2370.
19. **B. Bindu**, W. Goes, Ben Kaczer, and Tibor Grasser, "Analytical Solution of the Switching Trap Model for Negative Bias Temperature Stress," in *International Integrated Reliability Workshop* (IIRW), 2009, pp. 93–96.
20. **B. Bindu**, B. Cheng, G. Roy, X. Wang, S. Roy, and A. Asenov, "An Efficient Data Sampling Strategy for Statistical Parameter Extraction of Nano-MOSFETs," in *IEEE Workshop on Compact Modeling*, 2008, pp. 55–59.
21. **B. Bindu**, Nandita DasGupta, and Amitava DasGupta, "Analytical Model of Si/SiGe/Si p-channel MOSFETs for Circuit Simulation," in *International Workshop on Physics of*

Semiconductor Devices (IWPSD), 2005, pp. 1064–1068.

22. **B. Bindu**, N. Lakshmi, K. N. Bhat, and Amitava DasGupta, “Virtual Double Gate Operation in Conventional SOI CMOS Technology,” in **IEEE INDICON**, 2005, pp. 119–122.
23. Amitava DasGupta, **B. Bindu**, P. V. Nagaraju, D. S. Havaladar, and Nandita DasGupta, “Non-Classical Silicon Devices for Nano-CMOS technology,” in **International Conference on MEMS, NANO and Smart Systems**, 2005, pp. 112–116.
24. Christophe Labbe, Subhananda Chakrabarti, Gargi Raina, and **B. Bindu**, Book: **Nanoelectronic Materials and Devices**, springer, 2018.

Patents Published:

1. P. Manikandan and **B. Bindu**, A fast transient capacitor-less FVF low drop-out regulator with active feed forward compensation, published on 21/8/2020. Application No. 202041036036.