Members from Other University /Institutions

Member 4

Name: Dr.Bindu B

Designation: Associate Professor Senior

Department: School of Electronics Engineering (SENSE)

Name of the Organization/Institution: VIT University

Place: Chennai

Pin code: 600127

Email: bindu.boby@vit.ac.in

Area of Specialization: Nanoelectronics and VLSI

PUBLICATIONS:

2020

- 1. Y. M. Aneesh and B. Bindu, "A Physics-based Single Event Transient Pulse Width Model for CMOS VLSI Circuits," in IEEE Transactions on Device and Materials Reliability, *doi:* 10.1109/TDMR.2020.3023285.
- 2. M. Pappiah and B. Boby, "Capacitor-less FVF low drop-out regulator with active feed-forward compensation and efficient slew-rate enhancer circuit," in *IET Circuits*, *Devices & Systems*, vol. 14, no. 6, pp. 853-859, 9 2020, doi: 10.1049/iet-cds.2019.0495.
- 3. P. Manikandan, B. Bindu, "Dual-summed flipped voltage follower LDO regulator with active feed-forward compensation," in AEU International Journal of Electronics and Communications, vol 123, 2020, 153314, ISSN 1434-8411,doi:10.1016/j.aeue.2020.153314.
- 4. P. Manikandan, B. Bindu, "A push-pulled capacitor-less FVF LDO with active feed-forward compensator, "International Journal of Electronics, DOI: 10.1080/00207217.2020.1793413,2020
- 5. K. R. Pasupathy, B. Bindu, "Sensitivity of SET Pulse-Width and Propagation to Radiation Track Parameters in CMOS Inverter Chain," in IETE Journal of Research, doi: 10.1080/03772063.2020.1787875
- 6. P. Manikandan, B. Bindu, "A Cap-less Voltage Spike Detection and Correction Circuit for Low Dropout Regulator," in Journal of Circuits, Systems and Computers, doi: 10.1142/S0218126620200091
- 7. SR Sriram, B Bindu, "A physics-based model for LER-induced threshold voltage variations in double-gate MOSFET," Journal of Computational Electronics, Vol 19,Issue 2,pp.622-630,2020

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- 1. Y. M. Aneesh, S. R. Sriram, K. R. Pasupathy and B. Bindu, "An Analytical Model of Single-Event Transients in Double-Gate MOSFET for Circuit Simulation," in *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3710-3717, 2019, doi: 10.1109/TED.2019.2926883.
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- 4. S. R. Sriram and B. Bindu, "Analytical Model for RDF-Induced Threshold Voltage Fluctuations in Double-Gate MOSFET," in *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 2, pp. 370-377, June 2019, doi: 10.1109/TDMR.2019.2910197.
- 5. Sriram, S.R., Bindu, B" A physics-based 3-D potential and threshold voltage model for undoped triple-gate FinFET with interface trapped charges," J Comput Electron 18, 37–45,2019,https://doi.org/10.1007/s10825-018-1260-3
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