## Dr.K.P.Pradhan

## Indian Institute of Information Technology, Design and Manufacturing (IIITDM) Kancheepuram

TITLE	CITED BY	YEAR
Toward quantum efficiency enhancement of kesterite nanostructured absorber: A prospective of carrier quantization effect L Sravani, S Routray, KP Pradhan Applied Physics Letters 117 (13), 133901		2020
Effect of Nanostructure on Carrier Transport Mechanism of III- Nitride and Kesterite Solar Cells: A Computational Analysis S Routray, KP Pradhan, GP Mishra IEEE Journal of the Electron Devices Society		2020
An Optimized Ge Pocket SOI JLT with Efforts to Improve the Self-Heating Effect: Doping & Materials Perspective VP Ammina, SP Vankudothu, RR Shaik, KP Pradhan Silicon 12 (9), 2229-2239		2020
Label Free DNA Detection Techniques using Dielectric Modulated FET: Inversion or Tunneling? R Priyanka, L Chandrasekar, RR Shaik, KP Pradhan IEEE Sensors Journal		2020
Performance Evaluation of 10nm SMG FinFET with Architectural Variation towards DC/RF and Temperature Aspects GP Nikhil, C Dimri, PK Mohanty, KP Pradhan, GP Mishra, S Routray Silicon, 1-9		2020
Improvising the Switching Ratio through Low-k/High-k Spacer and Dielectric Gate Stack in 3D FinFET-a Simulation Perspective A Samal, KP Pradhan, SK Mohapatra Silicon, 1-6		2020
Extensive Study of Underlap Length Effect for 3-D SOI FinFET to Achieve High Switching Ratio and Low Power A Samal, KP Pradhan, SK Mohapatra Silicon, 1-6		2020
Assessment of Analog/RF performances for 10 nm Tri-metal Gate FinFET GP Nikhil, S Routray, KP Pradhan 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 1-4		2020

TITLE	CITED BY	YEAR
Performance Enhancement of Double Quantum Well Solar Cell by Strain-Modulated Piezo-Phototronics Effect S Routray, KP Pradhan, GP Mishra 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 1-4		2020
Carrier Density and Quantum Capacitance Model for Doped Graphene L Chandrasekar, KP Pradhan 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 1-4		2020
A Study of Workfunction Variation in Pocket Doped FD-SOI Technology Towards Temperature Analysis RR Shaik, G Arun, L Chandrasekar, KP Pradhan Silicon, 1-10	1	2020
Effect of Strain-Modulated Multiple Quantum Wells on Carrier Dynamics and Spectral Sensitivity of III-Nitride Photosensitive Devices  N Laxmi, S Routray, KP Pradhan IEEE Sensors Journal 20 (10), 5204-5212	1	2020
III-Nitride/Si Tandem Solar Cell for High Spectral Response: Key Attributes of Auto-tunneling Mechanisms N Laxmi, S Routray, KP Pradhan Silicon, 1-9		2019
Comparative Study on Nonlinearity of Doped and Undoped GFET using DC Characteristics KP Pradhan, P Kumar 2019 IEEE 16th India Council International Conference (INDICON), 1-4		2019
Optimization of Ge-pocket JLFET: An Approach to Extend The Scalable Limit AV Priya, VS Prasad, KP Pradhan 2019 IEEE 1st International Conference on Energy, Systems and Information		2019
InGaN/Si Hetero-Junction Tandem Solar Cell with Self Tunneling Effect: Proposal & Analysis N Laxmi, SR Routray, KP Pradhan 2019 Joint International EUROSOI Workshop and International Conference on		2019
Mole Fraction Dependency Electrical Performances of Extremely Thin SiGe on Insulator Junctionless Channel Transistor (SG-OI JLCT)  B Vandana, P Parashar, BS Patro, KP Pradhan, SK Mohapatra, JK Das Advances in Signal Processing and Communication, 573-581	1	2019

TITLE	CITED BY	YEAR
Electrically Modified SOI Structure to Reduce the Leakage RR Shaik, G Arun, KP Pradhan 2018 15th IEEE India Council International Conference (INDICON), 1-4		2018
3-D TCAD Assessment of Fin-Based Hybrid Devices Under Heavy Ion Irradiation in 20-nm Technology KP Pradhan, SK Saha, L Artola, PK Sahu IEEE Transactions on Device and Materials Reliability 18 (3), 474-480	1	2018
Device and circuit performance of Si-based accumulation- mode CGAA CMOS inverter SR Panda, KP Pradhan, PK Sahu Materials Science in Semiconductor Processing 66, 87-91	4	2017
Investigation of asymmetric high-k underlap spacer (AHUS) hybrid FinFET from temperature perspective KP Pradhan, PK Sahu Microsystem Technologies 23 (7), 2921-2926	8	2017
Exploration of Novel Attributes of Hybrid FinFETs towards Analog/RF and Reliability Aspects KP Pradhan		2017
RF and Noise performance exploration of Double Gate FinFET KP Pradhan, PK Sahu		2017
Study of fin tapering effect in nanoscale symmetric dual-k spacer (SDS) hybrid FinFETs KP Pradhan, PK Sahu Materials Science in Semiconductor Processing 57, 185-189	7	2017
Junctionless GAA nanowire transistor: towards circuit application SR Panda, R Sharma, KP Pradhan, PK Sahu 2016 3rd International Conference on Emerging Electronics (ICEE), 1-4	2	2016
Impact of fin height and fin angle variation on the performance matrix of hybrid FinFETs KP Pradhan, SK Saha, PK Sahu IEEE Transactions on Electron Devices 64 (1), 52-57	9	2016
Pros and cons of symmetrical dual-k spacer technology in hybrid FinFETs KP Pradhan, MGC Andrade, PK Sahu Superlattices and Microstructures 100, 335-341	5	2016
Heavy-Ion Irradiation effect in trigate SOI tunnel FETs with High-k Spacer technology KP Pradhan, PK Sahu 2016 IEEE Region 10 Conference (TENCON), 2373-2376	1	2016

TITLE	CITED BY	YEAR
Benefits of asymmetric underlap dual-k spacer hybrid fin field-effect transistor over bulk fin field-effect transistor (vol 10, pg 441, 2016)  KP Pradhan, PK Sahu IET CIRCUITS DEVICES & SYSTEMS 10 (6), 549-549		2016
Spacer engineered Trigate SOI TFET: An investigation towards harsh temperature environment applications R Ranjan, KP Pradhan, L Artola, PK Sahu Superlattices and Microstructures 97, 70-77	12	2016
Benefits of asymmetric underlap dual-k spacer hybrid fin field- effect transistor over bulk fin field-effect transistor KP Pradhan, KP Sahu IET Circuits, Devices & Systems 10 (5), 441-447	12	2016
A comprehensive investigation of silicon film thickness (T SI) of nanoscale DG TFET for low power applications R Ranjan, KP Pradhan, PK Sahu Advances in Natural Sciences: Nanoscience and Nanotechnology 7 (3), 035009	4	2016
Dielectric engineered symmetric underlap double gate tunnel FET (DGTFET): An investigation towards variation of dielectric materials R Ranjan, KP Pradhan, PK Sahu Superlattices and Microstructures 96, 226-233	4	2016
A complete analytical potential based solution for a 4H-SiC MOSFET in nanoscale MK Yadav, KP Pradhan, PK Sahu Advances in Natural Sciences: Nanoscience and Nanotechnology 7 (2), 025011	1	2016
Investigation on asymmetric dual-k spacer (ADS) Trigate Wavy FinFET: A novel device KP Pradhan, PK Sahu, R Ranjan 2016 3rd International Conference on Devices, Circuits and Systems (ICDCS	6	2016
Performance analysis of symmetric high-k spacer (SHS) Trigate SOI TFET M Rao, R Ranjan, KP Pradhan, PK Sahu 2016 3rd International Conference on Devices, Circuits and Systems (ICDCS	2	2016
Exploration of symmetric high-k spacer (SHS) hybrid FinFET for high performance application KP Pradhan, PK Sahu Superlattices and Microstructures 90, 191-197	31	2016

TITLE	CITED BY	YEAR
Temperature dependency of double material gate oxide (DMGO) symmetric dual-k spacer (SDS) wavy FinFET KP Pradhan, PK Sahu	15	2016
Superlattices and Microstructures 89, 355-361		