

Features

- Bluetooth® v4.1 specification fully qualified
- Radio includes integrated balun
- 80 MHz RISC MCU and 120 MHz Kalimba DSP
- Up to 120 MIPS DSP for intensive digital signal processing algorithms
- 24-bit audio
- 16 Mb internal flash; optional support for 64 Mb of external SPI flash
- Stereo codec with 2 channels of ADC and up to 6 microphone inputs (includes bias generation and digital microphone support)
- Audio interfaces:
 - 2 x I²S/PCM
 - 1 x SPDIF (independent of I²S/PCM ports)
- Serial interfaces: UART, USB 2.0 full-speed, I²C and SPI
- Integrated dual switch-mode regulators, linear regulators and battery charger
- 3 hardware LED controllers (for RGB) and ability to drive LCD segment display directly
- Support for up to 6 capacitive touch sensor inputs
- 6.5 x 6.5 x 1 mm, 0.5 mm pitch 112-ball VFBGA
- CSR8675 BGA application boards back compatible with CSR8670 BGA
- Green (RoHS compliant and no antimony or halogenated flame retardants)

BlueCore® CSR8675 BGA

Bluetooth Smart Ready

Low-power Solution for
DSP Intensive Audio Applications

Production Information

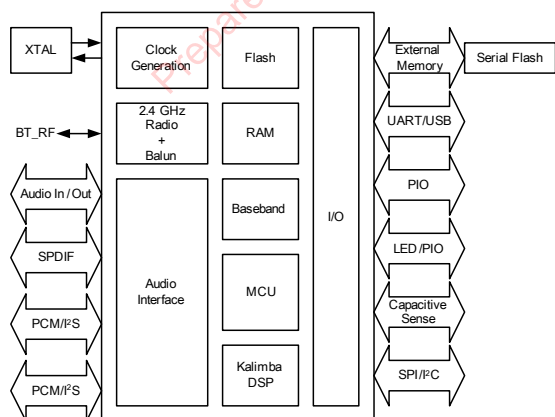
CSR8675B

Issue 5



General Description

CSR8675 BGA consumer audio platform for wired and wireless applications integrates an ultra-low-power DSP and application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, LED and LCD drivers and capacitive touch sensor inputs in a SoC IC.



Applications

- High-end wired/wireless stereo headphones
- High-end wired/wireless stereo headsets
- High-end wired/wireless active headsets
- Wireless stereo speakers
- Low-end docking stations and soundbars
- Gaming headsets

The dual-core architecture with flash memory enables manufacturers to easily differentiate their products with new features without extending development cycles.

The enhanced Kalimba DSP coprocessor with up to 120 MIPS supports more digital signal processing requirements in stereo headphones, headsets, gaming headsets and soundbars.

The audio codec supports 2 ADC channels, up to 6 microphone inputs, stereo output and a variety of audio standards.

CSR's popular BlueCore® CSR8670™ and BlueCore®5-Multimedia platforms are software-portable to the CSR8675 BGA, with easy migration of a broad range of solutions from CSR's eXtension partners. This enables rapid time-to-market deployment for a broad range of consumer electronic products.

Ordering Information

| Device | Package | | | Order Number |
|---------|-----------------------------|----------------------------------|-----------------|-----------------|
| | Type | Size | Shipment Method | |
| CSR8675 | VFBGA-112-ball (Pb free) | 6.5 x 6.5 x 1 mm 0.5 mm pitch | Tape and reel | CSR8675B-IBBH-R |

Note:

Minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

Contacts

General information

Information on this product

Customer support for this product

Details of compliance and standards

Help with this document

www.csr.com

sales@csr.com

www.csrsupport.com

product.compliance@csr.com

comments@csr.com

CSR8675 Development Kit Ordering Information

| Description | Order Number |
|--|---------------------|
| CSR8675 BGA Audio Development Kit | DK-CSR8675-10197-1A |
| CSR8675 BGA Development Kit (Board Only) | DB-CSR8675-10200-1A |

Device Details

Bluetooth low energy

- Dual-mode Bluetooth low energy radio
- Support for Bluetooth basic rate / EDR and low energy connections
- 3 Bluetooth low energy connections at the same time as basic rate A2DP

Bluetooth Radio

- On-chip balun (50 Ω impedance in TX and RX modes)
- No external trimming is required in production
- Bluetooth v4.1 specification software/hardware

Bluetooth Transmitter

- Typical RF transmit power
 - Basic rate 10 dBm
 - EDR -1 dB (relative power)
 - Bluetooth low energy 9 dBm
- 6-bit DAC level control
- Class 1, Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Bluetooth Receiver

- Typical RF receiver sensitivity:
 - Basic rate -90 dBm
 - EDR -92 dBm
 - Bluetooth low energy -93 dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available to application
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

Bluetooth Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 19.2 MHz to 32 MHz or an external clock 19.2 MHz to 40 MHz (default 26 MHz)

Kalimba DSP

- Enhanced Kalimba 5 DSP coprocessor
- 120 MHz clock, up to 120 MIPS performance
- 24-bit fixed-point core
- Single-cycle MAC:
 - 24 x 24-bit multiply
 - 56-bit accumulate
- Improved architecture and instructions for better performance over CSR8670 BGA
- 32-bit instruction word
- Dual 24-bit data memory
- 12 K x 32-bit program RAM including 1 K instruction cache for executing out of internal flash
- 2-bank data RAM:
 - DM1 32 K x 24-bit
 - DM2 32 K x 24-bit

Baseband and Software

- 16 Mb internal flash
- Memory protection unit supporting accelerated VM
- 56 KB internal RAM, enables full-speed data transfer, mixed voice/data and full piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ -law and linear voice via PCM and A-law, μ -law and CVSD voice over air

Audio Interfaces

- Audio codec with 2 high-quality dedicated ADCs
- 24-bit audio processing support
- 2 microphone bias generators and up to 2 analogue microphone inputs
- Up to 6 digital microphone inputs (MEMS)
- G.722 compatible, includes improved digital IIR filter path for stop-band attenuation required for G.722 compliance
- Enhanced side-tone gain control
- Supported sample rates of 8, 11.025, 16, 22.05, 32, 44.1, 48, 96 kHz and 192kHz (DAC only)

Physical Interfaces

- UART interface
- USB 2.0 interface (full-speed)
- Master and slave bit-serialiser (I²C and SPI)
- Up to 32 PIOs (includes 12 general purpose PIOs and unused digital interfaces also available as PIOs)
- SPI debug and programming interface with read access disable locking
- 2 x PCM/I²S and 1 x SPDIF supported simultaneously
- Dual/quad external serial flash memory interface
- 3 LED drivers (includes RGB) with PWM flasher on sleep clock
- Support for up to 6 capacitive touch sensor inputs
- 2 analogue PIOs

Integrated Power Control and Regulation

- 2 high-efficiency switch-mode regulators with 1.8 V and 1.35 V outputs from battery supply
- 3.3 V USB pad supply linear regulator
- Low-voltage linear regulator for internal digital supply
- Low-voltage linear regulator for internal analogue supply with 1.35 V output
- Power-on-reset detects low supply voltage
- Power management includes digital shutdown and wake-up commands with low-power crystal drive for ultra-low power Park/Sniff/Hold mode

Battery Charger

- Lithium ion / Lithium polymer battery charger with instant-on
- Fast charging support up to 200 mA with no external components
- Higher charge currents using external pass device
- Supports USB BCv1.2 CDP, DCP and SDP charger detection
- Charger pre-calibrated by CSR
- PSE compliance:
 - Design to JIS-C 8712/8714 (batteries)
 - Testing based on IEEE 1725

Auxiliary Features

- Customer application space available
- Crystal oscillator with built-in digital trimming
- Auxiliary ADC and DAC available to applications

Package Option

- 6.5 x 6.5 x 1 mm, 0.5 mm pitch 112-ball VFBGA

Production Information
© Cambridge Silicon Radio Limited 2013-2014
Confidential Information - This Material is Subject to CSR's Non-Disclosure Agreement



Document History

| Revision | Date | Change Reason |
|----------|-----------|---|
| 1 | 27 FEB 13 | Original publication of this document. Issue 1 content set as: <ul style="list-style-type: none"> Technical Overview material Functional block diagram Package information PIO configuration Example application schematic Green and RoHS information Tape and reel information |
| 2 | 12 FEB 14 | Full-version of Advance Information data sheet created. |
| 3 | 25 SEP 14 | Production Information added. |
| 4 | 26 SEP 14 | Additional Power Consumption information added. |
| 5 | 08 OCT 14 | Integrated Digital IIR Filter information updated. |

Status Information

The status of this Data Sheet is **Production Information**. CSR Product Data Sheets progress according to the following format:

- **Advance Information:**
 - Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
- **Engineering Sample:**
 - Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
 - All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.
- **Pre-production Information:**
 - Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
 - All electrical specifications may be changed by CSR without notice.
- **Production Information:**
 - Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.
 - Production Data Sheets supersede all previous document versions.

Device Implementation

Important Note:

As the feature-set of the CSR8675 BGA is firmware build-specific, see the relevant software release note for the exact implementation of features on the CSR8675 BGA.

Life Support Policy and Use in Safety-critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

CSR Green Semiconductor Products and RoHS Compliance

CSR8675 BGA devices meet the requirements of Directive 2011/65/EU of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). CSR8675 BGA devices are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

Trademarks, Patents and Licences

Unless otherwise stated, words and logos marked with [™] or [®] are trademarks registered or owned by CSR plc or its affiliates. Bluetooth[®] and the Bluetooth[®] logos are trademarks owned by Bluetooth[®] SIG, Inc. and licensed to CSR. Other products, services and names used in this document may have been trademarked by their respective owners.

The publication of this information does not imply that any license is granted under any patent or other rights owned by CSR plc and/or its affiliates.

CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

Refer to www.csrsupport.com for compliance and conformance to standards information.

Contents

| | | |
|----------|--|-----------|
| | Ordering Information | 2 |
| | Contacts | 2 |
| | CSR8675 Development Kit Ordering Information | 2 |
| | Device Details | 3 |
| | Functional Block Diagram | 4 |
| 1 | Package Information | 13 |
| 1.1 | Pinout Diagram | 13 |
| 1.2 | Device Terminal Functions | 14 |
| 1.3 | Package Dimensions | 23 |
| 1.4 | PCB Design and Assembly Considerations | 24 |
| 1.5 | Typical Solder Reflow Profile | 24 |
| 2 | System Architecture | 25 |
| 3 | Bluetooth Modem | 26 |
| 3.1 | RF Ports | 26 |
| 3.1.1 | BT_RF | 26 |
| 3.2 | RF Receiver | 26 |
| 3.2.1 | Low Noise Amplifier | 26 |
| 3.2.2 | RSSI Analogue to Digital Converter | 26 |
| 3.3 | RF Transmitter | 26 |
| 3.3.1 | IQ Modulator | 26 |
| 3.3.2 | Power Amplifier | 27 |
| 3.4 | Bluetooth Radio Synthesiser | 27 |
| 3.5 | Baseband | 27 |
| 3.5.1 | Burst Mode Controller | 27 |
| 3.5.2 | Physical Layer Hardware Engine | 27 |
| 4 | Clock Generation | 28 |
| 4.1 | Clock Architecture | 28 |
| 4.2 | Input Frequencies and PS Key Settings | 28 |
| 4.3 | External Reference Clock | 28 |
| 4.3.1 | Input: XTAL_IN | 28 |
| 4.3.2 | XTAL_IN Impedance in External Mode | 29 |
| 4.3.3 | Clock Timing Accuracy | 29 |
| 4.4 | Crystal Oscillator: XTAL_IN and XTAL_OUT | 30 |
| 4.4.1 | Crystal Calibration | 30 |
| 4.4.2 | Crystal Specification | 30 |
| 5 | Bluetooth Stack Microcontroller | 31 |
| 5.1 | VM Accelerator | 31 |
| 6 | Kalimba DSP | 32 |
| 7 | Memory Interface and Management | 33 |
| 7.1 | Memory Management Unit | 33 |
| 7.2 | System RAM | 33 |
| 7.3 | Kalimba DSP RAM | 33 |
| 7.4 | eFlash Memory (16 Mb) | 33 |
| 7.5 | Serial Quad I/O Flash Interface (SQIF) | 33 |
| 8 | Serial Interfaces | 35 |
| 8.1 | USB Interface | 35 |
| 8.2 | UART Interface | 35 |
| 8.2.1 | UART Configuration While Reset is Active | 36 |
| 8.3 | Programming and Debug Interface | 36 |

| | | |
|-----------|---|-----------|
| 8.3.1 | Instruction Cycle | 37 |
| 8.3.2 | Multi-slave Operation | 37 |
| 8.3.3 | SPI-lock | 37 |
| 8.4 | I ² C Interface | 37 |
| 9 | Interfaces | 38 |
| 9.1 | Programmable I/O Ports, PIO | 38 |
| 9.2 | Analogue I/O Ports, AIO | 39 |
| 9.3 | Capacitive Touch Sensor | 39 |
| 9.3.1 | Capacitive Range Control: | 40 |
| 9.3.2 | Sampling Front End | 40 |
| 9.3.3 | ADC | 40 |
| 9.3.4 | Digital Signal Conditioning (Digital Processing) | 40 |
| 9.3.5 | Software Signal Conditioning (Firmware) | 41 |
| 9.3.6 | VM | 41 |
| 9.4 | LED Drivers | 41 |
| 10 | Audio Interface | 43 |
| 10.1 | Audio Input and Output | 44 |
| 10.2 | Audio Codec Interface | 44 |
| 10.2.1 | Audio Codec Block Diagram | 45 |
| 10.2.2 | Codec Set-up | 45 |
| 10.2.3 | ADC | 45 |
| 10.2.4 | ADC Sample Rate Selection | 46 |
| 10.2.5 | ADC Audio Input Gain | 46 |
| 10.2.6 | ADC Pre-amplifier and ADC Analogue Gain | 46 |
| 10.2.7 | ADC Digital Gain | 46 |
| 10.2.8 | ADC Digital IIR Filter | 47 |
| 10.2.9 | DAC | 47 |
| 10.2.10 | DAC Sample Rate Selection | 47 |
| 10.2.11 | DAC Digital Gain | 47 |
| 10.2.12 | DAC Analogue Gain | 48 |
| 10.2.13 | DAC Digital FIR Filter | 48 |
| 10.2.14 | IEC 60958 Interface | 48 |
| 10.2.15 | Microphone Input | 49 |
| 10.2.16 | Digital Microphone Inputs | 50 |
| 10.2.17 | Line Input | 51 |
| 10.2.18 | Output Stage | 51 |
| 10.2.19 | Mono Operation | 52 |
| 10.2.20 | Side Tone | 53 |
| 10.2.21 | Integrated Digital IIR Filter | 54 |
| 10.3 | PCM1 and PCM2 Interface | 55 |
| 10.3.1 | PCM Interface Master/Slave | 55 |
| 10.3.2 | Long Frame Sync | 56 |
| 10.3.3 | Short Frame Sync | 57 |
| 10.3.4 | Multi-slot Operation | 57 |
| 10.3.5 | GCI Interface | 57 |
| 10.3.6 | Slots and Sample Formats | 58 |
| 10.3.7 | Additional Features | 59 |
| 10.3.8 | PCM Timing Information | 59 |
| 10.3.9 | PCM_CLK and PCM_SYNC Generation | 63 |
| 10.3.10 | PCM Configuration | 63 |
| 10.4 | I ² S1 and I ² S2 Interface | 64 |
| 11 | WLAN Coexistence Interface | 67 |

| | | |
|-----------|--|------------|
| 12 | Power Control and Regulation | 68 |
| 12.1 | 1.8V Switch-mode Regulator | 71 |
| 12.2 | 1.35V Switch-mode Regulator | 72 |
| 12.3 | 1.8V and 1.35V Switch-mode Regulators Combined | 73 |
| 12.4 | Bypass LDO Linear Regulator | 74 |
| 12.5 | Low-voltage VDD_DIG Linear Regulator | 75 |
| 12.6 | Low-voltage VDD_AUX Linear Regulator | 75 |
| 12.7 | Low-voltage VDD_ANA Linear Regulator | 75 |
| 12.8 | Voltage Regulator Enable | 75 |
| 12.9 | External Regulators and Power Sequencing | 75 |
| 12.10 | Reset, RST# | 76 |
| 12.10.1 | Digital Pin States on Reset | 76 |
| 12.10.2 | Status After Reset | 77 |
| 12.11 | Automatic Reset Protection | 77 |
| 13 | Battery Charger | 78 |
| 13.1 | Battery Charger Hardware Operating Modes | 78 |
| 13.1.1 | Disabled Mode | 79 |
| 13.1.2 | Trickle Charge Mode | 79 |
| 13.1.3 | Fast Charge Mode | 79 |
| 13.1.4 | Standby Mode | 79 |
| 13.1.5 | Error Mode | 79 |
| 13.2 | Battery Charger Trimming and Calibration | 79 |
| 13.3 | VM Battery Charger Control | 79 |
| 13.4 | Battery Charger Firmware and PS Keys | 79 |
| 13.5 | External Mode | 80 |
| 14 | Example Application Schematic | 81 |
| 15 | Example Application Using Different Power Supply Configurations | 82 |
| 16 | Electrical Characteristics | 85 |
| 16.1 | Absolute Maximum Ratings | 85 |
| 16.2 | Recommended Operating Conditions | 86 |
| 16.3 | Input/Output Terminal Characteristics | 87 |
| 16.3.1 | Regulators: Available For External Use | 87 |
| 16.3.2 | Regulators: For Internal Use Only | 89 |
| 16.3.3 | Regulator Enable | 90 |
| 16.3.4 | Battery Charger | 90 |
| 16.3.5 | Reset | 92 |
| 16.3.6 | USB | 93 |
| 16.3.7 | Clocks | 93 |
| 16.3.8 | Stereo Codec: Analogue to Digital Converter | 94 |
| 16.3.9 | Stereo Codec: Digital to Analogue Converter | 95 |
| 16.3.10 | Digital | 96 |
| 16.3.11 | LED Driver Pads | 96 |
| 16.3.12 | Auxiliary ADC | 97 |
| 16.3.13 | Auxiliary DAC | 97 |
| 16.4 | ESD Protection | 98 |
| 16.4.1 | USB Electrostatic Discharge Immunity | 98 |
| 17 | Power Consumption | 100 |
| 18 | CSR Green Semiconductor Products and RoHS Compliance | 101 |
| 19 | Software | 102 |
| 19.1 | On-chip Software | 102 |
| 19.1.1 | Stand-alone CSR8675 BGA and Kalimba DSP Applications | 102 |
| 19.1.2 | BlueCore HCI Stack | 102 |

| | |
|---|------------|
| 19.2 Off-chip Software | 103 |
| 19.2.1 CSR8675 Development Kit | 103 |
| 19.2.2 eXtension Program Support | 104 |
| 20 Tape and Reel Information | 105 |
| 20.1 Tape Orientation | 105 |
| 20.2 Tape Dimensions | 105 |
| 20.3 Reel Information | 106 |
| 20.4 Moisture Sensitivity Level | 106 |
| 21 Document References | 107 |
| Terms and Definitions | 108 |

List of Figures

| | |
|--|----|
| Figure 1.1 Pinout Diagram | 13 |
| Figure 2.1 Standard Headset | 25 |
| Figure 2.2 Extended Headset | 25 |
| Figure 2.3 Processing 5.1 Channels | 25 |
| Figure 2.4 DDFA Companion Device | 25 |
| Figure 3.1 Simplified Circuit BT_RF | 26 |
| Figure 4.1 Clock Architecture | 28 |
| Figure 4.2 TCXO Clock Accuracy | 29 |
| Figure 6.1 Kalimba DSP Interface to Internal Functions | 32 |
| Figure 7.1 Serial Quad I/O Flash Interface | 33 |
| Figure 8.1 Universal Asynchronous Receiver Transmitter (UART) | 35 |
| Figure 8.2 Break Signal | 36 |
| Figure 9.1 Capacitive Touch Sensor Block Diagram | 39 |
| Figure 9.2 LED Equivalent Circuit | 41 |
| Figure 10.1 Audio Interface | 43 |
| Figure 10.2 Audio Codec Input and Output Stages | 45 |
| Figure 10.3 Audio Input Gain | 46 |
| Figure 10.4 Example Circuit for SPDIF Interface (Co-axial) | 49 |
| Figure 10.5 Example Circuit for SPDIF Interface (Optical) | 49 |
| Figure 10.6 Microphone Biasing | 50 |
| Figure 10.7 Differential Input | 51 |
| Figure 10.8 Single-ended Input | 51 |
| Figure 10.9 Speaker Output | 52 |
| Figure 10.10 Side Tone | 53 |
| Figure 10.11 PCM Interface Master | 56 |
| Figure 10.12 PCM Interface Slave | 56 |
| Figure 10.13 Long Frame Sync (Shown with 8-bit Companded Sample) | 56 |
| Figure 10.14 Short Frame Sync (Shown with 16-bit Sample) | 57 |
| Figure 10.15 Multi-slot Operation with 2 Slots and 8-bit Companded Samples | 57 |
| Figure 10.16 GCI Interface | 58 |
| Figure 10.17 16-bit Slot Length and Sample Formats | 59 |
| Figure 10.18 PCM Master Timing Long Frame Sync | 60 |
| Figure 10.19 PCM Master Timing Short Frame Sync | 61 |
| Figure 10.20 PCM Slave Timing Long Frame Sync | 62 |
| Figure 10.21 PCM Slave Timing Short Frame Sync | 63 |
| Figure 10.22 I ² S Digital Audio Interface Modes | 64 |
| Figure 10.23 Digital Audio Interface Slave Timing | 65 |
| Figure 10.24 Digital Audio Interface Master Timing | 66 |
| Figure 12.1 1.80V and 1.35V Dual-supply Switch-mode System Configuration | 69 |

| | | |
|-------------|--|-----|
| Figure 12.2 | 1.80V Parallel-supply Switch-mode System Configuration | 70 |
| Figure 12.3 | External 1.8V System Configuration | 71 |
| Figure 12.4 | 1.8V Switch-mode Regulator Output Configuration | 72 |
| Figure 12.5 | 1.35V Switch-mode Regulator Output Configuration | 73 |
| Figure 12.6 | 1.8V and 1.35V Switch-mode Regulators Outputs Parallel Configuration | 74 |
| Figure 13.1 | Battery Charger Mode-to-Mode Transition Diagram | 78 |
| Figure 13.2 | Battery Charger External Mode Typical Configuration | 80 |
| Figure 15.1 | External 1.8V Supply Example Application | 82 |
| Figure 15.2 | External 3.3V Supply Example Application | 83 |
| Figure 15.3 | USB Dongle Example Application | 84 |
| Figure 19.1 | Stand-alone CSR8675 BGA and Kalimba DSP Applications | 102 |
| Figure 19.2 | BlueCore HCI Stack | 103 |
| Figure 20.1 | Tape Orientation | 105 |
| Figure 20.2 | Tape Dimensions | 105 |
| Figure 20.3 | Reel Dimensions | 106 |

List of Tables

| | | |
|-------------|---|----|
| Table 1.1 | RF Interface | 14 |
| Table 1.2 | Clock Interface | 14 |
| Table 1.3 | UART Interface | 14 |
| Table 1.4 | USB Interface | 14 |
| Table 1.5 | Debug SPI Interface | 15 |
| Table 1.6 | PIO Port: LED Drivers | 15 |
| Table 1.7 | PIO Port: Serial Quad I/O Flash/SRAM Interface | 16 |
| Table 1.8 | PIO Port: PCM 1/I ² S 1 Interface | 17 |
| Table 1.9 | PIO Port: UART Interface | 17 |
| Table 1.10 | PIO Port: General I/O PIO[15:8] | 18 |
| Table 1.11 | PIO Port: PCM 2/I ² S 2 Interface | 18 |
| Table 1.12 | PIO Port: General I/O PIO[3:0] | 19 |
| Table 1.13 | Analogue I/O Interface | 19 |
| Table 1.14 | Capacitive Touch Sensor Interface | 19 |
| Table 1.15 | Reset | 19 |
| Table 1.16 | Analogue Audio Interface | 19 |
| Table 1.17 | Power Supplies and Control | 20 |
| Table 1.18 | Grounds | 22 |
| Table 4.1 | PS Key Values for CDMA/3G Phone TCXO | 28 |
| Table 4.2 | External Clock Specifications | 29 |
| Table 8.1 | Possible UART Settings | 36 |
| Table 8.2 | Instruction Cycle for a SPI Transaction | 37 |
| Table 9.1 | Alternative PIO Functions | 38 |
| Table 10.1 | Shared Pins on PCM/I ² S Interfaces | 44 |
| Table 10.2 | ADC Audio Input Gain Rate | 47 |
| Table 10.3 | DAC Digital Gain Rate Selection | 48 |
| Table 10.4 | DAC Analogue Gain Rate Selection | 48 |
| Table 10.5 | Side Tone Gain | 53 |
| Table 10.6 | PCM Master Timing | 59 |
| Table 10.7 | PCM Slave Timing | 62 |
| Table 10.8 | Digital Audio Interface Slave Timing | 65 |
| Table 10.9 | I ² S Slave Mode Timing | 65 |
| Table 10.10 | Digital Audio Interface Master Timing | 66 |
| Table 10.11 | I ² S Master Mode Timing Parameters, WS and SCK as Outputs | 66 |

| | | |
|------------|---|----|
| Table 12.1 | Recommended Configurations for Power Control and Regulation | 68 |
| Table 12.2 | Pin States on Reset | 76 |
| Table 13.1 | Battery Charger Operating Modes Determined by Battery Voltage and Current | 78 |
| Table 16.1 | ESD Handling Ratings | 98 |
| Table 16.2 | USB Electrostatic Discharge Protection Level | 98 |

List of Equations

| | | |
|---------------|--|----|
| Equation 4.1 | Crystal Calibration Using PSKEY_ANA_FTRIM_OFFSET | 30 |
| Equation 4.2 | Example of PSKEY_ANA_FTRIM_OFFSET Value for 2402.0168MHz | 30 |
| Equation 4.3 | Example of PSKEY_ANA_FTRIM_OFFSET Value for 2401.9832MHz | 30 |
| Equation 9.1 | LED Current | 41 |
| Equation 9.2 | LED PAD Voltage | 41 |
| Equation 10.1 | IIR Filter Transfer Function, $H(z)$ | 55 |
| Equation 10.2 | IIR Filter Plus DC Blocking Transfer Function, $H_{DC}(z)$ | 55 |
| Equation 10.3 | PCM_CLK Frequency Generated Using the Internal 48MHz Clock | 63 |
| Equation 10.4 | PCM_SYNC Frequency Relative to PCM_CLK | 63 |

1 Package Information

1.1 Pinout Diagram

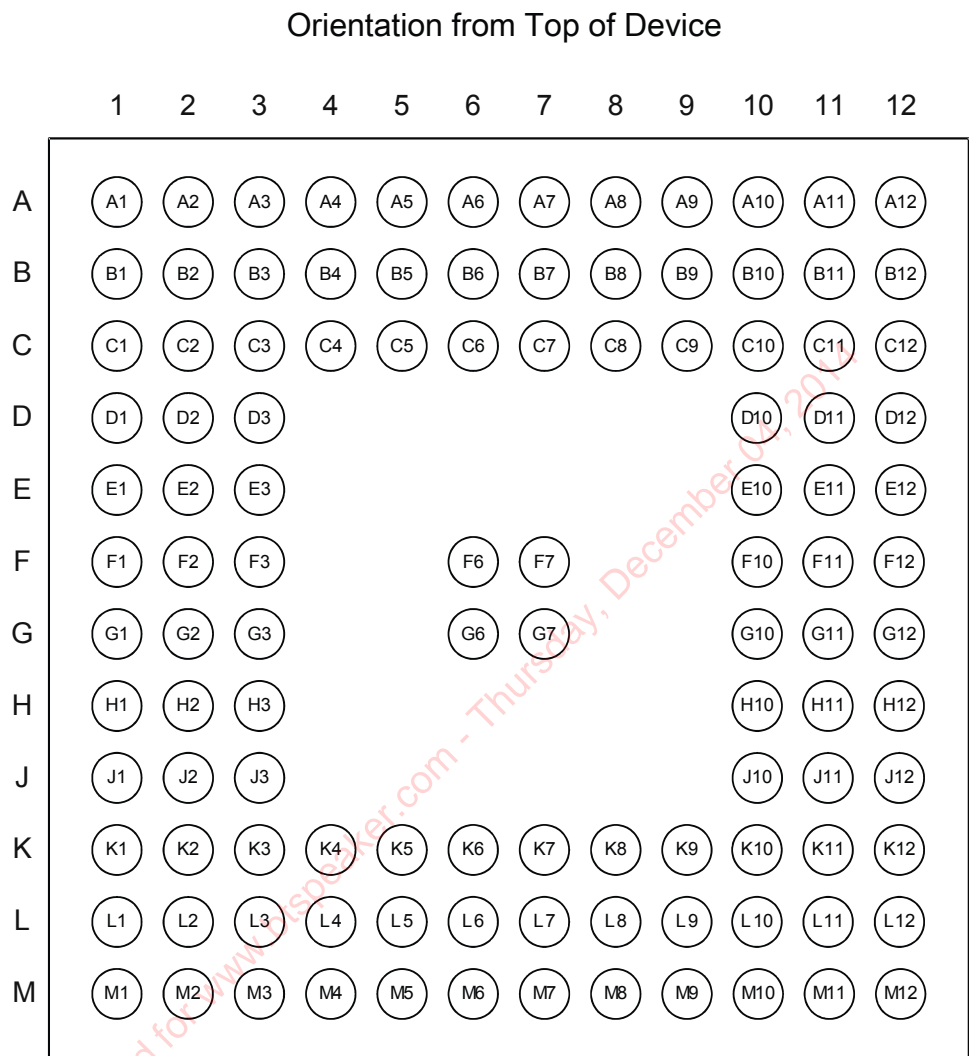


Figure 1.1: Pinout Diagram

1.2 Device Terminal Functions

Note:

Some terminals on CSR8675 BGA have programmable a pull resistor for direction (up or down) and strength (weak or strong). In this section, the pad type for these terminals represents the default configuration. For more information for the implementation of these terminals see the relevant software release note, as they are firmware build-specific.

| Radio | Ball | Pad Type | Supply Domain | Description |
|-------|------|----------|---------------|---|
| BT_RF | A3 | RF | VDD_BT_RADIO | Bluetooth 50Ω transmitter output / receiver input |

Table 1.1: RF Interface

| Synthesiser and Oscillator | Ball | Pad Type | Supply Domain | Description |
|----------------------------|------|----------|---------------|-------------------------------------|
| XTAL_IN | C1 | Analogue | VDD_AUX | For crystal or external clock input |
| XTAL_OUT | B1 | | | Drive for crystal |

Table 1.2: Clock Interface

| UART | Ball | Pad Type | Supply Domain | Description |
|----------|------|-----------------------------------|---------------|---------------------------------|
| UART_TX | M3 | Bidirectional with weak pull-up | VDD_PADS_1 | UART data output. |
| UART_RX | M2 | Bidirectional with strong pull-up | VDD_PADS_1 | UART data input. |
| UART_CTS | L3 | Bidirectional with weak pull-down | VDD_PADS_1 | UART clear to send, active low. |

Table 1.3: UART Interface

Note:

The UART ready to send pin (UART_RTS) is available on PIO[16], see Table 1.9.

| USB | Ball | Pad Type | Supply Domain | Description |
|-------|------|---------------|---------------|---|
| USB_P | M9 | Bidirectional | VDD_USB | USB data plus with selectable internal 1.5kΩ pull-up resistor |
| USB_N | M10 | | | USB data minus |

Table 1.4: USB Interface

| SPI Interface | Ball | Pad Type | Supply Domain | Description |
|---------------|------|----------------------------|---------------|---------------------------------|
| SPI_MISO | L2 | Output with weak pull-down | VDD_PADS_1 | SPI data output |
| SPI_MOSI | G3 | Input with weak pull-down | | SPI data input |
| SPI_CS# | M1 | Input with strong pull-up | | Chip select for SPI, active low |
| SPI_CLK | E1 | Input with weak pull-down | | SPI clock |

Table 1.5: Debug SPI Interface

Note:

Table 1.6 to Table 1.12 list alternative functions mapped on to the PIO ports. For more information, including where the SPDIF is mapped on to the PIO ports, see Section 9.1.

| PIO Port: LED Drivers | Ball | Pad Type | Supply Domain | Description |
|-----------------------|------|------------|---|--|
| PIO[31] | K5 | Open drain | VDD_PADS_1 Open drain tolerant to 4.25 V | Programmable I/O line 31. Main function: ■ LED[1]: LED driver 1. |
| PIO[30] | K4 | Open drain | VDD_PADS_1 Open drain tolerant to 4.25 V | Programmable I/O line 30. Main function: ■ LED[0]: LED driver 0. |
| PIO[29] | M4 | Open drain | VDD_PADS_1 Open drain tolerant to 4.25 V | Programmable I/O line 29. Main function: ■ LED[2]: LED driver 2. |

Table 1.6: PIO Port: LED Drivers

| PIO Port: Serial Quad I/O Flash | Ball | Pad Type | Supply Domain | Description |
|---------------------------------|------|-------------------------------------|---------------|---|
| PIO[28] | D12 | Bidirectional with strong pull-down | VDD_PADS_3 | Programmable I/O line 28. Alternative function: ■ QSPI_FLASH_IO[3]: serial quad I/O flash data bit 3. |
| PIO[27] | C10 | Bidirectional with strong pull-down | VDD_PADS_3 | Programmable I/O line 27. Alternative function: ■ QSPI_FLASH_IO[2]: serial quad I/O flash data bit 2. |
| PIO[26] | B11 | Bidirectional with strong pull-down | VDD_PADS_3 | Programmable I/O line 26. Alternative function: ■ QSPI_FLASH_IO[1]: serial quad I/O flash data bit 1. |
| PIO[25] | C11 | Bidirectional with strong pull-down | VDD_PADS_3 | Programmable I/O line 25. Alternative function: ■ QSPI_FLASH_IO[0]: serial quad I/O flash data bit 0. |
| PIO[24] | B10 | Bidirectional with strong pull-up | VDD_PADS_3 | Programmable I/O line 24. Alternative function: ■ QSPI_SRAM_CS#: SPI RAM chip select. |
| PIO[23] | D11 | Bidirectional with strong pull-up | VDD_PADS_3 | Programmable I/O line 23. Alternative function: ■ QSPI_FLASH_CS#: SPI flash chip select. |
| PIO[22] | B12 | Bidirectional with strong pull-down | VDD_PADS_3 | Programmable I/O line 22. Alternative function: ■ QSPI_SRAM_CLK: SPI RAM clock. |
| PIO[21] | C12 | Bidirectional with strong pull-down | VDD_PADS_3 | Programmable I/O line 21. Alternative function: ■ QSPI_FLASH_CLK: SPI flash clock |

Table 1.7: PIO Port: Serial Quad I/O Flash/SRAM Interface

| PIO Port: PCM 1/I ² S 1 Interface | Ball | Pad Type | Supply Domain | Description |
|--|------|-----------------------------------|---------------|---|
| PIO[20] | G2 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 20. Alternative function: <ul style="list-style-type: none"> PCM1_CLK: synchronous data clock. SCK1: I²S clock |
| PIO[19] | H2 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 19. Alternative function: <ul style="list-style-type: none"> PCM1_SYNC: synchronous data sync. WS1: I²S word select |
| PIO[18] | H3 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 18. Alternative function: <ul style="list-style-type: none"> PCM1_OUT: synchronous data output. SD1_OUT: I²S data output |
| PIO[17] | F1 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 17. Alternative function: <ul style="list-style-type: none"> PCM1_IN: synchronous data input. SD1_IN: I²S data input |

Table 1.8: PIO Port: PCM 1/I²S 1 Interface

| PIO Port: UART | Ball | Pad Type | Supply Domain | Description |
|----------------|------|---------------------------------|---------------|---|
| PIO[16] | K3 | Bidirectional with weak pull-up | VDD_PADS_1 | Programmable I/O line 16. Alternative function: <ul style="list-style-type: none"> UART_RTS: UART request to send, active low. |

Table 1.9: PIO Port: UART Interface

| PIO Port: General I/O | Ball | Pad Type | Supply Domain | Description |
|-----------------------|------|-----------------------------------|---------------|---------------------------|
| PIO[15] | L6 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 15. |
| PIO[14] | M7 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 14. |
| PIO[13] | J10 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 13. |
| PIO[12] | K10 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 12. |
| PIO[11] | L9 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 11. |
| PIO[10] | M8 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 10. |
| PIO[9] | L10 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 9. |
| PIO[8] | L8 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 8. |

Table 1.10: PIO Port: General I/O PIO[15:8]

| PIO Port: PCM 2/I ² S 2 Interface | Ball | Pad Type | Supply Domain | Description |
|--|------|-----------------------------------|---------------|--|
| PIO[7] | K9 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 7. Alternative function: <ul style="list-style-type: none"> PCM2_CLK: synchronous data clock. SCK2: I²S clock |
| PIO[6] | M6 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 6. Alternative function: <ul style="list-style-type: none"> PCM2_SYNC: synchronous data sync. WS2: I²S word select |
| PIO[5] | L7 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 5. Alternative function: <ul style="list-style-type: none"> PCM2_OUT: synchronous data output. SD2_OUT: I²S data output |
| PIO[4] | K8 | Bidirectional with weak pull-down | VDD_PADS_2 | Programmable I/O line 4. Alternative function: <ul style="list-style-type: none"> PCM2_IN: synchronous data input. SD2_IN: I²S data input |

Table 1.11: PIO Port: PCM 2/I²S 2 Interface

| PIO Port: General I/O | Ball | Pad Type | Supply Domain | Description |
|-----------------------|------|-----------------------------------|---------------|--------------------------|
| PIO[3] | K6 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 3. |
| PIO[2] | M5 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 2. |
| PIO[1] | L5 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 1. |
| PIO[0] | L4 | Bidirectional with weak pull-down | VDD_PADS_1 | Programmable I/O line 0. |

Table 1.12: PIO Port: General I/O PIO[3:0]

| Analogue I/O | Ball | Pad Type | Supply Domain | Description |
|--------------|------|---------------|---------------|-----------------------------------|
| AIO[1] | D1 | Bidirectional | VDD_AUX | Analogue programmable I/O line 1. |
| AIO[0] | C4 | Bidirectional | VDD_AUX | Analogue programmable I/O line 0. |

Table 1.13: Analogue I/O Interface

| Capacitive Touch Sensor | Ball | Pad Type | Supply Domain | Description |
|-------------------------|------|----------------|---------------|--------------------------------|
| CAP_SENSE[5] | F2 | Analogue input | VDD_AUX_1V8 | Capacitive touch sensor input. |
| CAP_SENSE[4] | F3 | | | |
| CAP_SENSE[3] | E3 | | | |
| CAP_SENSE[2] | E2 | | | |
| CAP_SENSE[1] | D3 | | | |
| CAP_SENSE[0] | D2 | | | |

Table 1.14: Capacitive Touch Sensor Interface

| Reset | Ball | Pad Type | Supply Domain | Description |
|-------|------|---------------------------|---------------|---|
| RST# | L1 | Input with strong pull-up | VDD_PADS_1 | Reset if low. Input debounced so must be low for >5ms to cause a reset. |

Table 1.15: Reset

| Codec | Ball | Pad Type | Supply Domain | Description |
|--------|------|-------------|---------------|----------------------------------|
| MIC_LP | A10 | Analogue in | VDD_AUDIO | Microphone input positive, left |
| MIC_LN | A11 | | | Microphone input negative, left |
| MIC_RP | C7 | Analogue in | VDD_AUDIO | Microphone input positive, right |
| MIC_RN | C8 | | | Microphone input negative, right |

| Codec | Ball | Pad Type | Supply Domain | Description |
|------------|------|--------------|-----------------|--|
| MIC_BIAS_A | A9 | Analogue out | VBAT / VOUT_3V3 | Microphone bias A |
| MIC_BIAS_B | B8 | Analogue out | VBAT / VOUT_3V3 | Microphone bias B |
| SPKR_LP | C5 | Analogue out | VDD_AUDIO_DRV | Speaker output positive, left |
| SPKR_LN | C6 | | | Speaker output negative, left |
| SPKR_RP | B7 | Analogue out | VDD_AUDIO_DRV | Speaker output positive, right |
| SPKR_RN | A7 | | | Speaker output negative, right |
| AU_REF | B9 | Analogue in | VDD_AUDIO | Decoupling of audio reference (for high-quality audio) |

Table 1.16: Analogue Audio Interface

| Power Supplies and Control | Ball | Description |
|----------------------------|----------|--|
| CHG_EXT | F11 | External battery charger control. |
| LX_1V35 | L12 | 1.35 V switch-mode power regulator output. |
| LX_1V8 | J12 | 1.8 V switch-mode power regulator output. |
| SMP_VBAT | K12 | 1.8 V and 1.35 V switch-mode power supply regulator inputs. Must be at the same potential as VBAT. |
| SMPS_1V35_SENSE | M11 | 1.35 V switch-mode power regulator sense input. |
| SMPS_1V8_SENSE | F10 | 1.8 V switch-mode power regulator sense input. |
| SMPS_3V3 | K11 | Alternative supply via bypass regulator for 1.8 V and 1.35 V switch-mode power supply regulator inputs. Must be at the same potential as VOUT_3V3. |
| VBAT | H12 | Battery positive terminal. |
| VBAT_SENSE | H11 | Battery charger sense input. |
| VCHG | G11, G12 | Battery charger input. |
| VOUT_3V3 | F12 | 3.3 V bypass linear regulator output. |
| VDD_ANA | C2 | Analogue LDO linear regulator output (1.35 V). |
| VDD_AUDIO | A8 | Positive supply for audio (1.35 V). |
| VDD_AUDIO_DRV | A6 | Positive supply for audio driver (1.8 V). |
| VDD_AUX | C3 | Auxiliary LDO. |
| VDD_AUX_1V8 | A1 | Auxiliary and analogue LDO linear regulator input (1.8 V) / auxiliary circuits. |

| Power Supplies and Control | Ball | Description |
|----------------------------|---------|--|
| VDD_BT_LO | A2 | Bluetooth radio local oscillator supply. Connect to the 1.35 V rail via a 2.2 Ω resistor and decouple locally with a 4.7 μ F capacitor, as schematics in Section 14 and Section 15 show. These additional components are required to meet published 3Mb EDR performance with heavy DSP use. This configuration is also compatible with CSR8670 BGA in applications requiring common layout. |
| VDD_BT_RADIO | A5 | Bluetooth radio supply, also optional sense input for 1.35 V analogue linear regulator. |
| VDD_DIG_EFLASH | E12, K2 | Digital LDO linear regulator output (0.85 to 1.2 V). CSR recommends due to increased current draw that K2 is connected to E12 on CSR8675 BGA designs. This is back compatible with CSR8670 BGA. |
| VDD_EFLASH_1V8 | J1 | Flash supply input. |
| VDD_PADS_1 | K1 | 1.7 V to 3.6 V positive supply input for input/output ports: <ul style="list-style-type: none"> ■ RST# ■ UART ■ PCM 1 ■ SPI ■ LED[2:0]/PIO[31:29] ■ PIO[3:0] Note: VDD_PADS1 must be present for CSR8675 BGA to exit reset state. |
| VDD_PADS_2 | K7 | 1.7 to 3.6 V positive supply input for digital input/output ports PIO[15:4]. |
| VDD_PADS_3 | A12 | 1.7 to 3.6 V positive supply input for PIO[28:21] (serial quad I/O flash port). |
| VDD_USB | L11 | Positive supply for USB ports. |
| VREGENABLE | E10 | Regulator enable input. |
| VREGIN_DIG | E11 | Digital LDO linear regulator input. |

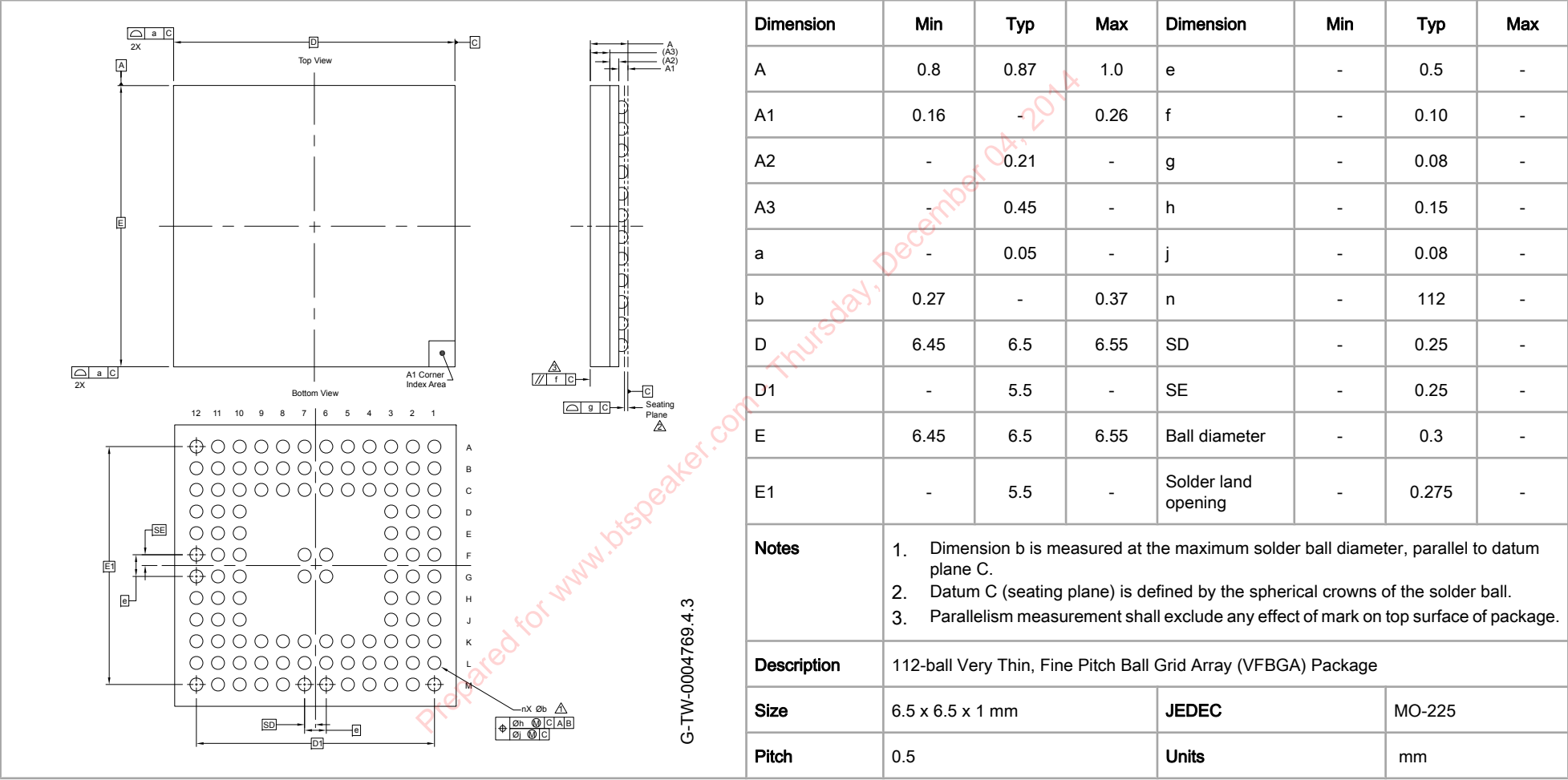
Table 1.17: Power Supplies and Control

| Grounds | Ball | Description |
|---------------|-----------------------|---|
| VSS_AUDIO | C9 | Ground connection for audio. |
| VSS_AUDIO_DRV | B6 | Ground connection for audio driver. |
| VSS_BT_LO_AUX | B2 | Ground connections for analogue circuitry and Bluetooth radio local oscillator. |
| VSS_BT_RF | A4, B5 | Bluetooth radio ground. |
| VSS_DIG | D10, F7, G7, G10, H10 | Ground connection for internal digital circuitry and pads |
| VSS_SMPS_1V35 | M12 | 1.35 V switch-mode regulator ground. |
| VSS_SMPS_1V8 | J11 | 1.8 V switch-mode regulator ground. |

Table 1.18: Grounds

| Unconnected Terminals | Ball | Description |
|-----------------------|------------------------|---|
| NC or optional ground | B3, B4 | Leave unconnected or ground connection. |
| NC | F6, G1, G6, H1, J2, J3 | Leave unconnected. |

1.3 Package Dimensions



1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 6.5 x 6.5 x 1 mm VFBGA 112-ball package:

- NSMD lands, i.e. lands smaller than the solder mask aperture, are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, use via-in-pad technology to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible, this needs to take into consideration its current carrying and the RF requirements.
- 35µm thick (1oz) copper lands are recommended rather than 17µm thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be the same as that on the package to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process because this adds to the final volume of solder in the joint, increasing its reliability.
- When using a nickel gold plating finish, the gold thickness should be kept below 0.5µm to prevent brittle gold/tin intermetallics forming in the solder.

1.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

2 System Architecture

Figure 2.1 shows a completely embedded solution using internal codec.

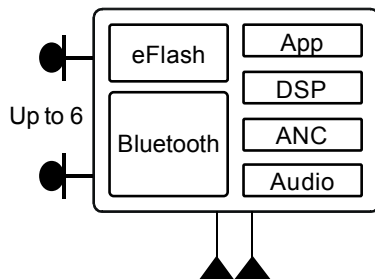


Figure 2.1: Standard Headset

Figure 2.3 shows processing 5.1 channels in the Kalimba DSP.

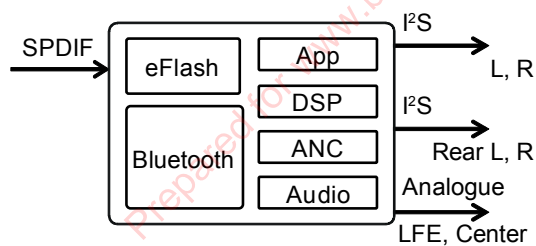


Figure 2.3: Processing 5.1 Channels

Figure 2.2 shows I²S loopback to an external DSP for processing. Audio output is via the DACs of the internal codec.

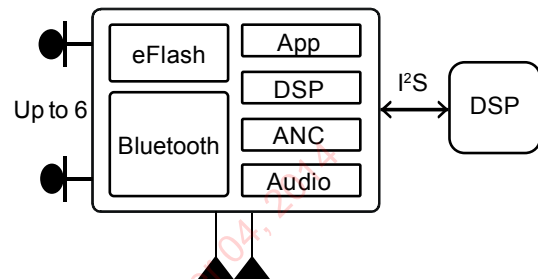


Figure 2.2: Extended Headset

Figure 2.4 shows SPDIF input for Soundbar/AVR applications (TV/DVD input) and I²S output for DDFA or equivalent.

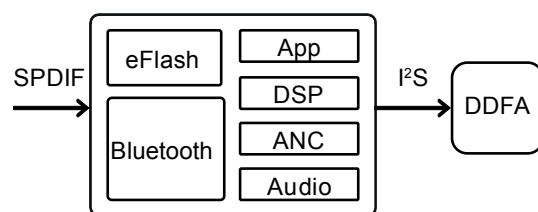


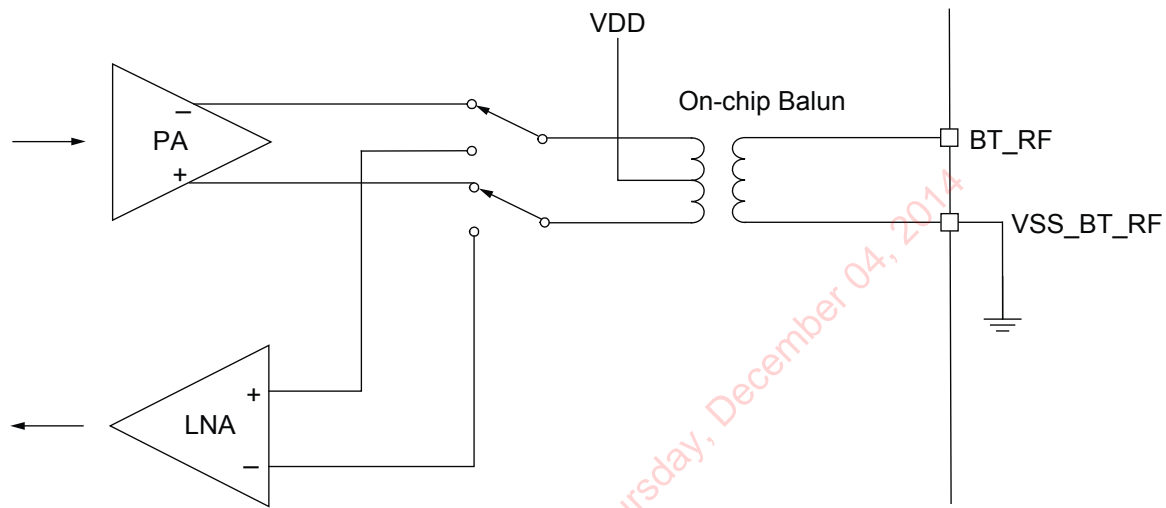
Figure 2.4: DDFA Companion Device

3 Bluetooth Modem

3.1 RF Ports

3.1.1 BT_RF

CSR8675 BGA contains an on-chip balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive. No matching components are needed as the receive mode impedance is 50Ω and the transmitter has been optimised to deliver power into a 50Ω load.



G-TW-0005523.2.2

Figure 3.1: Simplified Circuit BT_RF

3.2 RF Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. A digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise enables CSR8675 BGA to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

3.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the on-chip balun.

3.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

3.3 RF Transmitter

3.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

3.3.2 Power Amplifier

The internal PA output power is software controlled and configured through a PS Key. The internal PA on the CSR8675 BGA has a maximum output power that enables it to operate as a Class 1, Class 2 and Class 3 Bluetooth radio without requiring an external RF PA.

3.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.1 specification.

3.5 Baseband

3.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

3.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/ μ -law/linear voice data (from optional host)
- A-law/ μ -law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware can be used as part of a fully compliant Bluetooth v4.1 specification system.

4 Clock Generation

CSR8675 BGA requires a Bluetooth reference clock frequency of 19.2 MHz to 40 MHz (default 26 MHz) from either an externally connected crystal or from an external TCXO source.

All CSR8675 BGA internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external 19.2 MHz to 40 MHz (default 26 MHz) reference clock source or safely free-runs at a reduced frequency.

The Bluetooth operation determines the use of the watchdog clock in low-power modes.

4.1 Clock Architecture

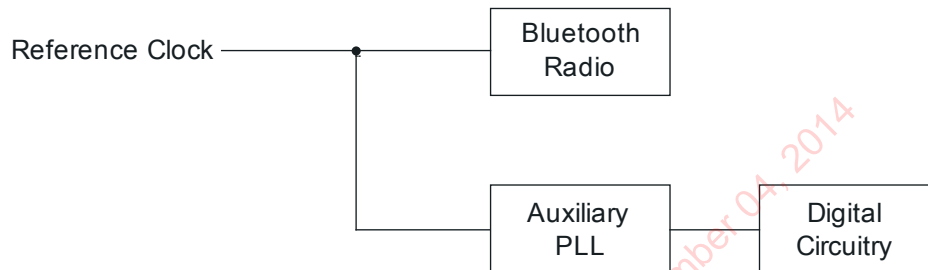


Figure 4.1: Clock Architecture

4.2 Input Frequencies and PS Key Settings

Configure the CSR8675 BGA to operate with the chosen reference frequency. Set PSKEY_ANA_FREQ for all frequencies with an integer multiple of 250kHz. The input frequency default setting in CSR8675 BGA is 26 MHz depending on the software build. Full details are in the software release note for the specific build from www.csr.support.com.

The following CDMA/3G phone TCXO frequencies are supported: 19.2, 19.44, 19.68, 19.8 and 38.4 MHz. The value of the PS Key is a multiple of 1kHz, so 38.4MHz is selected by using a PS Key value of 38400.

| Reference Crystal Frequency (MHz) | PSKEY_ANA_FREQ (kHz) |
|-----------------------------------|----------------------|
| 19.20 | 19200 |
| 19.44 | 19440 |
| 19.68 | 19680 |
| 19.80 | 19800 |
| 38.40 | 38400 |
| n x 0.25 | n x 250 |
| 26.00 (default) | 26000 |

Table 4.1: PS Key Values for CDMA/3G Phone TCXO

4.3 External Reference Clock

4.3.1 Input: XTAL_IN

Apply the external reference clock to the CSR8675 BGA XTAL_IN input. CSR8675 BGA is configured to accept the external reference clock at XTAL_IN by connecting XTAL_OUT to ground.

Supply the external clock with either a digital level square wave or low-level sinusoidal, coupling this directly to the XTAL_IN without the need for additional components. The DC clock level is permitted at any voltage level between the supply rails, i.e. VSS_BT_LO_AUX to VDD_AUX.

The external reference clock is required in active and deep sleep modes, so must be present when CSR8675 BGA is enabled.

Table 4.2 lists the specification for the external reference clock signal.

| | | | Min | Typ | Max | Unit |
|--------------------------------|---------------------|-----------------|-------|------------------------|------------------------|---------|
| Frequency ^(a) | | | 19.2 | 26 | 40 | MHz |
| Duty cycle | | | 40:60 | 50:50 | 60:40 | - |
| Edge jitter (at zero crossing) | | | - | - | 10 | ps rms |
| DC level | | | -0.4 | - | VDD_AUX + 0.4 | V |
| Signal level | AC coupled sinusoid | | 0.2 | 0.4 | VDD_AUX ^(b) | V pk-pk |
| | DC coupled digital | V _{IL} | - | VSS_BT_LO_AUX | - | V |
| | | V _{IH} | - | VDD_AUX ^(b) | - | V |

Table 4.2: External Clock Specifications

^(a) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

^(b) VDD_AUX is 1.35V nominal

4.3.2 XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between operating modes. When transitioning from deep sleep to active states the capacitive load can change, see PSKEY_XTAL_OSC_CONFIG. For this reason CSR recommends using a buffered clock input.

4.3.3 Clock Timing Accuracy

Figure 4.2 shows the 250ppm timing accuracy on the external clock is required 2ms after the firmware begins to run. This guarantees that the firmware maintains timing accuracy in accordance with the Bluetooth v4.1 specification. Radio activity occurs after 6ms after the firmware starts. Therefore, at this point the timing accuracy of the external clock source must be within $\pm 20\text{ppm}$.

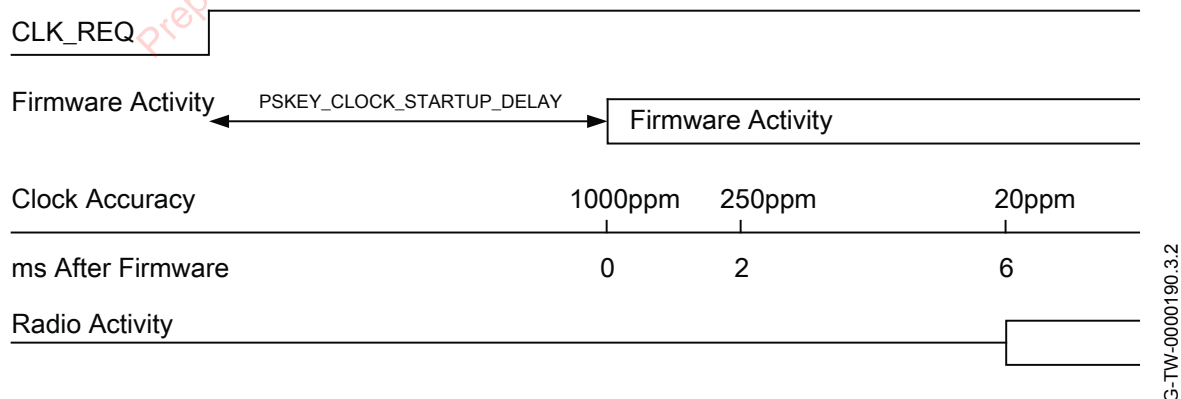


Figure 4.2: TCXO Clock Accuracy

4.4 Crystal Oscillator: XTAL_IN and XTAL_OUT

CSR8675 BGA contains a crystal driver circuit that acts as a transconductance amplifier driving an external crystal between XTAL_IN and XTAL_OUT. The crystal driver circuit forms a Pierce oscillator with the external crystal. No external crystal load capacitors are required for typical crystals.

4.4.1 Crystal Calibration

The actual crystal frequency depends on the capacitance of XTAL_IN and XTAL_OUT on the PCB and the CSR8675 BGA, as well as the capacitance of the crystal. Correct calibration of the Bluetooth radio is done on a per-device basis on the production line, with the trim value stored in non-volatile memory (PS Key).

Crystal calibration uses a single measurement. The measurement finds the actual offset from the desired frequency and the offset is stored in PSKEY_ANA_FTRIM_OFFSET. The firmware then compensates for the frequency offset on the CSR8675 BGA. Typically, a TXSTART radio test is performed to obtain the actual frequency and it is compared against the output frequency with the requested frequency using an RF analyser. The test station calculates the offset ratio and programs it into PSKEY_ANA_FTRIM_OFFSET. The value in PSKEY_ANA_FTRIM_OFFSET is a 16-bit 2's complement signed integer which specifies the fractional part of the ratio between the true crystal frequency, f_{actual} , and the value set in PSKEY_ANA_FREQ, f_{nominal} . Equation 4.1 shows the value of PSKEY_ANA_FTRIM_OFFSET in parts per 2^{20} rounded to the nearest integer.

For more information on TXSTART radio test see *BlueTest User Guide*.

$$\text{PSKEY_ANA_FTRIM_OFFSET} = \left(\frac{f_{\text{actual}}}{f_{\text{nominal}}} - 1 \right) \times 2^{20}$$

Equation 4.1: Crystal Calibration Using PSKEY_ANA_FTRIM_OFFSET

For a requested frequency of 2402MHz with an actual output of 2402.0168MHz the PSKEY_ANA_FTRIM_OFFSET value is 7, see Equation 4.2.

$$\text{PSKEY_ANA_FTRIM_OFFSET} = \left(\frac{2402.0168}{2402} - 1 \right) \times 2^{20} \approx 7$$

Equation 4.2: Example of PSKEY_ANA_FTRIM_OFFSET Value for 2402.0168MHz

For a requested frequency of 2402MHz with an actual output of 2401.9832MHz the PSKEY_ANA_FTRIM_OFFSET value is -7 (0xff9), see Equation 4.3.

$$\text{PSKEY_ANA_FTRIM_OFFSET} = \left(\frac{2401.9832}{2402} - 1 \right) \times 2^{20} \approx -7$$

Equation 4.3: Example of PSKEY_ANA_FTRIM_OFFSET Value for 2401.9832MHz

4.4.2 Crystal Specification

Section 16.3.7 shows the specification for an external crystal.

5 Bluetooth Stack Microcontroller

The CSR8675 BGA uses a 16-bit RISC 80MHz MCU for low power consumption and efficient use of memory. It contains a single-cycle multiplier and a memory protection unit for the VM accelerator, see Section 5.1.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

5.1 VM Accelerator

CSR8675 BGA contains a VM accelerator alongside the MCU. This hardware accelerator improves the performance of VM applications.

Prepared for www.btspeaker.com - Thursday, December 04, 2014

6 Kalimba DSP

The Kalimba DSP is an open platform DSP enabling signal processing functions to be performed on over-air data or codec data to enhance audio applications. Figure 6.1 shows the Kalimba DSP interfaces to other functional blocks within CSR8675 BGA.

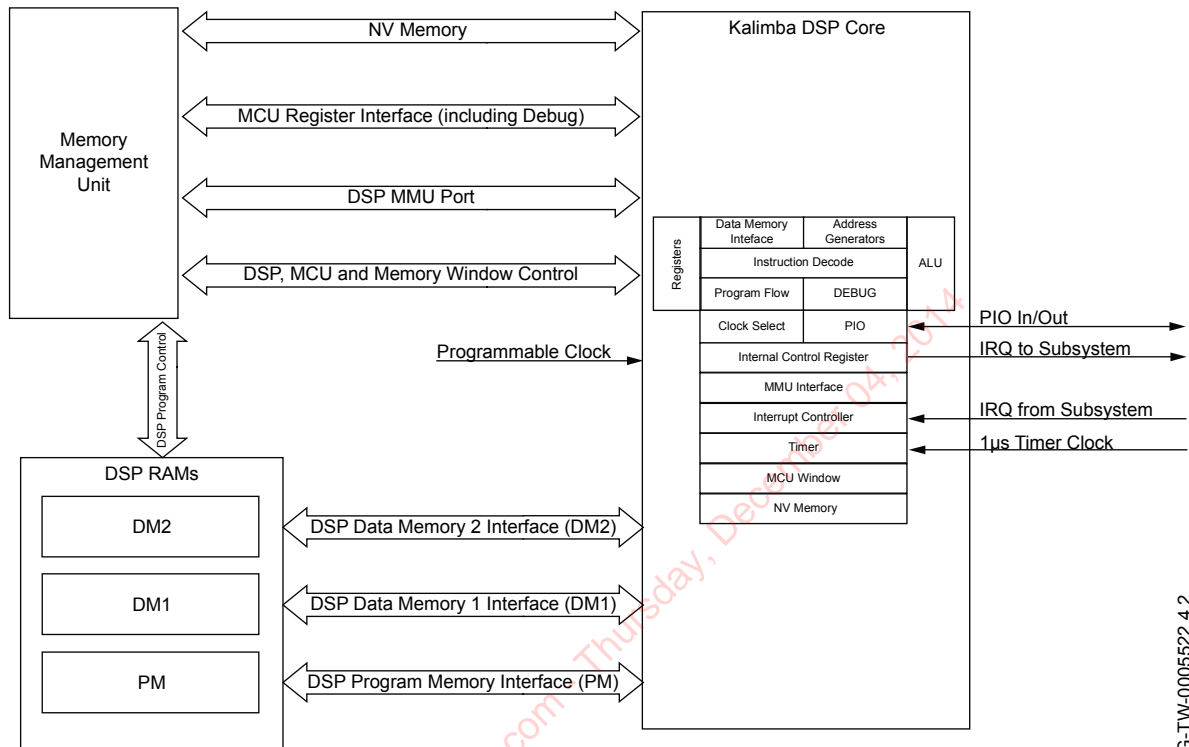


Figure 6.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 120 MHz clock, giving up to 120 MIPS performance
- 24-bit fixed-point DSP core
- Single-cycle MAC:
 - 24 x 24-bit multiply
 - 56-bit accumulate includes 2 rMAC registers
- New instructions for improved performance over previous CSR8670 BGA architecture
- 32-bit instruction word
- Separate program memory and dual data memory, enabling an ALU operation and up to 2 memory accesses in a single cycle
- Zero overhead looping
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 56-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

7 Memory Interface and Management

7.1 Memory Management Unit

The MMU provides dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers. The use of DMA ports also helps with efficient transfer of data to other peripherals.

7.2 System RAM

56 KB of integrated RAM supports the RISC MCU and is shared between the ring buffers for holding voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

7.3 Kalimba DSP RAM

Additional integrated RAM provides support for the Kalimba DSP:

- 32 K x 24-bit for data memory 1 (DM1)
- 32 K x 24-bit for data memory 2 (DM2)
- 12 K x 32-bit for program memory (PM)

Note:

The Kalimba DSP can also execute directly from internal flash or external SQIF, using a 1K-instruction on-chip cache.

7.4 eFlash Memory (16 Mb)

The internal flash memory provides 16 Mb of internal code and data storage. The internal flash stores CSR8675 BGA settings and program code, and Kalimba DSP coprocessor code and data. For improved performance, the internal flash memory has 45 ns access time and is organised as 64-bit wide.

7.5 Serial Quad I/O Flash Interface (SQIF)

CSR8675 BGA supports external serial flash and SRAM ICs. This enables additional data storage areas for device-specific data. CSR8675 BGA supports serial single, dual or quad I/O devices with a 1-bit, 2-bit or 4-bit multiplexed I/O flash-memory interface. Figure 7.1 shows a typical connection between the CSR8675 BGA and a serial flash and SRAM IC.

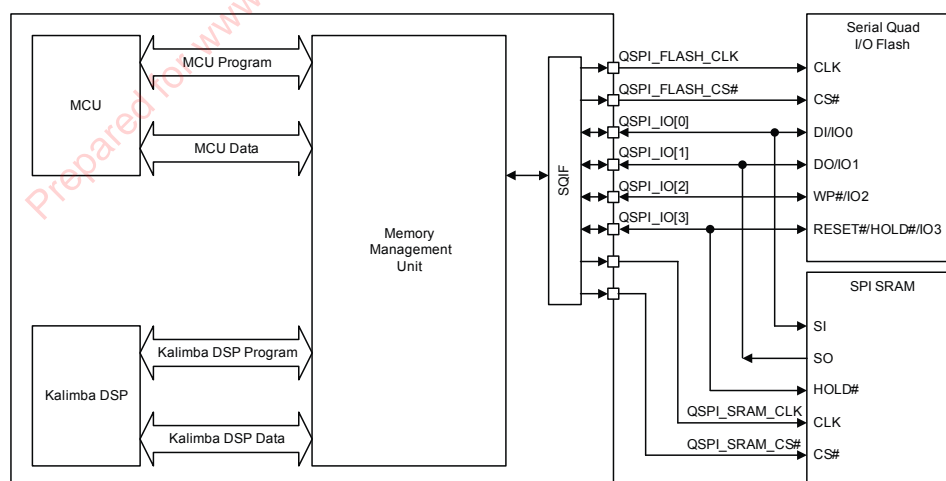


Figure 7.1: Serial Quad I/O Flash Interface

The SQIF interface on the CSR8675 BGA supports:

- Flash and SRAM serial memory, which are also visible in the MCU and Kalimba DSP program address space

Note:

SRAM serial memory support depends on firmware version, for more information contact CSR.

- MCU and Kalimba DSP data access through a generic window
- Concurrent program and / or data accesses from the MCU and / or Kalimba DSP (although efficiency suffers)
- Separate prefetch buffers for MCU program, MCU data, Kalimba DSP program, Kalimba DSP data:
 - Each buffer is 4 x 16-bit
 - Defined minimum length prefetch
 - Prefetch continues if accesses are contiguous (and buffer not full)
 - Prefetch does not automatically restart as buffer empties
 - Prefetch is enabled and disabled by software control, which enables optimisation of sequential / random data access patterns
 - Flash and SRAM use same prefetch buffer
- Serial flash devices up to 64Mb with 1-bit, 2-bit and 4-bit wide transfers, see firmware release note for up-to-date device support
- Selected serial SRAM devices up to 512Kb with 1-bit wide transfers, see firmware release note for up-to-date device support
- Flash / SRAM performance:
 - Clocks up to 80/16MHz
 - The control and address overhead is 14/24 cycles per burst read, with support for Word Read Quad Continuous (Winbond) and High Speed Read Quad (Microchip (SST)). Microchip (SST) indexed instructions are not supported.
 - Data transfer is 4/16 cycles per 16-bits
- Flash instruction sequences:
 - Requires considerable (run-time) programmable configuration
 - Set up for either read, or write (not both)
 - Software configures SQIF for specific flash attached
- SRAM instruction sequences:
 - Interface is hard wired
 - Reads and writes can interleave without need for any reconfiguration
- All other management of serial flash / SRAM via software:
 - Memory mapped registers support transfers of data to and from the flash
 - Software needs to read the serial flash JEDEC ID in order to index a table of flash characteristics
 - Software driven sequence to enable, e.g. the Winbond Continuous Read Mode

Note:

CSR8675 BGA cannot boot up from serial flash.

8 Serial Interfaces

8.1 USB Interface

CSR8675 BGA has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on CSR8675 BGA acts as a USB peripheral, responding to requests from a master host controller.

CSR8675 BGA supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)* and *USB Battery Charging Specification*, available from <http://www.usb.org>. For more information on how to integrate the USB interface on CSR8675 BGA see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring (when VBUS is >3.1)
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
 - Global suspend
 - Selective suspend, includes remote wake
 - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
 - Suspend mode current draw
 - PIO status in suspend mode
 - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

8.2 UART Interface

This is a standard UART interface for communicating with other serial devices.

CSR8675 BGA UART interface provides a simple mechanism for communicating with other serial devices using the RS-232 protocol.

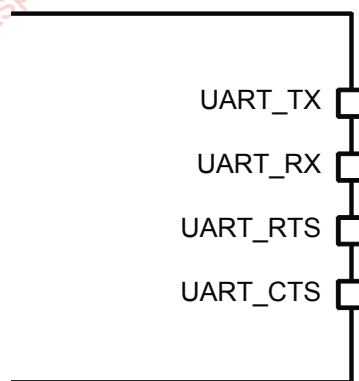


Figure 8.1: Universal Asynchronous Receiver Transmitter (UART)

Figure 8.1 shows the 4 signals that implement the UART function. When CSR8675 BGA is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement RS232 hardware flow control where both are active low indicators.

If UART_CTS and UART_RTS are not required for hardware flow control, they are reconfigurable as PIO.

UART configuration parameters, such as baud rate and packet format, are set using CSR8675 BGA firmware.

Note:

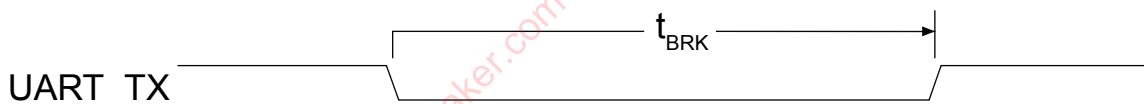
To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Table 8.1 shows the possible UART settings.

| Parameter | | Possible Values |
|---------------------|---------|-------------------------------|
| Baud rate | Minimum | 1200 baud ($\leq 2\%$ Error) |
| | | 9600 baud ($\leq 1\%$ Error) |
| | Maximum | 4 Mbaud ($\leq 1\%$ Error) |
| Flow control | | RTS/CTS or None |
| Parity | | None, Odd or Even |
| Number of stop bits | | 1 or 2 |
| Bits per byte | | 8 |

Table 8.1: Possible UART Settings

The UART interface resets CSR8675 BGA on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as Figure 8.2 shows. If t_{BRK} is longer than the value defined by the PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature enables a host to initialise the system to a known state. Also, CSR8675 BGA can issue a break character for waking the host.



G-TW-0000250.5.2

Figure 8.2: Break Signal

Refer to PSKEY_UART_BITRATE for more information about the baud rates and their values.

Generated baud rate is independent of selected incoming clock frequency.

8.2.1 UART Configuration While Reset is Active

The UART interface is tristate while CSR8675 BGA is being held in reset. This enables the user to connect other devices onto the physical UART bus. The restriction with this method is that any devices connected to this bus must tristate when CSR8675 BGA reset is de-asserted and the firmware begins to run.

8.3 Programming and Debug Interface

Important Note:

The SPI is for programming, configuring (PS Keys) and debugging the CSR8675 BGA. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

CSR8675 BGA uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

8.3.1 Instruction Cycle

The CSR8675 BGA is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8.2 shows the instruction cycle for a SPI transaction.

| | | |
|---|--------------------------|---|
| 1 | Reset the SPI interface | Hold SPI_CS# high for two SPI_CLK cycles |
| 2 | Write the command word | Take SPI_CS# low and clock in the 8-bit command |
| 3 | Write the address | Clock in the 16-bit address word |
| 4 | Write or read data words | Clock in or out 16-bit data word(s) |
| 5 | Termination | Take SPI_CS# high |

Table 8.2: Instruction Cycle for a SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the CSR8675 BGA on the rising edge of the clock line SPI_CLK. When reading, CSR8675 BGA replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. Taking SPI_CS# high terminates the transaction.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when transferring large amounts of data. To overcome this CSR8675 BGA offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.3.2 Multi-slave Operation

Avoid connecting CSR8675 BGA in a multi-slave arrangement by simple parallel connection of slave MISO lines. When CSR8675 BGA is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, CSR8675 BGA outputs 0 if the processor is running or 1 if it is stopped.

8.3.3 SPI-lock

CSR8675 BGA contains an SPI-lock security feature to prevent unauthorised access to CSR8675 BGA and its firmware.

Warranty:

- While exercising all reasonable care and diligence in the design of the SPI-lock feature, CSR does not warrant its functionality. CSR disclaims any liability arising out of the SPI-lock feature to the maximum extent permitted by law.

8.4 I²C Interface

CSR8675 BGA contains a configurable hardware I²C interface. For more information contact CSR.

Note:

CSR8675 BGA supports a software I²C interface for low speed functions, including driving a dot matrix LCD, keyboard scanner or EEPROM.

9 Interfaces

9.1 Programmable I/O Ports, PIO

CSR8675 BGA provides 32 lines of programmable bidirectional I/O, PIO[31:0]. Some of the PIOs on the CSR8675 BGA have alternative functions, see Table 9.1.

| PIO | Function | | | | |
|-----------|-----------|------------------|------------------|----------|--------|
| | PCM | I ² S | SPI Flash | UART | LED |
| PIO[31] | - | - | - | - | LED[1] |
| PIO[30] | - | - | - | - | LED[0] |
| PIO[29] | - | - | - | - | LED[2] |
| PIO[28] | - | - | QSPI_FLASH_IO[3] | - | - |
| PIO[27] | - | - | QSPI_FLASH_IO[2] | - | - |
| PIO[26] | - | - | QSPI_FLASH_IO[1] | - | - |
| PIO[25] | - | - | QSPI_FLASH_IO[0] | - | - |
| PIO[24] | - | - | QSPI_SRAM_CS# | - | - |
| PIO[23] | - | - | QSPI_FLASH_CS# | - | - |
| PIO[22] | - | - | QSPI_SRAM_CLK | - | - |
| PIO[21] | - | - | QSPI_FLASH_CLK | - | - |
| PIO[20] | PCM1_CLK | SCK1 | - | - | - |
| PIO[19] | PCM1_SYNC | WS1 | - | - | - |
| PIO[18] | PCM1_OUT | SD1_OUT | - | - | - |
| PIO[17] | PCM1_IN | SD1_IN | - | - | - |
| PIO[16] | - | - | - | UART_RTS | - |
| PIO[15:8] | - | - | - | - | - |
| PIO[7] | PCM2_CLK | SCK2 | - | - | - |
| PIO[6] | PCM2_SYNC | WS2 | - | - | - |
| PIO[5] | PCM2_OUT | SD2_OUT | - | - | - |
| PIO[4] | PCM2_IN | SD2_IN | - | - | - |
| PIO[3:0] | - | - | - | - | - |

Table 9.1: Alternative PIO Functions

Note:

The SPDIF interface is available on any unused PIO. The data output (SPDIF_OUT) is restricted to even numbered PIO, and the data input (SPDIF_IN) is restricted to odd numbered PIO.

See the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

9.2 Analogue I/O Ports, AIO

CSR8675 BGA has 2 general-purpose analogue interface pins, AIO[1:0], for accessing internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC and a 10-bit DAC. Signals selectable on this interface include the band gap reference voltage. When configured for analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals generated from within the analogue part of the device, the output voltage level is determined by VDD_AUX.

9.3 Capacitive Touch Sensor

CSR8675 BGA capacitive touch sensor interface features:

- Support for up to 6 capacitive touch sensing electrodes:
 - Printed on the PCB
 - Made from flex PCB
- Configuration for individual buttons
- Configuration for a wipe-type arrangement where 2 or more pads sense taps at each end or a wipe from one side to the other
- Operates in deep sleep and is a programmable source for wake-up

Figure 9.1 shows the system block diagram for the capacitive touch sensor interface. The interface depends on the capacitive touch sensor type. Therefore the overall control of the capacitive touch sensor interface resides in the VM, so it is easily modified in each end-user application.

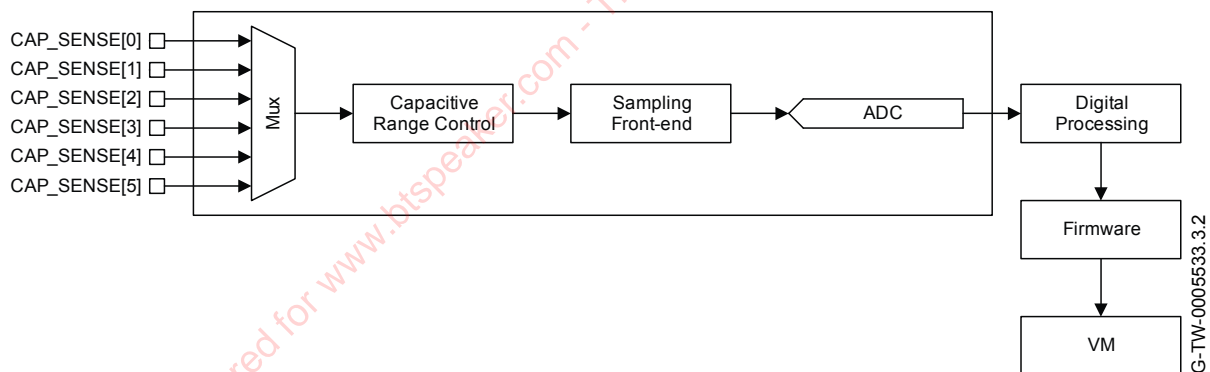


Figure 9.1: Capacitive Touch Sensor Block Diagram

The overall system-level specification for the capacitive touch sensor interface on the CSR8675 BGA is:

- 6 inputs multiplexed in to 1 touch sensor on the front-end
- Capacitances of 0 pF to 50 pF measured with a resolution of 4fF, where a touch is assumed to be between ± 50 fF and ± 1 pF
- Each reading takes 172 μ s:
 - 6 pads read every 1.03 ms
- System auto-calibrates to remove parasitic and environmental effects including:
 - PCB construction
 - Temperature
 - Humidity
- Works in normal and deep sleep modes
- System current is approximately 50 μ A from the battery
- The touch sensor also functions like a PIO

Figure 9.1 shows the system block diagram, it highlights the top-level architecture for the capacitive touch sensor interface and consists of:

- Capacitive range control, see Section 9.3.1
- Sampling front end, see Section 9.3.2
- ADC, see Section 9.3.3
- Digital signal conditioning (digital processing), see Section 9.3.4
- Software signal conditioning (firmware), see Section 9.3.5
- VM, see Section 9.3.6

For more information on CSR8675 BGA capacitive touch sensor configuration see *Configuring the Touch Sensor on CSR867x*.

9.3.1 Capacitive Range Control:

Figure 9.1 shows the capacitive range control function:

- Sets the rough capacitance of the touch sensor pad, which is product dependent
- Splits into 4 integrated capacitors
- The VM selects which capacitors are enabled, i.e. the range capacitance

9.3.2 Sampling Front End

Figure 9.1 shows the sampling front end function:

- An internal capacitance is trimmed by the digital state machine ensuring:
 - Touch Capacitance = Range Capacitance + Internal Capacitance
- When the internal capacitance is correctly trimmed:
 - The sense voltage is 0 V
 - A touch changes the touch capacitance, which then changes the sense voltage

9.3.3 ADC

Figure 9.1 shows the ADC:

- Uses a successive approximation, charge redistribution ADC
- Clocked at 64 kHz
- 9-bit resolution, where LSB is ± 2 fF and full range is ± 1 pF
- The internal capacitance is a 7-bit variable capacitor with 114 fF steps and 14.5 pF range
- The internal capacitance is trimmed, putting it in the mid range of the ADC. This enables measurements from 0 pF to 50 pF, where a capacitive touch is between ± 50 fF and ± 1 pF.

9.3.4 Digital Signal Conditioning (Digital Processing)

Figure 9.1 shows the digital processing block which is responsible for digital signal conditioning:

- Only the enabled inputs are scanned
- Enabling fewer inputs increases readings per second
- Averaging of ADC readings reduces noise, this is software programmable from 1 to 64 readings in intervals to the power of 2
- The internal capacitance updates using a rolling average of the ADC readings, software programmable from 1 to 2^{15} readings in intervals to the power of 2. For example, 32768 readings take approximately:
 - 5.6 s if polling one pad (no averaging)
 - 33.8 s if polling 6 pads (no averaging)
- Pulse skipping mode is possible, reducing the current consumption. Here the system waits a programmable number of 64 kHz clock cycles (maximum 2^9) before the next read, i.e. an 8 ms maximum pause.
- ADC trigger level is software programmable. If the threshold is crossed the firmware gets an interrupt.
- 6 hardware event registers store the pad number and trigger time, which enables the system to sense swipes.
- Programmable hysteresis, with one value for all pads

9.3.5 Software Signal Conditioning (Firmware)

Figure 9.1 shows the firmware block which is responsible for software signal conditioning:

- The firmware reads ADC and C_{int} values after an interrupt as the hardware only stores the pad number and trigger time
- Digital state machine scans pads and calibrates the internal capacitance
- If a swipe happens in deep sleep the firmware reads the trigger order and event time when it wakes up. It then reads the last ADC reading for each input, not the reading that triggered the interrupt.

9.3.6 VM

Figure 9.1 shows the VM block for the capacitive touch sensor interface:

- Configures the hardware and gets an interrupt when a programmable threshold is crossed
- Selects the range capacitance
- Decides whether an event is a valid touch

9.4 LED Drivers

CSR8675 BGA includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

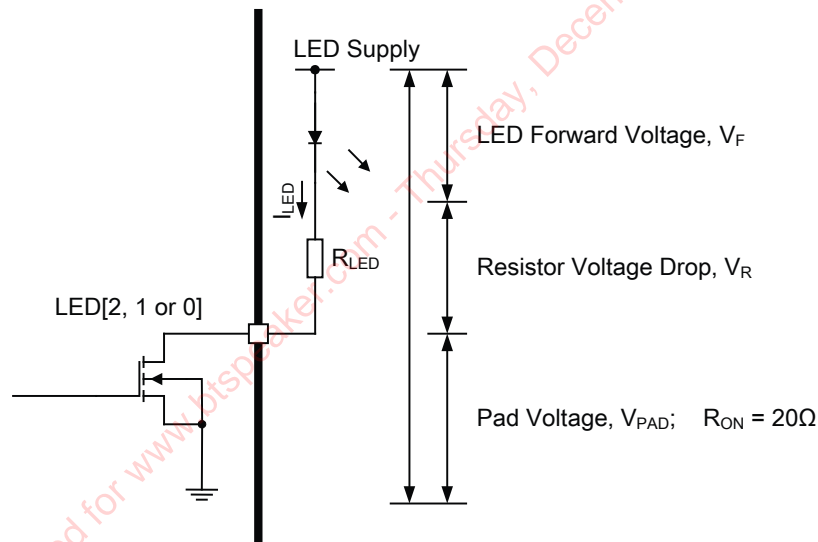


Figure 9.2: LED Equivalent Circuit

From Figure 9.2 it is possible to derive Equation 9.1 to calculate I_{LED} . If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{V_{DD} - V_F}{R_{LED} + R_{ON}}$$

Equation 9.1: LED Current

For the LED pads to act as resistance, the external series resistor, R_{LED} , needs to be such that the voltage drop across it, V_R , keeps V_{PAD} below 0.5V. Equation 9.2 also applies.

$$V_{DD} = V_F + V_R + V_{PAD}$$

Equation 9.2: LED PAD Voltage

Note:

The supply for domain in Section 1.2 for LED[2:0] must remain powered for LED functions to operate.

The LED current adds to the overall current. Conservative LED selection extends battery life.

Prepared for www.btspeaker.com - Thursday, December 04, 2014

10 Audio Interface

The audio interface circuit consists of:

- Stereo/dual-mono audio codec
- Dual analogue audio inputs
- Dual analogue audio outputs
- 6 digital MEMS microphone inputs
- 2 configurable PCM/I²S interfaces
- SPDIF interface

For more information on CSR8675 BGA audio path configuration see the CSR8675 Audio Development Kit (DK-CSR8675-10197-1A).

Figure 10.1 shows the functional blocks of the interface. The codec supports stereo/dual-mono playback and recording of audio signals at multiple sample rates with a 24-bit resolution. The ADC and the DAC of the codec each contain 2 independent high-quality channels. Any ADC or DAC channel runs at its own independent sample rate.

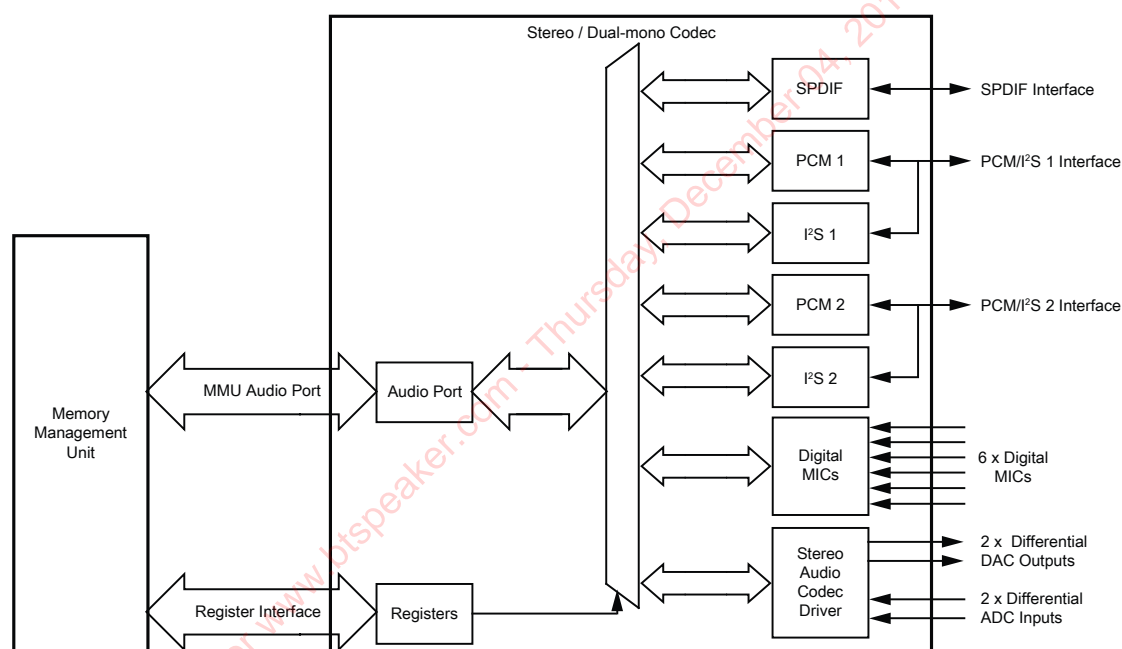


Figure 10.1: Audio Interface

CSR8675 BGA supports various digital audio bus interfaces:

- 2 configurable PCM/I²S interfaces:
 - PCM1 interface shares the same pins as I²S1 interface but the audio buses are mutually exclusive in their usage. Table 10.1 shows shared pins for the PCM/I²S 1 interface.
 - PCM2 interface shares the same pins as I²S2 interface but the audio buses are mutually exclusive in their usage. Table 10.1 shows shared pins for the PCM/I²S 2 interface.
- SPDIF interface which is available on any unused PIO. The data output (SPDIF_OUT) is restricted to even numbered PIO, and the data input (SPDIF_IN) is restricted to odd numbered PIO, see the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

| PIO | PCM Interface | I ² S Interface |
|---------|---------------|----------------------------|
| PIO[20] | PCM1_CLK | SCK1 |
| PIO[19] | PCM1_SYNC | WS1 |
| PIO[18] | PCM1_OUT | SD1_OUT |
| PIO[17] | PCM1_IN | SD1_IN |
| PIO[7] | PCM2_CLK | SCK2 |
| PIO[6] | PCM2_SYNC | WS2 |
| PIO[5] | PCM2_OUT | SD2_OUT |
| PIO[4] | PCM2_IN | SD2_IN |

Table 10.1: Shared Pins on PCM/I²S Interfaces

10.1 Audio Input and Output

The audio input circuitry consists of:

- 2 independent 24-bit high-quality ADC channels:
 - Programmable as either microphone or line input
 - Programmable as either stereo or dual-mono inputs
 - Multiplexed with 2 of the digital microphone inputs, see Section 10.2.16
 - Each channel is independently configurable to be either single-ended or fully differential
 - Each channel has an analogue and digital programmable gain stage for optimisation of different microphones
- 6 digital MEMS microphone channels, of which 4 have independent codec channels and 2 share their codecs with the 2 high-quality audio inputs

The audio output circuitry consists of a dual differential class A-B output stage.

Note:

CSR8675 BGA is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

10.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for up to 2 PCM interfaces including PCM master codecs that require an external system clock
- Support for up to 2 stereo I²S digital audio bus standard
- Support for IEC-60958 standard stereo digital audio bus standards, e.g. SPDIF and AES3 (also known as AES/EBU)

Important Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio output. With respect to audio input, software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel.

10.2.1 Audio Codec Block Diagram

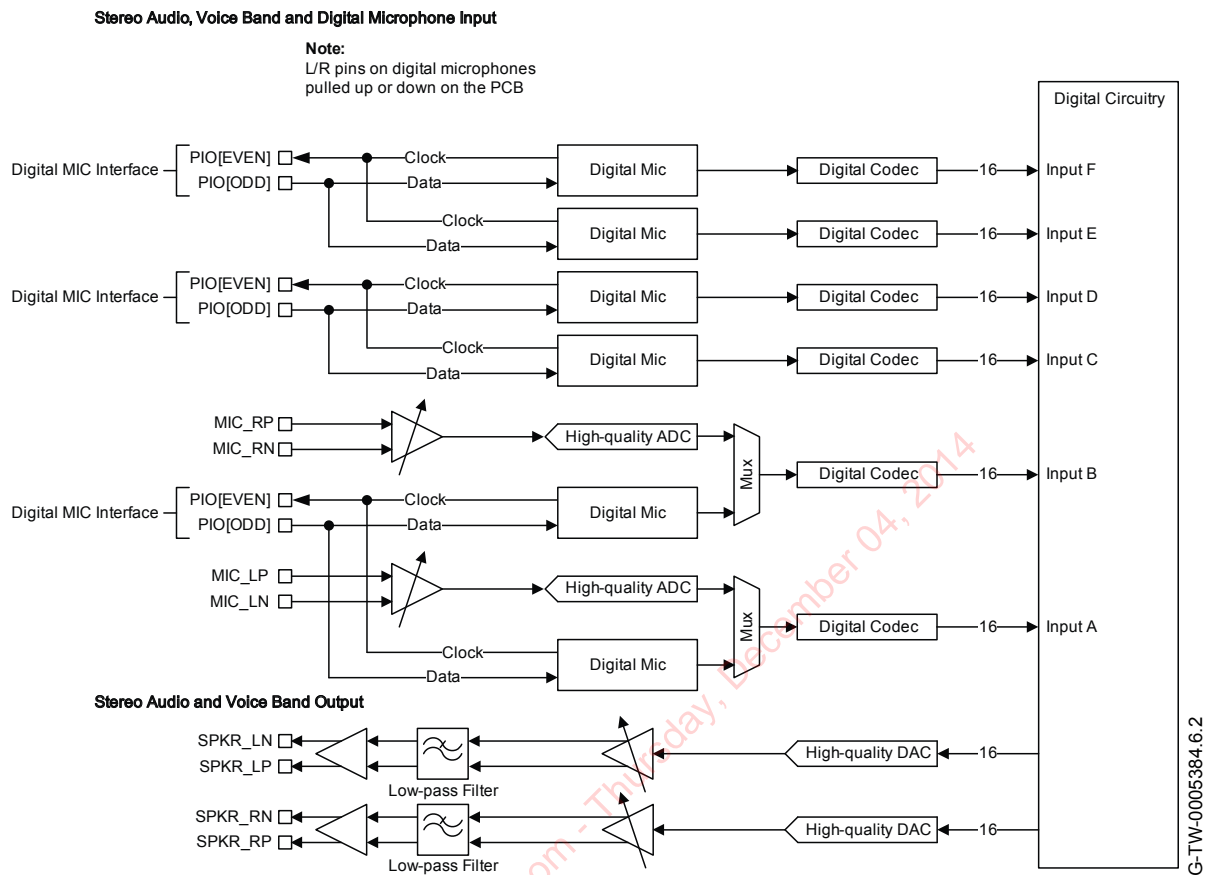


Figure 10.2: Audio Codec Input and Output Stages

The CSR8675 BGA audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO for the audio circuits and VDD_AUDIO_DRV for the audio driver circuits.

10.2.2 Codec Set-up

The configuration and control of the ADC is through software functions described in appropriate development kit documentation. This section is an overview of the parameters set up using the software functions.

The Kalimba DSP communicates its codec requirements to the MCU, and therefore also to the VM, by exchanging messages. Messages between the Kalimba DSP and the embedded MCU are based on interrupts:

- 1 interrupt between the MCU and Kalimba DSP
- 1 interrupt between the Kalimba DSP and the MCU

Message content is transmitted using shared memory. There are VM and DSP library functions to send and receive messages; see appropriate development kit documentation for further details.

10.2.3 ADC

Figure 10.2 shows the CSR8675 BGA consists of 2 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is a separate channel with identical functionality.
- There are 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage, see Section 10.2.5.

10.2.4 ADC Sample Rate Selection

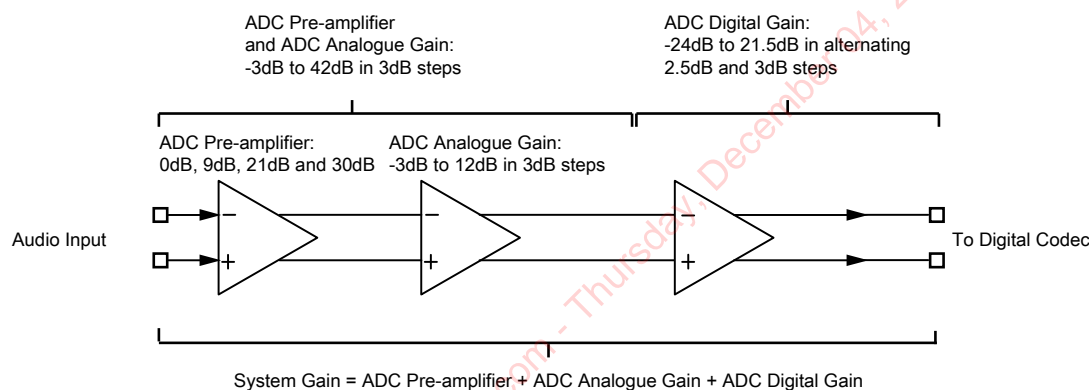
Each ADC supports the following pre-defined sample rates, although other rates are programmable, e.g. 40 kHz:

- 8 kHz
- 11.025 kHz
- 16 kHz
- 22.050 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz
- 96 kHz

10.2.5 ADC Audio Input Gain

Figure 10.3 shows that the CSR8675 BGA audio input gain consists of:

- An analogue gain stage based on a pre-amplifier and an analogue gain amplifier, see Section 10.2.6
- A digital gain stage, see Section 10.2.7



G-TW-0005535.4.3

Figure 10.3: Audio Input Gain

10.2.6 ADC Pre-amplifier and ADC Analogue Gain

CSR8675 BGA has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

- The ADC pre-amplifier has 4 gain settings: 0dB, 9dB, 21dB and 30dB
- The ADC analogue amplifier gain is -3dB to 12dB in 3dB steps
- The overall analogue gain for the pre-amplifier and analogue amplifier is -3dB to 42dB in 3dB steps, see Figure 10.3
- At mid to high gain levels it acts as a microphone pre-amplifier, see Section 10.2.15
- At low gain levels it acts as an audio line level amplifier

10.2.7 ADC Digital Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB, see Table 10.2. There is also a *fine gain interface* with a 9-bit gain setting allowing gain changes in 1/32 steps, for more information contact CSR.

The firmware controls the audio input gain.

| Digital Gain Selection Value | ADC Digital Gain Setting (dB) | Digital Gain Selection Value | ADC Digital Gain Setting (dB) |
|------------------------------|-------------------------------|------------------------------|-------------------------------|
| 0 | 0 | 8 | -24 |
| 1 | 3.5 | 9 | -20.5 |
| 2 | 6 | 10 | -18 |
| 3 | 9.5 | 11 | -14.5 |
| 4 | 12 | 12 | -12 |
| 5 | 15.5 | 13 | -8.5 |
| 6 | 18 | 14 | -6 |
| 7 | 21.5 | 15 | -2.5 |

Table 10.2: ADC Audio Input Gain Rate

10.2.8 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

- A *default* IIR filter suitable for music (>44.1kHz)
- G.722 filter is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance (which is the best selection for 8kHz / 16kHz / voice)

For more information contact CSR.

10.2.9 DAC

The DAC consists of:

- 2 fourth-order Sigma-Delta converters enabling 2 separate channels that are identical in functionality, as Figure 10.2 shows.
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage.

10.2.10 DAC Sample Rate Selection

Each DAC supports the following sample rates:

- 8 kHz
- 11.025 kHz
- 16 kHz
- 22.050 kHz
- 32 kHz
- 40 kHz
- 44.1 kHz
- 48 kHz
- 96 kHz
- 192 kHz

10.2.11 DAC Digital Gain

A digital gain stage inside the DAC varies from -24dB to 21.5dB, see Table 10.3. There is also a *fine gain interface* with a 9-bit gain setting enabling gain changes in 1/32 steps, for more information contact CSR.

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

| Digital Gain Selection Value | DAC Digital Gain Setting (dB) | Digital Gain Selection Value | DAC Digital Gain Setting (dB) |
|------------------------------|-------------------------------|------------------------------|-------------------------------|
| 0 | 0 | 8 | -24 |
| 1 | 3.5 | 9 | -20.5 |
| 2 | 6 | 10 | -18 |
| 3 | 9.5 | 11 | -14.5 |
| 4 | 12 | 12 | -12 |
| 5 | 15.5 | 13 | -8.5 |
| 6 | 18 | 14 | -6 |
| 7 | 21.5 | 15 | -2.5 |

Table 10.3: DAC Digital Gain Rate Selection

10.2.12 DAC Analogue Gain

Table 10.4 shows that the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps.

The firmware controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

| Analogue Gain Selection Value | DAC Analogue Gain Setting (dB) | Analogue Gain Selection Value | DAC Analogue Gain Setting (dB) |
|-------------------------------|--------------------------------|-------------------------------|--------------------------------|
| 7 | 0 | 3 | -12 |
| 6 | -3 | 2 | -15 |
| 5 | -6 | 1 | -18 |
| 4 | -9 | 0 | -21 |

Table 10.4: DAC Analogue Gain Rate Selection

10.2.13 DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default *long* FIR filter for best performance at ≥ 44.1 kHz.
- A *short* FIR to reduce latency.
- A *narrow* FIR (a very sharp roll-off at Nyquist) for G.722 compliance. Best for 8 kHz / 16 kHz.

10.2.14 IEC 60958 Interface

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and enables the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the 2 industry standards:

- AES3 (also known as AES/EBU)
- Sony and Philips interface specification SPDIF

The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4.

The SPDIF interface signals, SPDIF_IN and SPDIF_OUT, interface to:

- A 75Ω coaxial cable with an RCA connector, see Figure 10.4
- An optical link that uses Toslink optical components, see Figure 10.5.

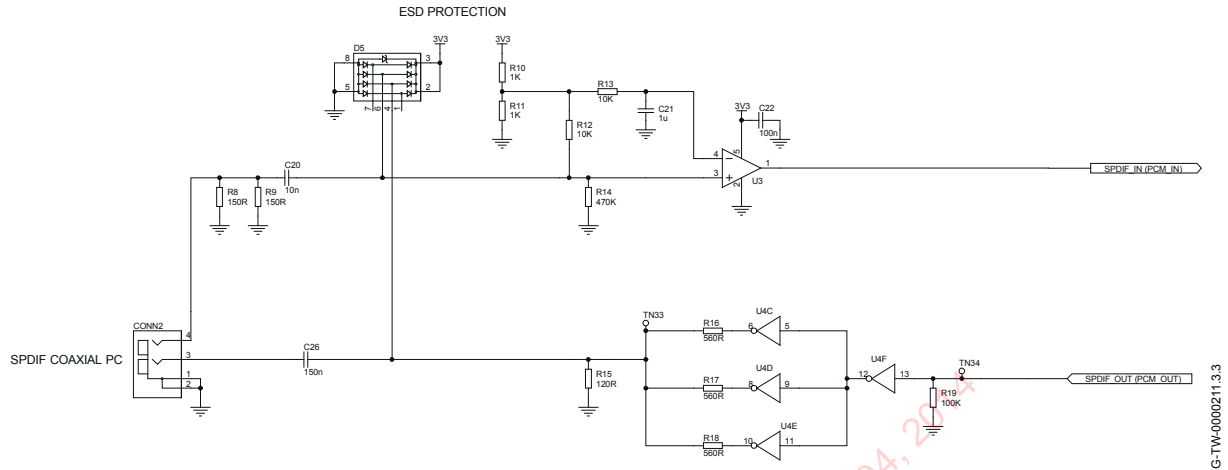


Figure 10.4: Example Circuit for SPDIF Interface (Co-axial)



Figure 10.5: Example Circuit for SPDIF Interface (Optical)

10.2.15 Microphone Input

CSR8675 BGA contains 2 independent low-noise microphone bias generators. The microphone bias generators are recommended for biasing electret condenser microphones. Figure 10.6 shows a biasing circuit for microphones with a sensitivity between about -40 to -60dB (0dB = 1V/Pa).

Where:

- The microphone bias generators derive their power from VBAT (via SMP_VBAT) or VOUT_3V3 (via SMPS_3V3) and require no capacitor on their output.
- The microphone bias generators maintain regulation within the limits 70μA to 2.8mA, supporting a 2mA source typically required by 2 electret condenser microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.
- Biasing resistors R1 and R2 equal 2.2kΩ.
- When the input pre-amplifier is enabled, the input impedance at MIC_LN, MIC_LP, MIC_RN and MIC_RP varies between 6kΩ (pre-amplifier gain >0dB) and 12kΩ (pre-amplifier gain = 0dB).
- C1, C2, C3 and C4 are 100/150nF if bass roll-off is required to limit wind noise on the microphone.
- R1 and R2 set the microphone load impedance and are normally around 2.2kΩ.

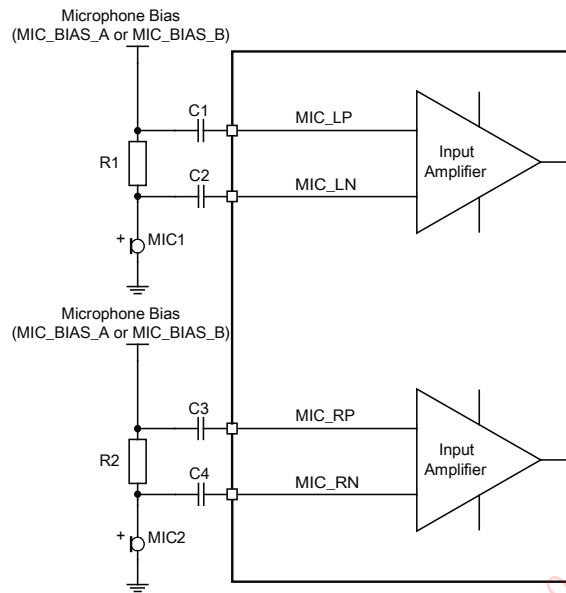


Figure 10.6: Microphone Biasing

The microphone bias characteristics include:

- Power supply:
 - CSR8675 BGA microphone supply is VBAT (via SMP_VBAT) or VOUT_3V3 (via SMPS_3V3)
 - Minimum input voltage = Output voltage + drop-out voltage
 - Maximum input voltage is 4.3V
- Drop-out voltage:
 - 300mV maximum
- Output voltage:
 - 1.8V or 2.6V
 - Tolerance 90% to 110%
- Output current:
 - 70μA to 2.8mA
- No load capacitor required

10.2.16 Digital Microphone Inputs

The CSR8675 BGA interfaces to 6 digital MEMS microphones. Figure 10.2 shows that 4 of the inputs have dedicated codec channels and 2 are multiplexed with the high-quality ADC channels.

Figure 10.2 shows that the digital microphone interface on the CSR8675 BGA has:

- Clock lines shared between 2 microphone outputs, linked to any even-numbered PIO pin as determined by the firmware.

Note:

Multiple digital microphones can share the same clock if they are configured for the same frequency, e.g. 1 clock for 6 digital microphones.

- Data lines shared between 2 microphone inputs, linked to any odd-numbered PIO as determined by the firmware.

Note:

For the digital microphone interface to work in this configuration ensure the microphone uses a tristate between edges.

- The left and right selection for the digital microphones are appropriately pulled up or down for selection on the PCB.

G-TW-0005536.3.2

10.2.17 Line Input

Figure 10.7 and Figure 10.8 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

In line input mode, the input impedance of the pins to ground varies from 6k Ω to 34k Ω depending on input gain setting.

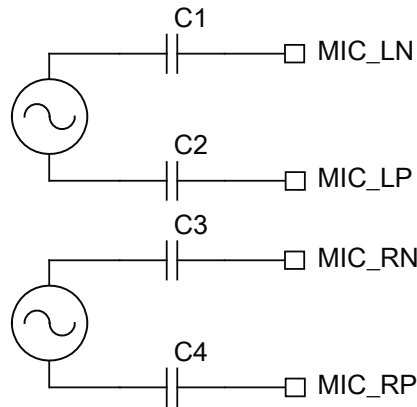


Figure 10.7: Differential Input

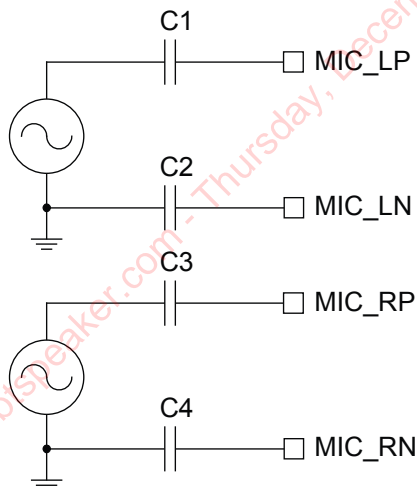


Figure 10.8: Single-ended Input

10.2.18 Output Stage

The output stage digital circuitry converts the signal from linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. Figure 10.9 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

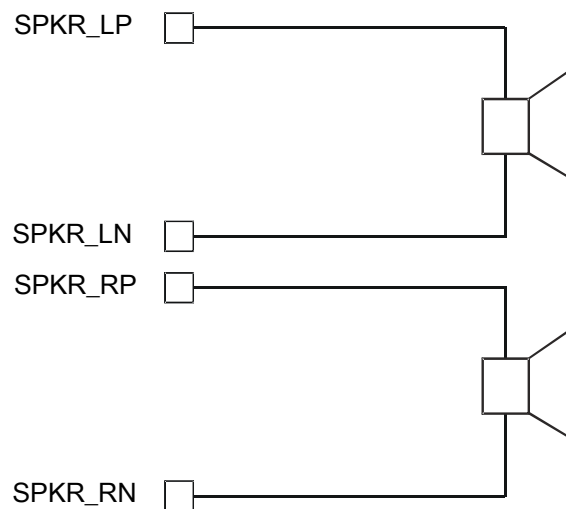


Figure 10.9: Speaker Output

10.2.19 Mono Operation

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

G-TW-0005537.1.1

10.2.20 Side Tone

In some applications it is necessary to implement side tone. This side tone function involves feeding a properly gained microphone signal in to the DAC stream, e.g. earpiece. The side tone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface, see Figure 10.10.

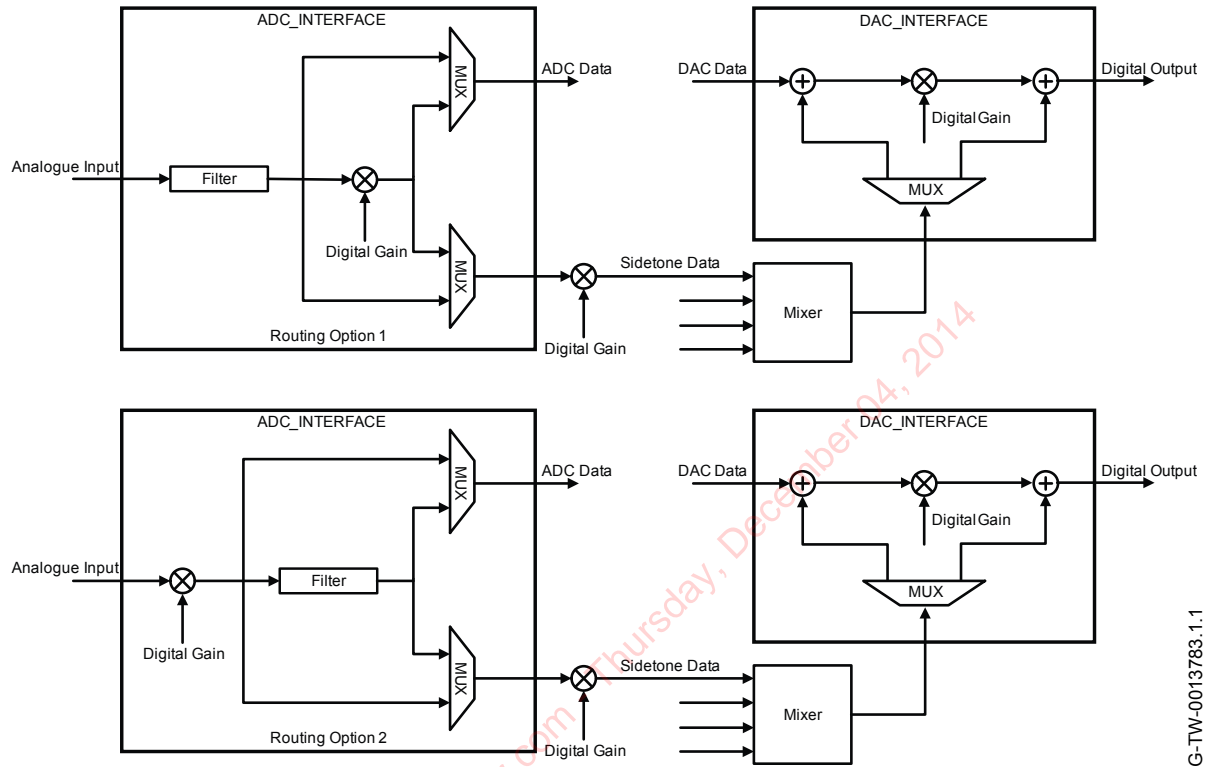


Figure 10.10: Side Tone

The ADC provides simple gain to the side tone data. The gain values range from -32.6dB to 12.0dB in alternating steps of 2.5dB and 3.5dB, see Table 10.5.

| Value | Side Tone Gain | Value | Side Tone Gain |
|-------|----------------|-------|----------------|
| 0 | -32.6dB | 8 | -8.5dB |
| 1 | -30.1dB | 9 | -6.0dB |
| 2 | -26.6dB | 10 | -2.5dB |
| 3 | -24.1dB | 11 | 0dB |
| 4 | -20.6dB | 12 | 3.5dB |
| 5 | -18.1dB | 13 | 6.0dB |
| 6 | -14.5dB | 14 | 9.5dB |
| 7 | -12.0dB | 15 | 12.0dB |

Table 10.5: Side Tone Gain

Note:

The values of side tone are shown for information only. During standard operation, the application software controls the side tone gain.

The following PS Keys configure the side tone hardware:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

10.2.21 Integrated Digital IIR Filter

CSR8675 BGA has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2-stage, second order IIR and is for functions such as custom wind noise reduction. The filter also has optional DC blocking.

The filter has 11 configuration words:

- 2 for gain values
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format NN.NNNNNNNNNN.

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

```
01.1111111111 = most positive number, close to 2
01.0000000000 = 1
00.0000000000 = 0
11.0000000000 = -1
10.0000000000 = -2, most negative number
```

Equation 10.1 shows the equation for the IIR filter. Equation 10.2 shows the equation for when the DC blocking is enabled.

The filter is configured, enabled and disabled from the VM via the `CodecSetIIRFilter` trap. This requires firmware support. The configuration function takes 11 variables in the following order:

- 0 : Gain₀ and Exp₀
- 1 : b₀₁
- 2 : b₀₂
- 3 : a₀₁
- 4 : a₀₂

- 5 : Gain₁
- 6 : b₁₁
- 7 : b₁₂
- 8 : a₁₁
- 9 : a₁₂
- a : DC Block (1 = enable, 0 = disable)

$$\text{Filter, } H(z) = (1 - z^{-1}) \times 2^{\text{Exp}_0} \times \text{Gain}_0 \times \left(\frac{1 + b_{01} z^{-1} + b_{02} z^{-2}}{1 + a_{01} z^{-1} + a_{02} z^{-2}} \right) \times \text{Gain}_1 \times \left(\frac{1 + b_{11} z^{-1} + b_{12} z^{-2}}{1 + a_{11} z^{-1} + a_{12} z^{-2}} \right)^{1/2} \times 2^{\text{Exp}_0}$$

Equation 10.1: IIR Filter Transfer Function, H(z)

$$\text{Filter with DC Blocking, } H_{\text{DC}}(z) = H(z) \times (1 - z^{-1})$$

Equation 10.2: IIR Filter Plus DC Blocking Transfer Function, H_{DC}(z)

10.3 PCM1 and PCM2 Interface

Important Note:

The term *PCM* in Section 10.3 and its subsections, Section 10.3.1 to Section 10.3.10, refers to PCM1 and PCM2 interfaces.

The PCM interface shares the same pins as I²S interface but the audio buses are mutually exclusive in their usage. Section 10.3 shows shared pins for the PCM/I²S interface.

The audio PCM interface on the CSR8675 BGA supports:

- On-chip routing to Kalimba DSP
- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on the CSR8675 BGA for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
 - Long Frame Sync
 - Short Frame Sync
 - GCI timing environments
- 24-bit / 16-bit / 13-bit linear, 8-bit μ-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

10.3.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, CSR8675 BGA generates PCM_CLK and PCM_SYNC.

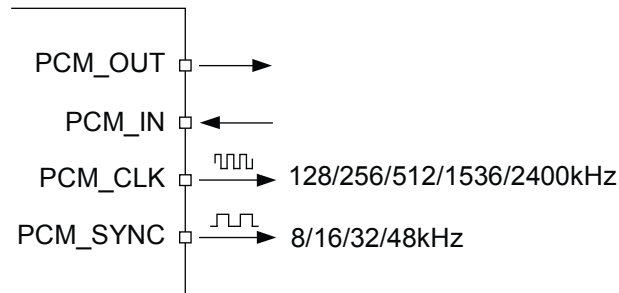


Figure 10.11: PCM Interface Master

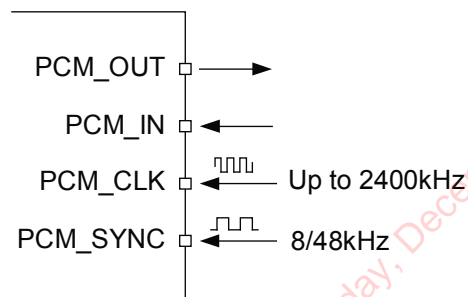


Figure 10.12: PCM Interface Slave

10.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When CSR8675 BGA is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When CSR8675 BGA is configured as PCM Slave, PCM_SYNC is from 1 cycle PCM_CLK to half the PCM_SYNC rate.

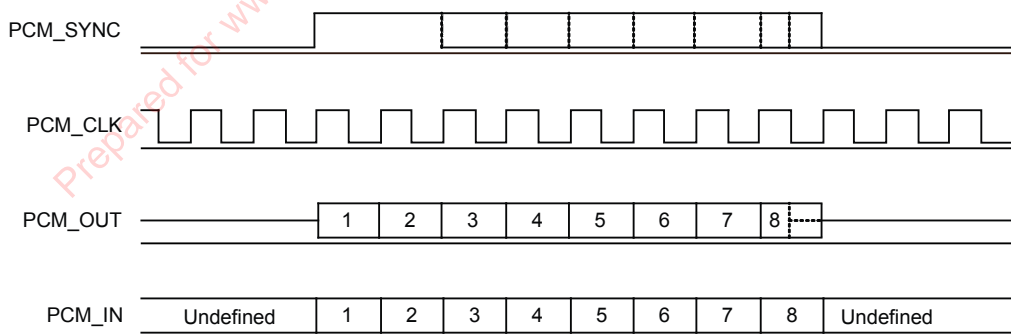
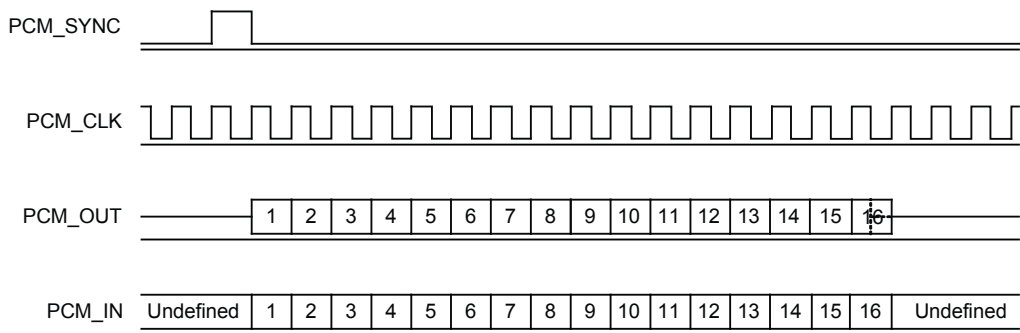


Figure 10.13: Long Frame Sync (Shown with 8-bit Companded Sample)

CSR8675 BGA samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always 1 clock cycle long.



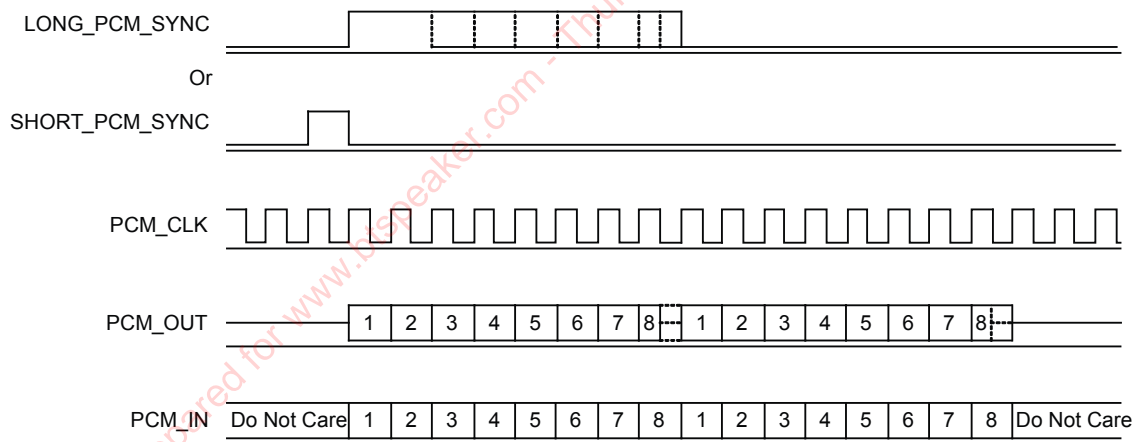
G-TW-0000220.2.3

Figure 10.14: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, CSR8675 BGA samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.3.4 Multi-slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections are carried over any of the first 4 slots.

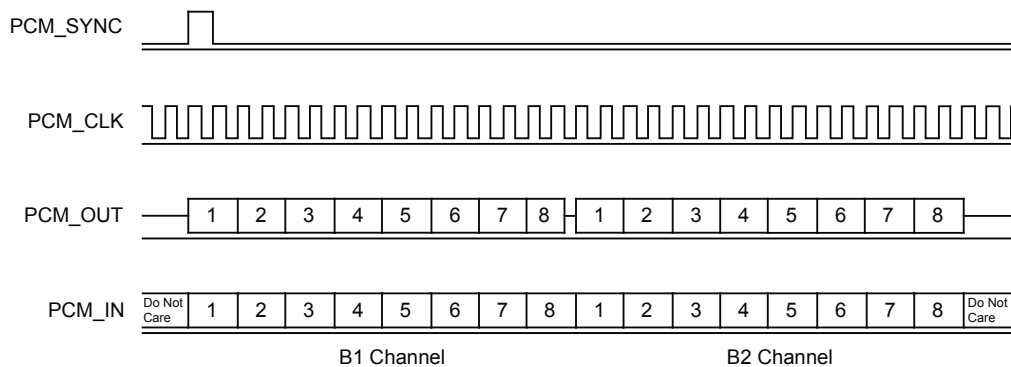


G-TW-0000221.3.2

Figure 10.15: Multi-slot Operation with 2 Slots and 8-bit Companded Samples

10.3.5 GCI Interface

CSR8675 BGA is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The 2 64kbps B channels are accessed when this mode is configured.



G-TW-0000222.2.3

Figure 10.16: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and typically runs at 8kHz/16kHz.

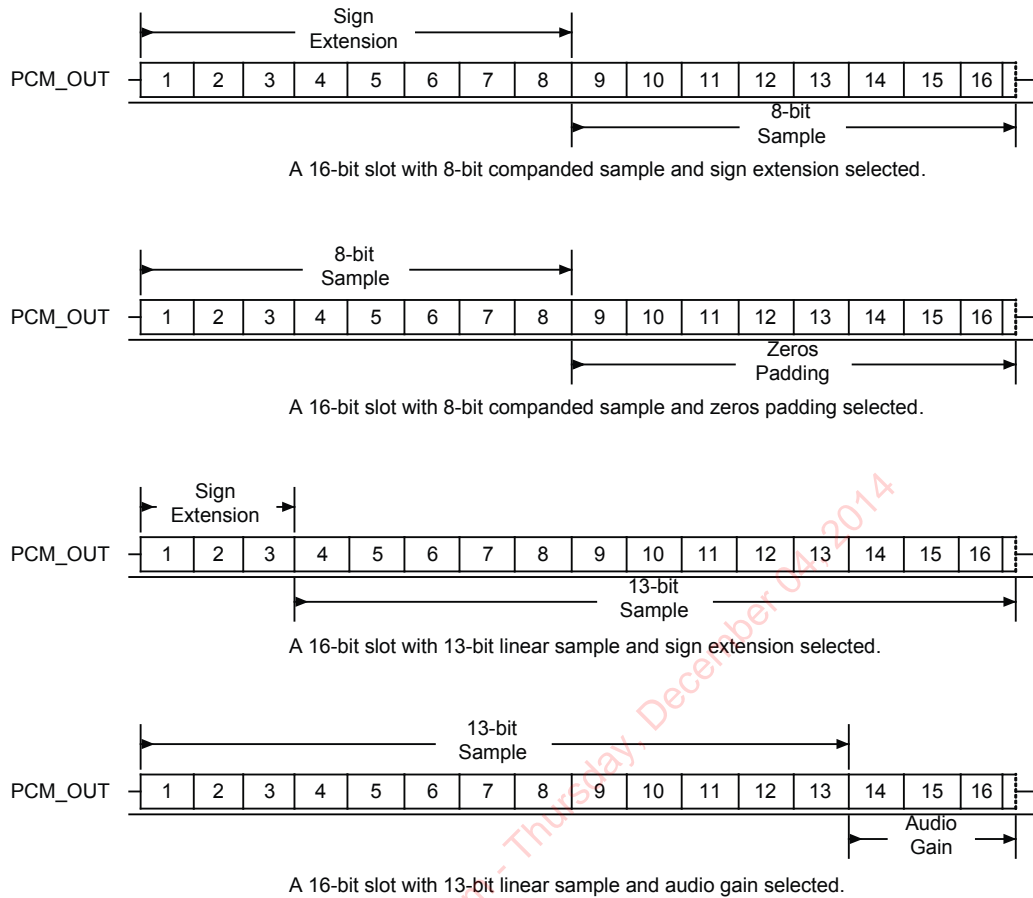
10.3.6 Slots and Sample Formats

CSR8675 BGA receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit or 16-bit sample formats.

CSR8675 BGA supports:

- 13-bit linear, 16-bit linear and 8-bit μ -law or A-law sample formats.
- A sample rate of 8ksamples/s, 16ksamples/s or 32ksamples/s.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.



G-TW-0000223.2.3

Figure 10.17: 16-bit Slot Length and Sample Formats

10.3.7 Additional Features

CSR8675 BGA has a mute facility that forces PCM_OUT to be 0. In master mode, CSR8675 BGA is compatible with some codecs which control power down by forcing PCM_SYNC to 0 while keeping PCM_CLK running.

10.3.8 PCM Timing Information

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-------------------|---------------------------------------|--|-----|-----|-----|------|
| f_{mclk} | PCM_CLK frequency | 4MHz DDS generation. Selection of frequency is programmable. See Section 10.3.10. | - | 128 | - | kHz |
| | | | | 256 | | |
| | | | | 512 | | |
| | | 48MHz DDS generation. Selection of frequency is programmable. See Section 10.3.10. | 2.9 | - | - | kHz |
| - | PCM_SYNC frequency for SCO connection | | - | 8 | - | kHz |
| $t_{mclkh}^{(a)}$ | PCM_CLK high | 4MHz DDS generation | 980 | - | - | ns |

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-------------------|--|----------------------|-----|-----|-----|----------|
| $t_{mclk}^{(a)}$ | PCM_CLK low | 4MHz DDS generation | 730 | - | - | ns |
| - | PCM_CLK jitter | 48MHz DDS generation | - | - | 21 | ns pk-pk |
| $t_{dmclkssyncl}$ | Delay time from PCM_CLK high to PCM_SYNC high | | - | - | 20 | ns |
| $t_{dmclkpout}$ | Delay time from PCM_CLK high to valid PCM_OUT | | - | - | 20 | ns |
| $t_{dmclkssyncl}$ | Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only) | | - | - | 20 | ns |
| $t_{dmclkssyncl}$ | Delay time from PCM_CLK high to PCM_SYNC low | | - | - | 20 | ns |
| $t_{dmclkpoutz}$ | Delay time from PCM_CLK low to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{dmclkhpoutz}$ | Delay time from PCM_CLK high to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{supinclk}$ | Set-up time for PCM_IN valid to PCM_CLK low | | 20 | - | - | ns |
| $t_{hpinclk}$ | Hold time for PCM_CLK low to PCM_IN invalid | | 0 | - | - | ns |

Table 10.6: PCM Master Timing

(a) Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

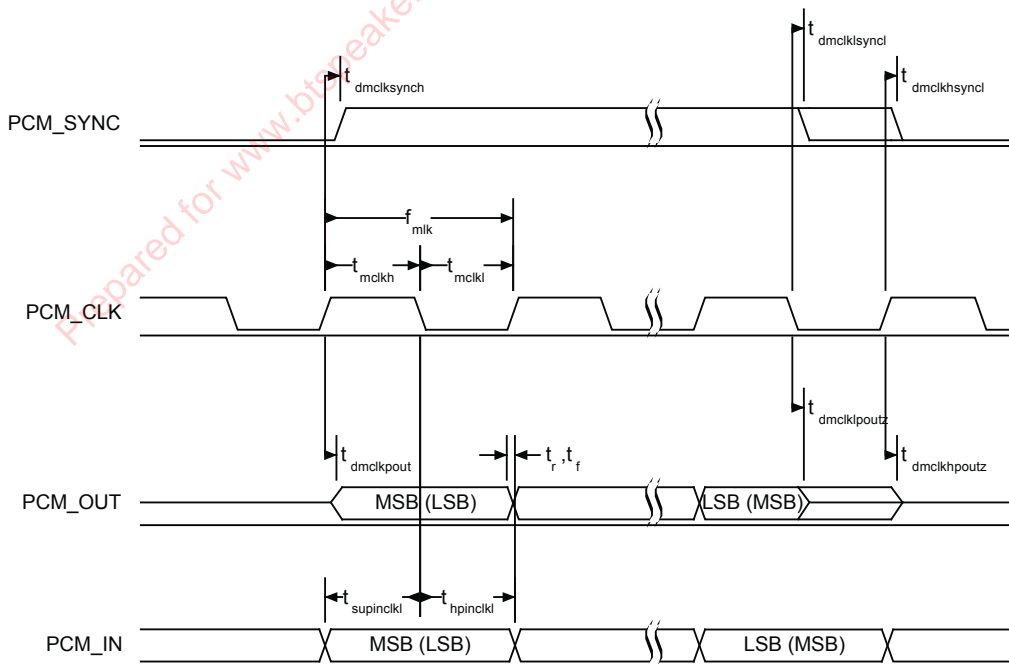


Figure 10.18: PCM Master Timing Long Frame Sync

G-TW-0000224.2.3

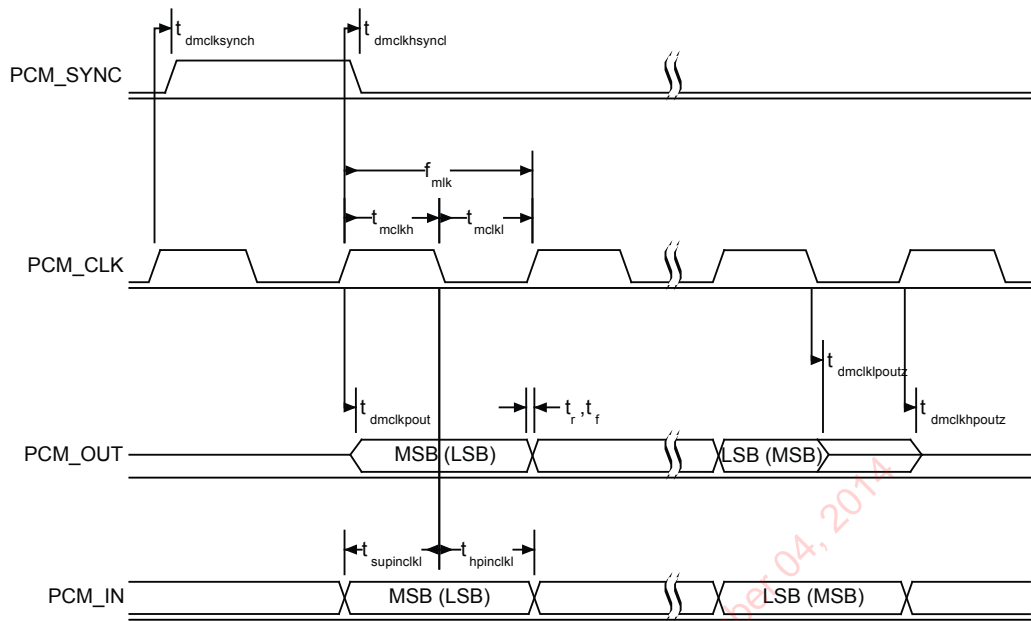


Figure 10.19: PCM Master Timing Short Frame Sync

G-TW-0000225 3.3

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|---|-----|-----|-----|------|
| f_{sclk} | PCM clock frequency (Slave mode: input) | 64 | - | (a) | kHz |
| f_{sclk} | PCM clock frequency (GCI mode) | 128 | - | (b) | kHz |
| t_{sclkl} | PCM_CLK low time | 200 | - | - | ns |
| t_{sclkh} | PCM_CLK high time | 200 | - | - | ns |
| $t_{\text{hscclksynch}}$ | Hold time from PCM_CLK low to PCM_SYNC high | 2 | - | - | ns |
| $t_{\text{susclksynch}}$ | Set-up time for PCM_SYNC high to PCM_CLK low | 20 | - | - | ns |
| t_{dpout} | Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (Long Frame Sync only) | - | - | 20 | ns |
| t_{dclkhout} | Delay time from CLK high to PCM_OUT valid data | - | - | 15 | ns |
| t_{dpoutz} | Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance | - | - | 15 | ns |
| $t_{\text{supinsclkl}}$ | Set-up time for PCM_IN valid to CLK low | 20 | - | - | ns |
| $t_{\text{hpinsclkl}}$ | Hold time for PCM_CLK low to PCM_IN invalid | 2 | - | - | ns |

Table 10.7: PCM Slave Timing

(a) Max frequency is the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

(b) Max frequency is twice the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

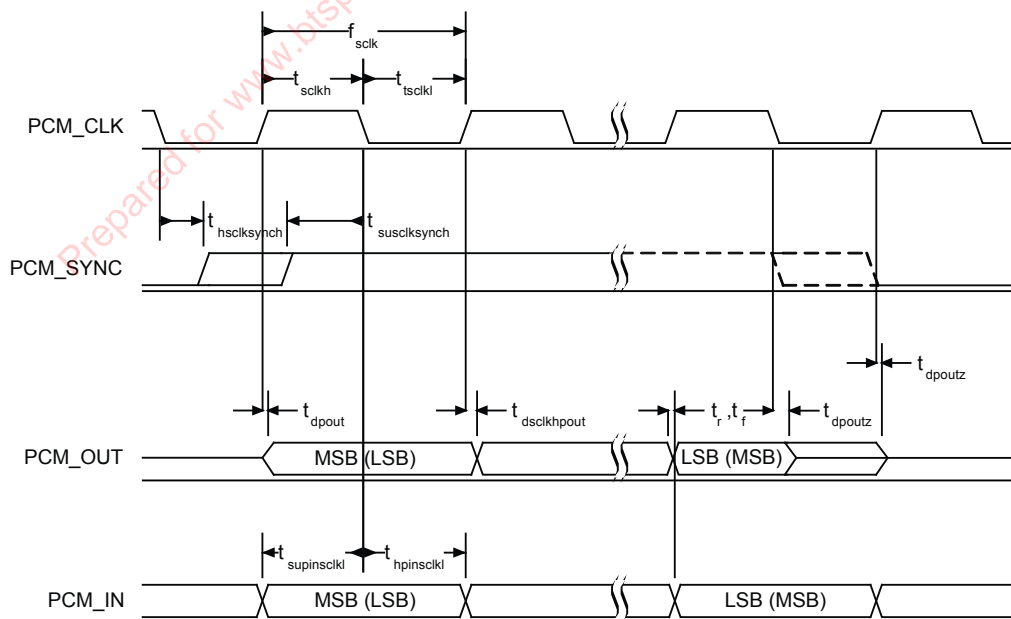


Figure 10.20: PCM Slave Timing Long Frame Sync

G-TW-0000226.3.2

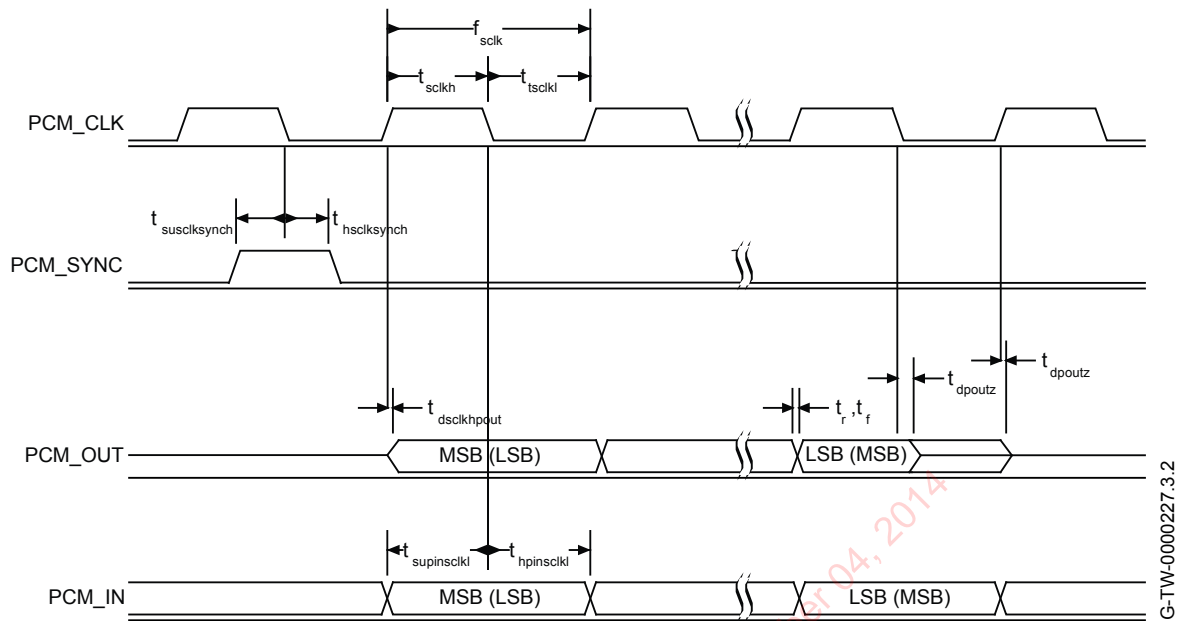


Figure 10.21: PCM Slave Timing Short Frame Sync

10.3.9 PCM_CLK and PCM_SYNC Generation

CSR8675 BGA has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from CSR8675 BGA internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock, which enables a greater range of frequencies to be generated with low jitter but consumes more power. To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 10.3 describes PCM_CLK frequency when generated from the internal 48MHz clock:

$$f = \frac{\text{CNT_RATE}}{\text{CNT_LIMIT}} \times 24\text{MHz}$$

Equation 10.3: PCM_CLK Frequency Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 10.4:

$$f = \frac{\text{PCM_CLK}}{\text{SYNC_LIMIT} \times 8}$$

Equation 10.4: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

10.3.10 PCM Configuration

Configure the PCM by using PSKEY_PCM_CONFIG32 and PSKEY_PCM_USE_LOW_JITTER_MODE, see *BlueCore Audio API Specification* and the PS Key file. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

10.4 I²S1 and I²S2 Interface

Important Note:

The term I²S refers to I²S1 and I²S2 interfaces.

The I²S interface shares the same pins as PCM interface but the audio buses are mutually exclusive in their usage. Section 10.3 shows shared pins for the PCM/I²S interface.

The I²S interface supports left-justified or right-justified.

Figure 10.22 shows the timing diagram.

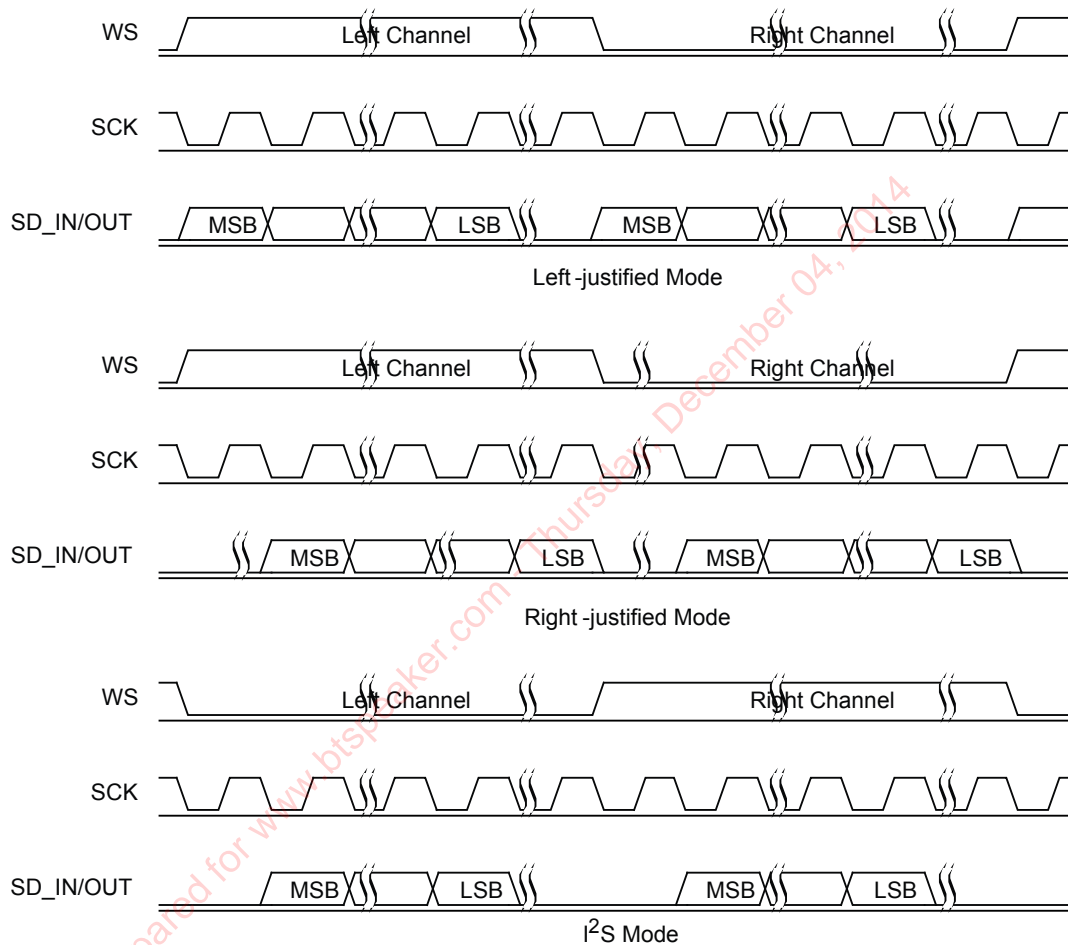


Figure 10.22: I²S Digital Audio Interface Modes

Configure the digital audio interface using PSKEY_DIGITAL_AUDIO_CONFIG, see *Firmware Configuration Keys for CSR8675* and the PS Key file.

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------|---------------|-----|-----|-----|------|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |
| t_{ch} | SCK high time | 80 | - | - | ns |
| t_{cl} | SCK low time | 80 | - | - | ns |

Table 10.8: Digital Audio Interface Slave Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|-------------------------------------|-----|-----|-----|------|
| t_{ssu} | WS valid to SCK high set-up time | 20 | - | - | ns |
| t_{sh} | SCK high to WS invalid hold time | 2.5 | - | - | ns |
| t_{opd} | SCK low to SD_OUT valid delay time | - | - | 20 | ns |
| t_{isu} | SD_IN valid to SCK high set-up time | 20 | - | - | ns |
| t_{ih} | SCK high to SD_IN invalid hold time | 2.5 | - | - | ns |

Table 10.9: I²S Slave Mode Timing

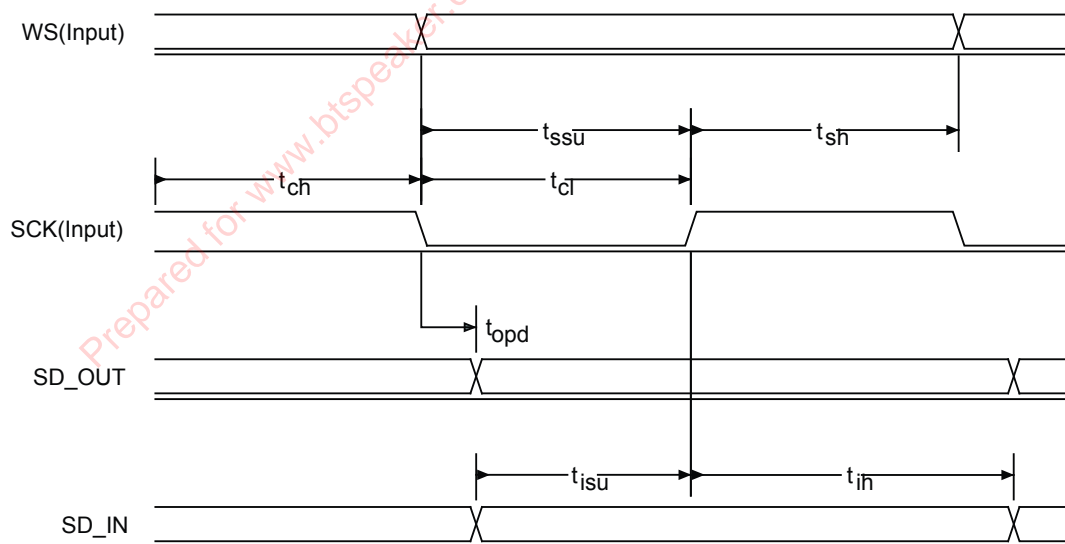


Figure 10.23: Digital Audio Interface Slave Timing

G-TW-0000231.2.2

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|---------------|-----|-----|-----|------|
| - | SCK Frequency | - | - | 6.2 | MHz |
| - | WS Frequency | - | - | 96 | kHz |

Table 10.10: Digital Audio Interface Master Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|-------------------------------------|-------|-----|-------|------|
| t_{spd} | SCK low to WS valid delay time | - | - | 39.27 | ns |
| t_{opd} | SCK low to SD_OUT valid delay time | - | - | 18.44 | ns |
| t_{isu} | SD_IN valid to SCK high set-up time | 18.44 | - | - | ns |
| t_{ih} | SCK high to SD_IN invalid hold time | 0 | - | - | ns |

Table 10.11: I²S Master Mode Timing Parameters, WS and SCK as Outputs

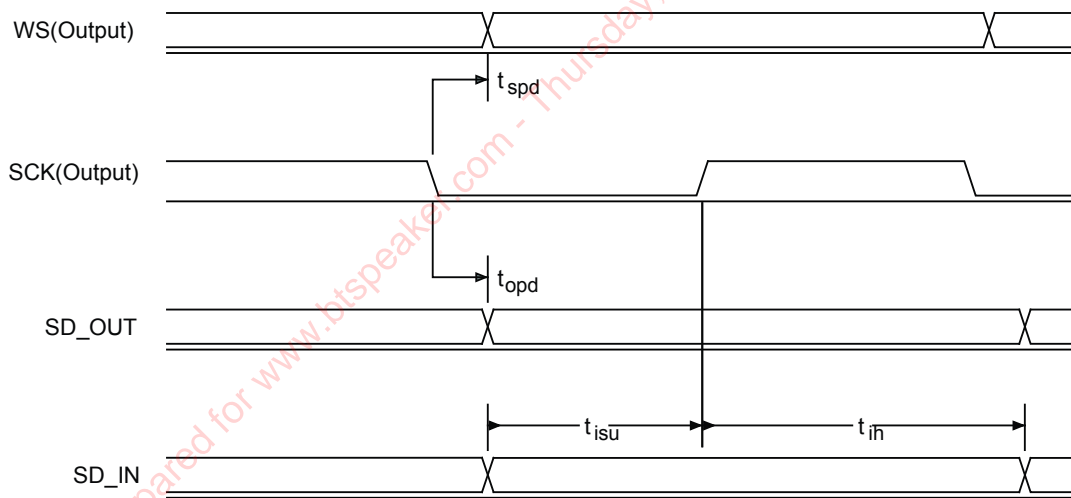


Figure 10.24: Digital Audio Interface Master Timing

11 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of WLAN coexistence schemes. There is support for:

- Channel skipping AFH
- Priority signalling
- Channel signalling
- Host passing of channel instructions

Planned support for WLAN coexistence schemes includes:

- Unity-3
- Unity-3e
- Unity+

For more information on WLAN coexistence schemes see *BlueCore Bluetooth/IEEE 802.11 Coexistence Application Note*.

For more information on WLAN coexistence schemes supported on CSR8675 BGA see software release note or contact CSR.

Prepared for www.btspeaker.com - Thursday, December 04, 2014

12 Power Control and Regulation

For greater power efficiency the CSR8675 BGA contains 2 switch-mode regulators:

- 1 generates a 1.80V supply rail with an output current of 185mA, see Section 12.1.
- 1 generates a 1.35V supply rail with an output current of 160mA, see Section 12.2.
- Combining the 2 switch-mode regulators in parallel generates a single 1.80V supply rail with an output current of 340mA, see Section 12.3.

CSR8675 BGA contains 4 LDO linear regulators:

- 3.30V bypass regulator, see Section 12.4.
- 0.85 V to 1.20 V VDD_DIG linear regulator, see Section 12.5.
- 1.35V VDD_AUX linear regulator, see Section 12.6.
- 1.35V VDD_ANA linear regulator, see Section 12.7.

The recommended configurations for power control and regulation on the CSR8675 BGA are:

- 3 switch-mode configurations:
 - A 1.80V and 1.35V dual-supply rail system using the 1.80V and 1.35V switch-mode regulators, see Figure 12.1. This is the default power control and regulation configuration for the CSR8675 BGA.
 - A 1.80V single-supply rail system using the 1.80V switch-mode regulator.
 - A 1.80V parallel-supply rail system for higher currents using the 1.80V and 1.35V switch-mode regulators with combined outputs, see Figure 12.2.
- A linear configuration using an external 1.8V rail omitting all regulators

Table 12.1 shows settings for the recommended configurations for power control and regulation on the CSR8675 BGA.

| Supply Configuration | Regulators | | | | Supply Rail | |
|-----------------------------|-------------|-------|--------------------------------|--------------------------------|-------------|-------|
| | Switch-mode | | VDD_AUX Linear Regulator | VDD_ANA Linear Regulator | | |
| | 1.8V | 1.35V | | | 1.8V | 1.35V |
| Dual-supply SMPS | ON | ON | OFF | OFF | SMPS | SMPS |
| Single-supply SMPS | ON | OFF | ON | ON | SMPS | LDO |
| Parallel-supply SMPS | ON | ON | ON | ON | SMPS | LDO |
| External 1.8V linear supply | OFF | OFF | ON | ON | External | LDO |

Table 12.1: Recommended Configurations for Power Control and Regulation

For more information on CSR8675 BGA power supply configuration see *Configuring the Power Supplies on CSR867x* application note.

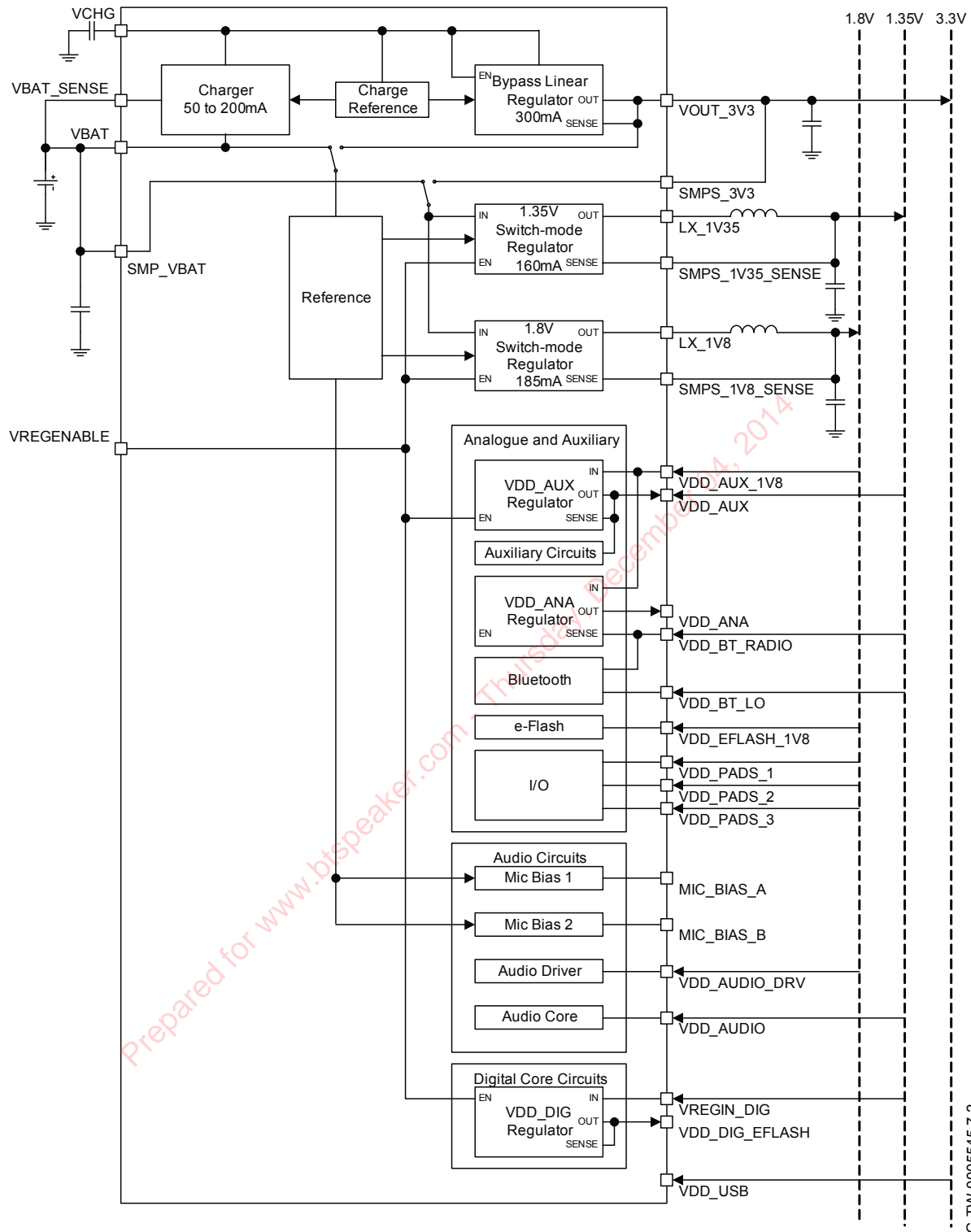


Figure 12.1: 1.80V and 1.35V Dual-supply Switch-mode System Configuration

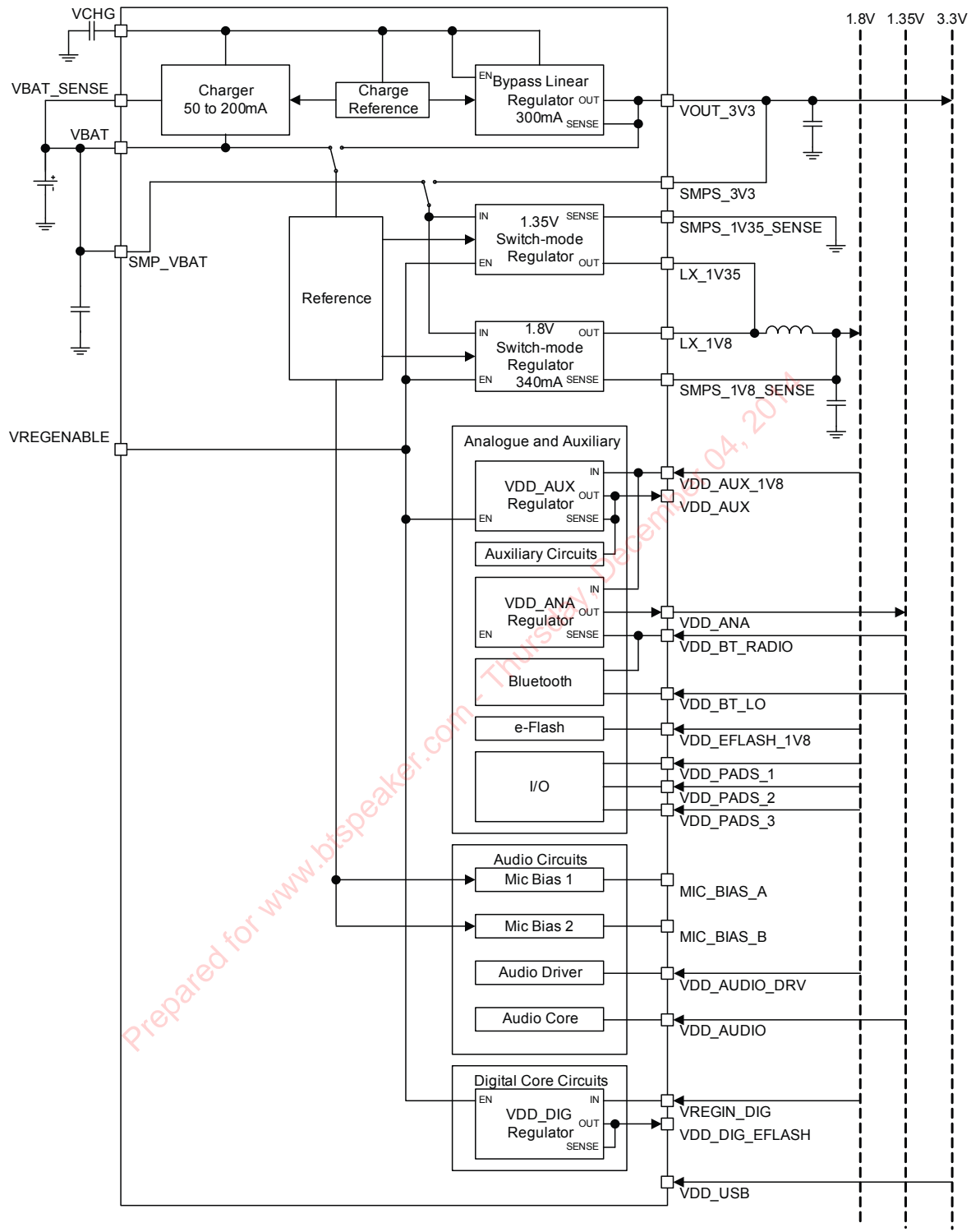


Figure 12.2: 1.80V Parallel-supply Switch-mode System Configuration

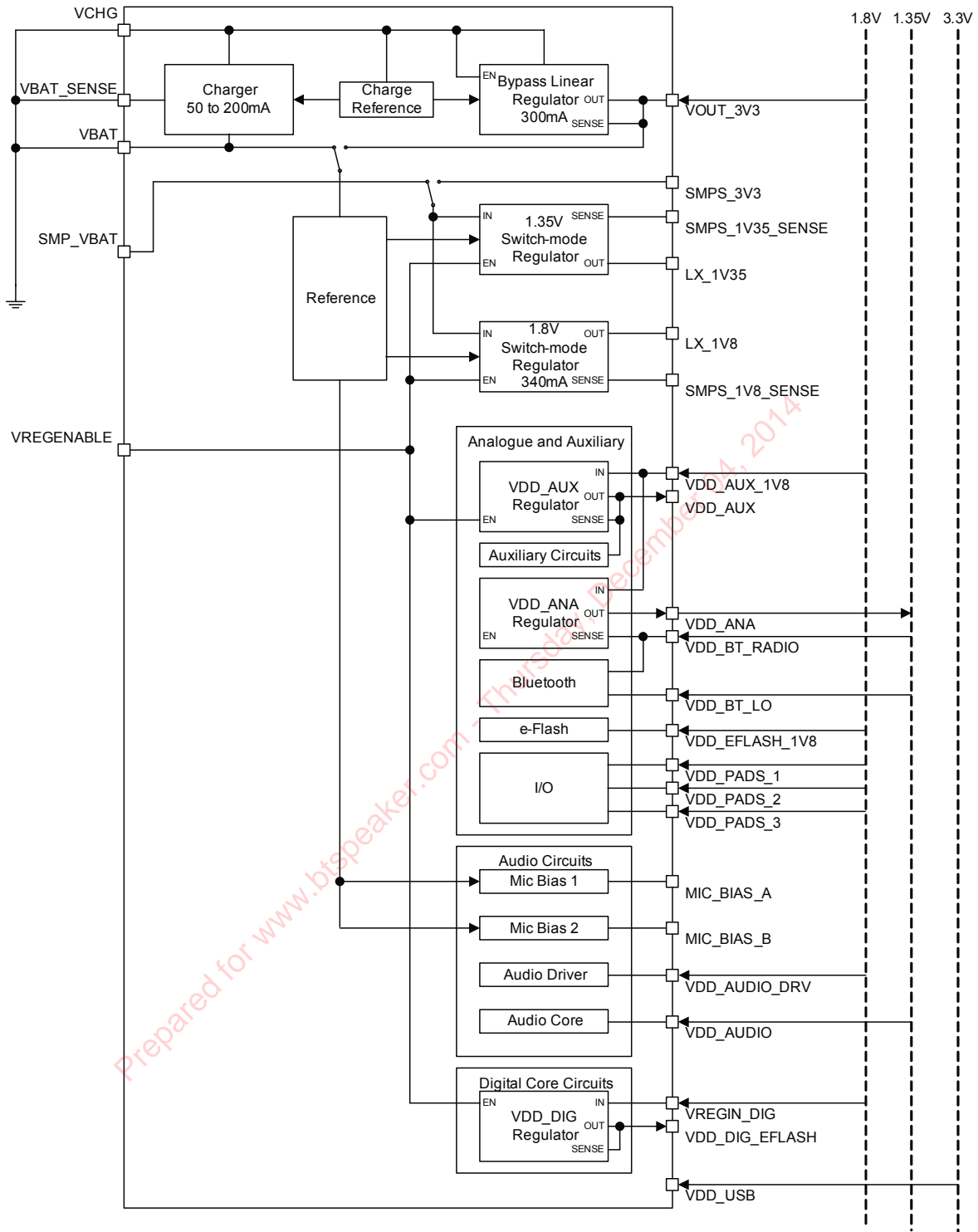


Figure 12.3: External 1.8V System Configuration

12.1 1.8V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.80V supply rail.

Figure 12.4 shows that an external LC filter circuit of a low-resistance series inductor, L1 (4.7μH), followed by a low ESR shunt capacitor, C3 (2.2μF), is required between the LX_1V8 terminal and the 1.80V supply rail. Connect the 1.80V supply rail and the SMPS_1V8_SENSE pin.

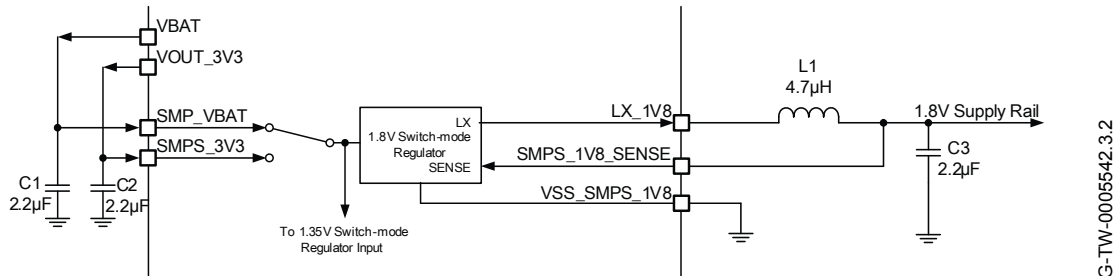


Figure 12.4: 1.8V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, SMP_VBAT and SMPS_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V8.

Also minimise the collective parasitic capacitance on the track between LX_1V8 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 16.3.1.1 requires a total resistance of <1.0Ω (<0.5Ω recommended) for the following:

- The track between the battery and SMP_VBAT.
- The track between LX_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80V supply rail.

The following enable the 1.80V switch-mode regulator:

- VREGENABLE pin
- The CSR8675 BGA firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.35V switch-mode regulator.

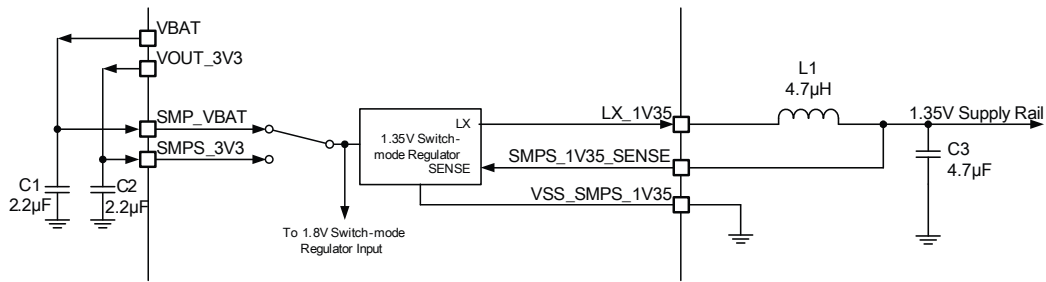
When the 1.80V switch-mode regulator is not required, leave unconnected:

- The regulator input SMP_VBAT and SMPS_3V3
- The regulator output LX_1V8

12.2 1.35V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.35V supply rail.

Figure 12.5 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7μH), followed by a low ESR shunt capacitor, C3 (4.7μF), is required between the LX_1V35 terminal and the 1.35V supply rail. Connect the 1.35V supply rail and the SMPS_1V35_SENSE pin.



G-TW-0005543.4.2

Figure 12.5: 1.35V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, SMP_VBAT and SMPS_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 16.3.2.1 requires a total resistance of $<1.0\Omega$ ($<0.5\Omega$ recommended) for the following:

- The track between the battery and SMP_VBAT.
- The track between LX_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.35V supply rail.

The following enable the 1.35V switch-mode regulator:

- VREGENABLE pin
- The CSR8675 BGA firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.80V switch-mode regulator.

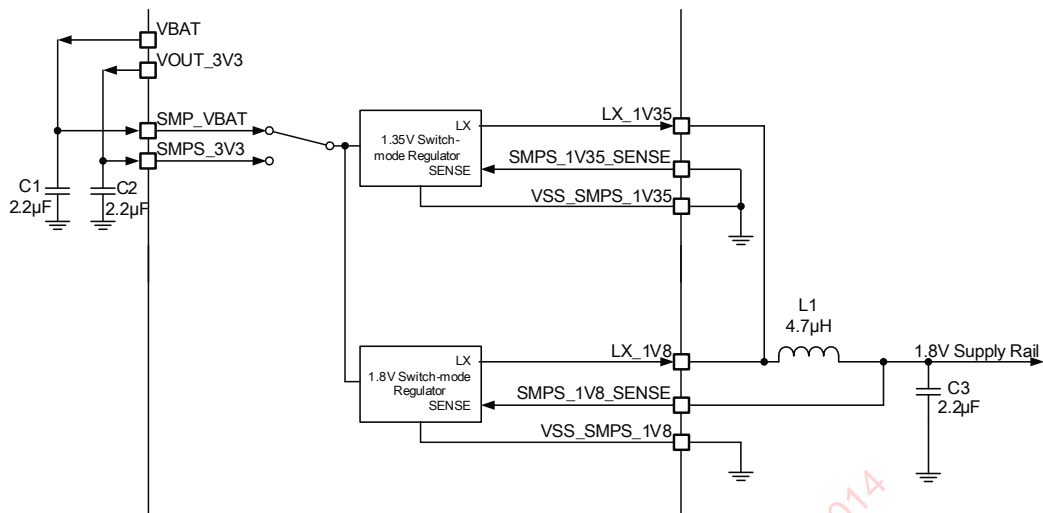
When the 1.35V switch-mode regulator is not required, leave unconnected:

- The regulator input SMP_VBAT and SMPS_3V3
- The regulator output LX_1V35

12.3 1.8V and 1.35V Switch-mode Regulators Combined

For applications that require a single 1.80V supply rail with higher currents CSR recommends combining the outputs of the integrated 1.80V and 1.35V switch-mode regulators in parallel to power a single 1.80V supply rail, see Figure 12.6.

Figure 12.6 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7µH), followed by a low ESR shunt capacitor, C3 (2.2µF), is required between the LX_1V8 terminal and the 1.80V supply rail. Connect the 1.80V supply rail and the SMPS_1V8_SENSE pin and ground the SMPS_1V35_SENSE pin.



G-TW-0005544.3.2

Figure 12.6: 1.8V and 1.35V Switch-mode Regulators Outputs Parallel Configuration

Minimise the series resistance of the tracks between the regulator input SMP_VBAT and SMPS_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3, VSS_SMPS_1V8 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V8, LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet the specifications in Section 16.3.1.2 requires a total resistance of $<1.0\Omega$ ($<0.5\Omega$ recommended) for the following:

- The track between the battery and SMP_VBAT.
- The track between LX_1V8, LX_1V35 and the inductor.
- The inductor L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80V supply rail.

The following enable the 1.80V switch-mode regulator:

- VREGENABLE pin
- The CSR8675 BGA firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00MHz using PSKEY_SMPS_FREQ_OFFSET.

When the 1.80V switch-mode regulator is not required, leave unconnected:

- The regulator input SMP_VBAT and SMPS_3V3
- The regulator output LX_1V8

12.4 Bypass LDO Linear Regulator

The integrated bypass LDO linear regulator is available as a 3.30V supply rail and is an alternative supply rail to the battery supply. This is especially useful when the battery has no charge and the CSR8675 BGA needs to power up. The input voltage should be between 4.25V and 6.50V. The maximum current from this regulator is 250mA.

Note:

The integrated bypass LDO linear regulator can operate down to 3.1V with a reduced performance.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 2.2µF to the VOUT_3V3 pin. With careful PCB layout this bypass capacitor can be shared with SMPS_3V3.

The output voltage is switched on when VCHG gets above 3.0V.

12.5 Low-voltage VDD_DIG Linear Regulator

The integrated low-voltage VDD_DIG linear regulator is available to power a 0.85 V to 1.20 V supply rail which includes the digital circuits on CSR8675 BGA. The input voltage range is between 1.30V and 1.95V. The maximum current from this regulator is 80mA.

Externally decouple the output of this regulator using a low ESR MLC capacitor of 470nF to VDD_DIG_EEFLASH1 and VDD_DIG_EEFLASH2 pins for optimum phase margin. CSR recommends due to increased current draw that K2 (VDD_DIG_EEFLASH2) is connected to E12 (VDD_DIG_EEFLASH1) on CSR8675 BGA designs. This is back compatible with CSR8670 BGA

The output voltage is enabled by VREGENABLE and the low-voltage VDD_DIG linear regulator must be on to run software code.

12.6 Low-voltage VDD_AUX Linear Regulator

The integrated low-voltage VDD_AUX linear regulator is available to power a 1.35V auxiliary supply rail (when the 1.35V switch-mode regulator is not used) which includes the analogue circuits on CSR8675 BGA. The input voltage should be between 1.70V and 1.95V. The maximum current from this regulator is 5mA.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 470nF to the VDD_AUX pin.

Connect a 2.2µF capacitor between the input to the regulator and ground to ensure stability.

This regulator is enabled by taking VREGENABLE or VCHG high and also the software controls the regulator enable/disable through PSKEY_PSU_ENABLES.

For safety, the initial output voltage of the low-voltage VDD_AUX linear regulator is 1.25V.

12.7 Low-voltage VDD_ANA Linear Regulator

The integrated low-voltage VDD_ANA linear regulator is available to power an optional 1.35V analogue supply rail which includes the analogue circuits on CSR8675 BGA. The input voltage should be between 1.70V and 1.95V. The maximum current from this regulator is 60mA.

If this regulator is required:

- Externally decouple the output of this regulator using a 2.2µF low ESR MLC capacitor to the VDD_ANA pin
- Connect a 2.2µF capacitor between the input to the regulator and ground to ensure stability

The software controls the regulator enable/disable through PSKEY_PSU_ENABLES.

12.8 Voltage Regulator Enable



When using the integrated regulators the voltage regulator enable pin, VREGENABLE, enables the CSR8675 BGA and the following regulators:

- 1.8V switch-mode regulator
- 1.35V switch-mode regulator
- Low-voltage VDD_DIG linear regulator
- Low-voltage VDD_AUX linear regulator

The VREGENABLE pin is active high, with a weak pull-down.

CSR8675 BGA boots-up when the voltage regulator enable pin is pulled high, enabling the regulators. The firmware then latches the regulators on. The voltage regulator enable pin can then be released.

The status of the VREGENABLE pin is available to firmware through an internal connection. VREGENABLE also works as an input line.

Note:

VREGENABLE should be asserted after the VBAT supply when VREGENABLE is not used as a power-on button.

12.9 External Regulators and Power Sequencing

CSR recommends that the integrated regulators supply the CSR8675 BGA and it is configured based on the information in this data sheet.

If any of the supply rails for the CSR8675 BGA are supplied from an external regulator, then it should match or be better than the internal regulator available on CSR8675 BGA. For more information see regulator characteristics in Section 16.

Note:

The internal regulators described in Section 12.1 to Section 12.7 are not recommended for external circuitry other than that shown in Section 14.

For information about power sequencing of external regulators to supply the CSR8675 BGA contact CSR.

12.10 Reset, RST#

CSR8675 BGA is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. CSR recommends applying RST# for a period >5ms.

The power-on reset occurs when:

- The VDD_DIG supply falls below typically 0.97V
- or
- The VDD_AUX_1V8 supply falls below typically 1.46V

And is released when:

- VDD_DIG rises above typically 1.10V
- or
- VDD_AUX_1V8 rises above typically 1.65V

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate. Following a reset, CSR8675 BGA assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until CSR8675 BGA is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in CSR8675 BGA free runs, again at a safe frequency.

12.10.1 Digital Pin States on Reset

Table 12.2 shows the pin states of CSR8675 BGA on reset. PU and PD default to weak values unless specified otherwise.

| Pin Name / Group | I/O Type | Full Chip Reset |
|------------------|-------------------------------|-----------------|
| USB_DP | Digital bidirectional | N/A |
| USB_DN | Digital bidirectional | N/A |
| UART_RX | Digital bidirectional with PU | Strong PU |
| UART_TX | Digital bidirectional with PU | Weak PU |
| UART_CTS | Digital bidirectional with PD | Weak PD |
| UART_RTS | Digital bidirectional with PU | Weak PU |
| SPI_CS# | Digital input with PU | Strong PU |
| SPI_CLK | Digital input with PD | Weak PD |

| Pin Name / Group | I/O Type | Full Chip Reset |
|--------------------|---------------------------------|-----------------|
| SPI_MISO | Digital tristate output with PD | Weak PD |
| SPI_MOSI | Digital input with PD | Weak PD |
| PCM_IN | Digital bidirectional with PD | Weak PD |
| PCM_OUT | Digital bidirectional with PD | Weak PD |
| PCM_SYNC | Digital bidirectional with PD | Weak PD |
| PCM_CLK | Digital bidirectional with PD | Weak PD |
| RST# | Digital input with PU | Strong PU |
| PIO[15:0] | Digital bidirectional with PD | Weak PD |
| QSPI_FLASH_IO[3:0] | Digital bidirectional with PD | Strong PD |
| QSPI_SRAM_CS# | Digital bidirectional with PU | Strong PU |
| QSPI_FLASH_CS# | Digital bidirectional with PU | Strong PU |
| QSPI_SRAM_CLK | Digital bidirectional with PD | Strong PD |
| QSPI_FLASH_CLK | Digital bidirectional with PD | Strong PD |

Table 12.2: Pin States on Reset

12.10.2 Status After Reset

The status of CSR8675 BGA after a reset is:

- Warm reset: baud rate and RAM data remain available
- Cold reset: baud rate and RAM data not available

12.11 Automatic Reset Protection

CSR8675 BGA includes an automatic reset protection circuit which restarts/resets CSR8675 BGA when an unexpected reset occurs, e.g. ESD strike or lowering of RST#. The automatic reset protection circuit enables resets from the VM without the requirement for external circuitry.

Note:

The reset protection is cleared after typically 2s (1.6s min to 2.4s max).

If RST# is held low for >2.4s CSR8675 BGA turns off. A rising edge on VREGENABLE or VCHG is required to power on CSR8675 BGA.

13 Battery Charger

13.1 Battery Charger Hardware Operating Modes

The battery charger hardware is controlled by the VM, see Section 13.3. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see Table 13.1 and Figure 13.1.

The internal charger circuit can provide up to 200mA of charge current, for currents higher than this the CSR8675 BGA can control an external pass transistor, see Section 13.5.

| Mode | Battery Charger Enabled | VBAT_SENSE |
|----------------|-------------------------|--|
| Disabled | No | X |
| Trickle charge | Yes | >0 and $<V_{fast}$ |
| Fast charge | Yes | $>V_{fast}$ and $<V_{float}$ |
| Standby | Yes | $I_{term}^{(a)}$ and $>(V_{float} - V_{hyst})$ |
| Error | Yes | $>(VCHG - 50mV)$ |

Table 13.1: Battery Charger Operating Modes Determined by Battery Voltage and Current

(a) I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting

Figure 13.1 shows the mode-to-mode transition voltages. These voltages are fixed and calibrated by CSR, see Section 13.2. The transition between modes can occur at any time.

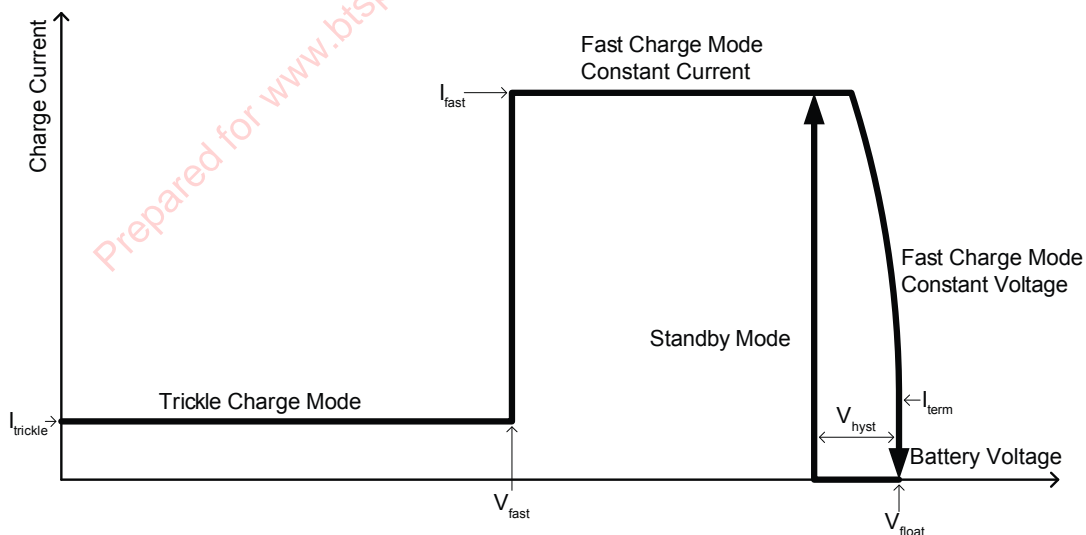


Figure 13.1: Battery Charger Mode-to-Mode Transition Diagram

Note:

The battery voltage remains constant in Fast Charge Constant Voltage Mode, the curved line on Figure 13.1 is for clarity only.

13.1.1 Disabled Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

13.1.2 Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the V_{fast} threshold, a current of approximately 10% of the fast charge current, I_{fast} , is sourced from the VBAT pin.

The V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.

13.1.3 Fast Charge Mode

When the voltage on VBAT_SENSE is greater than V_{fast} , the current sourced from the VBAT pin increases to I_{fast} . I_{fast} is between 10mA and 200mA set by PS Key or a VM trap. In addition, I_{fast} is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at I_{fast} until the voltage at VBAT_SENSE reaches V_{float} , then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin.

When the current sourced is below the termination current, I_{term} , the charging stops and the charger enters standby mode. I_{term} is typically 10% of the fast charge current.

13.1.4 Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at V_{hyst} below the final charging voltage, V_{float} , the charger re-enters fast charge mode.

13.1.5 Error Mode

The charger enters the error mode if the voltage on the VCHG pin is too low to operate the charger correctly (VBAT_SENSE is greater than VCHG - 50mV (typical)).

In this mode, charging is stopped. The battery charger does not require a reset to resume normal operation.

13.2 Battery Charger Trimming and Calibration

The battery charger default trim values are written by CSR into non-volatile memory when each IC is characterised. CSR provides various PS Keys for overriding the default trims, see Section 13.4.

13.3 VM Battery Charger Control

The VM charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery
- Monitoring the temperature of the die to protect against silicon damage
- Monitoring the time spent in the various charge states
- Enabling/disabling the charger circuitry based on the monitored information
- Driving the user visible charger status LED(s)

13.4 Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and traps called from the VM charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys.

For more information on the CSR8675 BGA, including details on setting up, calibrating, trimming and the PS Keys, see *Lithium Polymer Battery Charger Calibration and Operation for CSR867x* application note.

13.5 External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, R_{sense} , connected in series with the external pass device, see Figure 13.2. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across R_{sense} is typically 200mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

In Figure 13.2, R1 (220m Ω) and C1 (4.7 μ F) form an RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be <1.0 Ω .

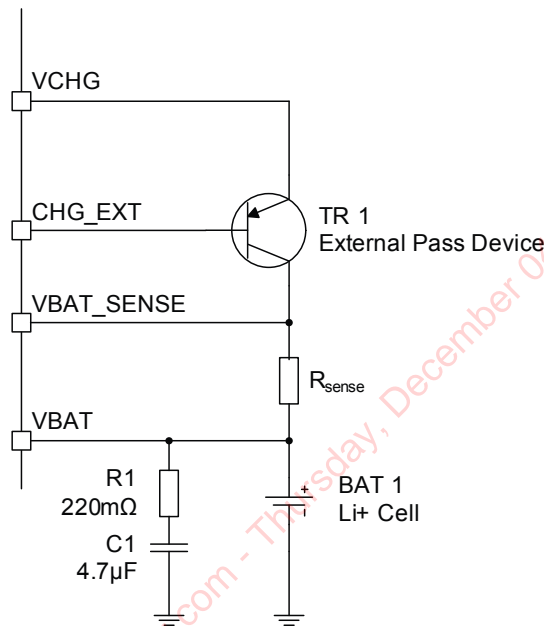


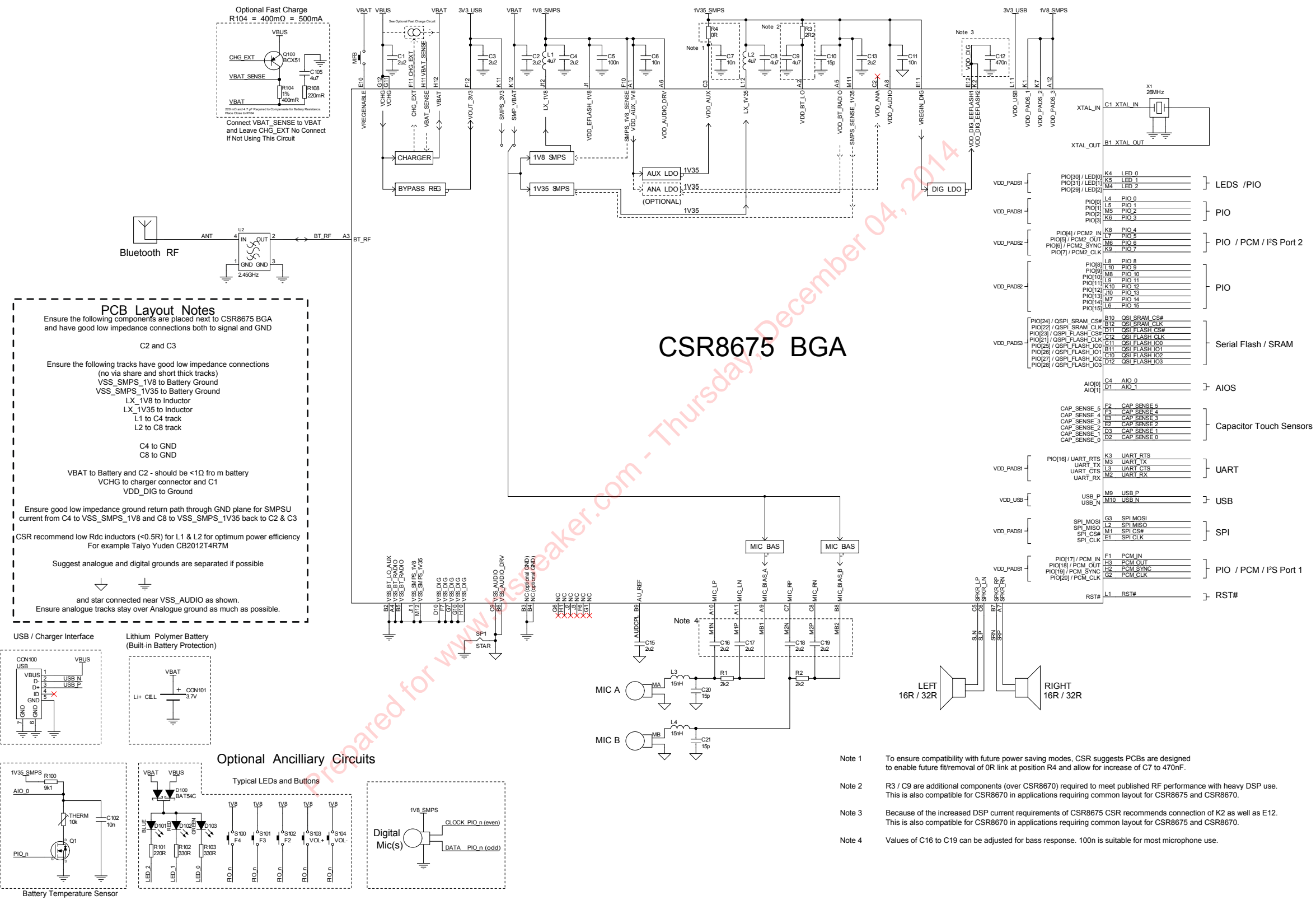
Figure 13.2: Battery Charger External Mode Typical Configuration

For optimum stability select TR1 to have Hfe current gain within the specification in Section 16.3.4 while ensuring that the CHG_EXT current remains below the limit stated in Section 16.3.4 at the desired charge current.

Ensure heat dissipation within TR1 and R_{sense} are considered within the design. Selectable external charge rates are possible with additional PIO controlled switches to change overall R_{sense} .

G-TW-0005585 2.3

14 Example Application Schematic



Production Information
© Cambridge Silicon Radio Limited 2013-2014
Confidential Information - This Material is Subject to CSR's Non-Disclosure Agreement



Figure 15.1: External 1.8V Supply Example Application

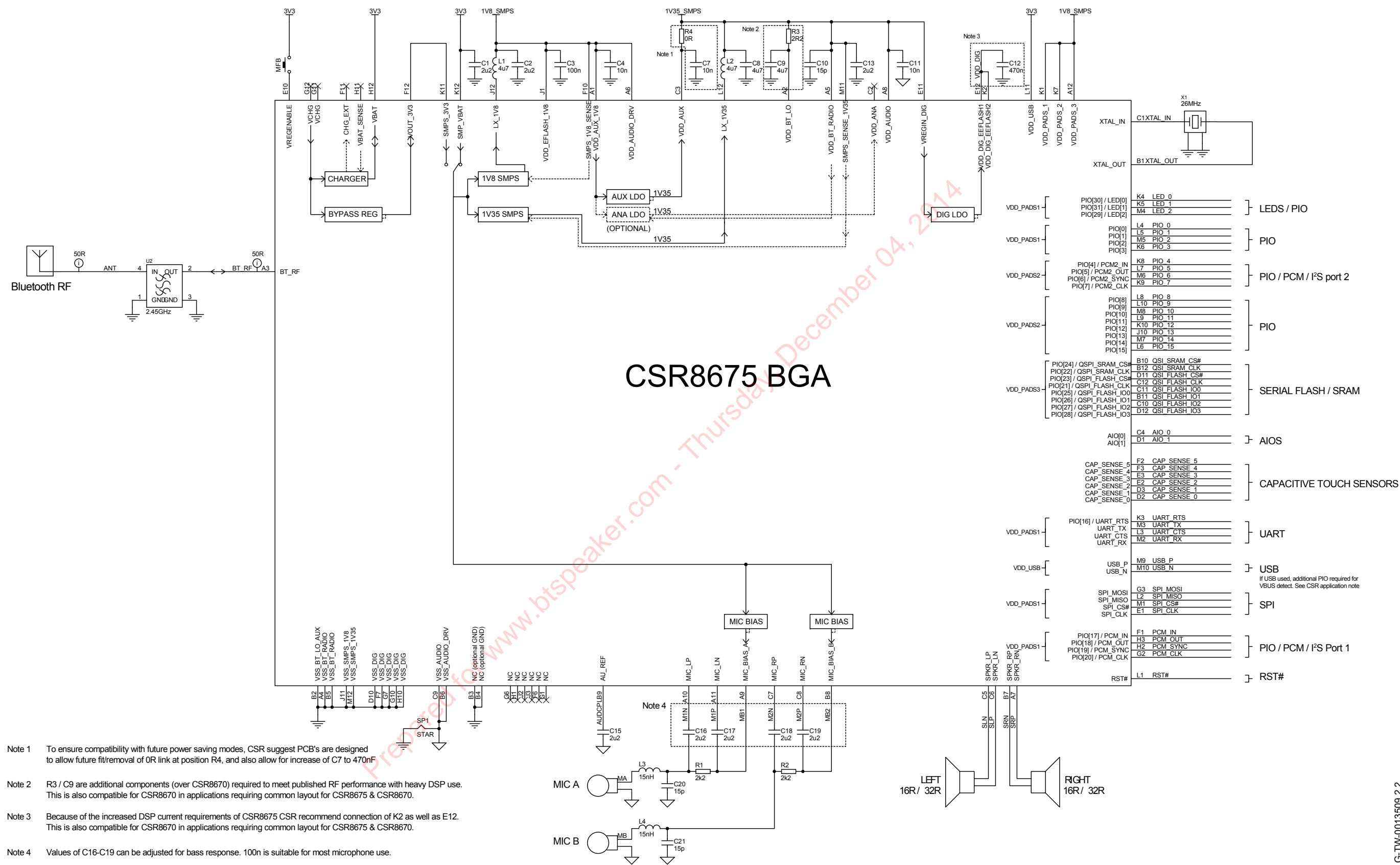


Figure 15.2: External 3.3V Supply Example Application

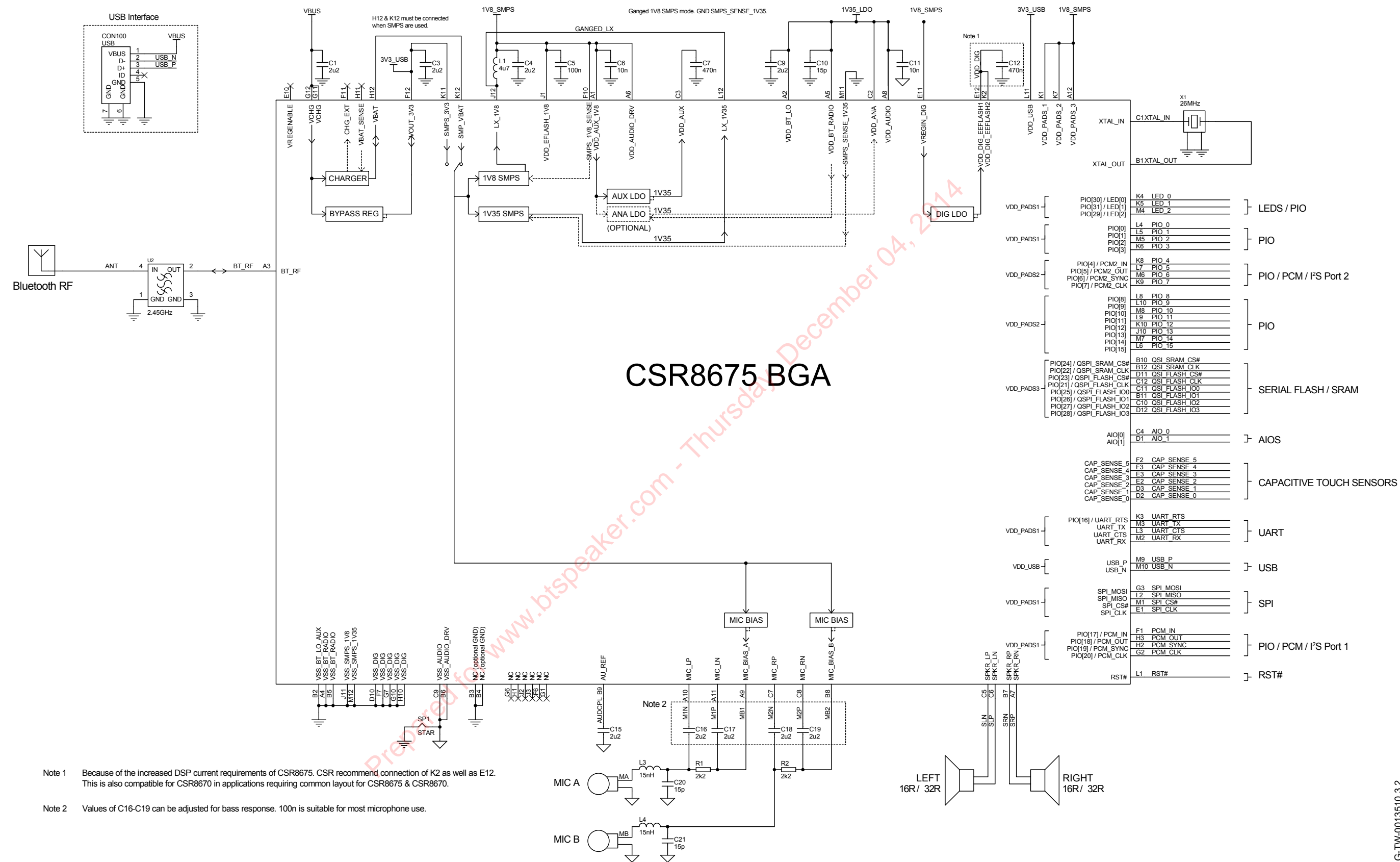


Figure 15.3: USB Dongle Example Application

16 Electrical Characteristics

16.1 Absolute Maximum Ratings

| Absolute Maximum Ratings | | Min | Max | Unit |
|--------------------------|-----------------|-----------|----------------------------|------|
| Storage temperature | | -40 | 105 | °C |
| Supply Voltage | | | | |
| 5 V (USB VBUS) | VCHG | -0.4 | 5.75 / 6.50 ^(a) | V |
| 3.3 V | SMPS_3V3 | -0.4 | 3.60 | V |
| | VDD_USB | -0.4 | 3.60 | V |
| Battery | LED[2:0] | -0.4 | 4.40 | V |
| | SMP_VBAT | -0.4 | 4.40 | V |
| | VBAT_SENSE | -0.4 | 5.75 | V |
| | VREGENABLE | -0.4 | 4.40 | V |
| PIO | VDD_PADS_1 | -0.4 | 3.60 | V |
| | VDD_PADS_2 | -0.4 | 3.60 | V |
| | VDD_PADS_3 | -0.4 | 3.60 | V |
| 1.8 V | VDD_AUDIO_DRV | -0.4 | 1.95 | V |
| | VDD_AUX_1V8 | -0.4 | 1.95 | V |
| | SMPS_1V8_SENSE | -0.4 | 1.95 | V |
| 1.35 V | SMPS_1V35_SENSE | -0.4 | 1.45 | V |
| | VDD_AUDIO | -0.4 | 1.45 | V |
| | VREGIN_DIG | -0.4 | 1.95 | V |
| Other terminal voltages | | VSS - 0.4 | VDD + 0.4 | V |

^(a) Standard maximum input voltage is 5.75 V, a 6.50 V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact CSR.

16.2 Recommended Operating Conditions

| Recommended Operating Conditions | | Min | Typ | Max | Unit |
|----------------------------------|-----------------|----------------------------|-----------------------------|----------------------------|------|
| Operating temperature range | | -40 | 20 | 85 | °C |
| Supply Voltage | | | | | |
| 5 V (USB VBUS) | VCHG | 4.75 / 3.10 ^(a) | 5.00 | 5.75 / 6.50 ^(b) | V |
| 3.3 V | SMPS_3V3 | 3.10 | 3.30 | 3.60 | V |
| | VDD_USB | 3.10 | 3.30 | 3.60 | V |
| Battery | LED[2:0] | 1.10 | 3.70 | 4.30 | V |
| | SMP_VBAT | 2.80 | 3.70 | 4.30 | V |
| | VBAT_SENSE | 0 | 3.70 | 4.30 | V |
| | VREGENABLE | 0 | 3.70 | 4.25 | V |
| PIO | VDD_PADS_1 | 1.70 | 1.80 | 3.60 | V |
| | VDD_PADS_2 | 1.70 | 1.80 | 3.60 | V |
| | VDD_PADS_3 | 1.70 | 1.80 | 3.60 | V |
| 1.8 V | VDD_AUDIO_DRV | 1.70 | 1.80 | 1.95 | V |
| | VDD_AUX_1V8 | 1.70 | 1.80 | 1.95 | V |
| | SMPS_1V8_SENSE | 1.70 | 1.80 | 1.95 | V |
| 1.35 V | SMPS_1V35_SENSE | 1.30 | 1.35 | 1.40 | V |
| | VDD_AUDIO | 1.30 | 1.35 | 1.40 | V |
| | VREGIN_DIG | 1.30 | 1.35 or 1.80 ^(c) | 1.95 | V |

^(a) Minimum input voltage of 4.75 V is required for full specification, regulator operates at reduced load current from 3.1 V.

^(b) Standard maximum input voltage is 5.75 V, a 6.50 V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact CSR.

^(c) Typical value depends on output required by the low-voltage VDD_DIG linear regulator, see Section 16.3.2.2.

16.3 Input/Output Terminal Characteristics

Note:

For all I/O terminal characteristics:

- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

16.3.1 Regulators: Available For External Use

16.3.1.1 1.8V Switch-mode Regulator

| 1.8V Switch-mode Regulator | Min | Typ | Max | Unit |
|---|-------|------|------|------|
| Input voltage | 2.80 | 3.70 | 4.25 | V |
| Output voltage | 1.70 | 1.80 | 1.90 | V |
| Normal Operation | | | | |
| Transient settling time | - | 30 | - | μs |
| Load current | - | - | 185 | mA |
| Current available for external use, stereo audio with 16Ω load ^(a) | - | - | 25 | mA |
| Peak conversion efficiency ^(b) | - | 90 | - | % |
| Switching frequency | 3.63 | 4.00 | 4.00 | MHz |
| Inductor saturation current, stereo and 16Ω load | 250 | - | - | mA |
| Inductor ESR | 0.1 | 0.3 | 0.8 | Ω |
| Low-power Mode, Automatically Entered in Deep Sleep | | | | |
| Transient settling time | - | 200 | - | μs |
| Load current | 0.005 | - | 5 | mA |
| Current available for external use | - | - | 5 | mA |
| Peak conversion efficiency | - | 85 | - | % |
| Switching frequency | 100 | - | 200 | kHz |

^(a) More current available for audio loads above 16Ω.

^(b) Conversion efficiency depends on inductor selection.

Note:

The regulator undershoots and overshoots when transitioning between modes.

16.3.1.2 Combined 1.8V and 1.35V Switch-mode Regulator

| Combined 1.8V and 1.35V Switch-mode Regulator | Min | Typ | Max | Unit |
|---|-------|------|------|------|
| Input voltage | 2.80 | 3.70 | 4.25 | V |
| Output voltage | 1.70 | 1.80 | 1.90 | V |
| Normal Operation | | | | |
| Transient settling time | - | 30 | - | μs |
| Load current | - | - | 340 | mA |
| Current available for external use, stereo audio with 16Ω load ^(a) | - | - | 25 | mA |
| Peak conversion efficiency ^(b) | - | 90 | - | % |
| Switching frequency | 3.63 | 4.00 | 4.00 | MHz |
| Inductor saturation current, stereo and 16Ω load | 400 | - | - | mA |
| Inductor ESR | 0.1 | 0.3 | 0.8 | Ω |
| Low-power Mode, Automatically Entered in Deep Sleep | | | | |
| Transient settling time | - | 200 | - | μs |
| Load current | 0.005 | - | 5 | mA |
| Current available for external use | - | - | 5 | mA |
| Peak conversion efficiency | - | 85 | - | % |
| Switching frequency | 100 | - | 200 | kHz |

^(a) More current available for audio loads above 16Ω.

^(b) Conversion efficiency depends on inductor selection.

Note:

The regulator undershoots and overshoots when transitioning between modes.

16.3.1.3 Bypass LDO Regulator

| Normal Operation | Min | Typ | Max | Unit |
|-------------------------------------|---------------------|------|---------------------|------|
| Input voltage | 4.25 ^(a) | 5.00 | 6.50 ^(b) | V |
| Output voltage ($V_{in} > 4.25V$) | 3.20 | 3.30 | 3.40 | V |
| Output current ($V_{in} > 4.75V$) | - | - | 250 | mA |

^(a) Minimum input voltage of 4.25 V is required for full specification, regulator operates at reduced load current from 3.1 V.

^(b) Standard maximum input voltage is 5.75 V, a 6.50 V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact CSR.

16.3.2 Regulators: For Internal Use Only

16.3.2.1 1.35V Switch-mode Regulator

| 1.35V Switch-mode Regulator | Min | Typ | Max | Unit |
|--|-------|------|------|------|
| Input voltage | 2.80 | 3.70 | 4.25 | V |
| Output voltage | 1.30 | 1.35 | 1.40 | V |
| Normal Operation | | | | |
| Transient settling time | - | 30 | - | μs |
| Load current | - | - | 160 | mA |
| Current available for external use | - | - | 0 | mA |
| Peak conversion efficiency ^(a) | - | 88 | - | % |
| Switching frequency | 3.63 | 4.00 | 4.00 | MHz |
| Inductor saturation current, stereo and 16Ω load | 220 | - | - | mA |
| Inductor ESR | 0.1 | 0.3 | 0.8 | Ω |
| Low-power Mode, Automatically Entered in Deep Sleep | | | | |
| Transient settling time | - | 200 | - | μs |
| Load current | 0.005 | - | 5 | mA |
| Current available for external use | - | - | 0 | mA |
| Peak conversion efficiency | - | - | 85 | % |
| Switching frequency | 100 | - | 200 | kHz |

^(a) Conversion efficiency depends on inductor selection.

Note:

The regulator undershoots and overshoots when transitioning between modes.

16.3.2.2 Low-voltage VDD_DIG Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|-------------------------------|------|--------------|------|------|
| Input voltage | 1.30 | 1.35 or 1.80 | 1.95 | V |
| Output voltage ^(a) | 0.80 | 0.90 / 1.20 | 1.25 | V |
| Internal load current | - | - | 80 | mA |

^(a) Output voltage level is software controlled

16.3.2.3 Low-voltage VDD_AUX Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|-----------------------|------|------|------|------|
| Input voltage | 1.70 | 1.80 | 1.95 | V |
| Output voltage | 1.30 | 1.35 | 1.45 | V |
| Internal load current | - | - | 5 | mA |

16.3.2.4 Low-voltage VDD_ANA Linear Regulator

| Normal Operation | Min | Typ | Max | Unit |
|------------------|------|------|------|------|
| Input voltage | 1.70 | 1.80 | 1.95 | V |
| Output voltage | 1.30 | 1.35 | 1.45 | V |
| Load current | - | - | 60 | mA |

16.3.3 Regulator Enable

| VREGENABLE, Switching Threshold | Min | Typ | Max | Unit |
|---------------------------------|-----|-----|-----|------|
| Rising threshold | - | - | 1.0 | V |

16.3.4 Battery Charger

| Battery Charger | Min | Typ | Max | Unit |
|---------------------|----------------------------|------|----------------------------|------|
| Input voltage, VCHG | 4.75 / 3.10 ^(a) | 5.00 | 5.75 / 6.50 ^(b) | V |

^(a) Reduced specification from 3.1V to 4.75V. Full specification >4.75V.

^(b) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact CSR.

| Trickle Charge Mode | Min | Typ | Max | Unit |
|--|-----|-----|-----|------|
| Charge current I_{trickle} , as percentage of fast charge current | 8 | 10 | 12 | % |
| V_{fast} rising threshold | - | 2.9 | - | V |
| V_{fast} rising threshold trim step size | - | 0.1 | - | V |
| V_{fast} falling threshold | - | 2.8 | - | V |

| Fast Charge Mode | | Min | Typ | Max | Unit |
|---|-----------------------|------|------|------|------|
| Charge current during constant current mode, I_{fast} | Max, headroom > 0.55V | 194 | 200 | 206 | mA |
| | Min, headroom > 0.55V | - | 10 | - | mA |
| Reduced headroom charge current, as a percentage of I_{fast} | Mid, headroom = 0.15V | 50 | - | 100 | % |
| Charge current step size | | - | 10 | - | mA |
| V_{float} threshold, calibrated | | 4.16 | 4.20 | 4.24 | V |
| Charge termination current I_{term} , as percentage of I_{fast} | | 7 | 10 | 20 | % |

| Standby Mode | Min | Typ | Max | Unit |
|---|-----|-----|-----|------|
| Voltage hysteresis on VBAT, V_{hyst} | 100 | - | 150 | mV |

| Error Charge Mode | Min | Typ | Max | Unit |
|---|-----|-----|-----|------|
| Headroom ^(a) error falling threshold | - | 50 | - | mV |

^(a) Headroom = VCHG - VBAT

| External Charge Mode ^(a) | Min | Typ | Max | Unit |
|---|-----|-----|----------------------------|------|
| Fast charge current, I_{fast} | 200 | - | 500 | mA |
| Control current into CHG_EXT | 0 | - | 20 | mA |
| Voltage on CHG_EXT | 0 | - | 5.75 / 6.50 ^(b) | V |
| External pass device h_{fe} | 25 | 50 | 250 | - |
| Sense voltage, between VBAT_SENSE and VBAT at maximum current | 195 | 200 | 205 | mV |

^(a) In the external mode, the battery charger meets all the previous charger electrical characteristics and the additional or superseded electrical characteristics are listed in this table.

^(b) Standard maximum input voltage is 5.75 V, a 6.50 V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact CSR.

16.3.5 Reset

| Power-on Reset | Min | Typ | Max | Unit |
|--|-----|------|-----|------|
| VDD_DIG falling threshold (active mode) | - | 0.97 | - | V |
| VDD_DIG rising threshold (active mode) | - | 1.10 | - | V |
| VDD_DIG hysteresis (active mode) | - | 130 | - | mV |
| VDD_DIG falling threshold (deep sleep mode) | - | 0.77 | - | V |
| VDD_AUX_1V8 falling threshold ^(a) | - | 1.46 | - | V |
| VDD_AUX_1V8 rising threshold | - | 1.65 | - | V |
| VDD_AUX_1V8 hysteresis | - | 190 | - | mV |

^(a) The 1.8V switch-mode power supply rail can briefly drop to >1.3V during deep sleep exit. This is expected behaviour and does not cause a reset.

16.3.6 USB

| USB | Min | Typ | Max | Unit |
|--|----------------|------|----------------|------|
| VDD_USB for correct USB operation | 3.10 | 3.30 | 3.60 | V |
| Input Threshold | | | | |
| V _{IL} input logic level low | - | - | 0.30 x VDD_USB | V |
| V _{IH} input logic level high | 0.70 x VDD_USB | - | - | V |
| Output Voltage Levels to Correctly Terminated USB Cable | | | | |
| V _{OL} output logic level low | 0 | - | 0.2 | V |
| V _{OH} output logic level high | 2.80 | - | VDD_USB | V |

16.3.7 Clocks

| Crystal Oscillator | Min | Typ | Max | Unit |
|-----------------------------------|------|-----|-----|------|
| Frequency | 19.2 | 26 | 32 | MHz |
| External crystal load capacitance | - | 0 | - | pF |
| On-chip crystal load capacitance | - | 9 | - | pF |
| Frequency stability | - | - | ±20 | ppm |
| Transconductance | 2 | - | - | mS |

| External Clock | Min | Typ | Max | Unit |
|--|------|-----|---------------|---------|
| Input frequency ^(a) | 19.2 | 26 | 40 | MHz |
| Clock input level ^(b) | 0.2 | 0.4 | VDD_AUX | V pk-pk |
| Edge jitter (allowable jitter), at zero crossing | - | - | 10 | ps rms |
| XTAL_IN input impedance | 30 | - | - | kΩ |
| XTAL_IN input capacitance | - | - | 1 | pF |
| DC level | -0.4 | - | VDD_AUX + 0.4 | V |

^(a) Clock input is any frequency from 19.2 MHz to 40 MHz (default 26 MHz) in steps of 250 kHz plus CDMA/3G TCXO frequencies of 19.2, 19.44, 19.68, 19.8 and 38.4 MHz.

^(b) Clock input is either sinusoidal or square wave. If the peaks of the signal are below VSS_BT_LO_AUX or above VDD_AUX. A DC blocking capacitor is required between the signal and XTAL_IN.

16.3.8 Stereo Codec: Analogue to Digital Converter

| Analogue to Digital Converter | | | | | | |
|---|--|---------------------|-----|-------|------|------|
| Parameter | Conditions | | Min | Typ | Max | Unit |
| Resolution | - | | - | 16 | - | Bits |
| Input Sample Rate, F_{sample} | - | | 8 | - | 96 | kHz |
| SNR | $f_{\text{in}} = 1\text{kHz}$ $B/W = 20\text{Hz} \rightarrow F_{\text{sample}}/2$ (20kHz max) A-Weighted $\text{THD+N} < 0.1\%$ $1.6V_{\text{pk-pk}}$ input | F_{sample} | | | | |
| | | 8kHz | - | 93 | - | dB |
| | | 16kHz | - | 92 | - | dB |
| | | 32kHz | - | 92 | - | dB |
| | | 44.1kHz | - | 92 | - | dB |
| | | 48kHz | - | 92 | - | dB |
| THD+N | $f_{\text{in}} = 1\text{kHz}$ $B/W = 20\text{Hz} \rightarrow F_{\text{sample}}/2$ (20kHz max) $1.6V_{\text{pk-pk}}$ input | F_{sample} | | | | |
| | | 8kHz | - | 0.004 | - | % |
| | | 48kHz | - | 0.008 | - | % |
| Digital gain | Digital gain resolution = 1/32 | | -24 | - | 21.5 | dB |
| Analogue gain | Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB Analogue setting = -3dB to 12dB in 3dB steps | | -3 | - | 42 | dB |
| Stereo separation (crosstalk) | Measurement bandwidth = 20Hz to 20kHz Amplitude response = RMS No weighting Input amplitude = 300mVrms, 20Hz, 1kHz, 20kHz tones, 48kHz sample rate Analogue gain set to 2, digital gain set to 0 | | - | -89 | - | dB |

16.3.9 Stereo Codec: Digital to Analogue Converter

| Digital to Analogue Converter | | | | | | |
|---|---|---------------------|---------------|-----|-------|--------|
| Parameter | Conditions | | Min | Typ | Max | Unit |
| Resolution | - | | - | 16 | - | Bits |
| Output Sample Rate, F_{sample} | - | | 8 | - | 192 | kHz |
| SNR | $f_{\text{in}} = 1\text{kHz}$ B/W = 20Hz→20kHz A-Weighted THD+N < 0.01% 0dBFS input | F_{sample} | Load | | | |
| | | 48kHz | 100k Ω | - | 96 | - dB |
| | | 48kHz | 32 Ω | - | 96 | - dB |
| | | 48kHz | 16 Ω | - | 96 | - dB |
| THD+N | $f_{\text{in}} = 1\text{kHz}$ B/W = 20Hz→20kHz 0dBFS input | F_{sample} | Load | | | |
| | | 8kHz | 100k Ω | - | 0.002 | - % |
| | | 8kHz | 32 Ω | - | 0.002 | - % |
| | | 8kHz | 16 Ω | - | 0.003 | - % |
| | | 48kHz | 100k Ω | - | 0.003 | - % |
| | | 48kHz | 32 Ω | - | 0.003 | - % |
| | | 48kHz | 16 Ω | - | 0.004 | - % |
| Digital Gain | Digital Gain Resolution = 1/32 | | -24 | - | 21.5 | dB |
| Analogue Gain | Analogue Gain Resolution = 3dB | | -21 | - | 0 | dB |
| Output voltage | Full-scale swing (differential) | | - | - | 778 | mV rms |
| Stereo separation (crosstalk) | Measurement bandwidth = 20Hz to 20kHz Amplitude response = RMS No weighting Input amplitude = 0dBFS, 20Hz, 1kHz, 20kHz tones, 48kHz sample rate Analogue gain set to 7, digital gain set to 0 | | - | -88 | - | dB |

16.3.10 Digital

| Digital Terminals | Min | Typ | Max | Unit |
|--|----------------------|------|----------------|---------------|
| Input Voltage | | | | |
| V_{IL} input logic level low | -0.4 | - | 0.4 | V |
| V_{IH} input logic level high | $0.7 \times V_{DD}$ | - | $V_{DD} + 0.4$ | V |
| T_r/T_f | - | - | 25 | ns |
| Output Voltage | | | | |
| V_{OL} output logic level low, $I_{OL} = 4.0\text{mA}$ | - | - | 0.4 | V |
| V_{OH} output logic level high, $I_{OH} = -4.0\text{mA}$ | $0.75 \times V_{DD}$ | - | - | V |
| T_r/T_f | - | - | 5 | ns |
| Input and Tristate Currents | | | | |
| Strong pull-up | -150 | -40 | -10 | μA |
| Strong pull-down | 10 | 40 | 150 | μA |
| Weak pull-up | -5 | -1.0 | -0.33 | μA |
| Weak pull-down | 0.33 | 1.0 | 5.0 | μA |
| C_I Input Capacitance | 1.0 | - | 5.0 | pF |

16.3.11 LED Driver Pads

| LED Driver Pads | | Min | Typ | Max | Unit |
|---|-------------------------|-----|-----|------|---------------|
| Current, I_{PAD} | High impedance state | - | - | 5 | μA |
| | Current sink state | - | - | 10 | mA |
| LED pad voltage, V_{PAD} | $I_{PAD} = 10\text{mA}$ | - | - | 0.55 | V |
| LED pad resistance | $V_{PAD} < 0.5\text{V}$ | - | - | 40 | Ω |
| V_{OL} output logic level low ^(a) | | - | 0 | - | V |
| V_{OH} output logic level high ^(a) | | - | 0.8 | - | V |
| V_{IL} input logic level low | | - | 0 | - | V |
| V_{IH} input logic level high | | - | 0.8 | - | V |

^(a) LED output port is open-drain and requires a pull-up

16.3.12 Auxiliary ADC

| Auxiliary ADC | | Min | Typ | Max | Unit |
|------------------------------------|-----|------|------|---------|-----------|
| Resolution | | - | - | 10 | Bits |
| Input voltage range ^(a) | | 0 | - | VDD_AUX | V |
| Accuracy (Guaranteed monotonic) | INL | -1 | - | 1 | LSB |
| | DNL | 0 | - | 1 | LSB |
| Offset | | -1 | - | 1 | LSB |
| Gain error | | -0.8 | - | 0.8 | % |
| Input bandwidth | | - | 100 | - | kHz |
| Conversion time | | 1.38 | 1.69 | 2.75 | µs |
| Sample rate ^(b) | | - | - | 700 | Samples/s |

^(a) LSB size = VDD_AUX/1023

^(b) The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

16.3.13 Auxiliary DAC

| Auxiliary DAC | | Min | Typ | Max | Unit |
|------------------------------|--|-------|------|---------|------|
| Resolution | | - | - | 10 | Bits |
| Supply voltage, VDD_AUX | | 1.30 | 1.35 | 1.40 | V |
| Output voltage range | | 0 | - | VDD_AUX | V |
| Full-scale output voltage | | 1.30 | 1.35 | 1.40 | V |
| LSB size | | 0 | 1.32 | 2.64 | mV |
| Offset | | -1.32 | 0 | 1.32 | mV |
| Integral non-linearity | | -1 | 0 | 1 | LSB |
| Settling time ^(a) | | - | - | 250 | ns |

^(a) The settling time does not include any capacitive load

Important Note:

Access to the auxiliary DAC is firmware-dependent, for more information about its availability contact CSR.

16.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 16.1 shows the ESD handling maximum ratings.

| Condition | Class | Max Rating |
|--|-------|--|
| Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001 | 2 | 2 kV (all pins except CHG_EXT, SMPS_1V35_SENSE and SMPS_1V8_SENSE at 1 kV) |
| Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101 | II | 200 V (all pins) |

Table 16.1: ESD Handling Ratings

16.4.1 USB Electrostatic Discharge Immunity

CSR8675 BGA has integrated ESD protection on the USB_DP and USB_DN pins as detailed in IEC 61000-4-2.

Depending on the software implementation on CSR8675 BGA and the device at the far end, self-recovery of the Bluetooth link is possible if CSR8675 BGA resets on an ESD strike. This classifies CSR8675 BGA as IEC 61000-4-2 classification 2 to level 4 (8 kV contact discharge / 15 kV air discharge). If self-recovery is not implemented, CSR8675 BGA is IEC 61000-4-2 classification 3 to level 4.

Note:

Any test detailed in the IEC-61000-4-2 level 4 test specification does not damage CSR8675 BGA.

The CSR8675 BGA USB VBUS pin is protected to level 4 using an external 2.2 μ F decoupling capacitor on VCHG.

Important Note:

CSR recommends correct PCB routing and to route the VBUS track through a decoupling capacitor pad.

When the USB connector is a long way from CSR8675 BGA, place an extra 1 μ F or 2.2 μ F capacitor near the USB connector.

No components (including 22 Ω series resistors) are required between CSR8675 BGA and the USB_DP and USB_DN lines.

To recover from an unintended reset, e.g. a large ESD strike, the watchdog and reset protection feature can restart CSR8675 BGA and signal the unintended reset to the VM.

Table 16.2 summarises the level of protection.

| IEC 61000-4-2 Level | ESD Test Voltage (Positive and Negative) | IEC 61000-4-2 Classification | Comments |
|---------------------|--|------------------------------|---|
| 1 | 2 kV contact / 2 kV air | Class 1 | Normal performance within specification limits |
| 2 | 4 kV contact / 4 kV air | Class 1 | Normal performance within specification limits |
| 3 | 6 kV contact / 8 kV air | Class 2 or class 3 | Temporary degradation or operator intervention required |
| 4 | 8 kV contact / 15 kV air | Class 2 or class 3 | Temporary degradation or operator intervention required |

Table 16.2: USB Electrostatic Discharge Protection Level



For more information contact CSR.

Prepared for www.btspeaker.com - Thursday, December 04, 2014

17 Power Consumption

| DUT Role | Connection | | Packet Type | Average Current | Unit |
|----------|-----------------------|---|-------------|-----------------|------|
| N/A | Deep sleep | With UART host connection | - | 76 | μA |
| N/A | Page scan | Page = 1280ms interval Window = 11.25ms | - | 261 | μA |
| N/A | Inquiry and page scan | Inquiry = 1280ms interval Page = 1280ms interval Window = 11.25ms | - | 482 | μA |
| Master | ACL | Sniff = 500ms, 1 attempt, 0 timeout | DH1 | 173 | μA |
| Master | ACL | Sniff = 1280ms, 8 attempts, 1 timeout | DH1 | 150 | μA |
| Master | SCO | Sniff = 100ms, 1 attempt, PCM | HV3 | 9.9 | mA |
| Master | SCO | Sniff = 100ms, 1 attempt, mono audio codec | HV3 | 10.7 | mA |
| Master | eSCO | Setting S3, sniff = 100ms, PCM | 2EV3 | 8.0 | mA |
| Master | eSCO | Setting S3, sniff = 100ms, PCM | 3EV3 | 7.7 | mA |
| Master | eSCO | Setting S3, sniff = 100ms, mono audio codec | 2EV3 | 9.9 | mA |
| Master | eSCO | Setting S3, sniff = 100ms, mono audio codec | 3EV3 | 9.5 | mA |
| Slave | ACL | Sniff = 500ms, 1 attempt, 0 timeout | DH1 | 182 | μA |
| Slave | ACL | Sniff = 1280ms, 8 attempts, 1 timeout | DH1 | 187 | μA |
| Slave | SCO | Sniff = 100ms, 1 attempt, PCM | HV3 | 10.2 | mA |
| Slave | SCO | Sniff = 100ms, 1 attempt, mono audio codec | HV3 | 12.0 | mA |
| Slave | eSCO | Setting S3, sniff = 100ms, PCM | 2EV3 | 8.4 | mA |
| Slave | eSCO | Setting S3, sniff = 100ms, PCM | 3EV3 | 8.1 | mA |
| Slave | eSCO | Setting S3, sniff = 100ms, mono audio codec | 2EV3 | 10.3 | mA |
| Slave | eSCO | Setting S3, sniff = 100ms, mono audio codec | 3EV3 | 10.0 | mA |

Note:

Current consumption values are taken with:

- HCI only
- VBAT pin = 3.7 V
- Firmware ID = 10528
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH off
- Pulse skipping mode disabled

18 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction on Hazardous Substances directive guidelines in the EU RoHS Directive 2011/65/EU¹.
- EU REACH, Regulation (EC) No 1907/2006¹:
 - List of substances subject to authorisation (Annex XIV)
 - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
 - When requested by customers, notification of substances identified on the Candidate List as Substances of Very High Concern (SVHC)¹.
- POP regulation (EC) No 850/2004¹
- EU Packaging and Packaging Waste, Directive 94/62/EC¹
- Montreal Protocol on substances that deplete the ozone layer.
- Conflict minerals, Section 1502, Dodd-Frank Wall Street Reform and Consumer Protection act, which affects columbite-tantalite (coltan / tantalum), cassiterite (tin), gold, wolframite (tungsten) or their derivatives. CSR is a fabless semiconductor company: all manufacturing is performed by key suppliers. CSR have mandated that the suppliers shall not use materials that are sourced from "conflict zone mines" but understand that this requires accurate data from the EICC programme. CSR shall provide a complete EICC / GeSI template upon request.

CSR has defined the "CSR Green" standard based on current regulatory and customer requirements including free from bromine, chlorine and antimony trioxide.

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

This identifies the main environmental compliance regulatory restrictions CSR specify. For more information on the full "CSR Green" standard, contact product.compliance@csr.com.

¹ Including applicable amendments to EU law which are published in the EU Official Journal, or SVHC Candidate List updates published by the European Chemicals Agency (ECHA).

19 Software

CSR8675 BGA:

- Is supplied with on-chip Bluetooth v4.1 specification qualified HCI stack firmware
- Has on-chip software that can be loaded with applications from CSR's audio development kit, see Section 19.2.1.1
- Has on-chip software that can be loaded with applications from CSR's eXtension Program

19.1 On-chip Software

19.1.1 Stand-alone CSR8675 BGA and Kalimba DSP Applications

Figure 19.1 shows the structure of the stack for running on-chip software and applications, it is built on top of the HCI stack in Section 19.1.2. The stack firmware requires no host processor, but uses a host processor for debugging etc, as Figure 19.1 shows. The software layers for the application software run on the internal MCU in a protected user-software execution environment known as a VM and the DSP application code runs from the DSP program memory RAM.

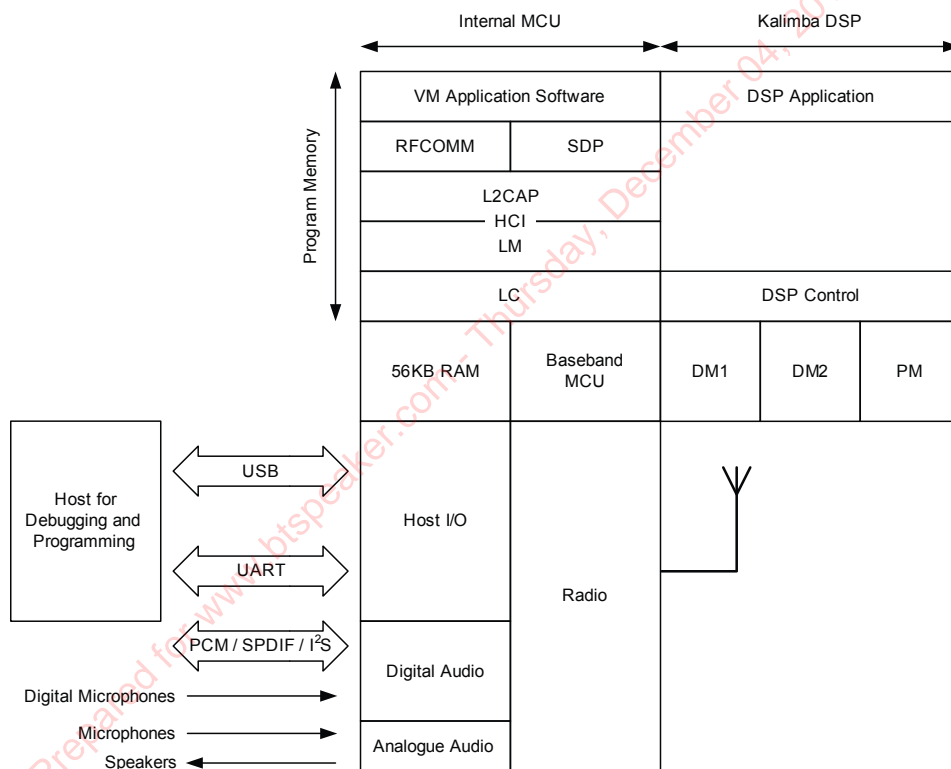


Figure 19.1: Stand-alone CSR8675 BGA and Kalimba DSP Applications

Note:

Program memory in Figure 19.1 is internal flash.

CSR provides a development kit that customers can configure to meet their audio and consumer end-product requirements.

The development kit include firmware components, applications and appropriate profile support. For more information see Section 19.2.1.

19.1.2 BlueCore HCI Stack

Figure 19.2 shows HCI stack implementation. The internal MCU runs the Bluetooth stack up to the HCI.

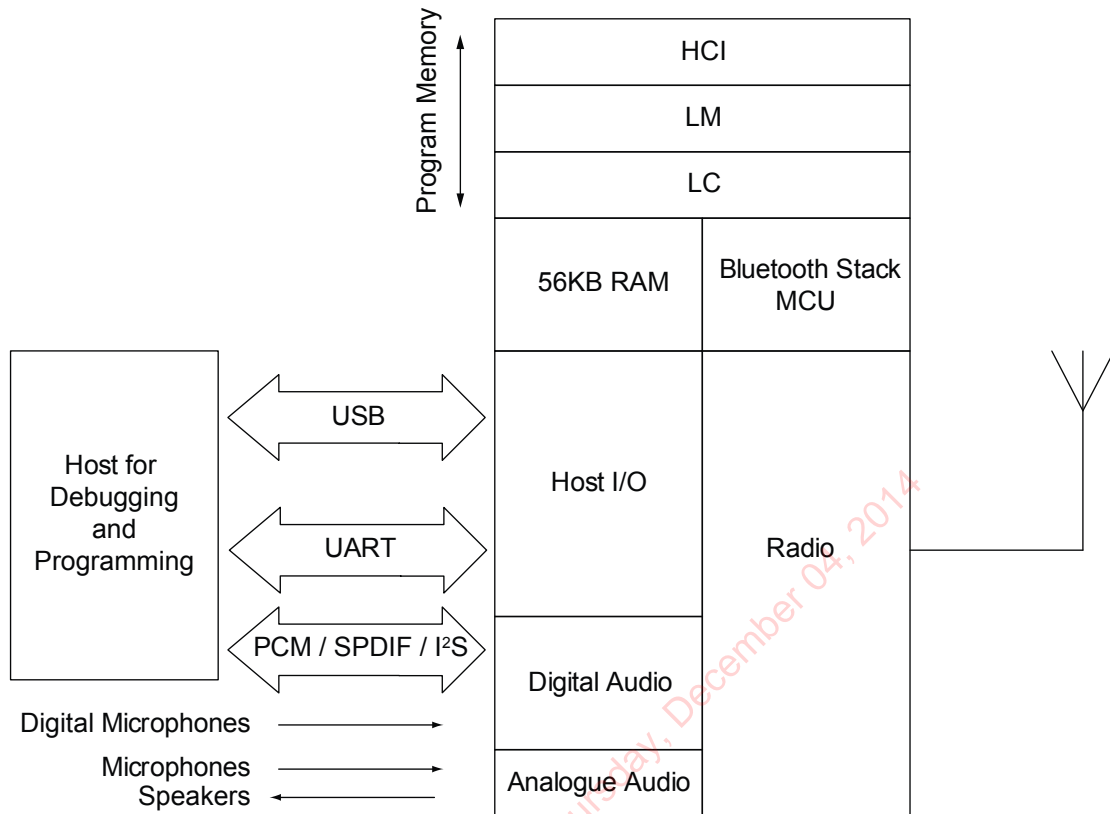


Figure 19.2: BlueCore HCI Stack

Note:

Program Memory in Figure 19.2 is internal flash.

19.1.2.1 Latest Features of the HCI Stack

CSR8675 BGA is qualified to the Bluetooth v4.1 specification.

19.2 Off-chip Software

19.2.1 CSR8675 Development Kit

CSR's audio development kit for the CSR8675 BGA, order code DK-CSR8675-10197-1A, includes a CSR8675 BGA demonstrator board (DB-CSR8675-10200-1A) and necessary interface adapters and cables are available. In conjunction with the CSR8675 Configurator tool and other supporting utilities the development kit provides the best environment for designing audio solutions with the CSR8675 BGA.

Important Note:

The CSR8675 BGA audio development kit is subject to change and updates, for up-to-date information see www.csrsupport.com.

19.2.1.1 Audio Development Kit Software

In conjunction with the CSR8675 audio development kit, software is available, it requires a *Bluetooth Developer's Licence* to use. CSR's current software includes:

- **Bluetooth Profiles:**
 - Bluetooth v4.1 specification support
 - HFP v1.6
 - HSP v1.2
 - A2DP v1.2
 - AVRCP v1.4
 - PBAP v1.0
 - MAP v1.0
 - SPP v1.0
- **Improved Audio Quality:**
 - CVC 1-mic far-end audio enhancements (narrowband)
 - CVC 2-mic far-end audio enhancements (narrowband)
 - CVC 1-mic far-end audio enhancements (hands-free)
 - CVC 1-mic far-end audio enhancements (wideband)
 - CVC 2-mic far-end audio enhancements (wideband)
 - CVC near-end audio enhancements
 - PLC / BEC
 - 1-mic WNR
 - 2-mic WNR
 - Sidetone
 - Frequency expansion for improved speech intelligibility
- **Music Enhancements:**
 - aptX codec technology
 - 5-band EQ
 - 3D stereo separation
 - Dynamic range control
 - Faststream codec
 - SBC decoder
 - MP3 decoder
 - AAC decoder
- **Additional Functionality:**
 - Multipoint for HFP, A2DP and advance user-cases
 - Programmable audio prompts (compressed / SBC)
 - Support for capacitive touch control
 - Support for speech recognition
 - Support for multi-language programmable audio prompts
 - CSR's proximity pairing and CSR's proximity connection
 - Multipoint support for HFP connection to 2 handsets for voice
 - Multipoint support for A2DP connection to 2 A2DP sources for music playback
 - Talk-time extension

19.2.2 eXtension Program Support

A wide range of software options is available from CSR's eXtension Program Support, see www.csr.com.

20 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

20.1 Tape Orientation

Figure 20.1 shows the general orientation of the CSR8675 BGA package in the carrier tape.

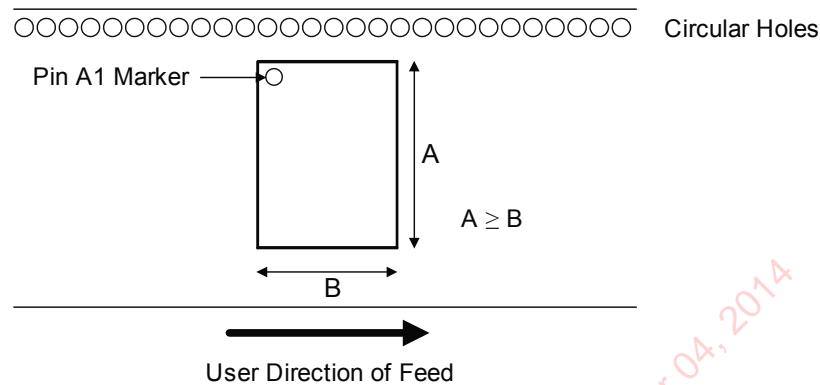


Figure 20.1: Tape Orientation

20.2 Tape Dimensions

Figure 20.2 shows the dimensions of the tape for the CSR8675 BGA.

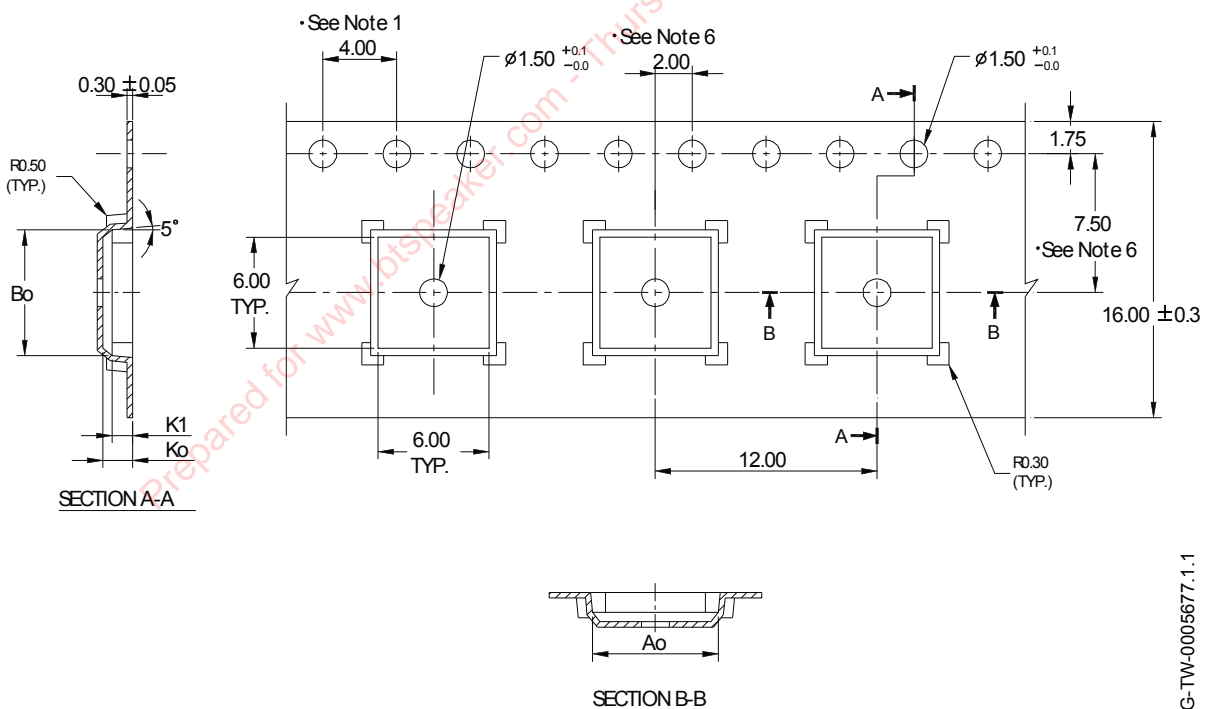
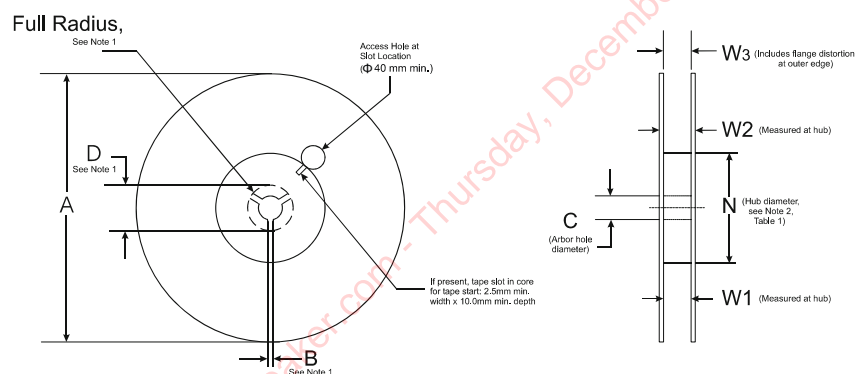


Figure 20.2: Tape Dimensions

| A ₀ | B ₀ | K ₀ | K ₁ | Unit | Notes |
|----------------|----------------|----------------|----------------|------|--|
| 6.80 | 6.80 | 1.60 | 1.10 | mm | <ol style="list-style-type: none"> 10 sprocket hole pitch cumulative tolerance ± 0.2. Camber not to exceed 1mm in 100mm. Material: black polystyrene. A₀ and B₀ measured on a plane 0.3mm above the bottom of the pocket. K₀ measured from a plane on the inside bottom of the pocket to the top surface of the carrier tape. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole |

20.3 Reel Information

Reel dimensions
(All dimensions in millimeters)



Notes:
1. Drive spokes optional; if used, dimensions B and D shall apply.
2. Maximum weight of reel and contents 13.6kg.

Figure 20.3: Reel Dimensions

| Package Type | Tape Width | A Max | B Max | C | D Min | N Min | W1 | W2 Max | W3 | | Units |
|------------------------|------------|-------|-------|-----------------|-------|-------|-----------------|--------|------|------|-------|
| | | | | | | | | | Min | Max | |
| 6.5 x 6.5 x 1 mm VFBGA | 16 | 332 | 1.5 | 13.0 (0.5/-0.2) | 20.2 | 50 | 16.4 (3.0/-0.2) | 19.1 | 16.4 | 19.1 | mm |

20.4 Moisture Sensitivity Level

CSR8675 BGA is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

21 Document References

| Document | Reference, Date |
|---|---|
| <i>BlueCore Audio API Specification</i> | CS-209064-DD |
| <i>BlueCore Bluetooth/IEEE 802.11 Coexistence Application Note</i> | CS-207808-AN |
| <i>BlueTest User Guide</i> | CS-102736-UG |
| <i>Bluetooth and USB Design Considerations</i> | CS-101412-AN |
| <i>Configuring the Power Supplies on CSR867x</i> | CS-204573-AN |
| <i>Configuring the Touch Sensor on CSR867x</i> | CS-204575-AN |
| <i>Core Specification of the Bluetooth System</i> | Bluetooth Specification Version 4.1, 03 December 2013 |
| <i>CSR8675 BGA Performance Specification</i> | CS-303731-SP |
| <i>CVC Two Microphone Headset Design Guidelines</i> | CS-218321-DC |
| <i>ESDA/JEDEC Joint Standard For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) - Component Level</i> | ANSI/ESDA/JEDEC JS-001-2011 |
| <i>Field-Induced Charged-Device Model Test Method for Electrostatic- Discharge-Withstand Thresholds of Microelectronic Components</i> | JESD22-C101E |
| <i>Firmware Configuration Keys for CSR8670</i> | CS-219481-AN |
| <i>IC Packing and Labelling Specification</i> | CS-112584-SP |
| <i>IEC 61000-4-2 Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test</i> | IEC 61000-4-2, Edition 2.0, 2008-12 |
| <i>Kalimba Architecture 5 DSP User Guide</i> | CS-318059-UG |
| <i>Lithium Polymer Battery Charger Calibration and Operation for CSR867x</i> | CS-204572-AN |
| <i>Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices</i> | IPC / JEDEC J-STD-020 |
| <i>Selection of I²C EEPROMS for Use with BlueCore</i> | bcore-an-008P |
| <i>Typical Solder Reflow Profile for Lead-free Device</i> | CS-116434-AN |
| <i>Universal Serial Bus Specification</i> | v2.0, 27 April 2000 |
| <i>USB Battery Charging Specification</i> | v1.1, 15 April 2009 |

Terms and Definitions

| Term | Definition |
|------------|--|
| 3G | 3 rd Generation of mobile communications technology |
| μ-law | Audio companding standard (G.711) |
| A-law | Audio companding standard (G.711) |
| A2DP | Advanced Audio Distribution Profile |
| AAC | Advanced Audio Coding |
| AC | Alternating Current |
| ACL | Asynchronous Connection-oriented |
| ADC | Analogue to Digital Converter |
| AES | Audio Engineering Society |
| AFC | Automatic Frequency Control |
| AFH | Adaptive Frequency Hopping |
| AGC | Automatic Gain Control |
| ALU | Arithmetic Logic Unit |
| AVRCP | Audio/Video Remote Control Profile |
| BCCMD | BlueCore CoMmanD |
| BCSP | BlueCore Serial Protocol |
| BEC | Bit Error Concealment |
| BIST | Built-In Self-Test |
| Bluetooth® | Set of technologies providing audio and data transfer over short-range radio connections |
| BMC | Burst Mode Controller |
| CDMA | Code Division Multiple Access |
| codec | Coder decoder |
| CRC | Cyclic Redundancy Check |
| CSR | Cambridge Silicon Radio |
| CVC | Clear Voice Capture |
| CVSD | Continuously Variable Slope Delta Modulation |
| DAC | Digital to Analogue Converter |
| DC | Direct Current |
| DDS | Direct Digital Synthesis |
| DFU | Device Firmware Upgrade |
| DMA | Direct Memory Access |

| Term | Definition |
|------------------|---|
| DNL | Differential Non Linearity (ADC accuracy parameter) |
| DSP | Digital Signal Processor (or Processing) |
| DUT | Device Under Test |
| e.g. | <i>exempli gratia</i> , for example |
| EBU | European Broadcasting Union |
| EDR | Enhanced Data Rate |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EIA | Electronic Industries Alliance |
| EMC | ElectroMagnetic Compatibility |
| EQ | EQualiser |
| eSCO | extended SCO |
| ESD | Electrostatic Discharge |
| ESR | Equivalent Series Resistance |
| etc | <i>et cetera</i> , and the rest, and so forth |
| FIR | Finite Impulse Response (filter) |
| FSK | Frequency Shift Keying |
| G.722 | An ITU-T standard wideband speech codec operating at 48, 56 and 64 kbps |
| GCI | General Circuit Interface |
| GSM | Global System for Mobile communications |
| H4DS | H4 Deep Sleep |
| HBM | Human Body Model |
| HCI | Host Controller Interface |
| HFP | Hands-Free Profile |
| HSP | HeadSet Profile |
| I ² C | Inter-Integrated Circuit Interface |
| I ² S | Inter-Integrated Circuit Sound |
| i.e. | <i>id est</i> , that is |
| I/O | Input/Output |
| IC | Integrated Circuit |
| ID | IDentifier |
| IEEE | Institute of Electronic and Electrical Engineers |
| IF | Intermediate Frequency |
| IIR | Infinite Impulse Response (filter) |

| Term | Definition |
|---------|---|
| INL | Integral Non-Linearity (ADC accuracy parameter) |
| IQ | In-Phase and Quadrature |
| ISDN | Integrated Services Digital Network |
| JEDEC | Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association) |
| Kalimba | An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression and file compression / decompression |
| Kb | Kilobit |
| LC | An inductor (L) and capacitor (C) network |
| LCD | Liquid-Crystal Display |
| LDO | Low (voltage) Drop-Out |
| LED | Light-Emitting Diode |
| LM | Link Manager |
| LNA | Low Noise Amplifier |
| LSB | Least Significant Bit (or Byte) |
| MAC | Multiplier and ACcumulator |
| MAP | Message Access Profile |
| Mb | Megabit |
| MCU | MicroController Unit |
| MEMS | Micro Electro Mechanical System |
| MIPS | Million Instructions Per Second |
| MISO | Master In Slave Out |
| MLC | MultiLayer Ceramic |
| MMU | Memory Management Unit |
| MP3 | MPEG-1 audio layer 3 |
| N/A | Not Applicable |
| NC | Not Connect |
| NSMD | Non-Solder Mask Defined |
| PA | Power Amplifier |
| PBAP | PhoneBook Access Profile |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PCM | Pulse Code Modulation |
| PD | Pull-down |
| PIO | Parallel Input/Output |

| Term | Definition |
|--------|---|
| PIO | Programmable Input/Output, also known as general purpose I/O |
| PLC | Packet Loss Concealment |
| plc | public limited company |
| ppm | parts per million |
| PS Key | Persistent Store Key |
| PU | Pull-Up |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| RC | A Resistor and Capacitor network |
| RCA | Radio Corporation of America, normally used to refer to a RCA connector (also known as phono connector or Cinch connector) |
| RF | Radio Frequency |
| RGB | Red Green Blue |
| RISC | Reduced Instruction Set Computer |
| RoHS | Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC) |
| RS-232 | Recommended Standard-232, a TIA/EIA standard for serial transmission between computers and peripheral devices (modem, mouse, etc.) |
| RSSI | Received Signal Strength Indication |
| RX | Receive or Receiver |
| SBC | Sub-Band Coding |
| SCO | Synchronous Connection-Oriented |
| SIG | (Bluetooth) Special Interest Group |
| SMPS | Switch-Mode Power Supply |
| SNR | Signal-to-Noise Ratio |
| SoC | System On-Chip |
| SPDIF | Sony/Philips Digital InterFace (also IEC 958 type II, part of IEC-60958). An interface designed to transfer stereo digital audio signals between various devices and stereo components with minimal loss. |
| SPI | Serial Peripheral Interface |
| SPP | Serial Port Profile |
| SQIF | Serial Quad I/O Flash (interface) |
| SRAM | Static Random Access Memory |
| TBD | To Be Defined |
| TCXO | Temperature Compensated crystal Oscillator |
| THD+N | Total Harmonic Distortion and Noise |

| Term | Definition |
|---------|--|
| TX | Transmit or Transmitter |
| UART | Universal Asynchronous Receiver Transmitter |
| Unity | Collective name for CSR's Bluetooth/Wi-Fi coexistence schemes |
| Unity+ | CSR's advanced coexistence scheme. Extra signalling wire used in conjunction with Unity-3 or Unity-3e for improved coexistence with periodic Bluetooth activity. |
| Unity-3 | De facto industry standard 3-wire coexistence signalling scheme |
| USB | Universal Serial Bus |
| VCO | Voltage Controlled Oscillator |
| VFBGA | Very thin, Fine pitch, Ball Grid Array |
| VM | Virtual Machine |
| W-CDMA | Wideband Code Division Multiple Access |
| WLAN | Wireless Local Area Network |
| WNR | Wind Noise Reduction |

Prepared for www.btspeaker.com - Thursday, December 04, 2014