I. MOUNIKA

Mobile No : +91-7396785465

E-mail : mounikaisampally.6@gmail.com

OBJECTIVE

To get a challenging career in a reputed organization that kindles my inner spirit and motivates my innovation by providing me with excellent opportunities.

ACADEMIC PROFILE

- **2015**-M. Tech (**Very Large Scale Integration**) from KSIT Engineering College, Hyderabad (affiliated to JNTUH University) with 84.10%
- **2013**-B.Tech (**Electronics and Communication**) from KSIT Engineering College, Hyderabad (affiliated to JNTUH university) with 80.90%
- **2009**-XII from NEW VISION Junior College, kukatapally, Board of Intermediate, with 80.00%.
- **2007**- X from VIVEKANANDA CONVENT HIGH SCHOOL, Bharath nagar colony (SSC State Board), with 70.01%.
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TECHNICAL SKILLS

- **Programming Languages** : C, C++,Verilog, System Verilog, Core Python, Basics of core Java
- **Web Technologies** : HTML, Cadence, Xilinx, Questa sim.
- **Operating System** : Windows Xp, Windows, Linux
- Testing tool : Manual and Automation in Selenium Tool,QTP.

INTERPERSONAL SKILLS

- Honest and hardworking
- Willingness to learn
- Good team player
- Good communication skills, Optimistic and positive attitude.

SOFTWARE TESTING SKILLS

Manual Testing

- Good Knowledge on Software Development life cycle(SDLC).
- Good Knowledge on Software Testing Life Cycle(STLC).
- Good writing Test Scenario,Test Cases,Defect Reports.
- Good Knowledge on Black box testing techniques and white box testing techniques.
- Good in Test Execution Process and Defect life cycle.
- Good Knowledge in various levels of testing topics like Smoke testing,Sanity testing,Retesting,Regression testing.

Automation Testing

- Have good exposure on Selenium IDE,Selenium WebDriver.
- Good knowledge on TestNG and Junit.
- Basic knowledge on Frameworks.

PROJECT DETAILS

Project Title : Scable Digital CMOS Comparator Using Parallel prefix tree

- **Role** : Team member
- **Description** : The Main Aim Of This Project Is To Reduce Dynamic Power Dissipation By Eliminating Unnecessary Transitions In A Parallel Prefix Structure That Generates The N-Bit Comparison Result After Cmos Gate Delays.

ACHIEVEMENTS

- Certificate Of Academic Excellence In Graduation
- VLSI design and verification course, UTL technologies ltd, Bangalore.

PERSONAL INFORMATION

- **Father name** : I.Vigneshwar rao
- **Date of Birth** : 29-12-1991
- **Gender** : Female.
- **Languages** : English, Telugu, Hindi.

DECLARATION

I do here by declare that the particulars of information and facts stated here in above are true, correct and complete to the best of my knowledge and belief.

Place :
Date : **[I. Mounika]**