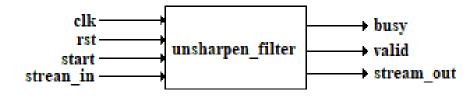
## Introduction

**Unsharpen Mask (USM)** 

$$kernel = \begin{bmatrix} 0 & -1 & 0 \\ -1 & 5 & -1 \\ 0 & -1 & 0 \end{bmatrix}$$

for more information about unsharpen filter go to Wikipedia

### **Block Diagram**



Signal Name	Description
clk	Clock signal
rst	Asynchronous Reset Signal
start	Before putting Image's Data on stream_in bus, the start signal must be asserted
	for one clock pulse, figure 1.
stream_in	Data Input Bus, put image's data on this bus one by one.
busy	When start signal is asserted at the next rising edge of clk, busy signal is asserted
	until the last pixel of processed image comes out, figure 1 and figure 2.
valid	When valid signal is asserted, you must read the stream_out' Data.
stream_out	Data Output Bus, read processed image's data at this bus one by one.

# Send Data to the Module (using stream\_in)

To send Raw Image to the Module, the input signals must be like figure 1.

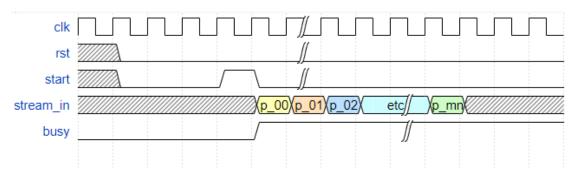


Figure 1 - input signals wave to send data to the module

in figure 1, p\_00 and p\_mn are the top left pixel and bottom right pixel of raw image respectively, assume the size of column is m+1 and size of row is n+1.

# **Read Data from the Module (using stream\_out)**

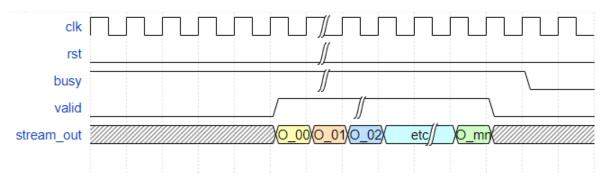


Figure 2 - output signals wave to read data from the module

in figure 1, O\_00 and O\_mn are the top left pixel and bottom right pixel of processed image respectively, assume the size of column is m+1 and size of row is n+1.

#### **Module Parameters**

row: Number of Row in the Raw Image

col: Number of Column in the Raw Image

wid: stream\_in and stream\_out bus width (Number of bits in the Raw Image's Pixel)