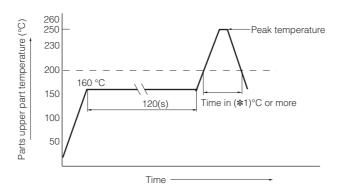
Recommendable reflow soldering

RoHS compliant



Lead-Free reflow

Reflow No.	Fig. (1)	Fig. (2)	Fig. (3)	Fig. (4)	
Category	φ4 to φ6.3	<i>φ</i> 8 to <i>φ</i> 10	ϕ 12.5 to ϕ 18	EB series (<i>φ</i> 10 to <i>φ</i> 18)	
Peak temperature	250 °C	235 °C	230 °C (220 °C)	230 °C	
Time in peak temperature	5 s	5 s	5 s (5 s)	5 s	
Time in (*1) °C or more	≥200 °C 60 s	≥200 °C 60 s	≥200 °C 20 s (30 s)	≥200 °C 20 s	
Time of reflow	1 time	1 time	1 time	1 time	

High tem	perature	Lead-F	ree ref	low

Reflow No.	Fig. (5)	Fig.	(6)	Fig.	(7)	Fig. (8)		
Category	φ4 to φ6.3	<i>φ</i> 8 to	φ10	<i>φ</i> 8 to	φ10	ϕ 6.3 to ϕ 10 (TK · TP series)		
Peak temperature	260 °C (255 °C)	245 °C	260 °C	250 °C	260 °C	255 °C	260 °C	
Time in peak temperature	≥250 °C 5 s (10 s)	≥240 °C 10 s	≥250 °C 5 s	≥240 °C 10 s	≥250 °C 5 s	≥250 °C 30 s	≥250 °C 20 s	
	≥230 °C 30 s	≥230 °C 30 s	≥230 °C 30 s	≥230 °C 30 s	≥230 °C 30 s	≥230 °C 40 s	≥230 °C 30 s	
Time in (*1) °C or more	≧217 °C 40 s	≧217 °C 40 s	≥217 °C 40 s	≧217 °C 40 s	≥217 °C 40 s	≥217 °C 65 s	≥217 °C 65 s	
	≥200 °C 70 s	≥200 °C 70 s	≥200 °C 70 s	≥200 °C 70 s	≥200 °C 70 s	≥200 °C 90 s	≥200 °C 70 s	
Time of reflow	2 times	2 times	1 time	2 times	1 time	2 times	2 times	

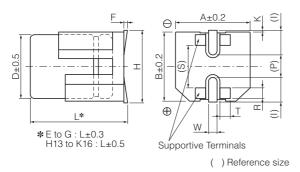
Reflow No.	Fig. (9)	Fig. (10)	Fig. (11)		
Category	ϕ 12.5 to ϕ 18 (FK, TK, HD series)	φ12.5 to φ18 (FK series) 50 V.DC to 63 V.DC	φ12.5 to φ18 (FK series) 80 V.DC to 100 V.DC		
	6.3 V.DC to 35 V.DC	(TK series) 50 V.DC	(TK series) 63 V.DC to 100 V.DC		
Peak temperature	245 °C	245 °C	245 °C		
Time in peak temperature	≥240 °C 30 s	≥240 °C 5 s	≥240 °C 5 s		
Time in (*1) °C or more	≥217 °C 90 s	≧217 °C 30 s	≧217 °C 30 s		
Time of reflow	2 times	2 times	1 time		

 $[\]boldsymbol{\ast}$ For reflow, use a thermal condition system such as infrared radiation (IR) or hot blast.

^{*} Panasonic have several series available for pure Tin terminal and ZVEI reflow based on J-STD-020D (JEDEC). (Please contact sales for details.)

Dimensions (Vibration-proof products)

* The size and shape are different from standard products. Please inquire details of our company.

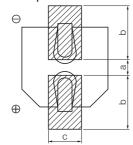


(Gilli													
	Size code	φD	L	А, В	H max.	F	I	W	Р	К	R	S	Т
	Е	8.0	6.5	8.3	9.5	0 to +0.15	3.4	0.7±0.1	2.2	0.35+0.15	0.70±0.2	5.3±0.2	1.7±0.2
	F	8.0	10.5	8.3	10.0	0 to +0.15	3.4	1.2±0.2	3.1	0.70±0.2	0.70±0.2	5.3±0.2	1.3±0.2
	G	10.0	10.5	10.3	12.0	0 to +0.15	3.5	1.2±0.2	4.6	0.70±0.2	0.70±0.2	6.9±0.2	1.3±0.2
	H13	12.5	13.8	13.5	15.0	-0.1 to +0.15	4.7	1.2±0.2	4.4	0.70±0.3	2.2±0.2	7.1±0.2	2.4±0.2
	J16	16.0	16.8	17.0	19.0	-0.1 to +0.15	5.5	1.4±0.2	6.7	0.70±0.3	3.0±0.2	9.0±0.2	1.9±0.2
	K16	18.0	16.8	19.0	21.0	-0.1 to +0.15	6.7	1.4±0.2	6.7	0.70±0.3	3.0±0.2	11.0±0.2	1.9±0.2

Land/Pad pattern

The circuit board land/pad pattern size for chip capacitors is specified in the following table. The land pitch influences installation strength and consider it.

Standard products



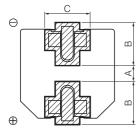


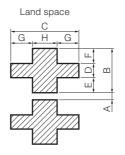
[Table of board land size vs. capacitor size]

	-	(OHIL : HIIII)
а	b	С
1.0	2.5	1.6
1.5	2.8	1.6
1.8	3.2	1.6
2.2	4.0	1.6
3.1	4.0	2.0
4.6	4.1	2.0
4.0	5.7	2.0
6.0	6.5	2.5
6.0	7.5	2.5
	1.0 1.5 1.8 2.2 3.1 4.6 4.0 6.0	1.0 2.5 1.5 2.8 1.8 3.2 2.2 4.0 3.1 4.0 4.6 4.1 4.0 5.7 6.0 6.5

(Unit · mm)

Vibration-proof products



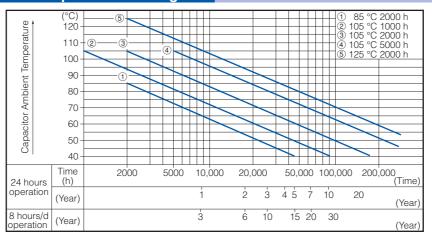


[Table of board land size vs. capacitor size]

							(Offit	. !!!!!!
Size code (Dimensions)	Α	В	С	D	Е	F	G	Н
$E (\phi 8 \times 6.5L)$	1.8	4.2	5.0	1.3	1.5	1.4	1.5	2.0
$F(\phi 8 \times 10.5L)$	2.7	4.0	4.7	1.3	1.0	1.7	1.1	2.5
G (\$\phi\$10)	3.9	4.4	4.7	1.3	1.2	1.9	1.1	2.5
H (ϕ 12.5)	3.9	6.0	6.9	2.8	1.3	1.9	2.2	2.5
J (<i>φ</i> 16)	5.8	6.8	6.2	3.6	1.3	1.9	1.7	2.8
K (<i>ϕ</i> 18)	5.8	7.3	6.2	3.6	1.8	1.9	1.7	2.8

^{*} When size "A" is wide, back fillet can be made, decreasing fitting strength.

Expected life estimate quick reference guide



^{*} When size "a" is wide, back fillet can be made, decreasing fitting strength.

^{*} Take mounting conditions, solderability and fitting strength into consideration when selecting parts for your company's design.