System Design: XOR Logic Circuit and HDL Description of Half Adder

System Design Overview

A **system** is a collection of components that are connected to form a coherent entity with a specific function or purpose.

Example: A computer or a logic circuit.

The system's overall function is defined by:

- The functions of its individual components.
- The way these components are interconnected.

System Representation

We represent a system using a **directed graph** $G = (V, E)$, where:

- $V = \{v_1, v_2, \ldots, v_n\}$ are vertices or nodes (components).
- $E = \{(v_i, v_j)\}$ are directed edges (signal flow from one component to another).

Structure vs. Behavior

Structure: Describes how the system is physically arranged — the block diagram showing components and interconnections.

Behavior: Describes what the system *does* for given inputs — the logic function or truth table.

XOR Gate Behavior

The behavior of the XOR function $f(x_1, x_2)$ is defined as:

$$f(x_1, x_2) = x_1 \oplus x_2$$

Truth Table

x_1	x_2	$f(x_1, x_2)$
0	0	0
0	1	1
1	0	1
1	1	0

Block Diagram of XOR Circuit

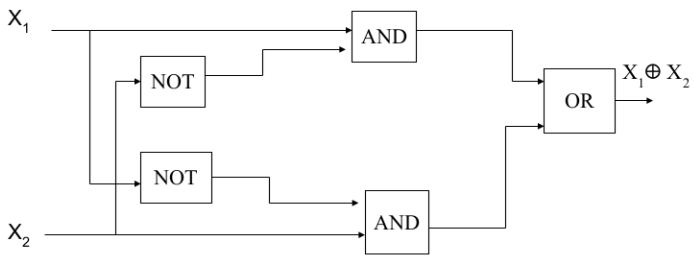

Figure 1: Block Diagram of XOR Logic Circuit

Hardware Description Language (HDL)

Hardware Description Language (HDL) is a programming-like language used to describe the structure and behavior of digital circuits. HDL is used for:

- Precise and technology-independent hardware design.
- Circuit documentation.
- Simulation and synthesis using CAD tools.

HDL resembles high-level programming languages like `C` and `Ada` but is used to describe hardware instead of software.

Half Adder Circuit Using VHDL

A **Half Adder** is a combinational circuit that computes the sum and carry of two binary digits.

- `sum` $= x \oplus y$
- `carry` $= x \cdot y$

VHDL Code for Half Adder

```
entity half_adder is
    port (x, y: in bit; sum, carry: out bit);
end half_adder;

architecture behavior of half_adder is
begin
    sum <= x xor y;
    carry <= x and y;
end behavior;
```

Listing 1: VHDL code for Half Adder

Explanation

- `entity`: Defines the interface of the half adder with inputs and outputs.
- `architecture`: Specifies the internal behavior of the circuit.
- `xor`, `and`: Logical operations used to compute `sum` and `carry`.

Advantages of HDL

1. Technology-independent design specification.
2. Suitable for multiple levels of abstraction (gate, RTL).
3. Facilitates simulation and automatic synthesis.
4. Enhances design documentation and reuse.