Core CPU Operations

1 Instruction Cycle: Core CPU Operations

1. Fetch

- The Control Unit (CU) fetches the instruction from memory (RAM or cache).
- The Program Counter (PC) holds the address of the next instruction to be fetched.

2. Decode

- The Instruction Decoder interprets the fetched instruction.
- It determines the operation to be performed and the operands required.

3. Execute

- The ALU (Arithmetic Logic Unit) or FPU (Floating Point Unit) performs the operation (e.g., add, subtract, AND, OR).
- This may involve accessing registers or memory.

4. Memory Access (if needed)

- If the instruction requires data fetch or storage, the memory is accessed accordingly.

5. Write-back

- The result of the operation is written back to a register or memory location.

2 CPU Components Involved

Component	**Role**
Program Counter (PC)	Holds the address of the next instruction to execute.
Instruction Register (IR)	Holds the currently fetched instruction.
Control Unit (CU)	Directs operations of the CPU components.
ALU	Performs arithmetic and logical operations.
Registers	Fast, local data storage within the CPU.
Bus Interface	Connects the CPU to memory and I/O subsystems.

Table 1: Key CPU Components and Their Roles

3 Instruction Cycle: Continuous Repetition

The CPU continually repeats the **fetch-decode-execute** cycle at high speed, often millions or billions of times per second. This repetition is governed by the system clock.

4 Example Instruction: `ADD R1, R2, R3`

- **Fetch:** The instruction is fetched from memory.
- **Decode:** The CPU determines it needs to add contents of registers R2 and R3.
- **Execute:** The ALU performs the addition.
- **Write-back:** The result is stored in register R1.