Combinational Array Multiplier: Detailed Notes

1. Introduction

A **combinational array multiplier** is a digital circuit that performs binary multiplication using a structured array of **AND gates**, **half adders (HA)**, and **full adders (FA)**. The circuit is **combinational** in nature, meaning that its output depends only on the current inputs, with no memory or clocking involved.

2. Binary Multiplication Basics

Let the two n-bit binary numbers be:

$$A = a_{n-1}a_{n-2}\ldots a_1a_0, \quad B = b_{n-1}b_{n-2}\ldots b_1b_0$$

Then,

$$A = \sum_{i=0}^{n-1} a_i \cdot 2^i, \quad B = \sum_{j=0}^{n-1} b_j \cdot 2^j$$

The binary multiplication of A and B is defined as:

$$P = A \cdot B = \sum_{j=0}^{n-1} \left(b_j \cdot A \cdot 2^j\right)$$

3. Array Multiplier Logic

Each bit of the multiplier B is ANDed with every bit of the multiplicand A, generating a row of **partial products**. These partial products are shifted according to their bit position and summed using an array of adders.

Mathematical Representation:

$$P = \sum_{j=0}^{n-1} \left(\sum_{i=0}^{n-1} (a_i \cdot b_j \cdot 2^{i+j}) \right)$$

Here,

- a_i: i^{th} bit of multiplicand
- b_j: j^{th} bit of multiplier

- $a_i \cdot b_j$: Individual partial product
- 2^{i+j}: Weight of each partial product in the final result

4. 2-bit $\times$ 2-bit Example

Let:

$$A = a_1 a_0, \quad B = b_1 b_0$$

The multiplication involves:

Partial Products:

$$PP_0 = a_0 b_0 \cdot 2^0$$
$$PP_1 = a_1 b_0 \cdot 2^1$$
$$PP_2 = a_0 b_1 \cdot 2^1$$
$$PP_3 = a_1 b_1 \cdot 2^2$$

Final Product:

$$P = PP_0 + PP_1 + PP_2 + PP_3$$

Result: 4-bit output: $P = p_3 p_2 p_1 p_0$

5. Hardware Structure

The structure consists of:

- **AND gates** to generate each $a_i \cdot b_j$
- **Full Adders** and **Half Adders** to sum the shifted partial products
- Regular, grid-like array architecture

6. Characteristics

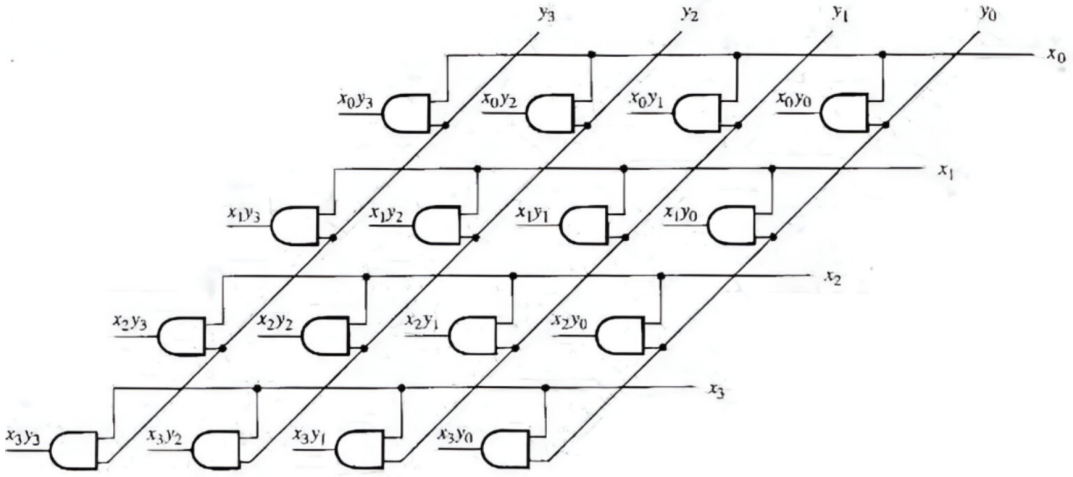
- **Speed:** Faster for small inputs, delay grows with n
- **Hardware Cost:** Grows quadratically with bit-width
- **Scalability:** Easily extendable to larger bit-widths

7. Applications

- Digital Signal Processors (DSP)
- Arithmetic Logic Units (ALU)
- Embedded Systems

8. Array Multiplication

AND Array for 4 X 4 bit Unsigned Multiplication



Full Adder Array for 4 X 4 bit Unsigned Multiplication