

CSE-3103: Microprocessor and Microcontroller

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Memory Segmentation of 8086

Base address of segment →
= segment address $\times 10\text{H}$,
segment starting address.
00000H, 00010H or 00020H, etc.

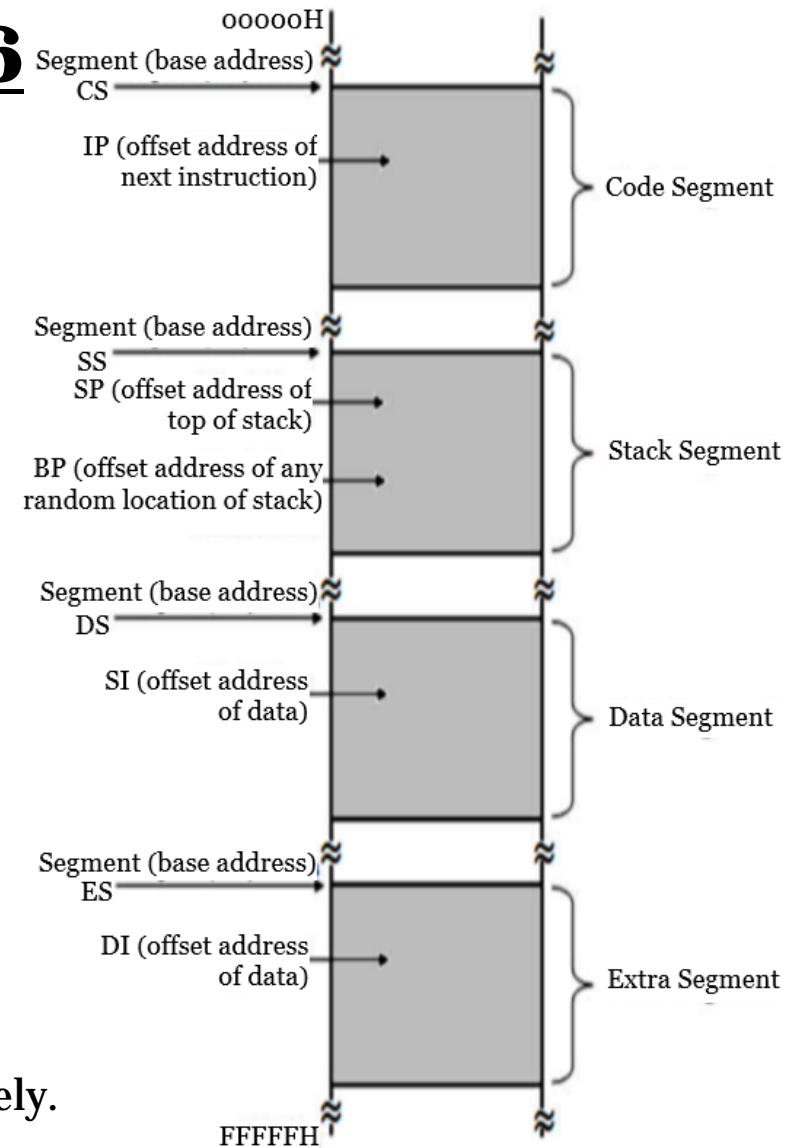
Offset address range = 0000H to FFFFH [$2^{16} = 64\text{ kB}$]

Advantages of memory segmentation →
address bus = 20 bits,
segmentation allows to work with 16-bit registers.

> 1 code, data, extra, stack segment can be used.
code, data, stack, extra segment > 64 kB long.

time-shared multitasking environment →
moves over from one user's program to another =
CPU reload four segment registers.

user's program (code) and data can be stored separately.



Logical Address, Base Segment Address and Physical Address

Segment address →

16-bit, reside in segment registers (CS, DS, ES, SS).

Base address →

20-bit, Segment address $\times 10H$

Offset address →

= Effective address,

16-bit, reside in IP, BP, SP, BX, SI, DI.

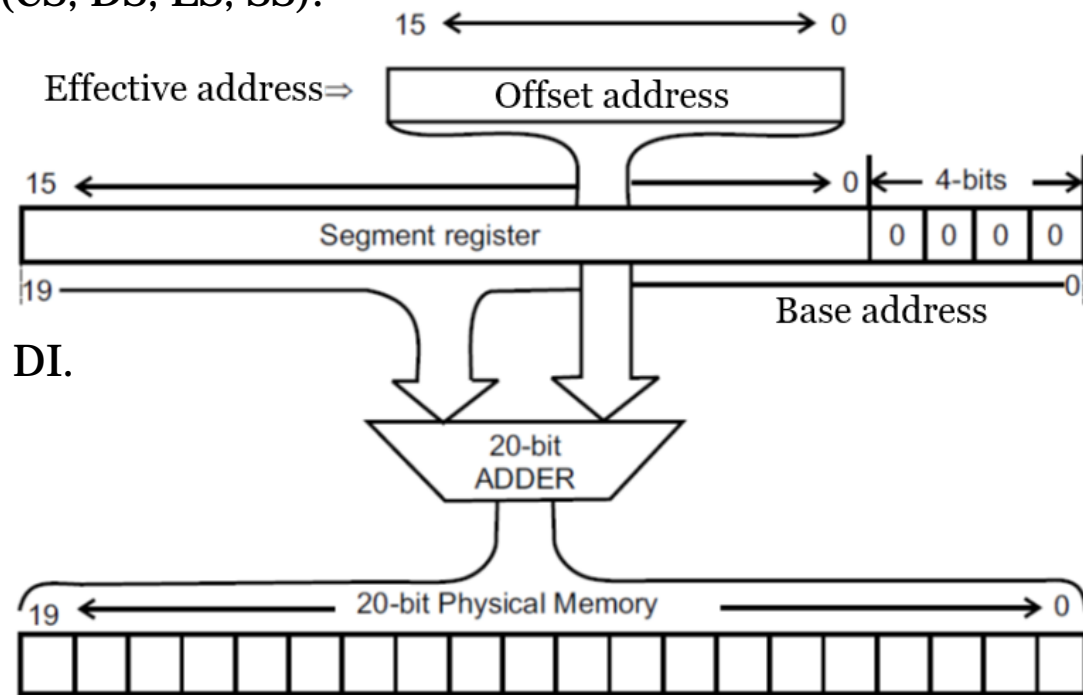
Logical address →

Segment : Offset = DS : 1234H

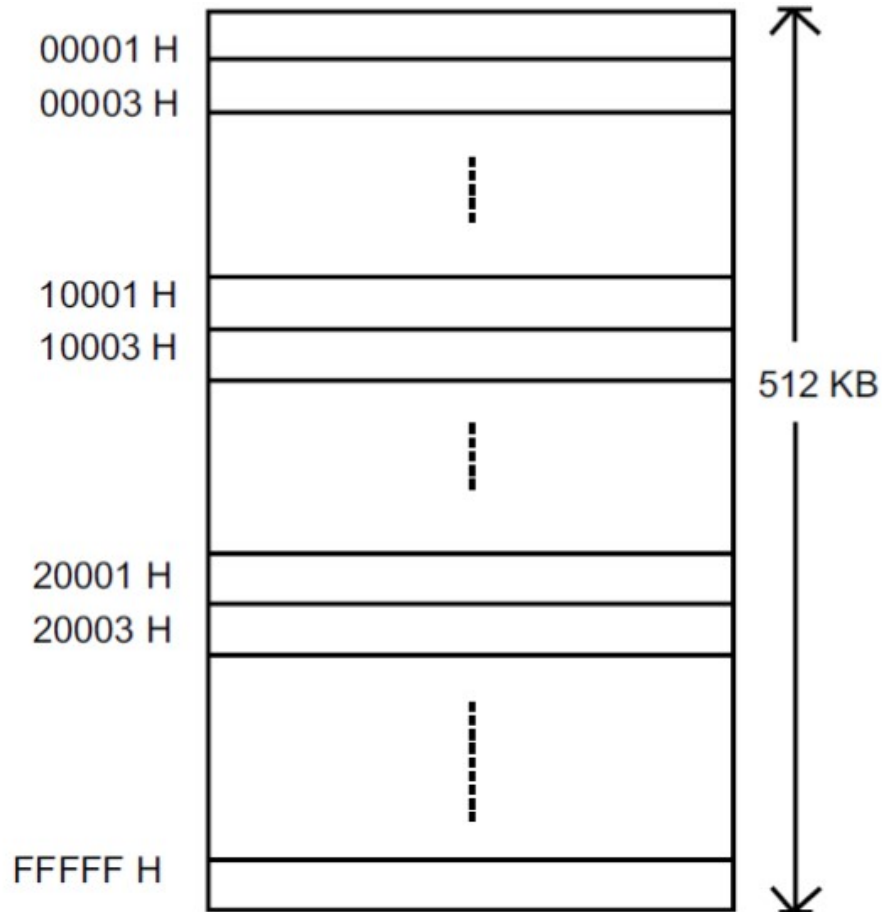
Physical address →

= Real address,

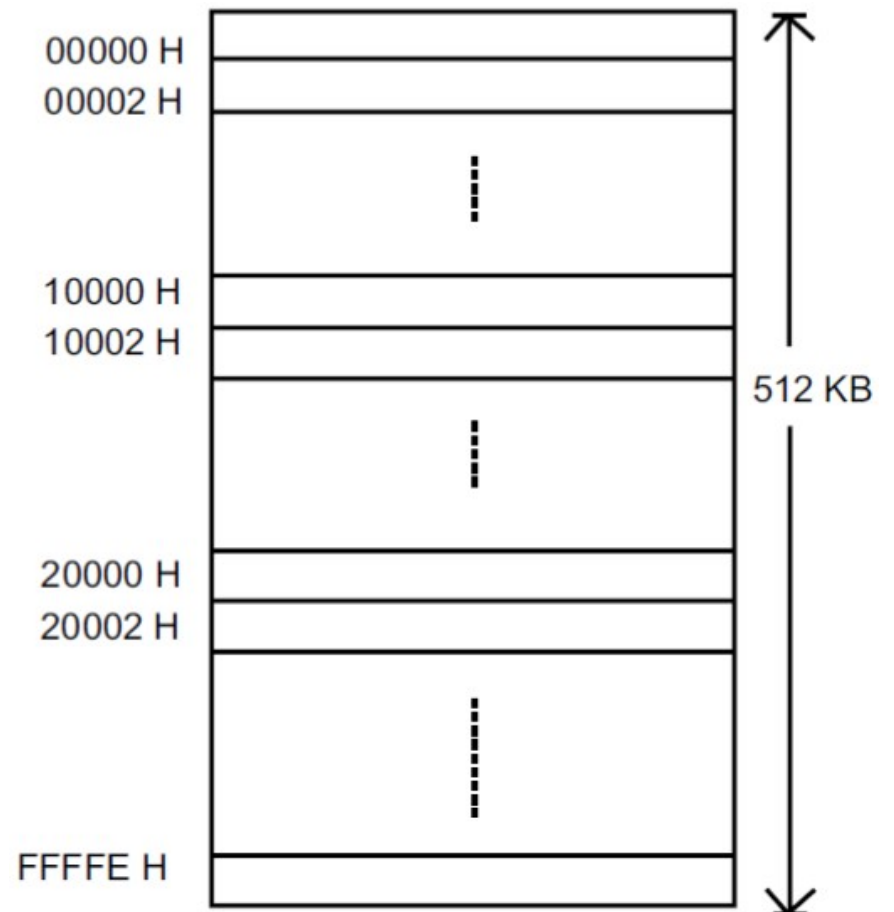
= Segment address $\times 10H$ + Offset address



Memory Organization

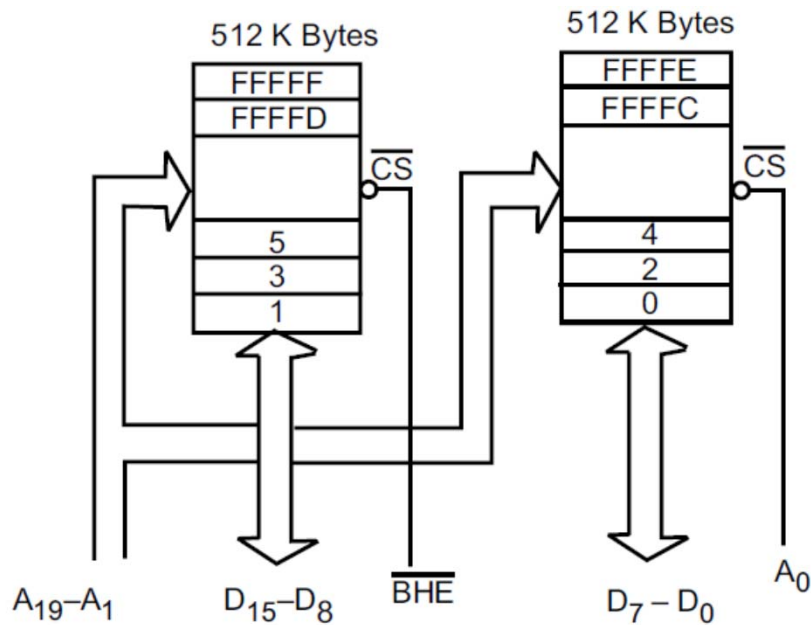


High bank (Odd bank) $\overline{BHE} = 0, A_0 = 1$

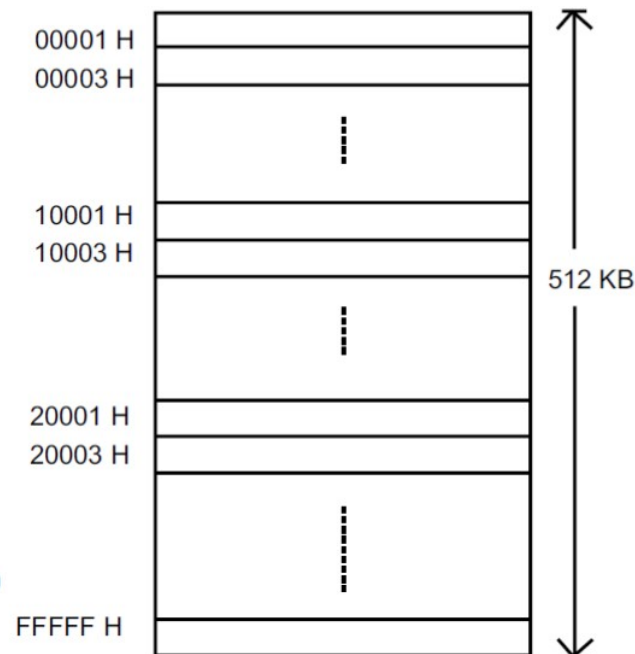


Low bank (Even bank) $\overline{BHE} = 1, A_0 = 0$

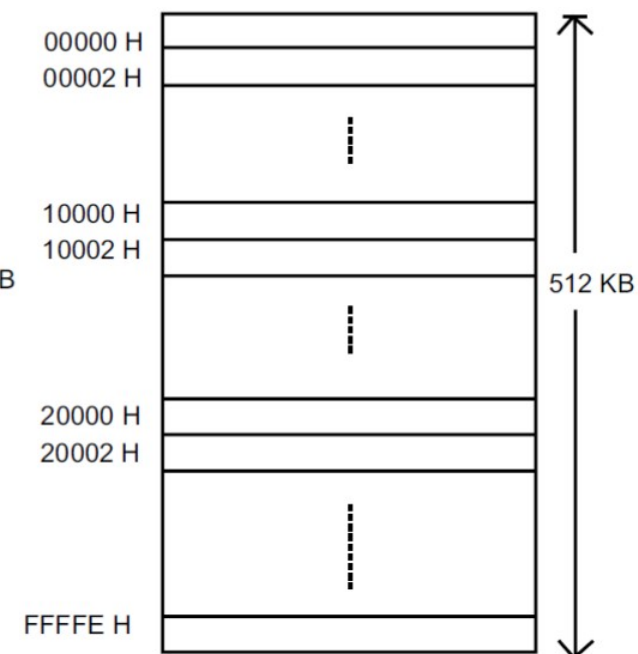
Memory Organization



$\overline{\text{BHE}}$	A_0	Word/byte access
0	0	Both banks active
0	1	Only high bank active
1	0	Only low bank active
1	1	No bank active



High bank (Odd bank) $\overline{\text{BHE}} = 0, A_0 = 1$

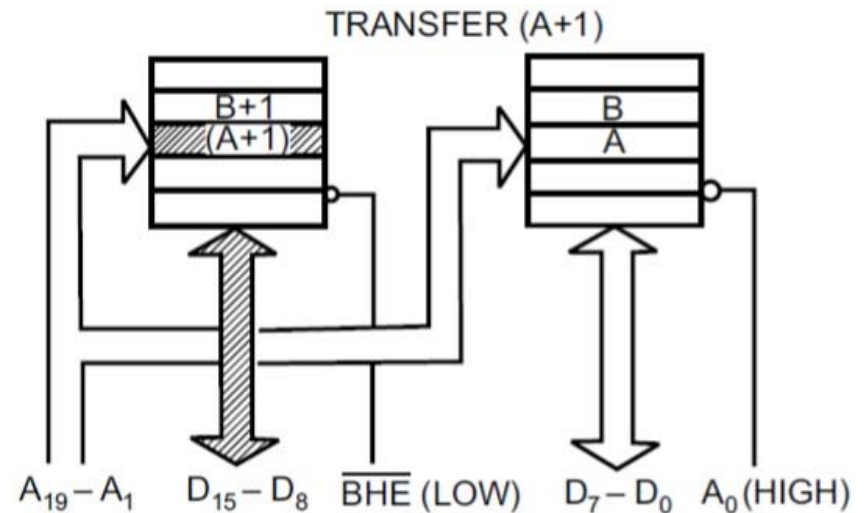
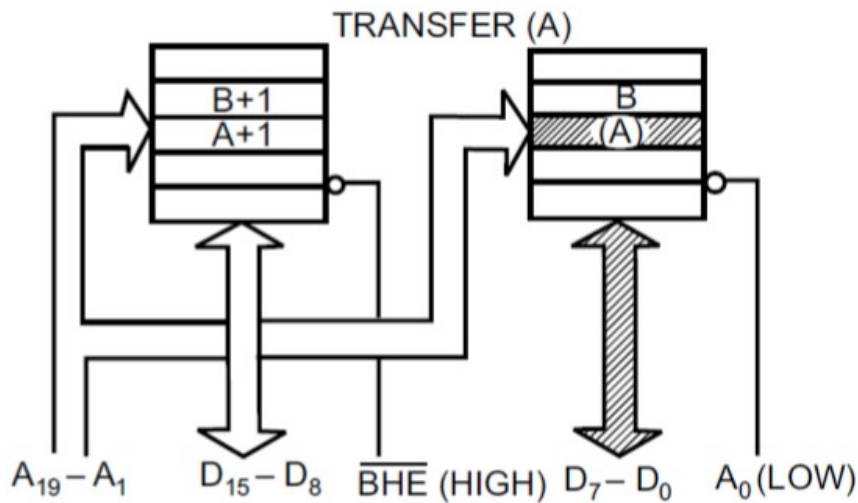


Low bank (Even bank) $\overline{\text{BHE}} = 1, A_0 = 0$

Byte and Word Transfer by 8086

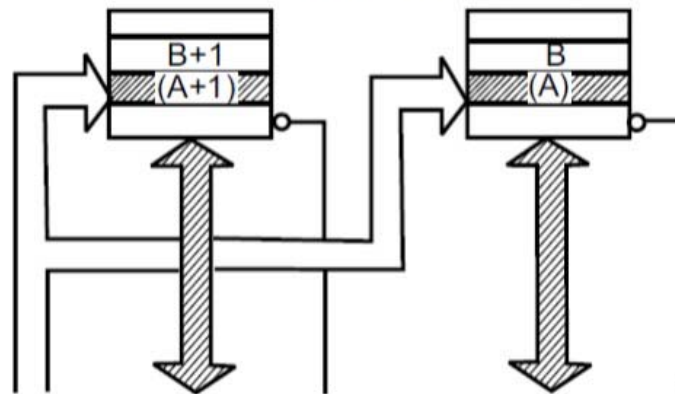
- (a) even-addressed byte transfer,
- (b) odd-addressed byte transfer,
- (c) even-addressed word transfer,
- (d) odd-addressed word transfer.

$\overline{\text{BHE}}$	A_0	Word/byte access
0	0	Both banks active
0	1	Only high bank active
1	0	Only low bank active
1	1	No bank active



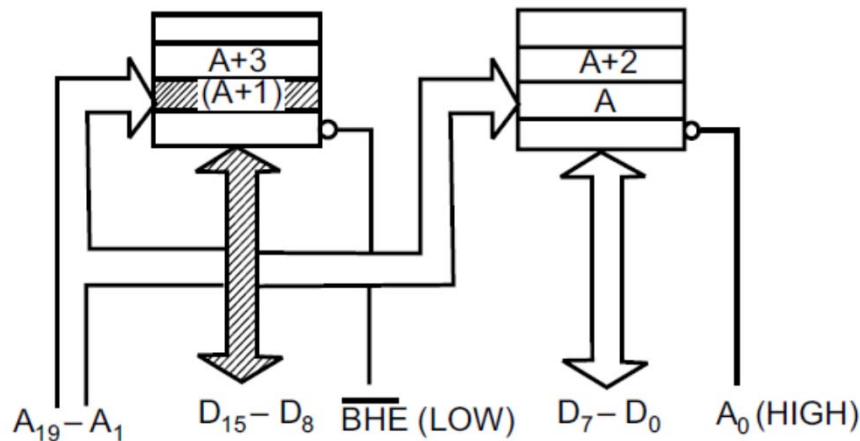
Byte and Word Transfer by 8086

TRANSFER (A+1), (A)

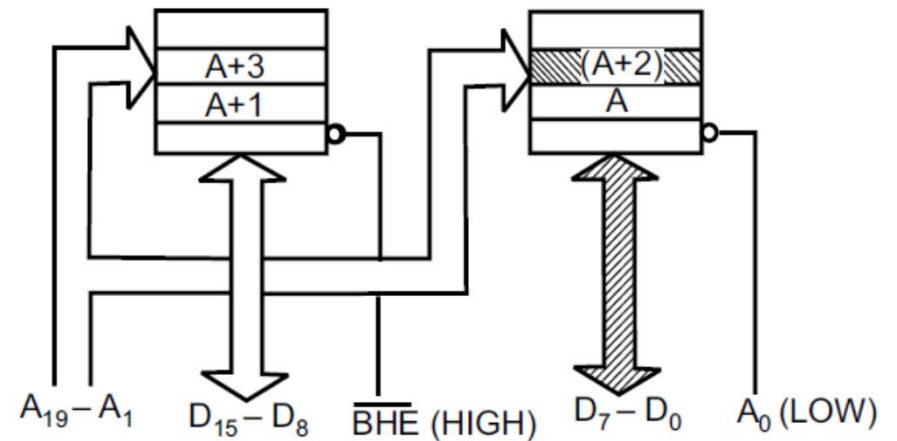


$\overline{\text{BHE}}$	A_0	Word/byte access
0	0	Both banks active
0	1	Only high bank active
1	0	Only low bank active
1	1	No bank active

$A_{19}-A_1$ $D_{15}-D_8$ $\overline{\text{BHE}}$ (LOW) D_7-D_0 A_0 (LOW)
FIRST BUS CYCLE



SECOND BUS CYCLE



Addressing Modes

Instruction = opcode + operand.

Operand may reside in

- (i) accumulator or
- (ii) general purpose register or
- (ii) memory location.

Addressing mode = manner in which operand is specified in instruction.

Different addressing modes of 8086 →

- (i) Immediate operand addressing.
- (ii) Register operand addressing.
- (iii) Memory operand addressing.

Different memory addressing modes →

- (i) Direct Addressing,
- (ii) Register Indirect Addressing,
- (iii) Based Addressing,
- (iv) Indexed Addressing,
- (v) Based Indexed Addressing,
- (vi) Relative Based Indexed Addressing.