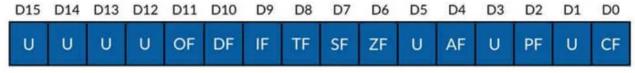
CSE-3103: Microprocessor and Microcontroller

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U - Unused

Conditional Flags

CF - Carry Flag

PF - Parity Flag

AF - Auxiliary Carry Flag

ZF - Zero Flag

SF - Sign Flag

OF - Overflow Flag

Control Flags

DF - Direction Flag

IF - Interrupt Flag

TF - Trap (Trace) Flag

Status Registers →

Flag register or Program Status Word (PSW) \rightarrow

16-bit register.

7 bits remain unused,

9 are used.

9 flags \rightarrow

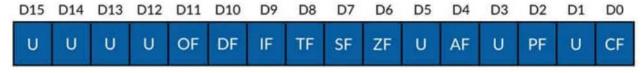
6 condition flags + 3 control flags.

control flags = TF, IF, DF.

condition flags = OF, SF, ZF, AF, PF, CF.

$$CF = 1 \rightarrow$$

addition = carry out of MSB position, subtraction = borrow is needed out of MSB position.



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Status Registers →

$$PF = 1 \rightarrow$$

lower 8-bits of result = even number of 1's.

 $AF = 1 \rightarrow$

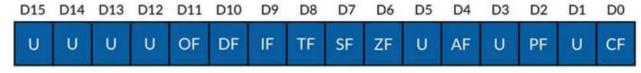
addition = carry out of bit 3, subtraction = borrow required from bit 4 into bit 3.

 $ZF = 1 \rightarrow$

arithmetic or logical operation = zero.

 $SF = 1 \rightarrow$

MSB of result of operation is 1. used for unsigned numbers.



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Status Registers →

 $OF = 1 \rightarrow$

result is too large = doesn't fit in destination. used for signed arithmetic operation.

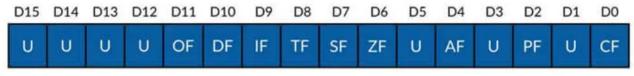
Control Flags →

set/reset by programmer.

 $TF = 1 \rightarrow$

processor operates in single stepping mode.
 interrupt is recognized, TF flag is cleared.
 CPU runs ISS (interrupt service subroutine).
 IRET →

CPU returns to main program from ISS, TF flag status is restored.



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Control Flags →

 $TF = set/reset \rightarrow$

push flag register on stack, change TF as desired,

pop flag register from stack.

$$IF = 1 \rightarrow$$

maskable interrupt INTR is enabled. interrupt is recognized, IF flag is cleared.

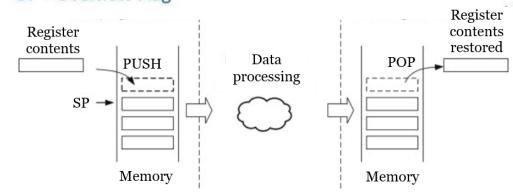
IRET in ISS \rightarrow

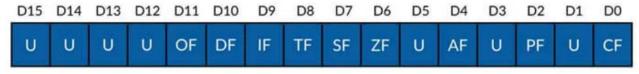
returns to main program, IF flag status is restored.

STI = IF set instruction,

CLI = IF clear instruction.

8086 is reset \rightarrow IF is cleared.





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Control Flags → DF →

DF - Direction Flag

IF - Interrupt Flag

Control Flags

TF - Trap (Trace) Flag

used in string operations.

STD = DF set instruction,

CLD = DF clear instruction.

$$DF = 1 \rightarrow$$

DI and SI are automatically decremented, access string from highest memory location

down to lowest memory location.

Pointers and Index Group of Registers:

SP and BP = pointer registers.

SI and DI = index registers.

All $4 \rightarrow 16$ -bit registers.

store offset addresses of memory locations.

$$SI = 2000H$$
,
 $MOV AH$, $[SI] \rightarrow$
 $AH \leftarrow FFH$
 $[SI+1:SI] = ABFFH$

SI, DI in string instructions \rightarrow

 $SI \rightarrow$ source index register, source address = $DS \times 10 + SI$

DI → destination index register, destination address = ES×10 + DI

2005H	0A	
2004H	07	
2003H	85	
2002H	90	
2001H	AB	
2000H	FF	← SI

Pointers and Index Group of Registers:

- SP → stack pointer.

 contains offset address or stack top address.

 stack address = [SS]×10 + [SP]
- BP → base pointer.

 used to access data area in stack segment.

 stack address = [SS]×10 + [BP]
- SP = 9F20H
 SS = 4000H

 Top of stack 49F20H
 Start of stack segment 40000H

End of stack segment 4FFFFH

- IP → instruction pointer.
 contains offset address of next instruction to be fetched.
 cannot be programmed by programmer.
- SI, DI, BP → also used as general purpose registers.