CPU Registers: 8086, 32-bit, and 64-bit Architectures

Overview

Registers are **fast storage units** inside the CPU that allow quick access to data and instructions. We will cover:

- 8086 (16-bit) Registers
- 32-bit General Purpose Registers (x86)
- 64-bit General Purpose Registers (x86-64)
- Segment, Pointer/Index, and Flag Registers

1. 8086 (16-bit) Registers

General Purpose Registers

General Purpose Registers (16-bit)

- AX (Accumulator) Arithmetic, logic, I/O
- BX (Base) Base pointer for memory access
- CX (Count) Loop counter / string operations
- DX (Data) I/O operations, multiply/divide

Each can be split into high/low bytes:

$$AX \to AH \mid AL$$
, $BX \to BH \mid BL$, $CX \to CH \mid CL$, $DX \to DH \mid DL$

$$AX = AH \mid AL$$

$$BX = BH \mid BL$$

$$CX = CH \mid CL$$

$$DX = DH \mid DL$$

Segment Registers

Segment Registers

- CS Code Segment
- DS Data Segment
- SS Stack Segment
- ES Extra Segment

Physical Address:

Physical Address = $(Segment \times 16) + Offset$

Pointer and Index Registers

Pointer / Index Registers

- SP Stack Pointer
- BP Base Pointer
- SI Source Index
- DI Destination Index
- IP Instruction Pointer (points to next instruction)

Flag Register

Flag Register

- 16-bit register to indicate CPU status
- Condition Flags: CF, PF, AF, ZF, SF, OF
- Control Flags: TF, IF, DF, etc.

2. 32-bit General Purpose Registers (x86)

32-bit GPRs

- EAX, EBX, ECX, EDX extended versions of AX, BX, CX, DX
- ESI, EDI extended SI and DI
- ESP, EBP extended stack pointer and base pointer

EAX
EBX
ECX
EDX
ESI
EDI
ESP
EBP

3. 64-bit General Purpose Registers (x86-64)

64-bit GPRs

- RAX, RBX, RCX, RDX extended EAX, EBX, ECX, EDX
- RSI, RDI extended ESI, EDI
- RSP, RBP extended ESP, EBP
- R8 R15 additional 64-bit general-purpose registers

RAX
RBX
RCX
RDX
RSI
RDI
RSP
RBP
R8
R9
R10
R11
R12
R13
R14
R15

Summary

- 8086 registers 16-bit, segmented, for memory, stack, and flags
- 32-bit x86 EAX, EBX, ECX, EDX, ESI, EDI, ESP, EBP
- 64-bit x86-64 RAX–R15, extended pointers and data registers
- All architectures have dedicated flag registers for status and control