206 Quiz - July 2021

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The characteristic table of **AB flip-flop** is given below. If you are given a JK flip-flop to implement AB flip-flop, minimum how many additional basic gates will you have to use?

A	B	Q(t+1)
0	0	1
0	1	Q'(t)
1	0	Q(t)
1	1	0

- 2
- 3
- 1
- 4

If you want to implement a function f(A,B,C,D)=∑(0,1,4,6,7,8,10,12,14,15) using basic gates and a single 4-to-1 MUX with C & D as selector bits, then what would be equation for the input I_1 (i.e., the input line that would be selected when CD=01)?

- 1
- Correct answer not given
- AB
- ~A
- ~(A+B)

What is the minimum number of flipflops necessary to create a 4-bit Register that only holds the following states: 1, 3, 4, 8, 12 ?

- 4
- 2
- 3
- 5

If y'=(a (bcd) 'e)', for y=1 the value of a, b, c, d, e will be-

- a=b=c=d=e=0
- a=b=c=d=e=1
- a=e=1, b=c=d=0
- b=c=d=1, a=e=0

You are given an edge triggered flip-flop without any **direct reset** input. All the gates used to design this flip-flop are 2-input. You are asked to add a direct reset input for this flip-flop. Minimum how many additional basic gates can you use?

- 2
- 3
- 1
- 4

The number of enables in 74138 is--

- 4
- 3
- 1
- 2

Which of the following is called equivalence gate--

- Xnor
- Nand
- Xor
- Nor

Gray code is used in K-Map because _____

- ◯ None of the other options
- ◯ in a code, there is odd number of 1s.
- ◯ in two adjacent codes, there is change in three bits.
- ◯ in two adjacent codes, there is change in one bit.

State whether each of the below statements are True or False. Putting a tick mark to the True statements will suffice.

- ☐ There is a minimum time called the setup time during which the D input of a D Flip-flop must not change after the application of the positive/negative transition of the clock
- ☐ T flip-flop can be constructed from JK flip-flop without using any additional gates
- ☐ The output of a latch cannot be applied through a combinational logic to the input of another latch.
- ☐ The most economical flip-flop is the edge triggered D flip-flop.

The simplified equation for the given K-map is -

A_3A_2 \ A_1A_0	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

- Y = $A_2A_3' + A_3A_2'$
- Y = $A_1' A_2 + A_2' A_1$
- Y = $A_1'A_3 + A_3'A_1$
- Y = $A_1'A_0 + A_0'A_1$

What is the minimum number of basic gates required to build a 4-to-1 MUX? Assume, **2-input** gates.

- 13
- 7
- 9
- 5
- Correct answer not given

For 6 bit input, the maximum possible BCD value will be _____.

Your answer

f(x,y,z) = (x → y) → ~z , select the maxterms for POS of f(x ,y, z) from 0, 1, 2, 3, 4, 5, 6, 7 (Select the checkboxes that apply)

- [ ] 1
- [ ] 2
- [ ] 3
- [ ] 4
- [ ] 5
- [ ] 6
- [ ] 7
- [ ] 0

Which of the following statements is False?

- ○ You can simulate a mod 16 counter through a mod 8 counter and some combinatorial circuits.
- ○ It is possible to pause a Counter without pausing the clock.
- ○ All Counters are dependent on initial state.
- ○ It is possible to transform one counter to another if both has same number of states.

Which one of the following is correct?

- None of the options
- For proper operation of 7483, its C_in must not be left open
- 7483 is a low speed 4 bit adder
- For proper operation of 7483, its C_in can be left open

The number of enables and type of enables for each 4x1 multiplexer module in 74153 is

- 1, Active low
- 2, Active high
- 2, Active low
- 1, Active high

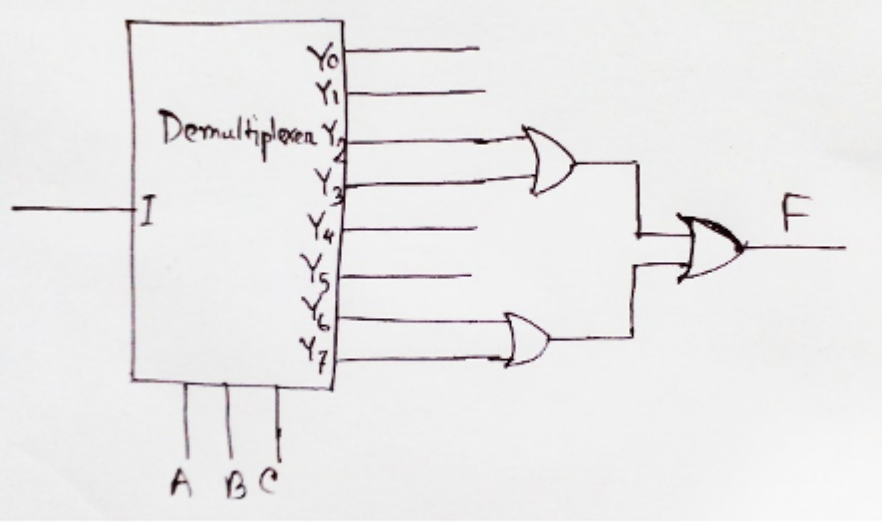
Which of the following statements is True?

- You can design a Universal Shift Register with asynchronous flipflops.
- You cannot simulate Left/Right Shift in a register that only supports Parallel Load.
- It is impossible to simulate a SIPO Register through a PIPO Register.
- It is possible to design a Shift Register that takes 2 clock cycles to shift left by 1 bit.

What is the minimum number of flipflops required to output the following sequence: 0,1,0,2,0,1,0,2,...?

- 4
- Impossible
- 3
- 2

For the following Demultiplexer, if the Input I=1, then what will be the functional form of F(A,B,C)? Note that gates used in the figure are 2-input OR gates.



- AB
- A'B
- BC
- B
- Correct answer not given

Which one of the following is correct for Logisim?

- The circuits implemented in Logisim require Vcc and Gnd connection for proper operation.
- The circuits implemented in Logisim do not require Vcc and Gnd connection for proper operation
- The circuits implemented in Logisim require only Gnd connection for proper operation
- The circuits implemented in Logisim require only Vcc connection for proper operation.

What are the minimum number of two input NOR gates to perform XOR operation?

- 7
- 5
- 6
- 4

The SOP form for the function f(A,B,C,D)= ∑m(0,2,4,8,10,14) is--

- B'D +ACD' +A'C'D'
- B'D' +AC'D +A'C'D'
- B'D' +ACD' +A'C'D'
- BD' +ACD' +A'C'D'

Excess 3 code for 12 will be --

- 0011
- 1111
- Dont Care
- 1100

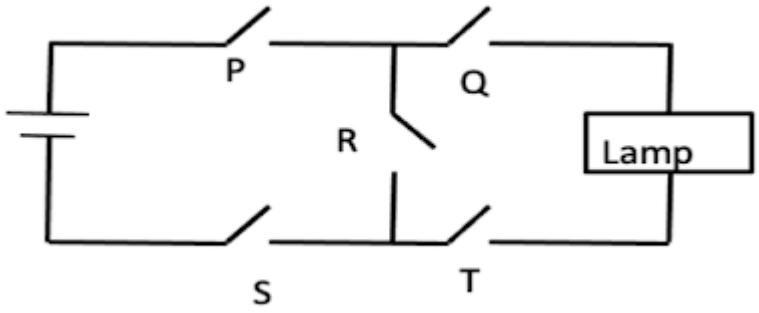
You are provided with a D flip-flop and are asked to design a new flip-flop which incorporates no change operation along with the operations offered by the D flip-flop. **Minimum** how many additional basic gates do you need for accomplishing the task?

- 5
- 3
- 6
- 2

It should be kept in mind that Don't Care terms should be used along with the terms that are present in-

- Expressions
- Minterms
- Latches
- K-Map

Select the logical function f (P, Q, R, S, T) for the following circuit -



- R(PS+QT)
- P(S(QT+R))
- PR+ST
- P(RS+QT)

What is the minimum number of flipflops required to output the following sequence: 0,0,1,1,0,0,1,1,...?

- Impossible
- 1
- 2
- 3

A three (3) variable K-map contains _____ cells.

- 4
- 32
- 8
- 16

Four routers are connected in a network that can be represented by the logical function f(w, x, y, z)= wx' + y(z+x) + wz'+ x', For AND gate there is a delay of 5ns, and for OR gate the delay is 6ns. What is the value of minimum possible delay of that function f in ns? (write only the value. For example: 100)

Your answer

The POS form for the function f(A,B,C,D)= ∑m(0,2,4,8,10,14) is--

- D'(A+B'+C') (A'+B'+C)
- D'(A+B'+C) (A'+B'+C)
- D'(A+B'+C') (A+B'+C)
- D'(A+B'+C') (A'+B+C)

A boolean function with five (5) variables has an octet of one (1). How many variable(s) will the final literal contain?

- 3
- 1
- 4
- 2

What is the minimum number of flipflops required to produce the output sequence of the 4-bit Johnson counter?

- 3
- 4
- 2
- 5

Which of the following is NOT considered for forming groups in K-map?

- Vertical
- Rolling
- Horizontal
- Diagonal

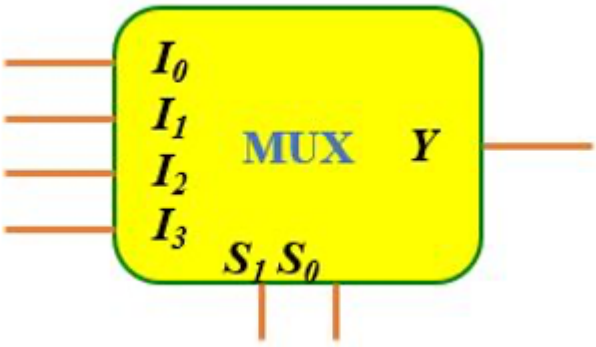
The minimized form of f(A,B,C)=AB +A'C+BC is--

- B(A+C)
- AB +A'C
- C(A'+B)
- None of the above

The outputs in 74138 are--

- active low and active high
- active high
- None of the options
- active low

Consider the following 4-to-1 MUX. Suppose, the S_0 selector bit of the MUX is malfunctioning and so, you want to use it as a 2-to-1 MUX. How many additional gates are required, at minimum, to make it usable as a 2-to-1 Mux?



- 2
- It is not possible to use this as a 2-to-1 MUX
- 1
- 4
- 0

You have a 4-bit SIPO Shift Register (i.e. NO PARALLEL LOAD) that currently holds 1001. What is the minimum number of clock cycles required for the shift register to hold 1000?

- 4
- 2
- 3
- 1

Which one of the following is correct?

- ◯ 7483 has no internal carry look ahead
- ◯ 7483 is cascadable in 3 bit increments
- ◯ 7483 is cascadable in 4 bit increments
- ◯ 7483 is cascadable in 2 bit increments

$P \oplus Q = R$, then

- ◯ $P \oplus R = R'$
- ◯ $Q \oplus R = PQ$
- ◯ Option 5
- ◯ $P \oplus R = Q$
- ◯ $P \oplus R = Q'$

Can you use T-flipflops to create a Universal Shift Register?

- ◯ No
- ◯ Yes

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