For Sequential cells, the following characterizations have to be performed and filled.

1. **Input pin capacitances:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Pins** | **Rise Cap (pF)** | **Fall Cap (pF)** | **Average Cap (pF)** |
| D | 2.585 | 2.587 | 2.586 |
| CLK | 9.9 | 10.3 | 10.1 |

1. **Set-up Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.236 | 0.316 |
| **1000 ps** | 0.22 | 0.442 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.073 | 0.245 |
| **1000 ps** | 0.223 | 0.402 |

1. **Hold Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.114 | 0.317 |
| **1000 ps** | 0.196 | 0.379 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.073 | 0.032 |
| **1000 ps** | 0.032 | 0.196 |

1. **Transition Time Table (for Q output, CLK will have minimum slew of 10 ps):** (please strictly consider 20% and 80% of VDD for transition time)

**(i) Output Rise Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.068 | 0.068 | 0.068 |
| **10 fF** | 0.093 | 0.093 | 0.093 |
| **100 fF** | 0.59 | 0.59 | 0.6 |

**(ii) Output Fall Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.063 | 0.063 | 0.063 |
| **10 fF** | 0.105 | 0.105 | 0.105 |
| **100 fF** | 0.64 | 0.64 | 0.64 |

1. **CLK-to-Q Delay Time Table**: (delay between clock transition and data transition. Use 50% of CLK to 50% of output to simulate propagation delay).

**Considering T=3000p for all the simulations**

**(i) Cell Rise Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.16 | 0.207 | 0.309 |
| **10 fF** | 0.219 | 0.245 | 0.386 |
| **100 fF** | 0.581 | 0.6 | 0.744 |

**(ii) Cell Fall Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.23 | 0.227 | 0.409 |
| **10 fF** | 0.298 | 0.310 | 0.493 |
| **100 fF** | 0.734 | 0.744 | 0.93 |

1. **Static Power (all possible input combinations of CLK and D).**

|  |  |
| --- | --- |
| **Condition (CLK, D)** | **Power (nW)** |
| 00 | 1589 |
| 01 | 0.476 |
| 10 | 0.476 |
| 11 | 0.581 |

1. **Dynamic Power Table: (CLK will have minimum slew of 10 ps)**

**(i) Rise Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 3224 | 24730 | 239777 |
| **10 fF** | 3221 | 24695.8 | 239431 |
| **100 fF** | 3220 | 24690 | 239374 |

**(ii) Fall Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 999.6 | 2430.8 | 268391 |
| **10 fF** | 999.6 | 2425.8 | 268499 |
| **100 fF** | 1292 | 5357 | 268542 |