DEVRELER ve SİSTEMLER

BIMU2058 – CSBM2092

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İÇERİK

Transistorlar

- Bipolar Transistorlar
  - BJT
- Alan Etkili Transistorlar
  - FET
    - jFET
    - MOSFET

BIPOLAR JUNCTION TRANSISTORS (BJTs)

Transistor Construction

There are two types of transistors:

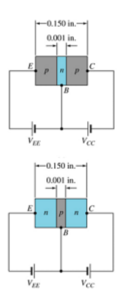
- *pnp*
- *npn*

The terminals are labeled:

- E - Emitter
- B - Base
- C - Collector

pnp

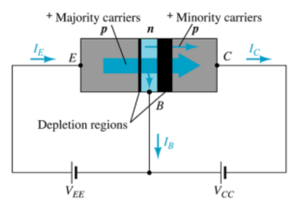
npn



Transistor Operation

With the external sources, V_{EE} and V_{CC}, connected as shown:

- The emitter-base junction is forward biased
- The base-collector junction is reverse biased



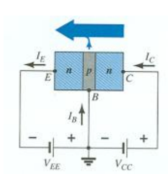
Currents in a Transistor

Emitter current is the sum of the collector and base currents:

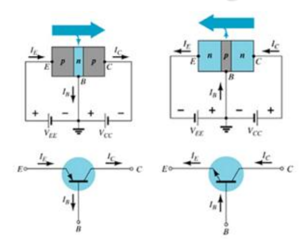
$$I_E = I_C + I_B$$

The collector current is comprised of two currents:

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$



Common-Base Configuration

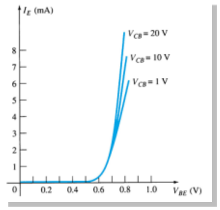


The base is common to both input (emitter–base) and output (collector–base) of the transistor.

Common-Base Amplifier

Input Characteristics

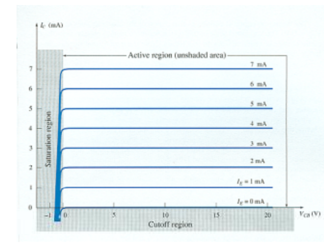
This curve shows the relationship between of input current (I_E) to input voltage (V_{BE}) for three output voltage (V_{CB}) levels.



Common-Base Amplifier

Output Characteristics

This graph demonstrates the output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E).



Operating Regions

- **Active** – Operating range of the amplifier.
- **Cutoff** – The amplifier is basically off. There is voltage, but little current.
- **Saturation** – The amplifier is full on. There is current, but little voltage.

Approximations

Emitter and collector currents:

$$I_C \cong I_E$$

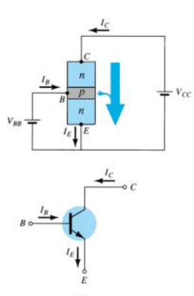
Base-emitter voltage:

$$V_{BE} = 0.7\,\text{V} \quad \text{(for Silicon)}$$

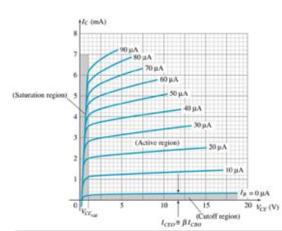
Common–Emitter Configuration

The emitter is common to both input (base-emitter) and output (collector-emitter).

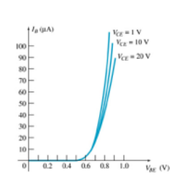
The input is on the base and the output is on the collector.



Common-Emitter Characteristics



Collector Characteristics



Base Characteristics

Beta (β)

β represents the amplification factor of a transistor. (β is sometimes referred to as h_{fe}, a term used in transistor modeling calculations)

In DC mode:

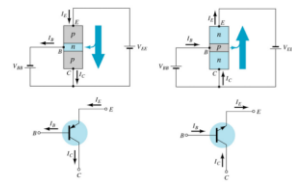
$$\beta_{dc} = \frac{I_C}{I_B}$$

In AC mode:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}=\text{constant}}$$

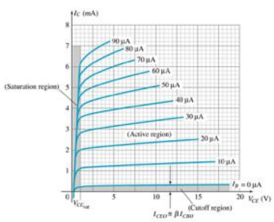
Common–Collector Configuration

The input is on the base and the output is on the emitter.



Common–Collector Configuration

The characteristics are similar to those of the common-emitter configuration, except the vertical axis is I_E.

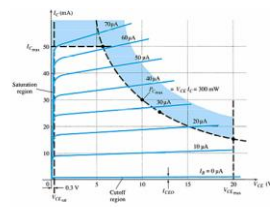


Operating Limits for Each Configuration

V_{CE} is at maximum and I_C is at minimum ($I_{Cmax} = I_{CEO}$) in the cutoff region.

I_C is at maximum and V_{CE} is at minimum ($V_{CE\ max} = V_{CEsat} = V_{CEO}$) in the saturation region.

The transistor operates in the active region between saturation and cutoff.



Power Dissipation

Common-base:

$$P_{Cmax} = V_{CB} I_C$$

Common-emitter:

$$P_{Cmax} = V_{CE} I_C$$

Common-collector:

$$P_{Cmax} = V_{CE} I_E$$

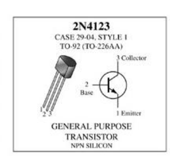
Transistor Specification Sheet

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{θJC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{θJA}$	200	°C/W



Transistor Specification Sheet

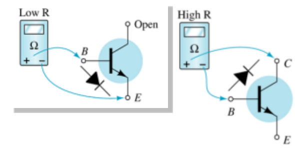
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_E = 0)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) (I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{BE(sat)}$	–	0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	250		MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 MHz)	C_{obo}	–	4.0	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{ibo}	–	8.0	pF
Collector-Base Capacitance (I_E = 0, V_{CB} = 5.0 V, f = 100 kHz)	C_{cb}	–	4.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50	200	–
Current Gain – High Frequency (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz) (I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	2.5 50	– 200	–
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k ohm, f = 1.0 kHz)	NF	–	6.0	dB

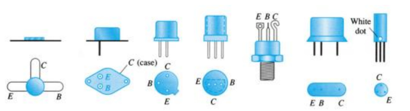
(1) Pulse Test: Pulse Width = 300 μs. Duty Cycle = 2.0%

Transistor Testing

- **Curve Tracer**
  Provides a graph of the characteristic curves.
- **DMM**
  Some DMMs measure β_{DC} or h_{FE}.
- **Ohmmeter**



Transistor Terminal Identification



FETs vs. BJTs

The BJT transistor is a bipolar device—the prefix bi- revealing that the conduction level is a function of two charge carriers, electrons and holes. The FET (Field Effect Transistor) is a unipolar device depending solely on either electron (n-channel) or hole (p-channel) conduction.

Similarities:
- **Amplifiers**
- **Switching devices**
- **Impedance matching circuits**

Differences:
- **FETs are voltage controlled devices. BJTs are current controlled devices.**
- **FETs have a higher input impedance. BJTs have higher gains.**
- **FETs are less sensitive to temperature variations and are more easily integrated on ICs.**
- **FETs are generally more static sensitive than BJTs.**

FET Types

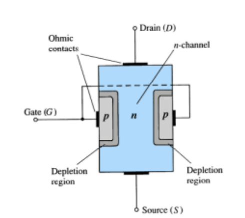
- **JFET:** **Junction FET**
- **MOSFET:** **Metal–Oxide–Semiconductor FET**
  - **D-MOSFET:** **Depletion MOSFET**
  - **E-MOSFET:** **Enhancement MOSFET**

JFET Construction

There are two types of JFETs

- ***n*-channel**
- ***p*-channel**

The n-channel is more widely used.



There are three terminals:

- **Drain (D) and Source (S) are connected to the *n*-channel**
- **Gate (G) is connected to the *p*-type material**

JFET Operation: The Basic Idea

JFET operation can be compared to a water spigot.

The source of water pressure is the accumulation of electrons at the negative pole of the drain-source voltage.

The drain of water is the electron deficiency (or holes) at the positive pole of the applied voltage.

The control of flow of water is the gate voltage that controls the width of the n-channel and, therefore, the flow of charges from source to drain.

JFET Operating Characteristics

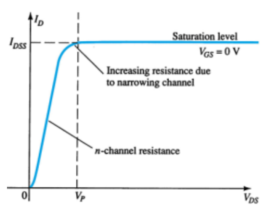
There are three basic operating conditions for a JFET:

- **$V_{GS} = 0$, V_{DS} increasing to some positive value**
- **$V_{GS} < 0$, V_{DS} at some positive value**
- **Voltage-controlled resistor**

JFET Operating Characteristics: Saturation

At the pinch-off point:

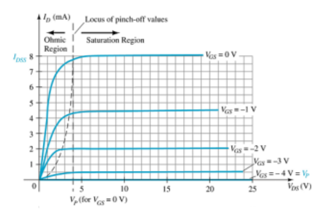
- **Any further increase in V_{GS} does not produce any increase in I_D. V_{GS} at pinch-off is denoted as V_p.**
- **I_D is at saturation or maximum. It is referred to as I_{DSS}.**
- **The ohmic value of the channel is maximum.**



JFET Operating Characteristics

As V_{GS} becomes more negative:

- **The JFET experiences pinch-off at a lower voltage (V_P).**
- **I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.**
- **Eventually I_D reaches 0 A. V_{GS} at this point is called V_p or $V_{GS(off)}$.**



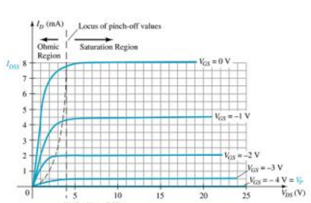
Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

JFET Operating Characteristics: Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the ohmic region.

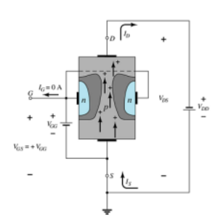
The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

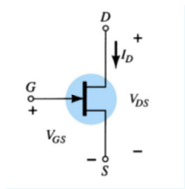


p-Channel JFETS

The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.



N-Channel JFET Symbol



JFET Transfer Characteristics

The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.

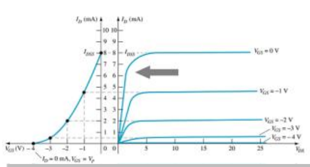
In a BJT, β indicates the relationship between I_B (input) and I_C (output).

In a JFET, the relationship of V_{GS} (input) and I_D (output) is a little more complicated:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.



JFET Specifications Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = –10 µAdc, V_{DS} = 0)		$V_{(BR)GSS}$	–25	–	–	Vdc
Gate Reverse Current (V_{GS} = –15 Vdc, V_{DS} = 0)		I_{GSS}	–	–	–1.0	nAdc
(V_{GS} = –15 Vdc, V_{DS} = 0, T_A = 100°C)			–	–	–200	
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	–0.5	–	–6.0	Vdc
Gate Source Voltage (V_{DS} = 15 Vdc, I_D = 100 µAdc)	2N5457	V_{GS}	–	–2.5	–	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5457	$\lvert y_{fs} \rvert$	1000	–	5000	µmhos
Output Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\lvert y_{os} \rvert$	–	10	50	µmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

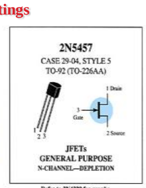
*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%.

JFET Specifications Sheet

Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	–25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C



Refer to 2N4220 for graphs.

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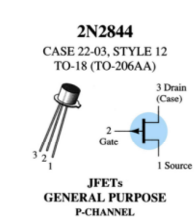
Case and Terminal Identification



Testing JFETs

- **Curve Tracer**
  A curve tracer displays the I_D versus V_{DS} graph for various levels of V_{GS}.
- **Specialized FET Testers**
  These testers show I_{DSS} for the JFET under test.

MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.

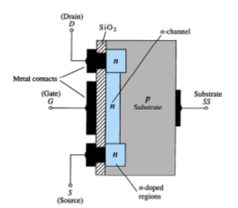
There are two types of MOSFETs:

- Depletion-Type
- Enhancement-Type

Depletion-Type MOSFET Construction

The **Drain** (D) and **Source** (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the **Gate** (G) via a thin insulating layer of SiO_2.

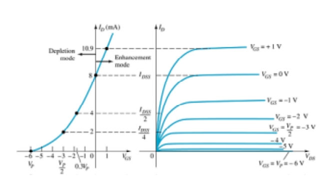
The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called **Substrate** (SS).



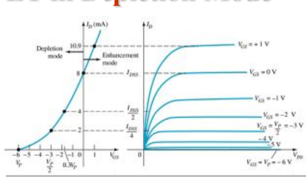
Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

- Depletion mode
- Enhancement mode



D-Type MOSFET in Depletion Mode



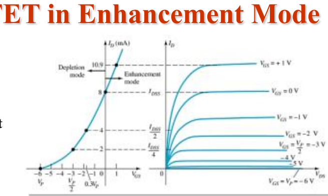
Depletion Mode

The characteristics are similar to a JFET.

- When $V_{GS} = 0$ V, $I_D = I_{DSS}$
- When $V_{GS} < 0$ V, $I_D < I_{DSS}$
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

D-Type MOSFET in Enhancement Mode



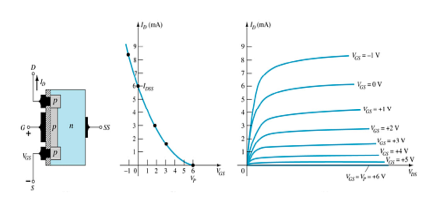
Enhancement Mode

- $V_{GS} > 0$ V
- I_D increases above I_{DSS}
- The formula used to plot the transfer curve still applies:

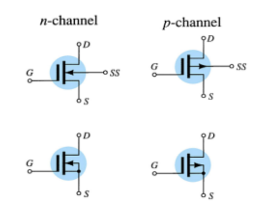
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Note that V_{GS} is now a positive polarity

p-Channel D-Type MOSFET



D-Type MOSFET Symbols

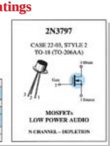


Specification Sheet

Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage 2N3797	V_{DS}	20	Vdc
Gate-Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	−65 to +200	°C



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Specification Sheet

Electrical Characteristics

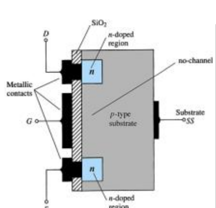
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage ($V_{GS} = -7.0$ V, $I_D = 5.0$ μA)	2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) ($V_{GS} = -10$ V, $V_{DS} = 0$) ($V_{GS} = -10$ V, $V_{DS} = 0$, $T_A = 150°C$)		I_{GSS}	– –	– –	1.0 200	pAdc
Gate Source Cutoff Voltage ($I_D = 2.0$ μA, $V_{DS} = 10$ V)	2N3797	$V_{GS(off)}$	–	−5.0	−7.0	Vdc
Drain-Gate Reverse Current (1) ($V_{DG} = 10$ V, $I_S = 0$)		I_{DGO}	–	–	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$)	2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current ($V_{DS} = 10$ V, $V_{GS} = +3.5$ V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz)	2N3797	$\|y_{fs}\|$	1500	2300	3000	μmhos
($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)	2N3797		1500	–	–	
Output Admittance ($I_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz)	2N3797	$\|y_{os}\|$	–	27	60	μmhos
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)	2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)		C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz, R_S = 3 megohms)		NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

E-Type MOSFET Construction

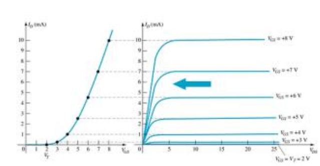
- The **Drain** (D) and **Source** (S) connect to the to *n*-doped regions. These *n*-doped regions would be connected via an *n*-channel
- The **Gate** (G) connects to the *p*-doped substrate via a thin insulating layer of SiO_2
- There is no channel
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the **Substrate** (SS)



Basic Operation of the E-Type MOSFET

The enhancement-type MOSFET operates only in the enhancement mode.

- V_{GS} is always positive
- As V_{GS} increases, I_D increases
- As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level, V_{DSsat} is reached

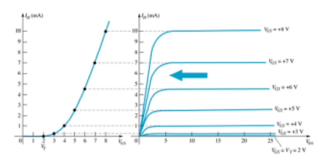


E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

$I_D = k(V_{GS} - V_T)^2$

Where:
V_T = threshold voltage or voltage at which the MOSFET turns on



k, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

V_{DSsat} can be calculated by:

$V_{Dsat} = V_{GS} - V_T$

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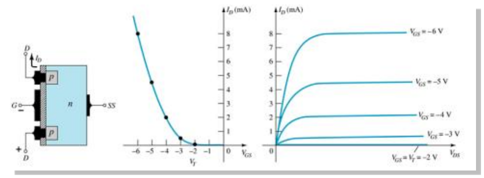
p-Channel E-Type MOSFETs



The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

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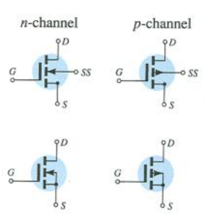
MOSFET Symbols



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Specification Sheet

Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

more…

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Specification Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10\ \mu A$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) $T_A = 25°C$ $T_A = 150°C$	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10\ \mu A$)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance ($V_{DS} = 10$ V, $I_D = 2.0$ mA, f = 1.0 kHz)	$\lvert y_{fs}\rvert$	1000	–	μmho
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)} = 10$ V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance ($V_{GS} = 10$ V, $I_D = 0$, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5) — $I_D = 2.0$ mAdc, $V_{DS} = 10$ Vdc, ($V_{GS} = 10$ Vdc) (See Figure 9; Times Circuit Determined)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

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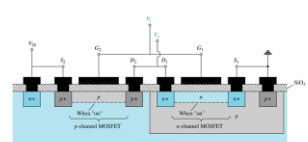
CMOS Devices

CMOS (complementary MOSFET) uses a *p*-channel and *n*-channel MOSFET; often on the same substrate as shown here.



Advantages

- Useful in logic circuit designs
- Higher input impedance
- Faster switching speeds
- Lower operating power levels

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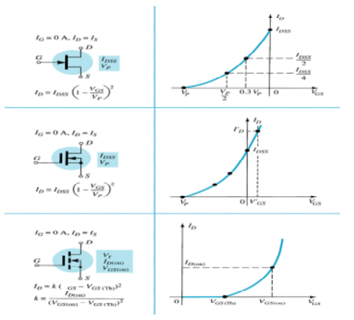
Summary Table



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