EE 464

STATIC POWER CONVERSION-I

Spring 2022-2023

Complete Design Report and Test Results

Autobots

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Introduction

This report presents the design decisions for the hardware project. Furthermore, it gives the details computer simulation results and component selection details. In addition, the report presents test results. The design calculations are done mainly on MATLAB and complete MATLAB code is given in Appendix 1.

Topology Selection

The converter needs to be isolated. Therefore, the alternatives are listed below:

- Flyback converter
- Forward converter
- Push-Pull converter

Among these converter topologies, the flyback converter is chosen as an appropriate converter for given requirements. When compared with other topologies, it is easier to increase the output voltage with Flyback due to its input-output voltage relation. Thus, it requires fewer turns ratio with the same duty cycle or, it requires less duty cycle with the same turns ratio. This may decrease the losses on copper or conduction losses of switching devices. Additionally, the Flyback converter requires fewer components than the other converter topologies, so its control is less complex.

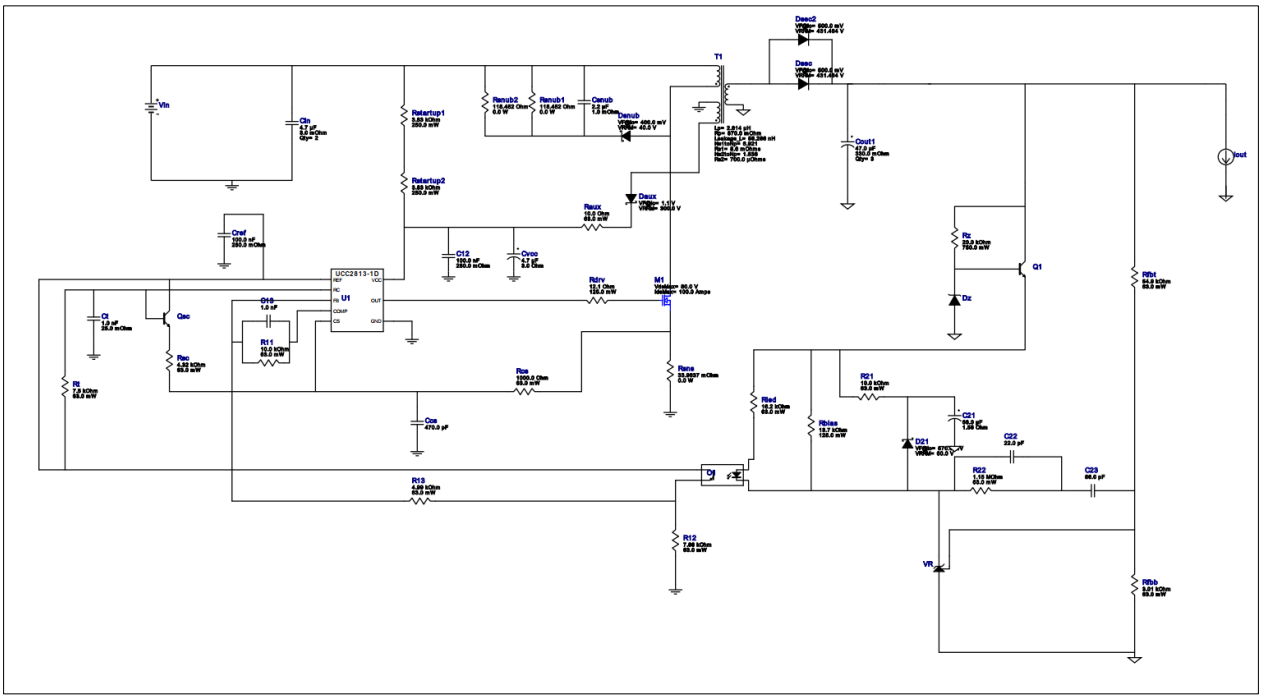

Figure 1: TI Webench design [Appendix 2]

Magnetic Design

a) The duty range of the converter is selected as [0.278 – 0.336] to match the design by the Ti Webench. According to the duty range determination, the turn ratio is calculated via the MATLAB code below.

```
clearvars
syms d turnsRatio
v_o = 48
d_min = 0.278; v_d_minduty = 18;
d_max = 0.366; v_d_maxduty = 12
turnsRatio_minduty = ( (d_min/(1-d_min)) * (v_d_minduty/v_o) )^-1
turnsRatio_maxduty = ( (d_max/(1-d_max)) * (v_d_maxduty/v_o) )^-1
```

According to the code above, the transformer turns ratio (N_s/N_p) is calculated as 6.93.

b)

1. The available cores and coil formers are investigated. Firstly, due to its available stock number is high, PCB5530-FA is selected as the coil former. Therefore, the compatible core 0P45530EC is selected as the transformer core.
2. Using the MATLAB code below, the primary turn number is found 1.14, while the secondary turn number is 7.93. The magnetizing inductance is 8 uH. 1.14 turn makes no sense and increasing the inductance a little bit makes no harm. Therefore, the primary turns are made into 2 turns. The corresponding secondary turns number then becomes 13.89, which is pretty close to 14. Hence, the primary wounded 2 turns while the secondary wound 14 turns.

```
U_o = v_o;
v_t = d_max;
f_sw = 100e3;
i_out = 1;
i_avgSec = i_out/(1-v_t);
xformerCurrRipple = 0.5; % percent
L_sec = (U_o*(1-v_t))/(xformerCurrRipple*i_avgSec*f_sw)
L_pri = L_sec/(turnsRatio_maxduty^2)
% (turnsRatio_maxduty^2)*2.814e-6
```

```
syms priTurns secTurns
AL = 6130e-9 % nH/T^2; minimal

priTurns = double(solve(L_pri == AL*priTurns^2))
secTurns = double(solve(L_sec == AL*secTurns^2))
% make sure core is not saturated
ampTurns = i_out*secTurns
```

3. According to the AWG table, the secondary should be wounded using 2 parallel 24 AWG wires. The primary, on the other hand, 2 parallel 17 AWG wires will be used. The AWG calculation is done by the snippet below.

```
p_o = i_out * v_o
i_in_max = v_o/v_d_maxduty
% Primary selected as 17  AWG
selectedAWGRating_pri = 2.9;
primaryDiameter_mm = 1.15062;
cableAreaPri_mm2 = 1.04;
% Secondary selected as 24  AWG
selectedAWGRating_sec = 0.577;
secondaryDiameter_mm = 0.5;
cableAreaSec_mm2 = 0.327;


primaryRadius_mm = primaryDiameter_mm/2
secondaryRadius_mm = secondaryDiameter_mm/2
num_of_paralles_sec = i_out/selectedAWGRating_sec
num_of_paralles_pri = i_in_max/selectedAWGRating_pri
```

4. According to the code below, the fill factor is 1.75%, which is low but reasonable.

```
windowArea_mm2 = 537;
priTurns = ceil(priTurns(priTurns>0))
secTurns = ceil(secTurns(secTurns>0))
num_of_paralles_pri = ceil(num_of_paralles_pri)
num_of_paralles_sec = ceil(num_of_paralles_sec)


primaryArea_mm2 = priTurns*num_of_paralles_pri*cableAreaPri_mm2
secondaryArea_mm2 = secTurns*num_of_paralles_sec*cableAreaSec_mm2
totalCableArea_mm2 = primaryArea_mm2 + secondaryArea_mm2
fillFactor_perc = 100*totalCableArea_mm2/windowArea_mm2
```

5. Cable resistance calculation is done by the code below:

```
skinDepth_mm = 75/sqrt(f_sw)
innerRadiusPri_mm = primaryRadius_mm - skinDepth_mm
hollowAreaPri_mm2 = pi*innerRadiusPri_mm^2
effectiveAreaPri = cableAreaPri_mm2 - hollowAreaPri_mm2
innerRadiusSec_mm = secondaryRadius_mm - skinDepth_mm
hollowAreaSec_mm2 = pi*innerRadiusSec_mm^2
effectiveAreaSec = cableAreaSec_mm2 -  hollowAreaSec_mm2
% calculate the ratios to convert DC resistance to AC resistance
DC_to_AC_ratio_pri = cableAreaPri_mm2/effectiveAreaPri
```

```
DC_to_AC_ratio_sec = cableAreaSec_mm2/effectiveAreaSec

windingLengthPerTurn_mm = 68.2
ohms_per_meter = 212.872 / 1e3
primaryLength_m = windingLengthPerTurn_mm * priTurns * 1e-3
secondaryLength_m = windingLengthPerTurn_mm * secTurns * 1e-3
primary_DC_resistance_ohm = ohms_per_meter * primaryLength_m /
num_of_paralles_pri
secondary_DC_resistance_ohm = ohms_per_meter * secondaryLength_m /
num_of_paralles_sec
```

According to the results the snippet outputs, the primary AC Resistance is 22.2 mOhm while the secondary AC Resistance is 58.2 mOhm.

6. Copper losses are calculated by the code below:

```
primary_AC_resistance_ohm = primary_DC_resistance_ohm*DC_to_AC_ratio_pri
secondary_AC_resistance_ohm = secondary_DC_resistance_ohm*DC_to_AC_ratio_sec
resistancePri_ohm = vpa(primary_AC_resistance_ohm * u.Ohm)
resistanceSec_ohm = vpa(secondary_AC_resistance_ohm * u.Ohm)
copperLossPri = vpa(unitConvert((i_in_max*u.A)^2 * resistancePri_ohm, u.W))
copperLossSec = vpa(unitConvert((i_out*u.A)^2 * resistanceSec_ohm, u.W))
copperLoss_W = copperLossPri + copperLossSec
```

According to the calculations, the total copper losses are **0.41 W**.

7. Core losses are calculated by the code below:

```
wattLoss_mW_cm3 = 142*u.mW/u.cm^3
volume_mm3 = 52000;
volume_cm3 = vpa(unitConvert(volume_mm3*u.mm^3, u.cm^3))
coreLoss_w = vpa(unitConvert(wattLoss_mW_cm3 * volume_cm3, u.W))
```

Core Loss: 7.38 W

The core loss is way greater than the copper loss. Therefore, the efficiency will suck. However, the other available cores resulted in high leakage inductance experimentally. This core gives the best results in terms of leakage inductance. Therefore, we will proceed with this core, even though its efficiency sucks.

c) The open-loop flyback design is simulated on Simulink as shown in Figure 2. The circuit is simulated at its edges, namely, 12V input voltage and 0.366 duty and 18V input voltage and 0.278

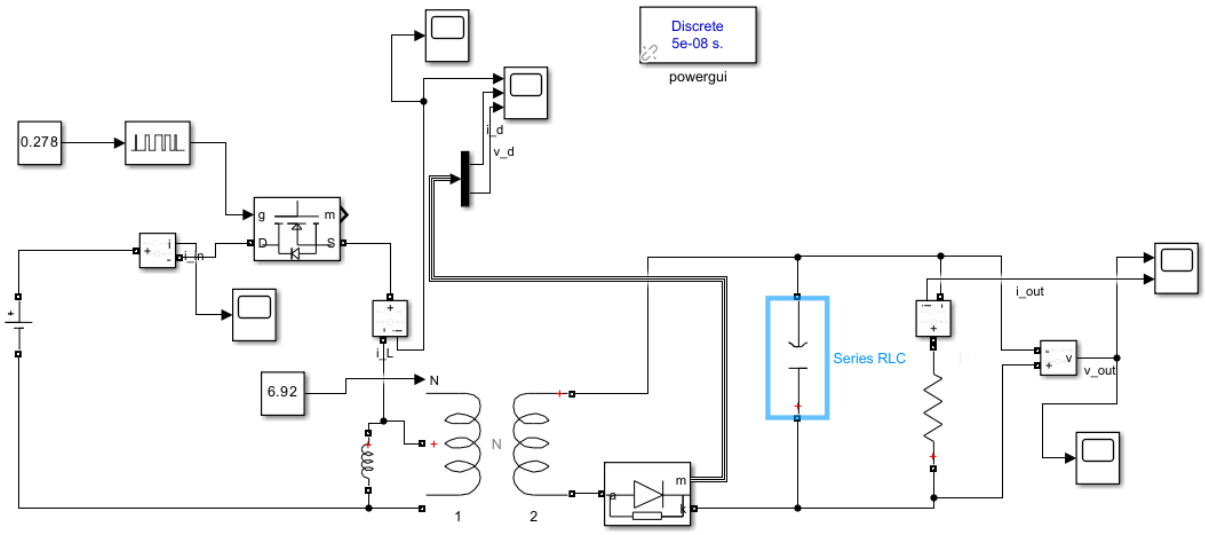

Figure 2: The Flyback converter in Simulink

duty. The simulation results are shown in Figures 3-6 for 0.278 duty and Figures 7-10 for 0.366 duty.

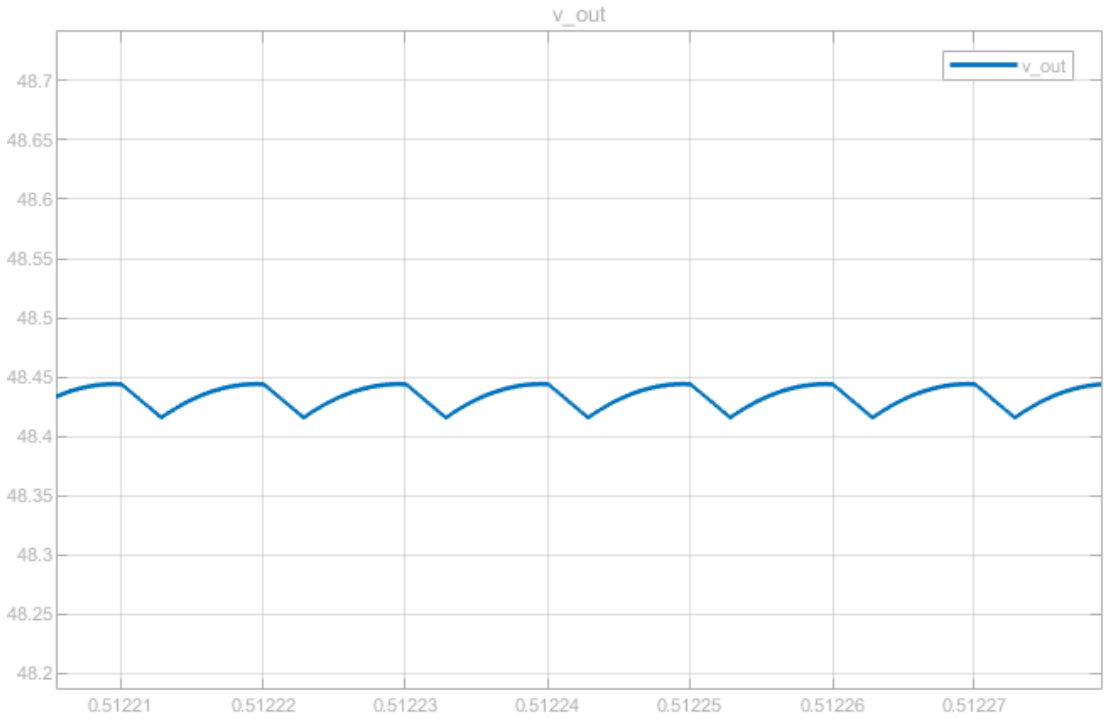

Figure 3: Output voltage ripple for 0.278 duty

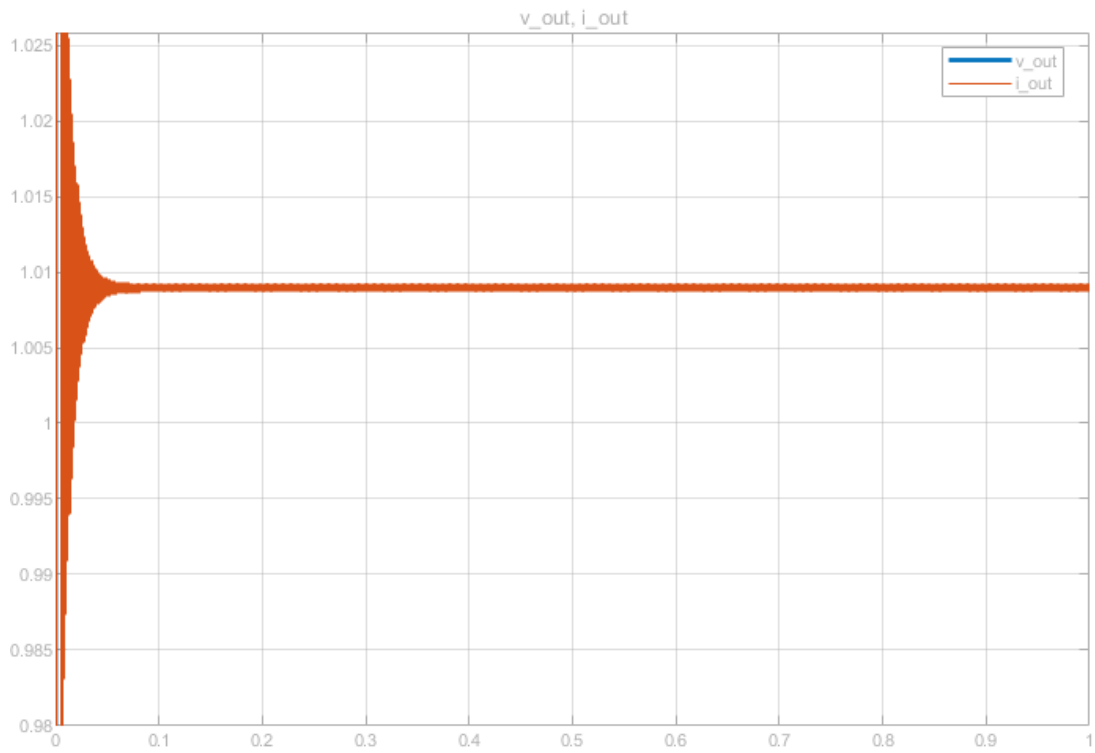

Figure 4: Output current waveform for 0.278 duty

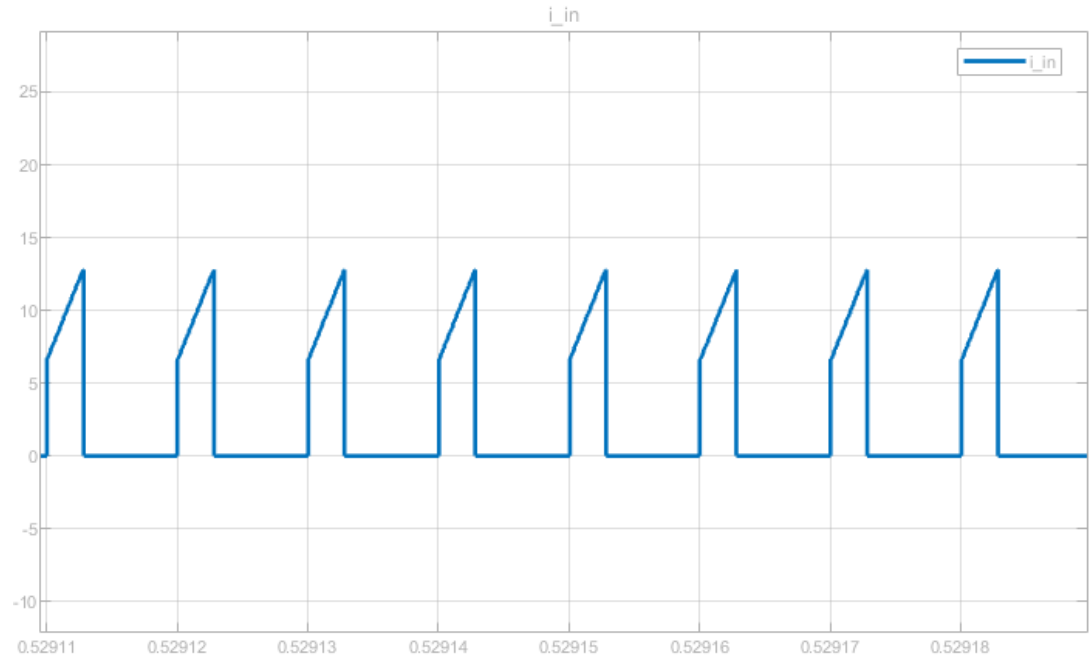

Figure 5: Input current waveform for 0.278 duty

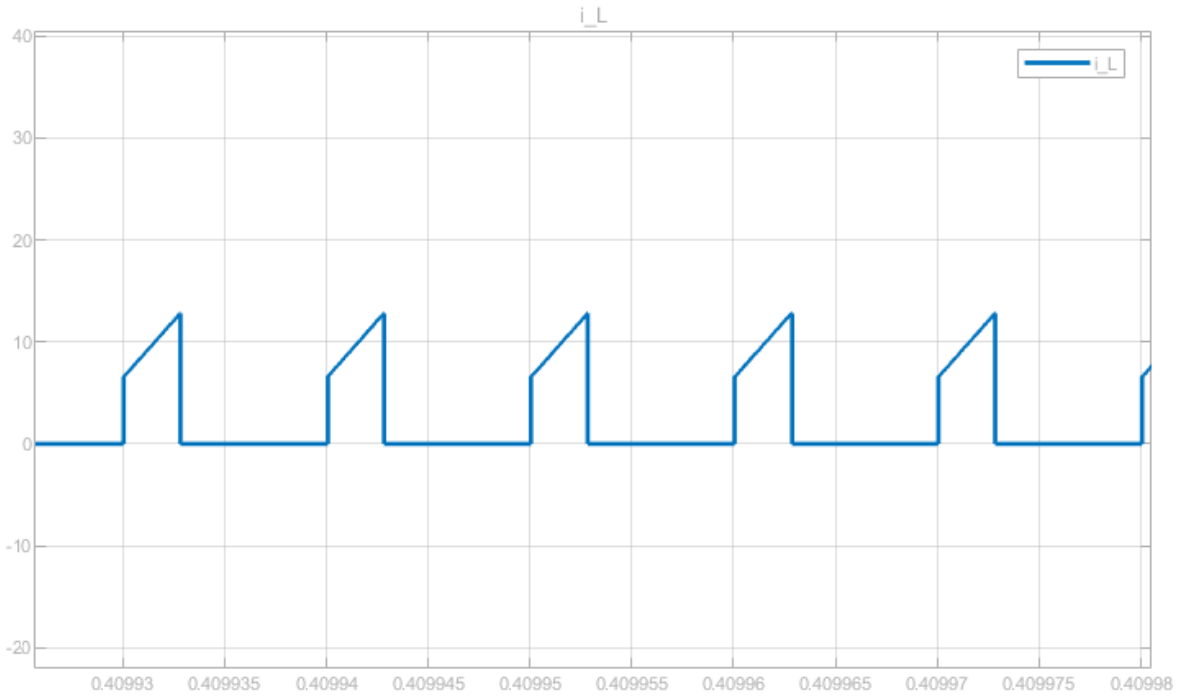

Figure 6: Transformer primary current waveform for 0.278 duty

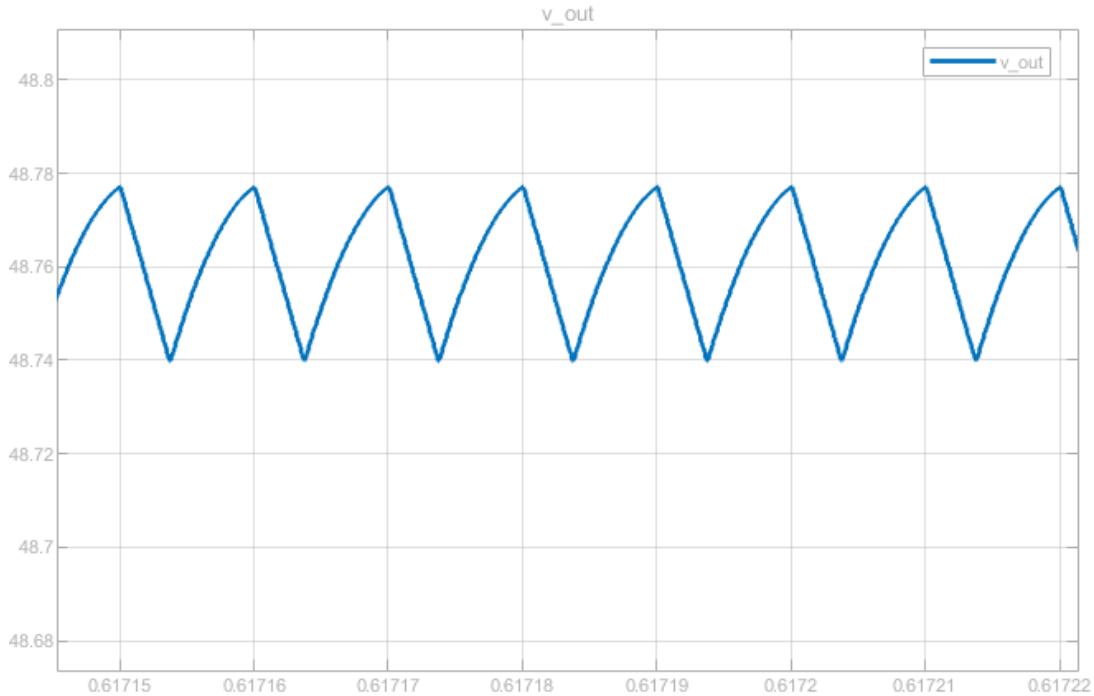

Figure 7: Output voltage ripple for 0.366 duty

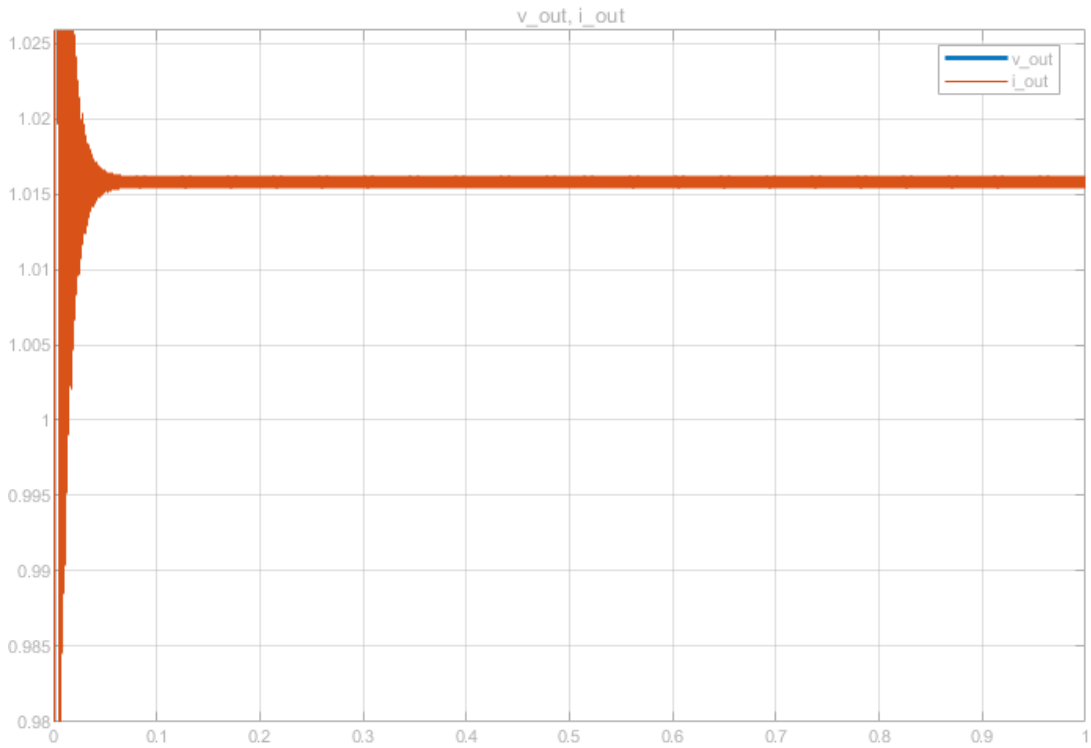

Figure 8: Output current waveform for 0.366 duty

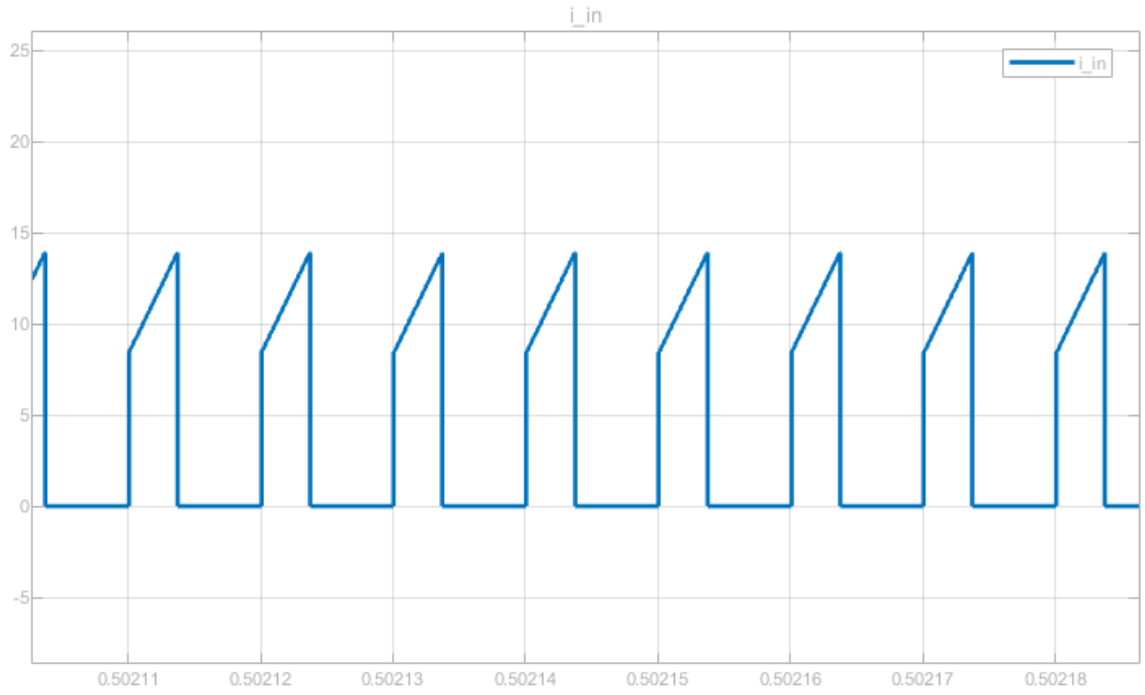

Figure 9: Input current waveform for 0.366 duty

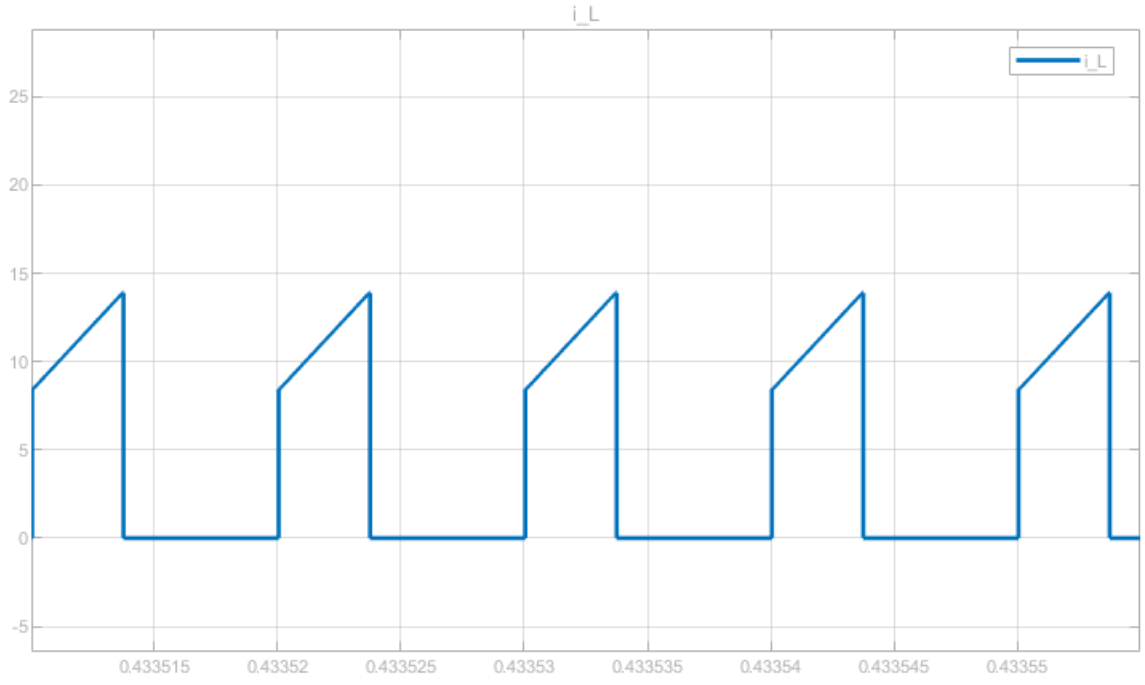

Figure 10: Transformer primary current waveform for 0.366 duty

d) The minimum load current to avoid DCM is calculated with the code below:

```
Lm = 8*10^-6; f_sw = 100*10^3;

% DCM
% for Vs = 12V
Vs = 12; D = 0.366;
deltaI_lm = Vs*D/(Lm*f_sw);
P_min = Vs^2 * D^2 / (2*Lm*f_sw);
I_load_min = P_min / 48

% for Vs = 18V
Vs = 18; D = 0.278;
deltaI_lm = Vs*D/(Lm*f_sw);
P_min = Vs^2 * D^2 / (2*Lm*f_sw);
I_load_min = P_min / 48
```

Minimum load current to operate in CCM when input is 12V = 0.251mA
Minimum load current to operate in CCM when input is 18V = 0.326mA

The maximum current that can flow through the transformer is calculated with the code below:

```
% max I_Lm current occurs when input voltage is 12V and at 100% load
Vs = 12; D = 0.366;
turnsRatio = 6.92; R = 48;
deltaI_lm = Vs*D/(Lm*f_sw);
P_out = Vs^2 * D^2 * turnsRatio^2 / ((1-D)^2 * R);
I_Lm_max = deltaI_lm/2 + P_out/(Vs*D)
```

Current can rise up to the 13.645A while converter is working with 100% load and 12V input voltage.

e)

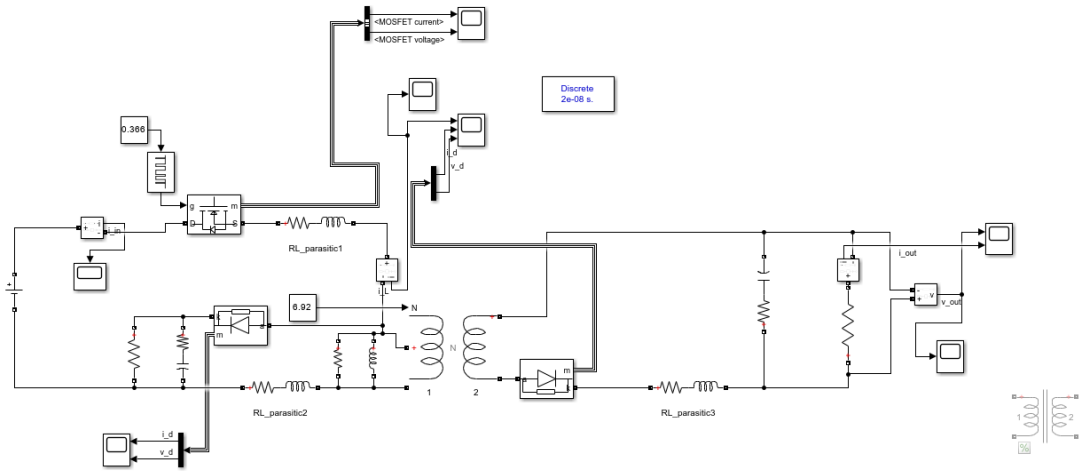

Figure 11: Simulation of the converter with parasitic elements of transformer and switching device.

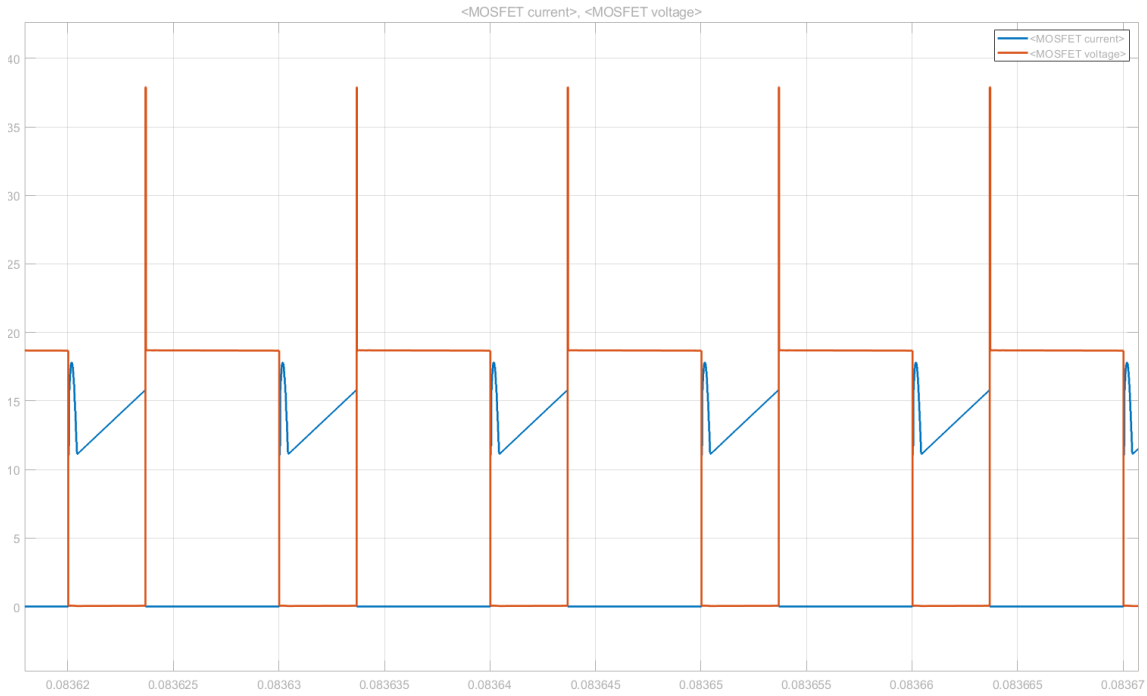

Figure 12: Voltage and current waveforms of MOSFET with parasitic elements.

In Figure 12, it can be seen that, due to parasitic inductances, there are voltage spikes on MOSFET while switching. Because of leakage inductance, a snubber must be used to discharge the leakage inductance. Snubber design is taken from the recommended design of Webench.

f)

The flyback converter is simulated with parasitic elements and non-ideal switching devices as shown in Figure 13.

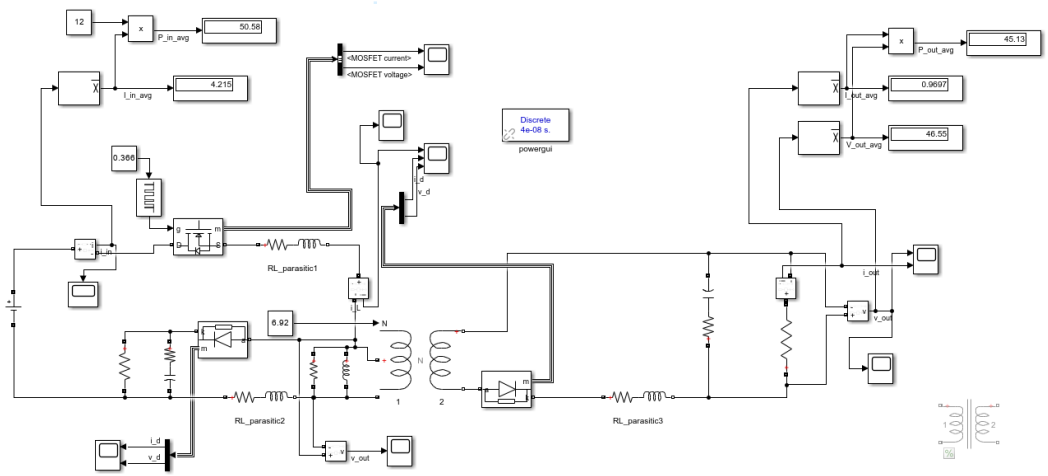

Figure 13: Simulation design for efficiency test.

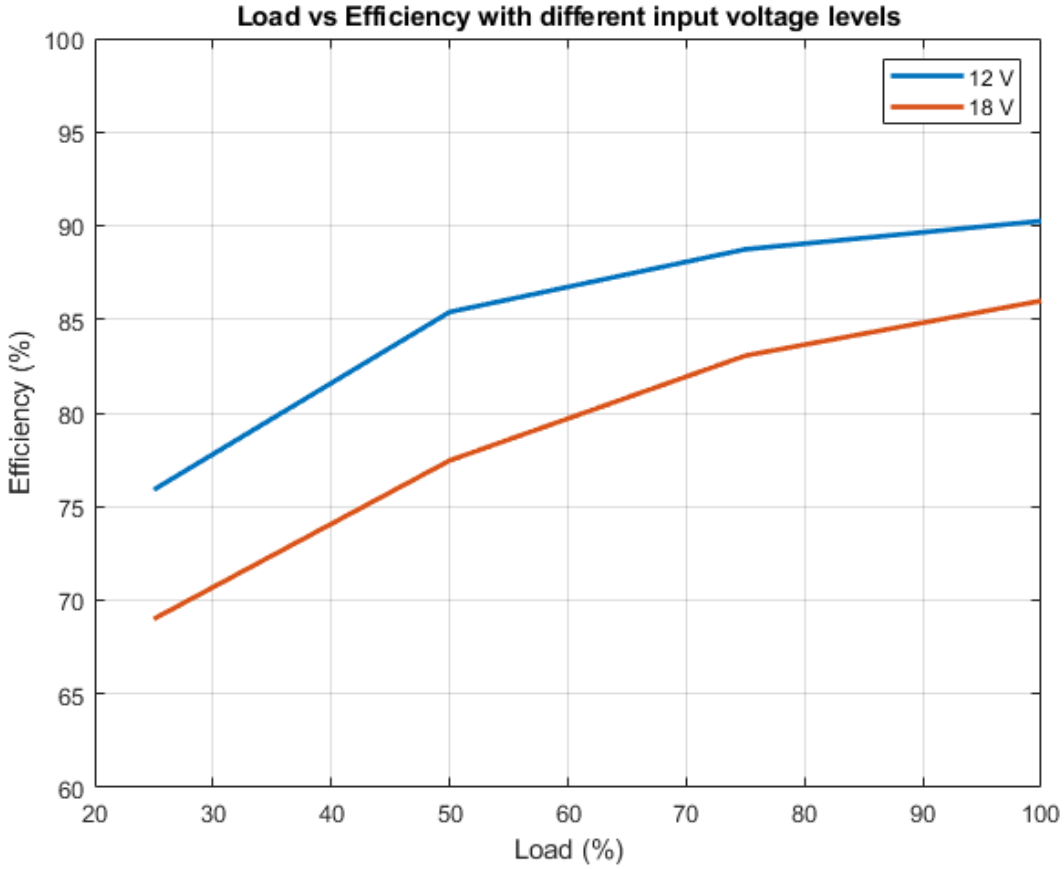

Figure 14: Efficiency vs Load curves for different voltage input levels.

Table 1: Simulation result of efficiency values for different input voltage and load conditions.

Load (%)	Efficiency (%)	
	12V	18V
25	75.9	69
50	85.39	77.46
75	88.74	83.06
100	90.25	85.99

Table 2: Calculated efficiency values without snubber losses.

Load (%)	Efficiency (%)	
	12V	18V
25	87.7	87.89
50	92.78	93.03
75	94.3	94.62
100	94.94	95.33

The efficiency of the flyback converter decreases with less load since core loss and snubber losses become dominant. Also, when the input voltage increases, the losses on the switching device increase quadratically; thus, the converter becomes less efficient with a higher input voltage. Lastly, how inefficient is snubber can be seen by comparing two results.

Component Selection

Switching Device

Peak switching current and voltage can be calculated equations below:

```
V_sw = Vs + 1/turnsRatio*48
I_sw = 1./(1-duty).*turnsRatio.*I_out_avg + 1/turnsRatio.*
       (1-duty)./2./L_pri./f_sw*48
```

Switching voltages are calculated as 18.94V and 24.94V, respectively with 12V and 18V input voltage, and the maximum switching current is calculated as 13.65A. However, due to leakage inductances and parasitic elements, there are voltage spikes while switching. Thus, also it can be seen in Webench design, a Mosfet with 80V rated voltage and 100A rated current is selected [1]. For less rated voltages it is easy and cheap to find high current rated Mosfets, which also results in fewer losses on Mosfet due to less Rds value.

Secondary Diode:

```
V_d_max = Vs*turnsRatio + 48
I_d_max = I_sw./turnsRatio
```

By using the above equations, the maximum voltage on the diode is found as 131.04V and 172.56V, respectively, with 12V and 18V input voltage, and the maximum current is calculated as 1.976A. The voltage rating of the diode should be selected higher because the effect of voltage spikes increases with the turns ratio at the secondary side. Thus, the diode is selected with a 600V rated voltage, and 3A rated current with a forward voltage drop of 1.0V [2].

Output Capacitor:

The maximum allowed voltage ripple at the output is 3%.

```
C_min = duty/f_sw/R/ripple
```

The minimum capacitance value of the output capacitor is found as 2.54µF with the equation above. However, the output voltage is 48V, and to be safe rated voltage of the capacitor should be higher. A high voltage-rated capacitor is found as an aluminum capacitor which has high ESR values compared with other types. Found capacitors in the market have high voltage ratings, so they also have high ESR values. Because ESR values become dominant on output ripple, a capacitor with high capacitances is selected. The selected capacitor has 47µF capacitance and 2Ω ESR. The effect of ESR can be calculated equation below:

```
V_ESR = ESR * I_out_avg
```

The ripple due to ESR can be around 2V when a single capacitor is used. Thus, four of the selected capacitors [3] must be connected in parallel.

Controller IC:

UCC2813DTR-1 is selected which is appropriate for Webench's design. It is a current-mode PWM controller that can drive the gate of the Mosfet with respect to sensed current and output voltage [4].

Transformer:

The detailed calculation of the transformer's turn ratio, cable parameters, core, magnetizing inductance, etc. is given in the magnetic design section.

Experimental results of transformer on first try:

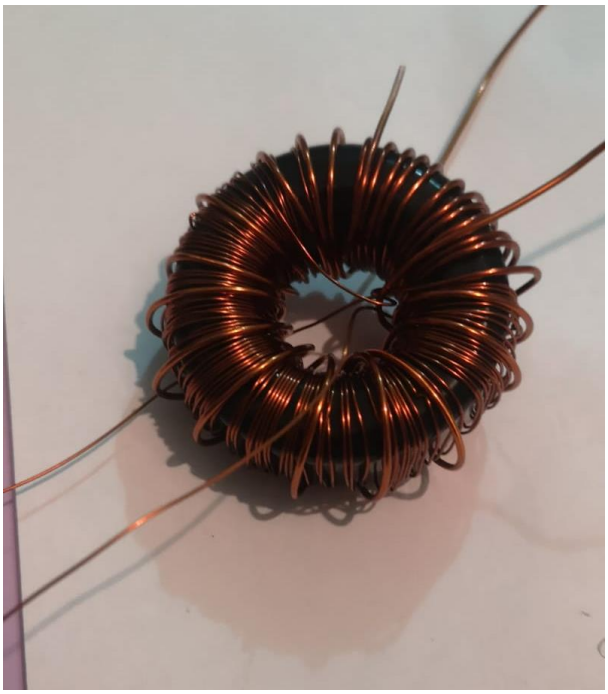

Figure 15: Wound transformer for initial experiments.

Figure 16: Primary is open circuited to measure leakage + magnetizing inductance at secondary.

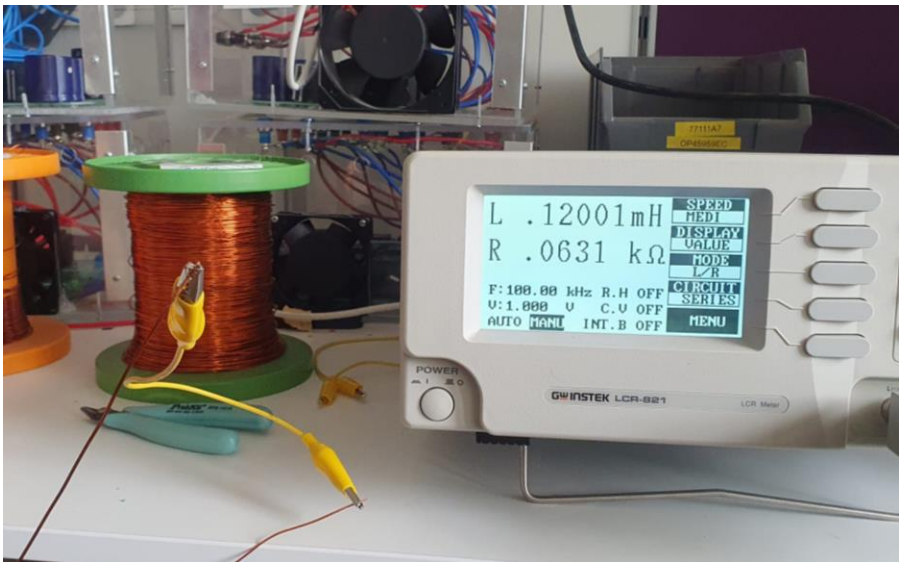

Figure 17: Primary is short circuited to measure leakge inductance at secondary.

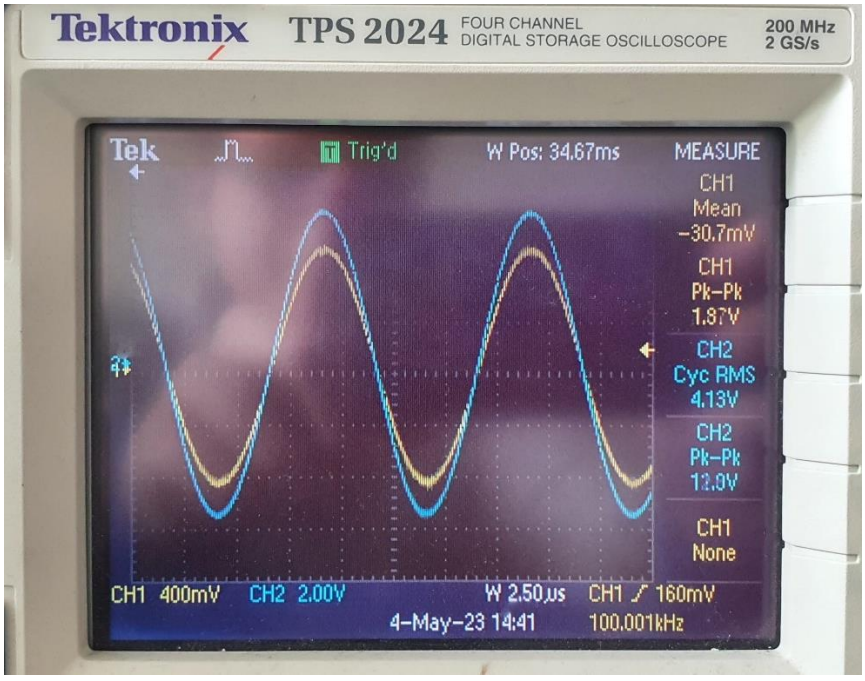

Figure 18: Input and output voltage ratio to observe turns ratio.

The leakage inductance at the secondary is measured as 120µH and by subtracting this value from the total inductance measured as 577µH, magnetizing inductance is measured as 457µH. Also, the turns ratio, which is the ratio of output and input voltage, is measured as 6. It can be seen that the leakage inductance is too high than the expected values. This may be caused by the toroid core because winding around a toroid core is difficult and results in high leakage which can be seen also Figure 15.

Some additional plots are given on Page 4 of Appendix – 2.

Experimental results of transformer on last try:

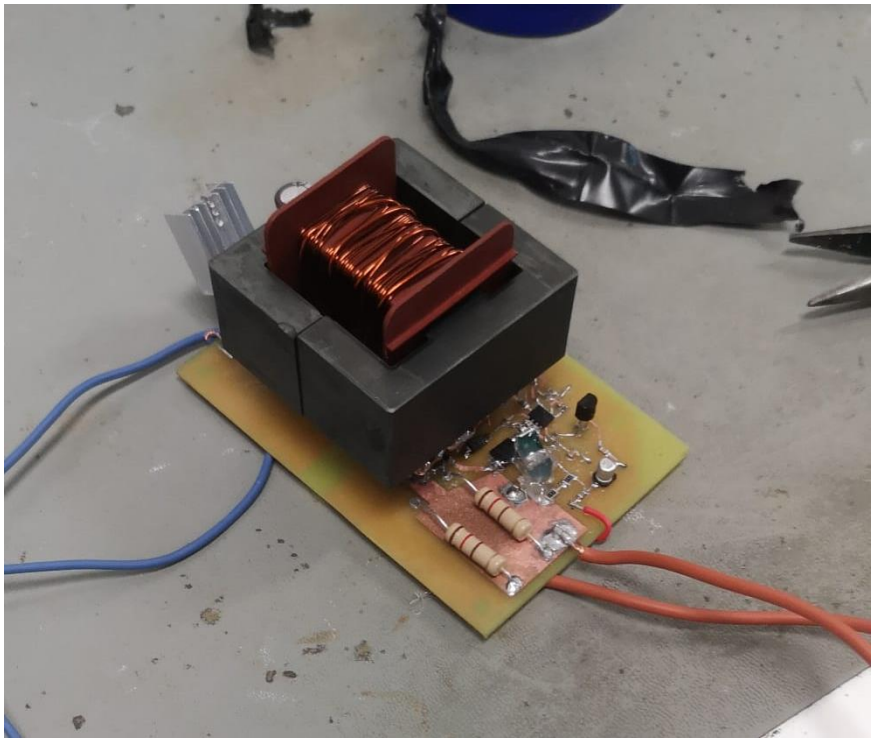

Figure 19: The PCB with last transformer soldered

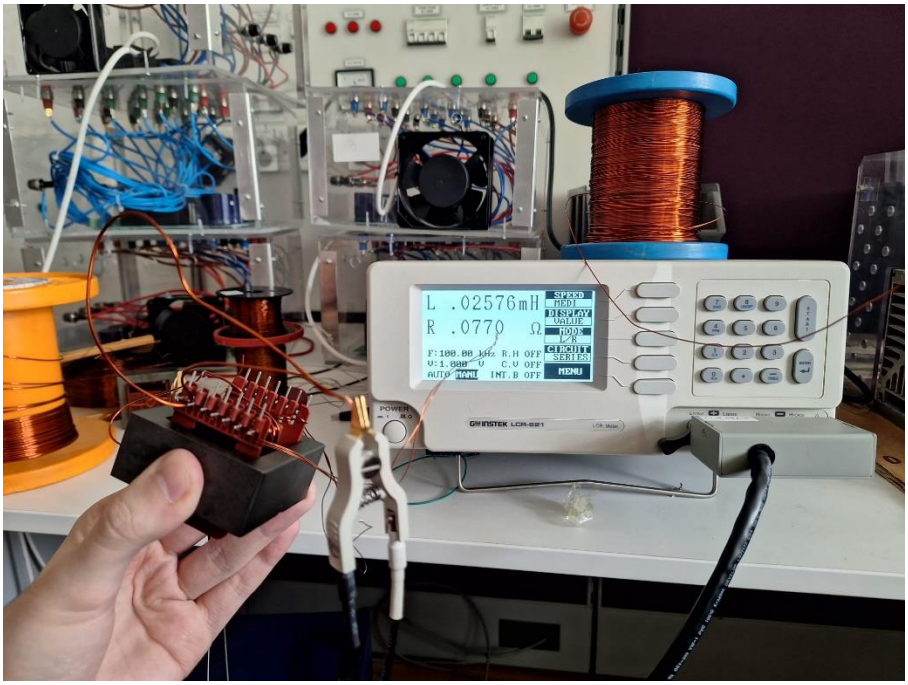

Figure 20: Secondary is open circuited to measure leakage + magnetizing inductance at primary

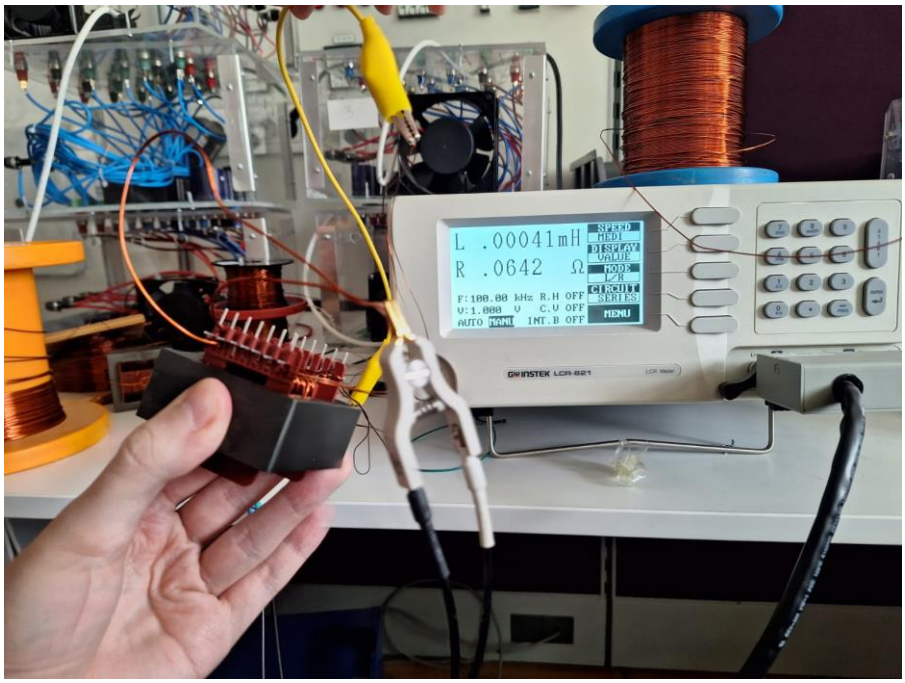

Figure 21: Secondary is short circuited to measure leakge inductance at primary

The leakage inductance at the secondary is measured as 41 nH and by subtracting this value from the total inductance measured as 25.7µH, magnetizing inductance is measured as 25.7µH. In addition, leakage is calculated as 0.2 %. Considering the primary inductance should greater than 8 µH according to the calc.mlx, this transformer should work.

PCB Design

Most of the our components are SMD packets. Therefore, we need to design a PCB in order four our circuit to work. Moreover, we aimed PCB bonus.

The 2D view of the designed PCB is shown in Figure 22. In Figure 22, the red layer is front layer while the blue layer is the back layer. The 3D view of the PCB is shown in Figure 23.

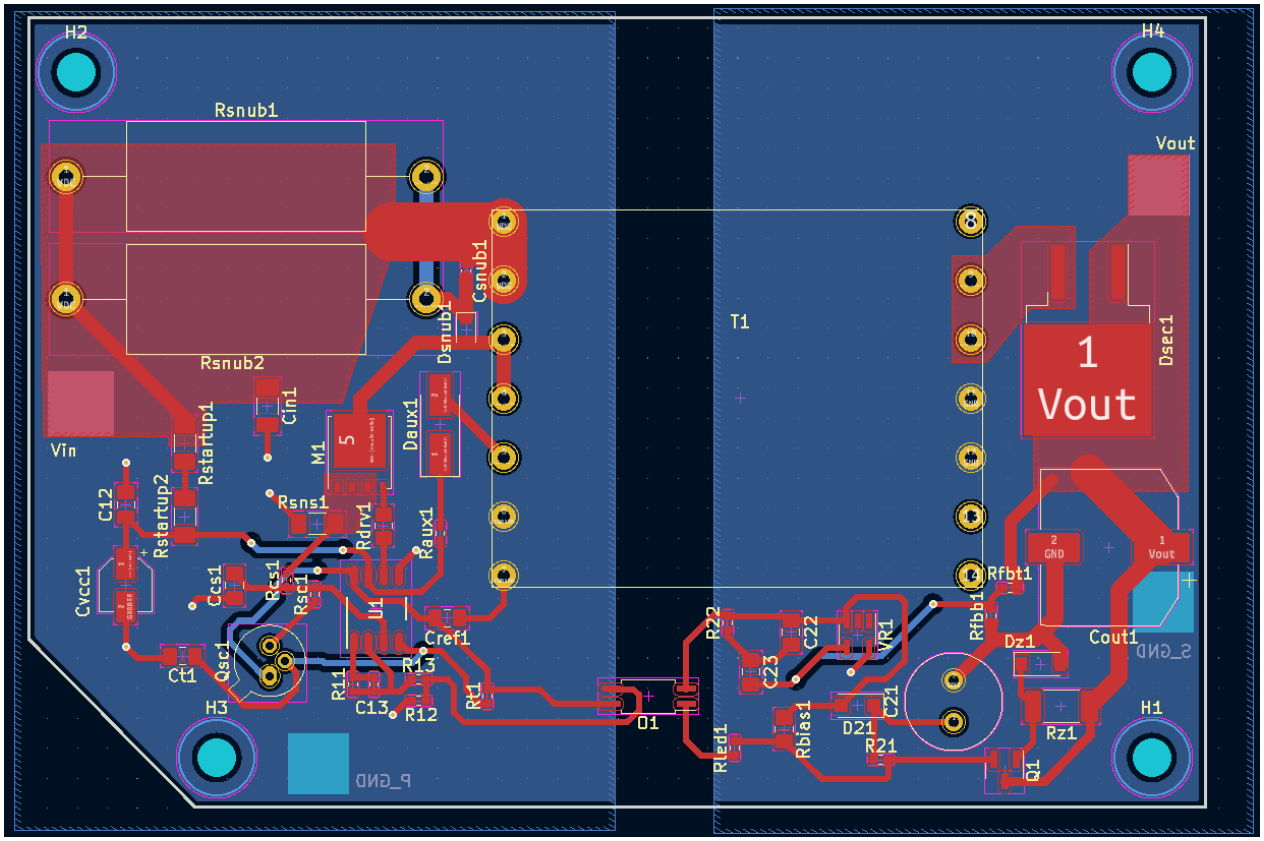

Figure 22: The PCB design in 2D view

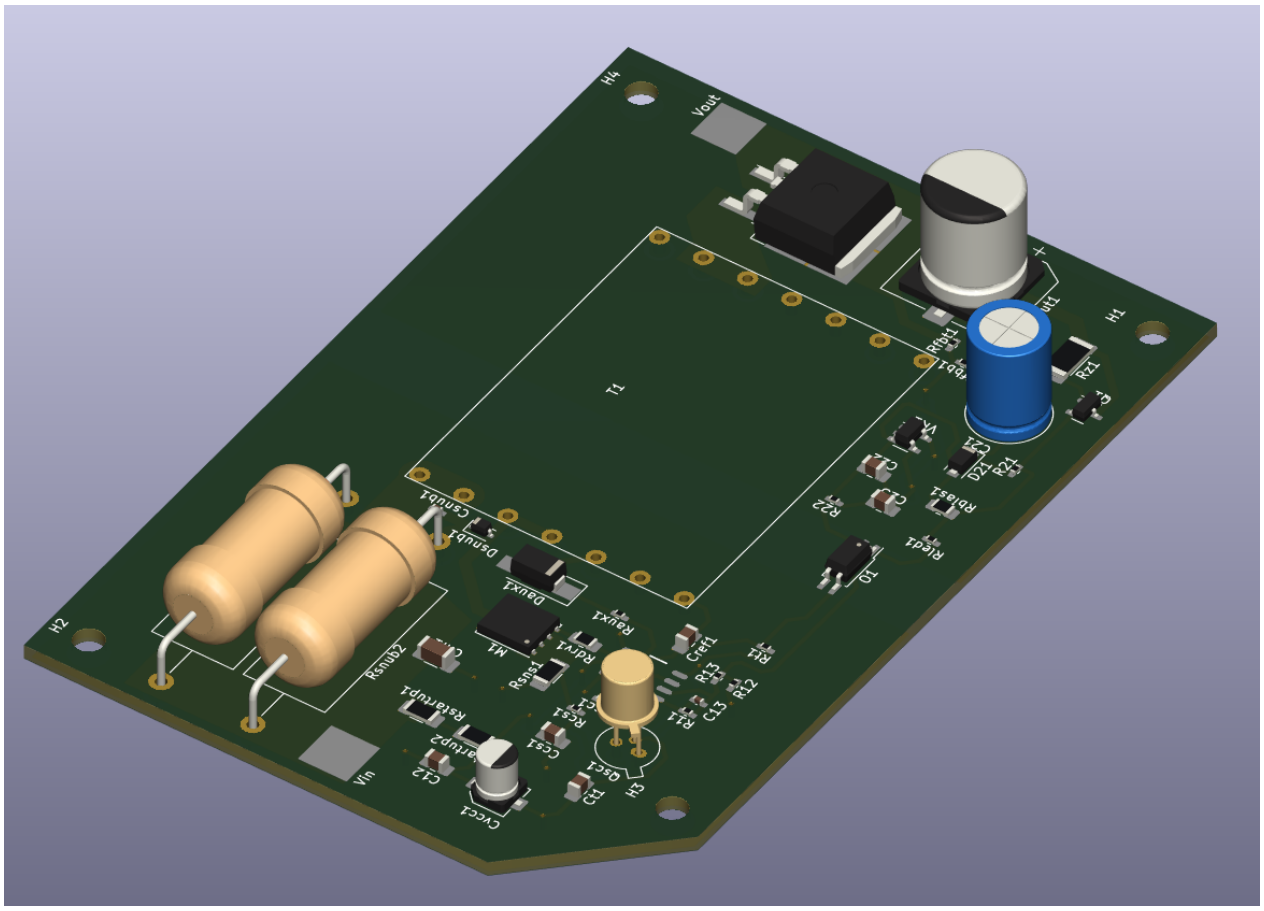

Figure 23: The PCB design in 3D view

We aimed industrial design bonus, so the box in Figure 24 is designed.

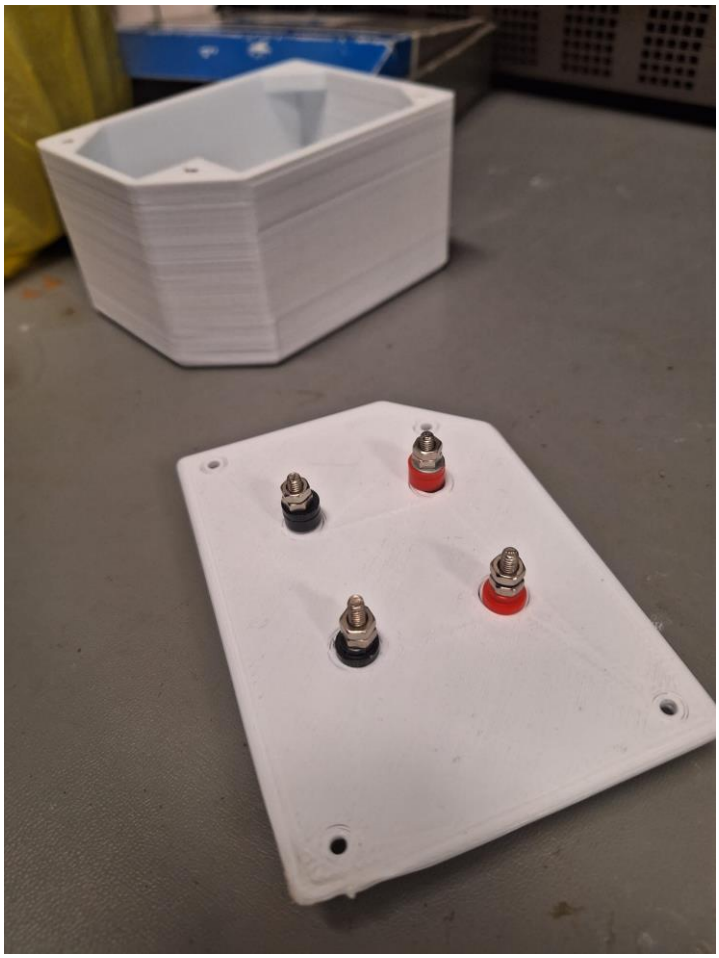

Figure 24: The box for the PCB

Tests

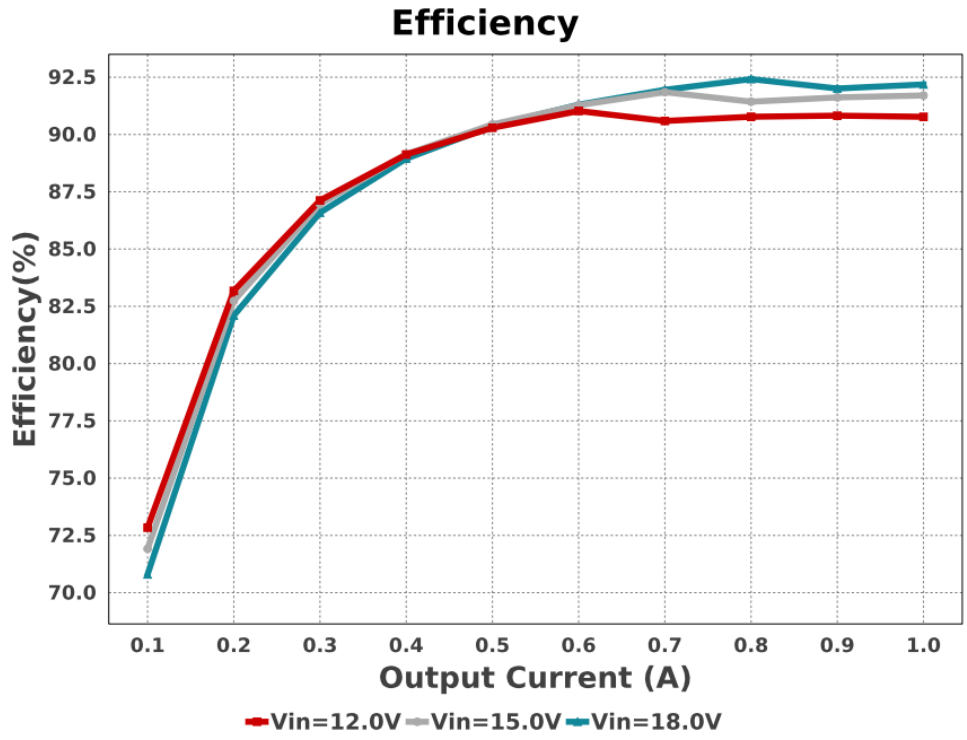

Figure 25: Closed-loop simulation efficiency result.

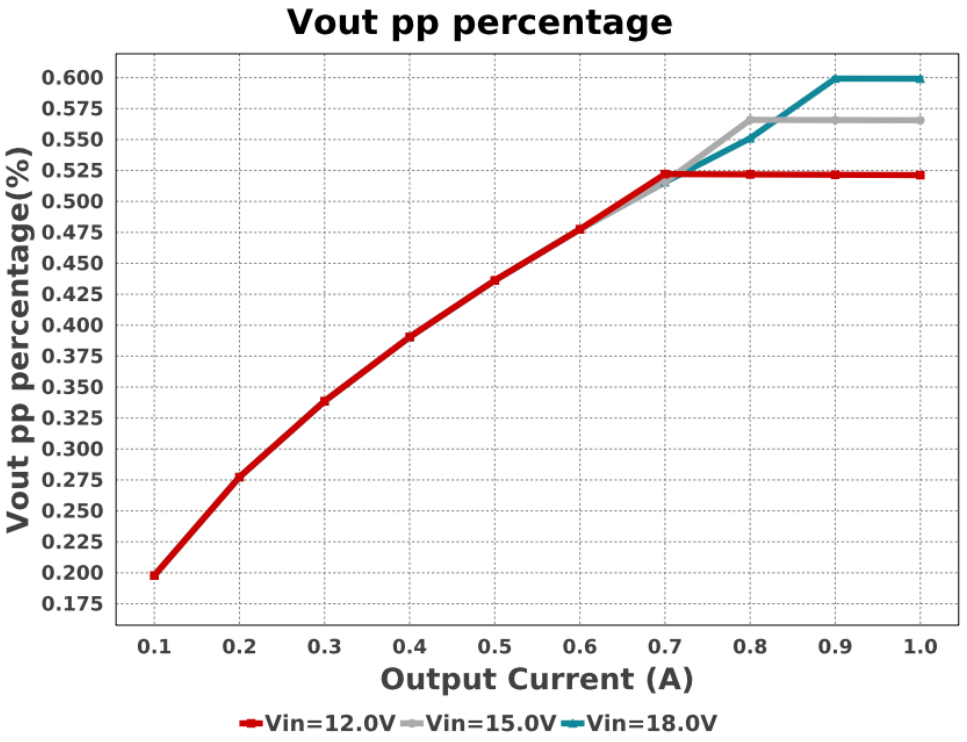

Figure 26: Closed-loop simulation output voltage ripple percentages.

The closed-loop simulations are operated in WEBench app, and Figure 25 and Figure 26 is obtained. It can be seen that the maximum voltage rippe occurs when the input voltage is 18V. The efficiency seems to be around at 90%; however, in the practical design, chosen core has higher core losses than the expected. Thus, the efficiency would probably be lower at the experiment, if the design was working.

Experimental Demo

Because the clearance on the PCB was not enough, the arcing between the lines observed. Although we tried to isolate the arcing points with silicon, other points started to arc. Due to time limitation, we were unable to design and fabricate a new PCB.

Conclusion

In conclusion, this report has effectively demonstrated the design process, computer simulations, and component selection for the flyback converter project. Through meticulous analysis and optimization, the design decisions were made with the primary goal of maximizing efficiency and reliability. Moreover, preliminary experimental results have shown promising outcomes, with measured magnetizing inductance and leakage inductance falling within acceptable ranges. The transformer, capacitor, and semiconductor components were carefully chosen to complement the overall design and meet performance requirements. In additon, the PCB and enclosure box designed for the target bonuses.

However, unfortunately, the design did not work. Even though the design is not working; however, we gained lots of useful experience. For example, we understood that the supply chain is a key factor in a hardware design job. Furthermore, we learned that some extra time needs to be allotted for bug fixes while planning the time schedule of a project.

References

[1] Ozdisan, "STB100N10F7 - MOSFET DIS.80A 100V N-CH TO263(D2PAK) SMT," [Online]. Available: https://ozdisan.com/guc-yari-iletkenleri/mosfetler/discrete-mosfetler/STB100N10F7/585449. [Accessed 05 05 2023].

[2] Ozdisan, "STTH3R06S - DIODE U.FAST Single 3A 600V SMT DO214AB (SMC)," [Online]. Available: https://ozdisan.com/guc-yari-iletkenleri/diyotlar-modul-diyotlar-ve-dogrultucular/genel-amacli-diyotlar/STTH3R06S/497200. [Accessed 05 05 2023].

[3] Ozdisan, "PKLH-400V470MJ200 - CAP.EL.47UF 400V 16X20 7.5MM 105C L.ESR 5000H," [Online]. Available: https://ozdisan.com/pasif-komponentler/kondansatorler/aluminyum-kondansatorler/PKLH-400V470MJ200/487365. [Accessed 05 05 2023].

[4] Digikey, "UCC2813DTR-1," [Online]. Available: https://www.digikey.com/en/products/detail/texas-instruments/UCC2813DTR-1/1911585. [Accessed 05 05 2023].