**EE 464**

**STATIC POWER CONVERSION-I**

**Spring 2022-2023**

**Complete Design Report**

**and Test Results**

**Autobots**

Mehmet Emre Doğan – 2374825

Metehan Küçükler – 2305068

Table of Contents

[Introduction 3](#_Toc138763143)

[Topology Selection 3](#_Toc138763144)

[Magnetic Design 4](#_Toc138763145)

[Component Selection 15](#_Toc138763146)

[Switching Device 15](#_Toc138763147)

[Secondary Diode: 15](#_Toc138763148)

[Output Capacitor: 15](#_Toc138763149)

[Controller IC: 15](#_Toc138763150)

[UPDATE TRANSFORMER: 16](#_Toc138763151)

[Tests 18](#_Toc138763152)

[PCB Design 18](#_Toc138763153)

[Conclusion 18](#_Toc138763154)

[References 19](#_Toc138763155)

# Introduction

This report presents the design decisions for the hardware project. Furthermore, it gives the details computer simulation results and component selection details. In addition, the report presents test results.

# Topology Selection

The converter needs to be isolated. Therefore, the alternatives are listed below:

* Flyback converter
* Forward converter
* Push-Pull converter

Among these converter topologies, the flyback converter is chosen as an appropriate converter for given requirements. When compared with other topologies, it is easier to increase the output voltage with Flyback due to its input-output voltage relation. Thus, it requires fewer turns ratio with the same duty cycle or, it requires less duty cycle with the same turns ratio. This may decrease the losses on copper or conduction losses of switching devices. Additionally, the Flyback converter requires fewer components than the other converter topologies, so its control is less complex.

diyagram içeren bir resim

Açıklama otomatik olarak oluşturuldu

Figure 1: TI Webench design

# Magnetic Design

1. The duty range of the converter is selected as [0.278 – 0.336] to match the design by the Ti Webench. According to the duty range determination, the turn ratio is calculated via the MATLAB code below.

clearvars

syms d turnsRatio

v\_o = 48

d\_min = 0.278; v\_d\_minduty = 18;

d\_max = 0.366; v\_d\_maxduty = 12

turnsRatio\_minduty = ( (d\_min/(1-d\_min)) \* (v\_d\_minduty/v\_o) )^-1

turnsRatio\_maxduty = ( (d\_max/(1-d\_max)) \* (v\_d\_maxduty/v\_o) )^-1

According to the code above, the transformer turns ratio (Ns/Np) is calculated as 6.93.

2. The available cores and coil formers are investigated. Firstly, due to its available stock number is high, PCB5530-FA is selected as the coil former. Therefore, the compatible core 0P45530EC is selected as the transformer core.
3. Using the MATLAB code below, the primary turn number is found 1.14, while the secondary turn number is 7.93. The magnetizing inductance is 8 uH. 1.14 turn makes no sense and increasing the inductance a little bit makes no harm. Therefore, the primary turns are made into 2 turns. The corresponding secondary turns number then becomes 13.89, which is pretty close to 14. Hence, the primary wounded 2 turns while the secondary wound 14 turns.

U\_o = v\_o;

v\_t = d\_max;

f\_sw = 100e3;

i\_out = 1;

i\_avgSec = i\_out/(1-v\_t);

xformerCurrRipple = 0.5; % percent

L\_sec = (U\_o\*(1-v\_t))/(xformerCurrRipple\*i\_avgSec\*f\_sw)

L\_pri = L\_sec/(turnsRatio\_maxduty^2)

% (turnsRatio\_maxduty^2)\*2.814e-6

syms priTurns secTurns

AL = 6130e-9 % nH/T^2; minimal

priTurns = double(solve(L\_pri == AL\*priTurns^2))

secTurns = double(solve(L\_sec == AL\*secTurns^2))

% make sure core is not saturated

ampTurns = i\_out\*secTurns

1. According to the AWG table, the secondary should be wounded using 2 parallel 24 AWG wires. The primary, on the other hand, 2 parallel 17 AWG wires will be used. The AWG calculation is done by the snippet below.

p\_o = i\_out \* v\_o

i\_in\_max = v\_o/v\_d\_maxduty

% Primary selected as 17 AWG

selectedAWGRating\_pri = 2.9;

primaryDiameter\_mm = 1.15062;

cableAreaPri\_mm2 = 1.04;

% Secondary selected as 24 AWG

selectedAWGRating\_sec = 0.577;

secondaryDiameter\_mm = 0.5;

cableAreaSec\_mm2 = 0.327;

primaryRadius\_mm = primaryDiameter\_mm/2

secondaryRadius\_mm = secondaryDiameter\_mm/2

num\_of\_paralles\_sec = i\_out/selectedAWGRating\_sec

num\_of\_paralles\_pri = i\_in\_max/selectedAWGRating\_pri

1. According to the code below, the fill factor is 1.75%, which is low but reasonable.

windowArea\_mm2 = 537;

priTurns = ceil(priTurns(priTurns>0))

secTurns = ceil(secTurns(secTurns>0))

num\_of\_paralles\_pri = ceil(num\_of\_paralles\_pri)

num\_of\_paralles\_sec = ceil(num\_of\_paralles\_sec)

primaryArea\_mm2 = priTurns\*num\_of\_paralles\_pri\*cableAreaPri\_mm2

secondaryArea\_mm2 = secTurns\*num\_of\_paralles\_sec\*cableAreaSec\_mm2

totalCableArea\_mm2 = primaryArea\_mm2 + secondaryArea\_mm2

fillFactor\_perc = 100\*totalCableArea\_mm2/windowArea\_mm2

1. Cable resistance calculation is done by the code below:

skinDepth\_mm = 75/sqrt(f\_sw)

innerRadiusPri\_mm = primaryRadius\_mm - skinDepth\_mm

hollowAreaPri\_mm2 = pi\*innerRadiusPri\_mm^2

effectiveAreaPri = cableAreaPri\_mm2 - hollowAreaPri\_mm2

innerRadiusSec\_mm = secondaryRadius\_mm - skinDepth\_mm

hollowAreaSec\_mm2 = pi\*innerRadiusSec\_mm^2

effectiveAreaSec = cableAreaSec\_mm2 - hollowAreaSec\_mm2

% calculate the ratios to convert DC resistance to AC resistance

DC\_to\_AC\_ratio\_pri = cableAreaPri\_mm2/effectiveAreaPri

DC\_to\_AC\_ratio\_sec = cableAreaSec\_mm2/effectiveAreaSec

windingLengthPerTurn\_mm = 68.2

ohms\_per\_meter = 212.872 / 1e3

primaryLength\_m = windingLengthPerTurn\_mm \* priTurns \* 1e-3

secondaryLength\_m = windingLengthPerTurn\_mm \* secTurns \* 1e-3

primary\_DC\_resistance\_ohm = ohms\_per\_meter \* primaryLength\_m / num\_of\_paralles\_pri

secondary\_DC\_resistance\_ohm = ohms\_per\_meter \* secondaryLength\_m / num\_of\_paralles\_sec

According to the results the snippet outputs, the primary AC Resistance is 22.2 mOhm while the secondary AC Resistance is 58.2 mOhm.

1. Copper losses are calculated by the code below:

primary\_AC\_resistance\_ohm = primary\_DC\_resistance\_ohm\*DC\_to\_AC\_ratio\_pri

secondary\_AC\_resistance\_ohm = secondary\_DC\_resistance\_ohm\*DC\_to\_AC\_ratio\_sec

resistancePri\_ohm = vpa(primary\_AC\_resistance\_ohm \* u.Ohm)

resistanceSec\_ohm = vpa(secondary\_AC\_resistance\_ohm \* u.Ohm)

copperLossPri = vpa(unitConvert((i\_in\_max\*u.A)^2 \* resistancePri\_ohm, u.W))

copperLossSec = vpa(unitConvert((i\_out\*u.A)^2 \* resistanceSec\_ohm, u.W))

copperLoss\_W = copperLossPri + copperLossSec

According to the calculations, the total copper losses are **0.41 W**.

1. Core losses are calculated by the code below:

wattLoss\_mW\_cm3 = 142\*u.mW/u.cm^3

volume\_mm3 = 52000;

volume\_cm3 = vpa(unitConvert(volume\_mm3\*u.mm^3, u.cm^3))

coreLoss\_w = vpa(unitConvert(wattLoss\_mW\_cm3 \* volume\_cm3, u.W))

**Core Loss: 7.38 W**

The core loss is way greater than the copper loss. Therefore, the efficiency will suck. However, the other available cores resulted in high leakage inductance experimentally. This core gives the best results in terms of leakage inductance. Therefore, we will proceed with this core, even though its efficiency sucks.

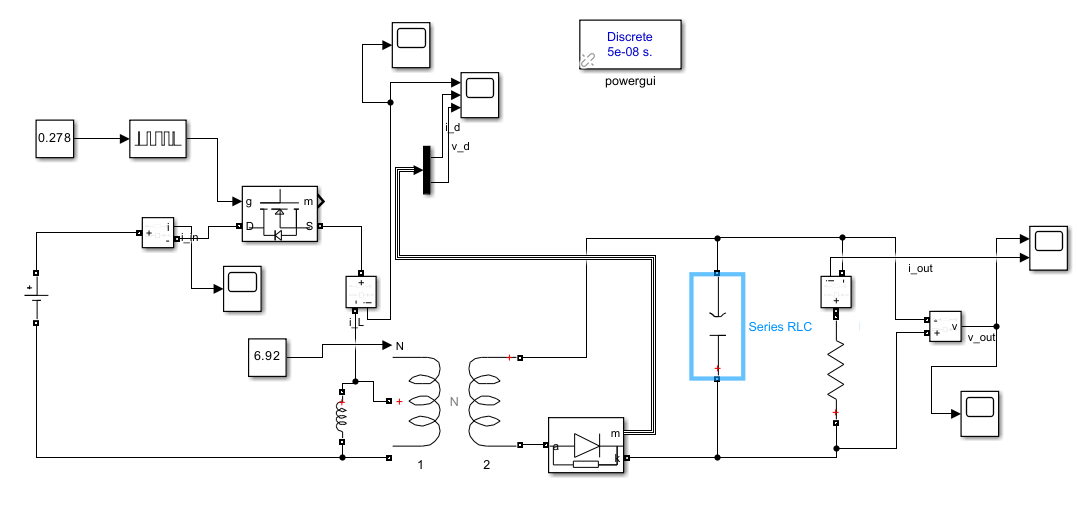
1. The open-loop flyback design is simulated on Simulink as shown in Figure 2. The circuit is simulated at its edges, namely, 12V input voltage and 0.366 duty and 18V input voltage and 0.278 duty. The simulation results are shown in Figures 3-6 for 0.278 duty and Figures 7-10 for 0.366 duty.

Figure 2: The Flyback converter in Simulink

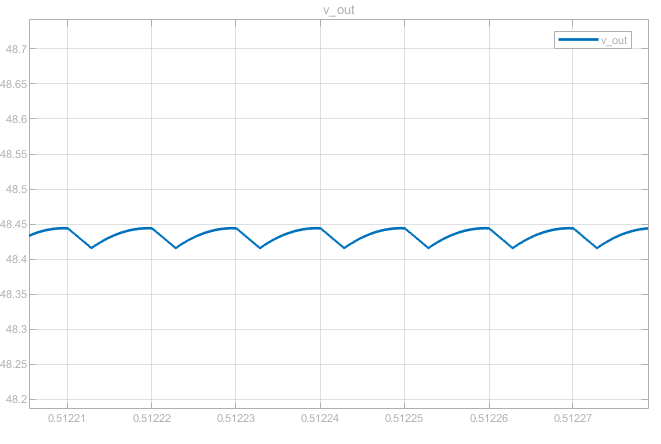


Figure 3: Output voltage ripple for 0.278 duty

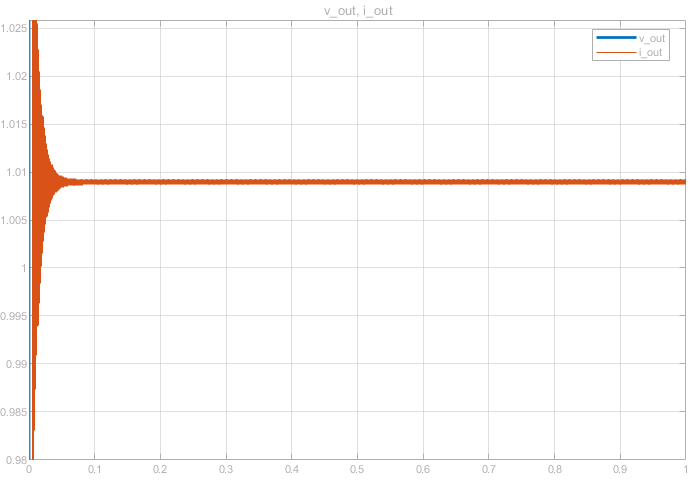
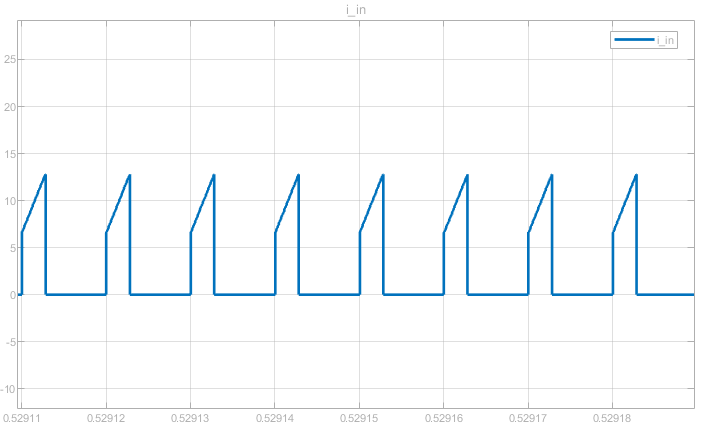


Figure 4: Output current waveform for 0.278 duty



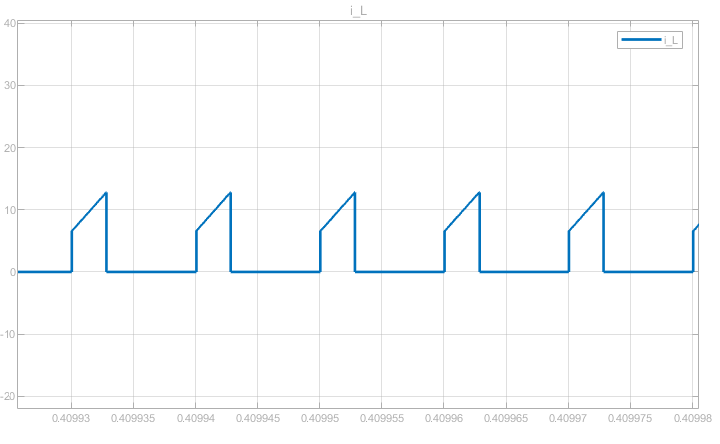


Figure 5: Input current waveform for 0.278 duty

Figure 6: Transformer primary current waveform for 0.278 duty

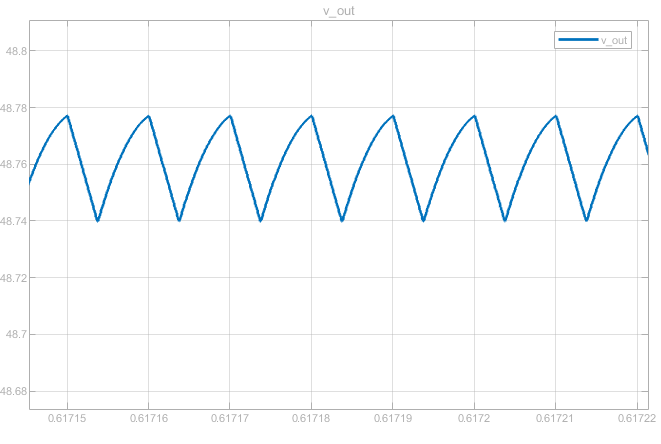


Figure 7: Output voltage ripple for 0.366 duty

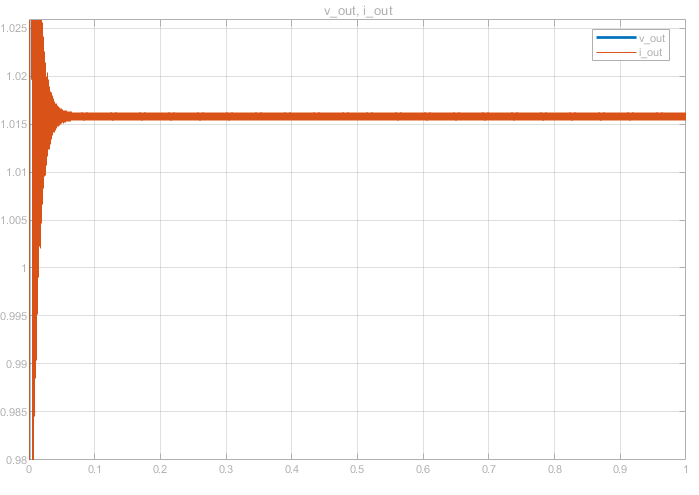


Figure 8: Output current waveform for 0.366 duty

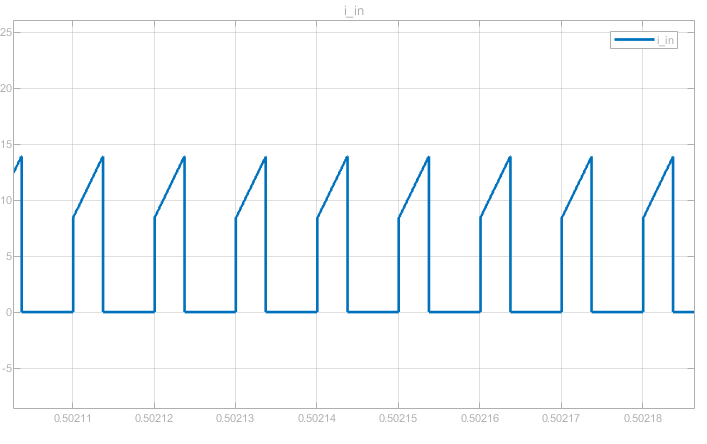


Figure 9: Input current waveform for 0.366 duty

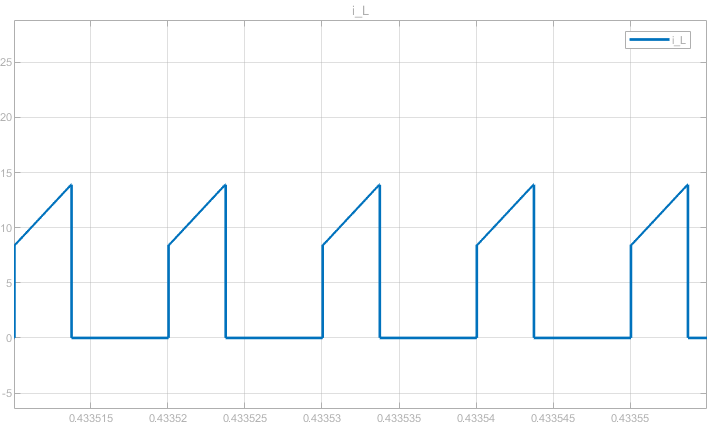


Figure 10: Transformer primary current waveform for 0.366 duty

1. The minimum load current to avoid DCM is calculated with the code below:

Lm = 8\*10^-6; f\_sw = 100\*10^3;

% DCM

% for Vs = 12V

Vs = 12; D = 0.366;

deltaI\_lm = Vs\*D/(Lm\*f\_sw);

P\_min = Vs^2 \* D^2 / (2\*Lm\*f\_sw);

I\_load\_min = P\_min / 48

% for Vs = 18V

Vs = 18; D = 0.278;

deltaI\_lm = Vs\*D/(Lm\*f\_sw);

P\_min = Vs^2 \* D^2 / (2\*Lm\*f\_sw);

I\_load\_min = P\_min / 48

Minimum load current to operate in CCM when input is 12V = 0.251mA

Minimum load current to operate in CCM when input is 18V = 0.326mA

The maximum current that can flow through the transformer is calculated with the code below:

% max I\_Lm current occurs when input voltage is 12V and at 100% load

Vs = 12; D = 0.366;

turnsRatio = 6.92; R = 48;

deltaI\_lm = Vs\*D/(Lm\*f\_sw);

P\_out = Vs^2 \* D^2 \* turnsRatio^2 / ((1-D)^2 \* R);

I\_Lm\_max = deltaI\_lm/2 + P\_out/(Vs\*D)

Current can rise up to the 13.645A while converter is working with 100% load and 12V input voltage.

diyagram, şematik içeren bir resim

Açıklama otomatik olarak oluşturuldu

Figure 11: Simulation of the converter with parasitic elements of transformer and switching device.

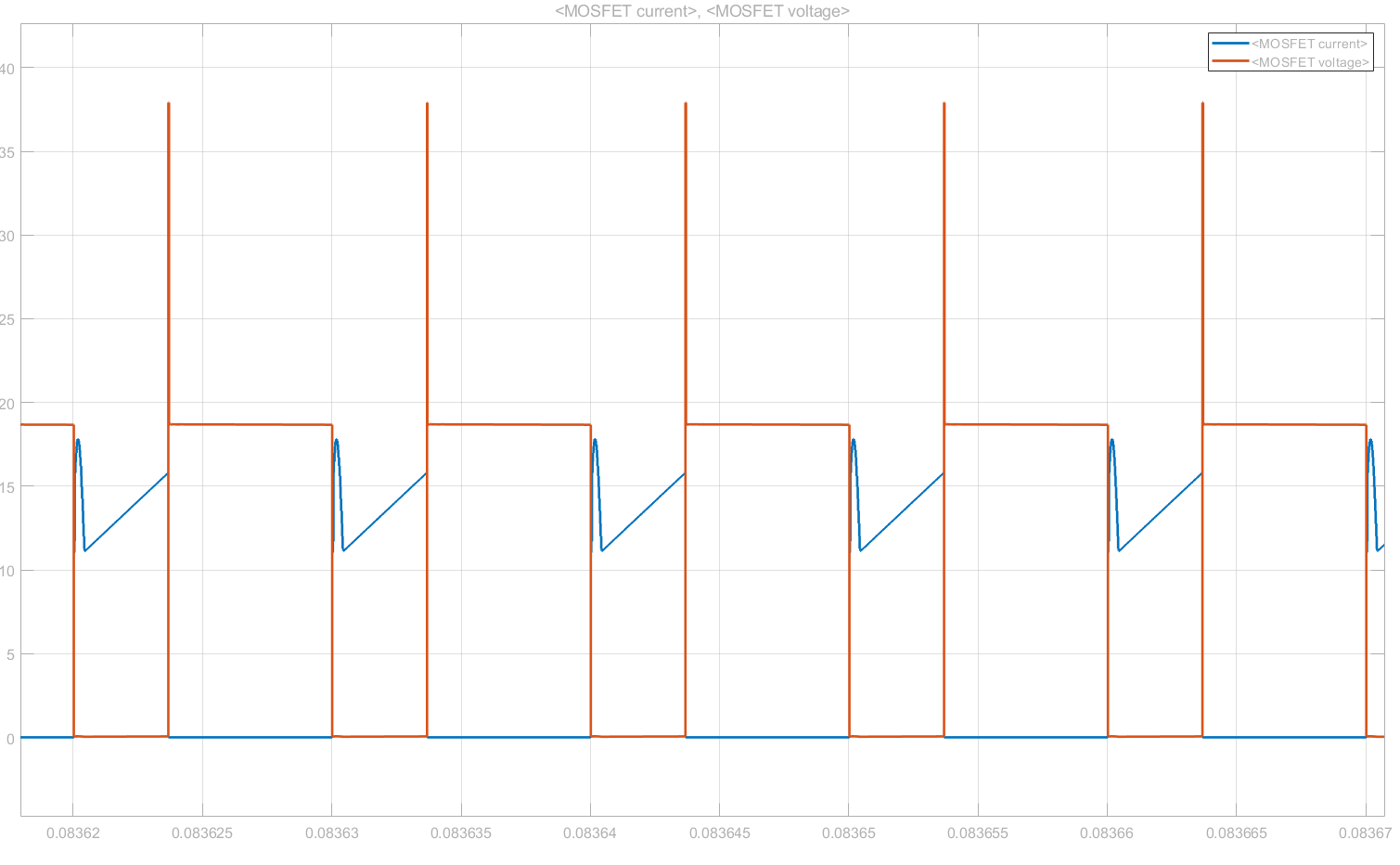


Figure 12: Voltage and current waveforms of MOSFET with parasitic elements.

In Figure 12, it can be seen that, due to parasitic inductances, there are voltage spikes on MOSFET while switching. Because of leakage inductance, a snubber must be used to discharge the leakage inductance. Snubber design is taken from the recommended design of Webench.

The flyback converter is simulated with parasitic elements and non-ideal switching devices as shown in Figure 13.

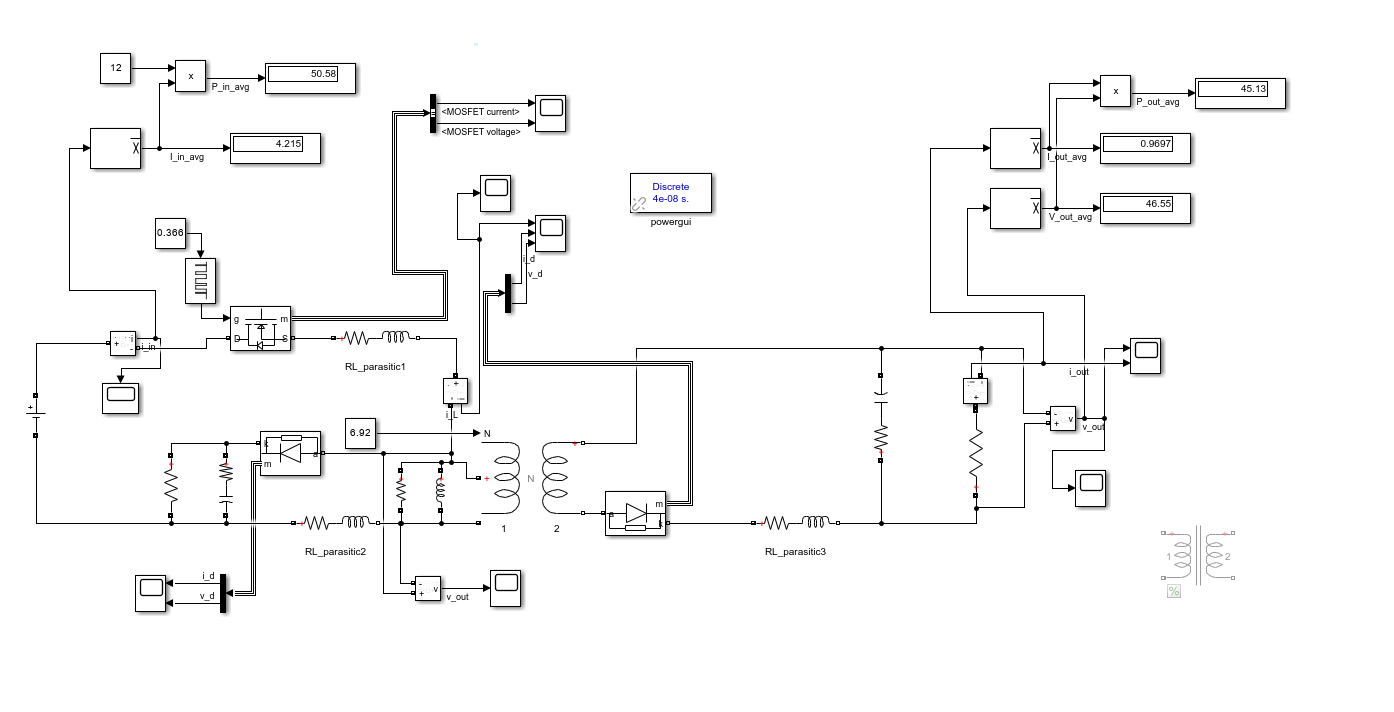


Figure 13: Simulation design for efficiency test.

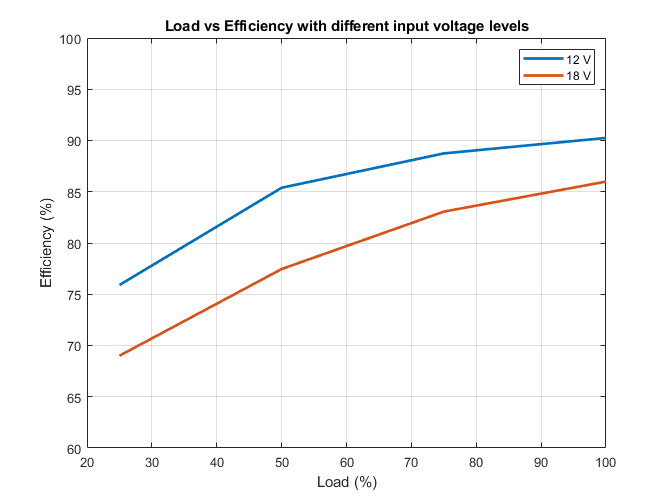


Figure 14: Efficiency vs Load curves for different voltage input levels.

Table 1: Simulation result of efficiency values for different

input voltage and load conditions.

|  |  |  |
| --- | --- | --- |
| Load (%) | Efficiency (%) | |
| 12V | 18V |
| 25 | 75.9 | 69 |
| 50 | 85.39 | 77.46 |
| 75 | 88.74 | 83.06 |
| 100 | 90.25 | 85.99 |

Table 2: Calculated efficiency values without snubber losses.

|  |  |  |
| --- | --- | --- |
| Load (%) | Efficiency (%) | |
| 12V | 18V |
| 25 | 87.7 | 87.89 |
| 50 | 92.78 | 93.03 |
| 75 | 94.3 | 94.62 |
| 100 | 94.94 | 95.33 |

The efficiency of the flyback converter decreases with less load since core loss and snubber losses become dominant. Also, when the input voltage increases, the losses on the switching device increase quadratically; thus, the converter becomes less efficient with a higher input voltage. Lastly, how inefficient is snubber can be seen by comparing two results.

# Component Selection

### Switching Device

Peak switching current and voltage can be calculated equations below:

V\_sw = Vs + 1/turnsRatio\*48

I\_sw = 1./(1-duty).\*turnsRatio.\*I\_out\_avg + 1/turnsRatio.\*

(1-duty)./2./L\_pri./f\_sw\*48

Switching voltages are calculated as 18.94V and 24.94V, respectively with 12V and 18V input voltage, and the maximum switching current is calculated as 13.65A. However, due to leakage inductances and parasitic elements, there are voltage spikes while switching. Thus, also it can be seen in Webench design, a Mosfet with 80V rated voltage and 100A rated current is selected [1]. For less rated voltages it is easy and cheap to find high current rated Mosfets, which also results in fewer losses on Mosfet due to less Rds value.

### Secondary Diode:

V\_d\_max = Vs\*turnsRatio + 48

I\_d\_max = I\_sw./turnsRatio

By using the above equations, the maximum voltage on the diode is found as 131.04V and 172.56V, respectively with 12V and 18V input voltage, and the maximum current is calculated as 1.976A. The voltage rating of the diode should be selected higher because the effect of voltage spikes increases with the turns ratio at the secondary side. Thus, the diode is selected with a 600V rated voltage and 3A rated current with a forward voltage drop of 1.0V [2].

### Output Capacitor:

The maximum allowed voltage ripple at the output is 3%.

C\_min = duty/f\_sw/R/ripple

The minimum capacitance value of the output capacitor is found as 2.54µF with the equation above. However, the output voltage is 48V and to be safe rated voltage of the capacitor should be higher. A high voltage-rated capacitor is found as an aluminum capacitor which has high ESR values compared with other types. Found capacitors in the market have high voltage ratings, so they have also high ESR values. Because ESR values become dominant on output ripple, a capacitor with high capacitances is selected. The selected capacitor has 47µF capacitance and 2Ω ESR. The effect of ESR can be calculated equation below:

V\_ESR = ESR \* I\_out\_avg

The ripple due to ESR can be around 2V when a single capacitor is used. Thus, four of the selected capacitors [3] must be connected in parallel.

### Controller IC:

UCC2813DTR-1 is selected which is appropriate for Webench’s design. It is a current-mode PWM controller that can drive the gate of the Mosfet with respect to sensed current and output voltage [4].

### UPDATE TRANSFORMER:

The detailed calculation of the transformer’s turn ratio, cable parameters, core, magnetizing inductance, etc. is given in the magnetic design section.

#### Experimental results of transformer on first try:

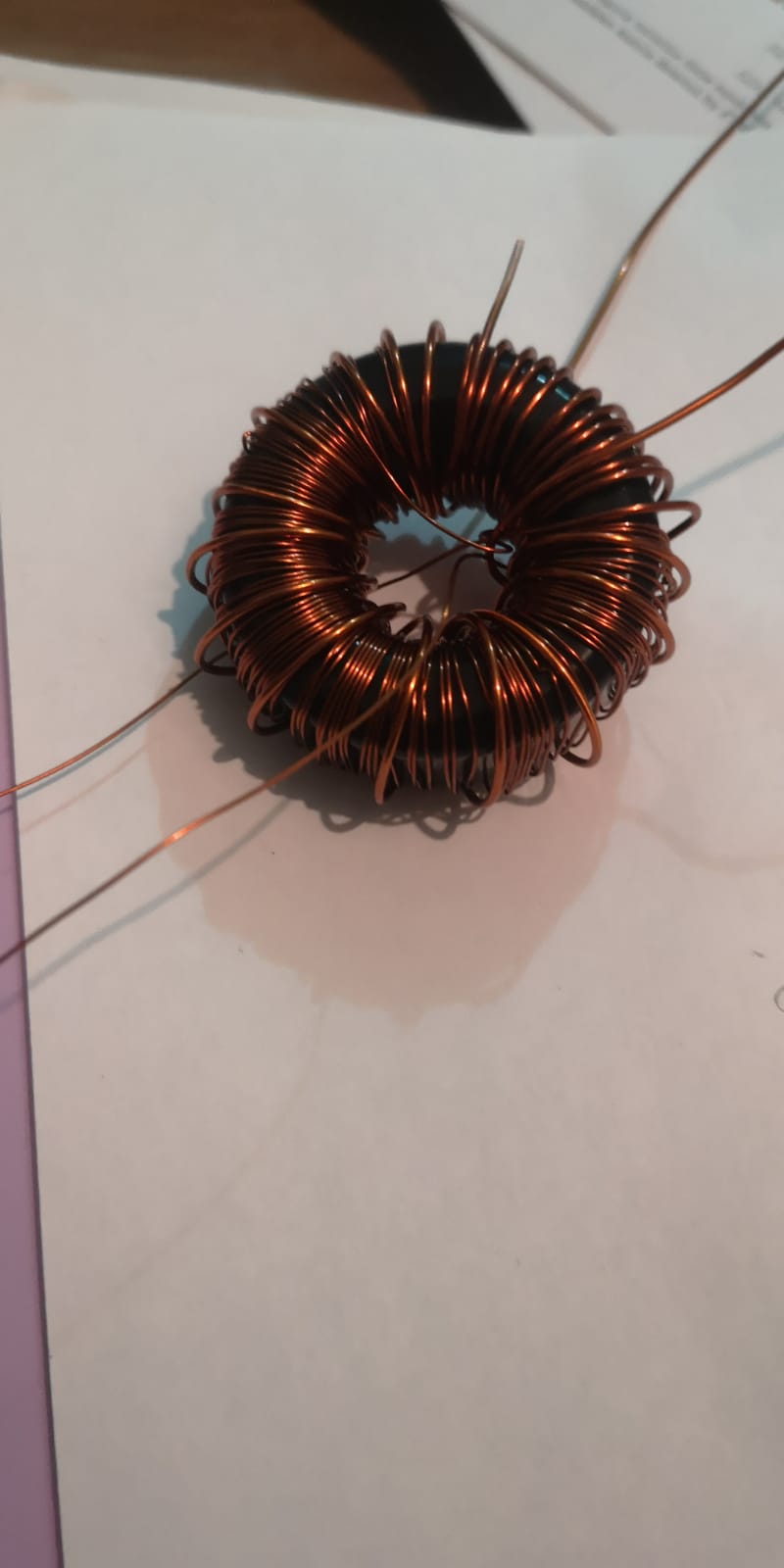


Figure 15: Wound transformer for initial experiments.

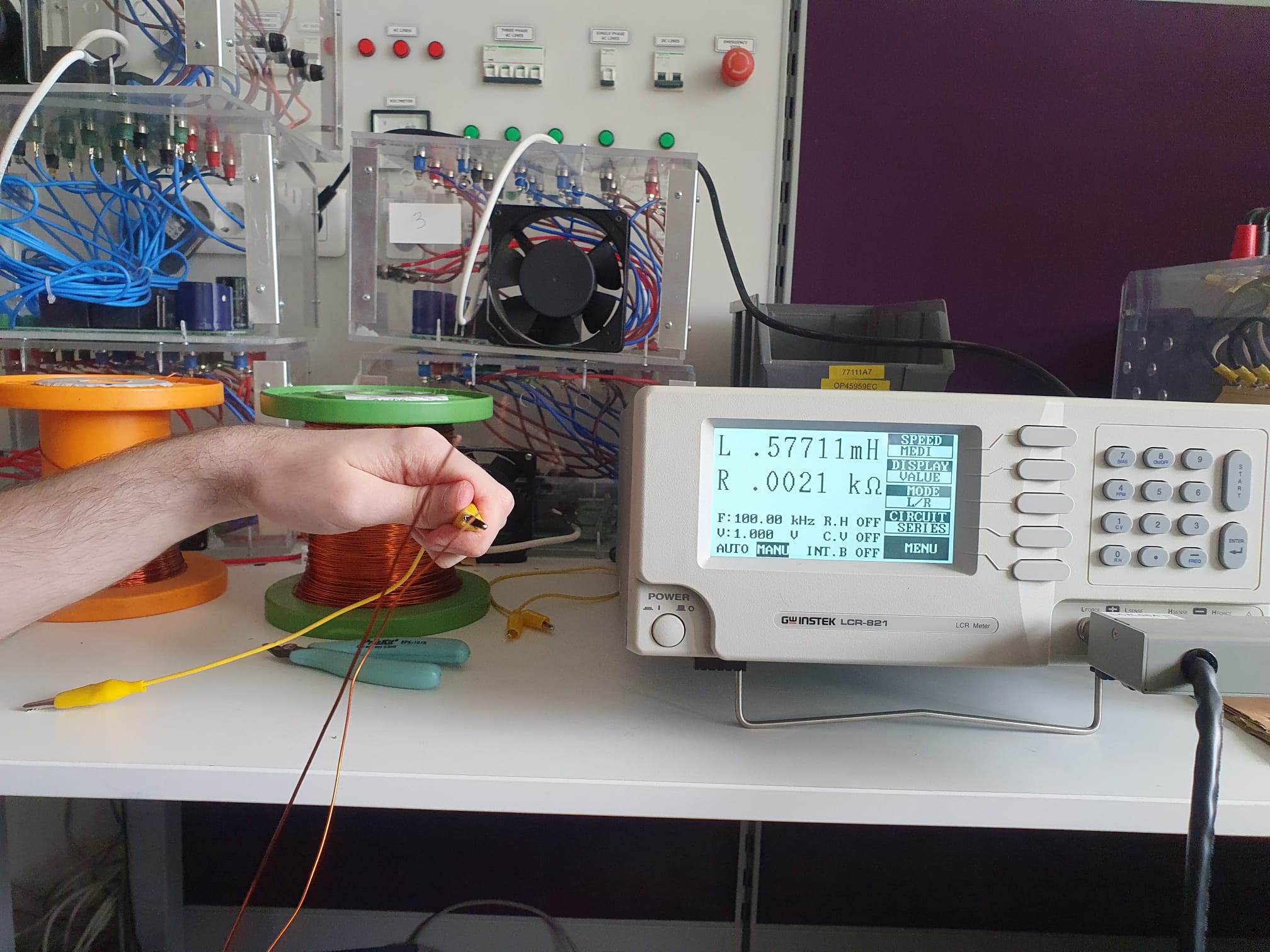


Figure 16: Primary is open circuited to measure leakage + magnetizing inductance at secondary.

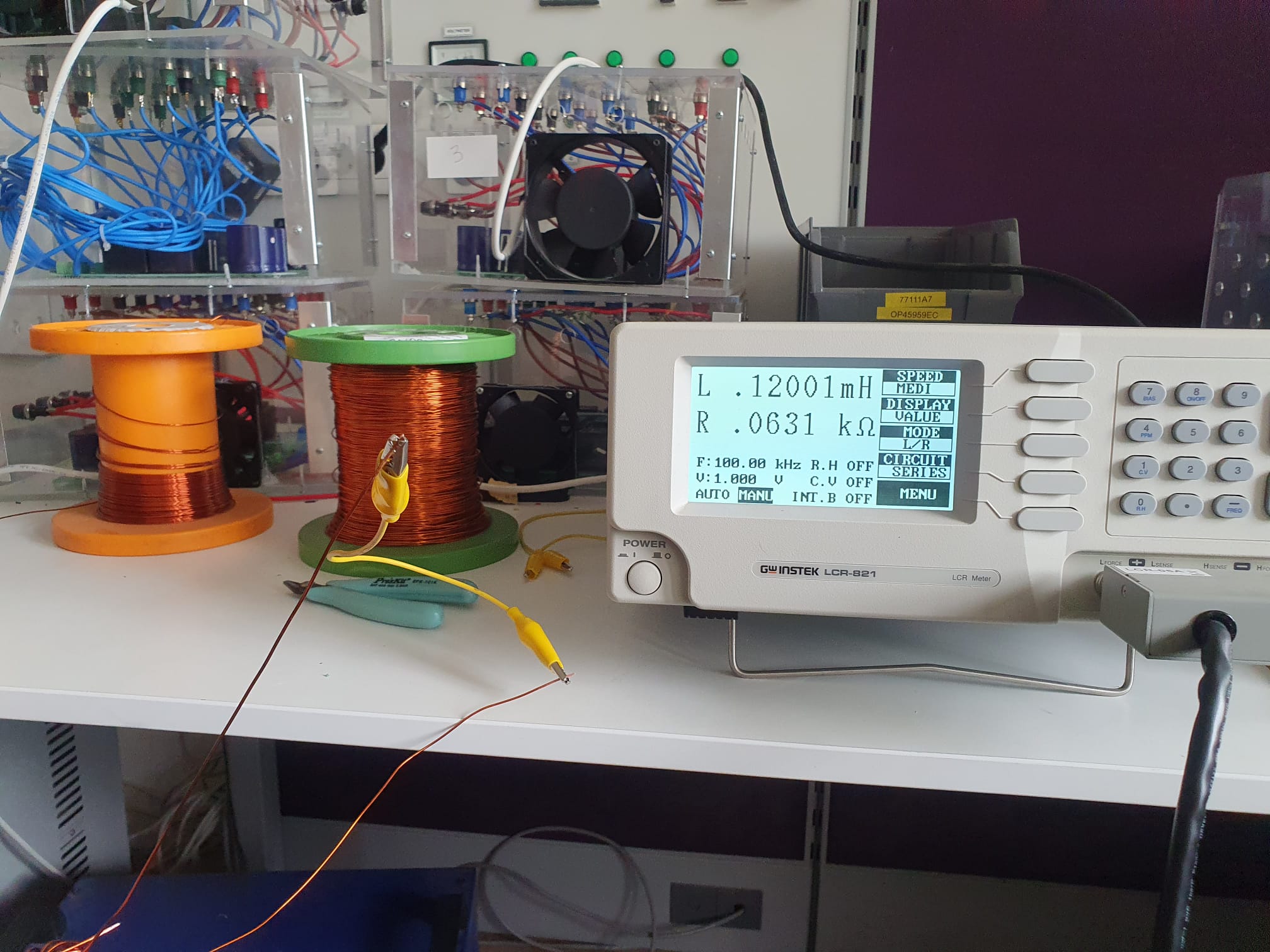


Figure 17: Primary is short circuited to measure leakge inductance at secondary.

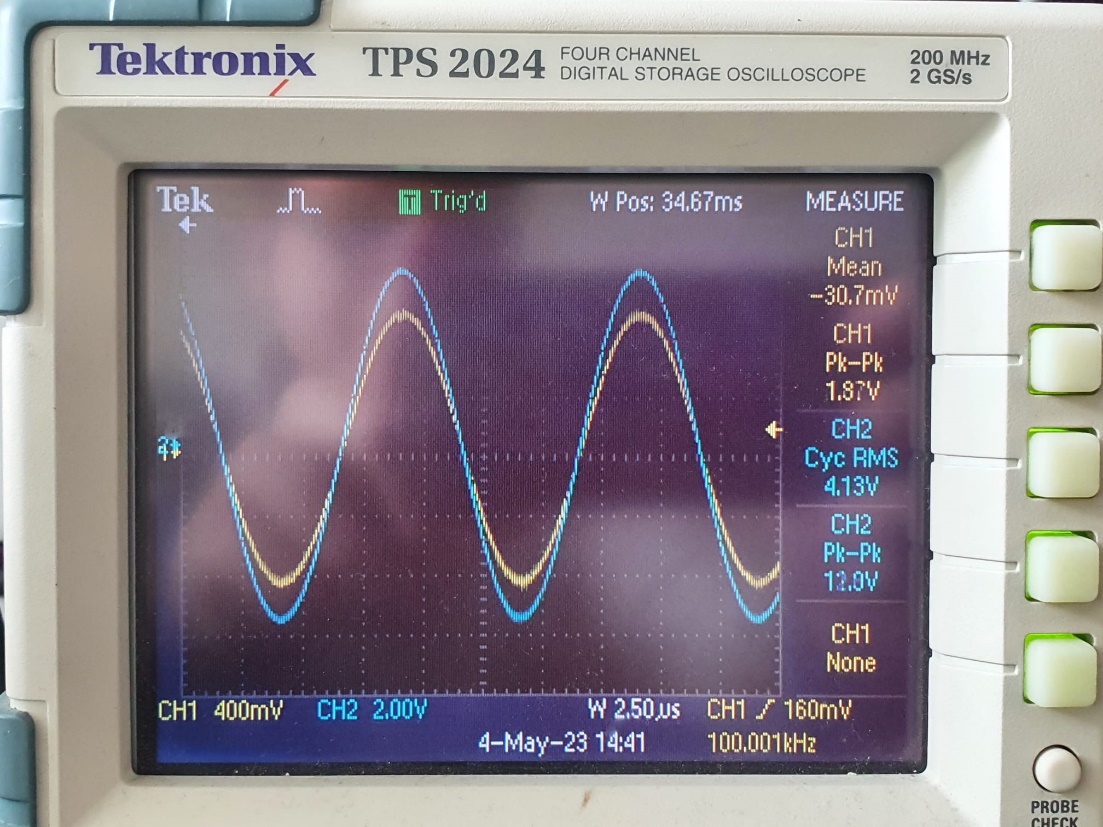


Figure 18: Input and output voltage ratio to observe turns ratio.

The leakage inductance at the secondary is measured as 120μH and by subtracting this value from the total inductance measured as 577μH, magnetizing inductance is measured as 457μH. Also, the turns ratio, which is the ratio of output and input voltage, is measured as 6. It can be seen that the leakage inductance is too high than the expected values. This may be caused by the toroid core because winding around a toroid core is difficult and results in high leakage which can be seen also Figure 15.

Some additional plots are given on Page 4 of Appendix – 2.

# Tests

Efficiency figures, start-up, ripple content, step-load response, low-voltage operation and discussions

# PCB Design

# Conclusion

In conclusion, this report has effectively demonstrated the design process, computer simulations, and component selection for the flyback converter project. Through meticulous analysis and optimization, the design decisions were made with the primary goal of maximizing efficiency and reliability. Moreover, preliminary experimental results have shown promising outcomes, with measured magnetizing inductance and leakage inductance falling within acceptable ranges. The transformer, capacitor, and semiconductor components were carefully chosen to complement the overall design and meet performance requirements. This comprehensive approach to the flyback converter design ensures that the final product is robust, efficient, and suitable for the required range of voltage and current.

# References

|  |  |
| --- | --- |
| [1] | Ozdisan, "STB100N10F7 - MOSFET DIS.80A 100V N-CH TO263(D2PAK) SMT," [Online]. Available: https://ozdisan.com/guc-yari-iletkenleri/mosfetler/discrete-mosfetler/STB100N10F7/585449. [Accessed 05 05 2023]. |
| [2] | Ozdisan, "STTH3R06S - DIODE U.FAST Single 3A 600V SMT DO214AB (SMC)," [Online]. Available: https://ozdisan.com/guc-yari-iletkenleri/diyotlar-modul-diyotlar-ve-dogrultucular/genel-amacli-diyotlar/STTH3R06S/497200. [Accessed 05 05 2023]. |
| [3] | Ozdisan, "PKLH-400V470MJ200 - CAP.EL.47UF 400V 16X20 7.5MM 105C L.ESR 5000H," [Online]. Available: https://ozdisan.com/pasif-komponentler/kondansatorler/aluminyum-kondansatorler/PKLH-400V470MJ200/487365. [Accessed 05 05 2023]. |
| [4] | Digikey, "UCC2813DTR-1," [Online]. Available: https://www.digikey.com/en/products/detail/texas-instruments/UCC2813DTR-1/1911585. [Accessed 05 05 2023]. |