EE 464
STATIC POWER CONVERSION-I
Spring 2022-2023

Homework 2
Complete Simulation Report

Mehmet Emre Doğan – 2374825

Metehan Küçükler – 2305068

Table of Contents

Introduction

This report explains the design decisions for the hardware project. Furthermore, it presents the details of the Magnetic Design of the Isolated Power Supply and the simulation results for the selected topology.

Topology Selection

The converter needs to be isolated. Therefore, the alternatives are listed below:

➤ Flyback converter
➤ Forward converter
➤ Push-Pull converter

Among these converter topologies, flyback converter is chosen as an appropriate converter for given requirements. When compared with other topologies, it is easier to increase the output voltage with Flyback due to its input-output voltage relation. Thus, it requires less turns ratio with same duty cycle or, it requires less duty cycle with same turns ratio. This may decrease the losses on copper or conduction losses of switching devices. Additionally, Flyback converter requires less component than the other converter topologies, so its control is less complex.
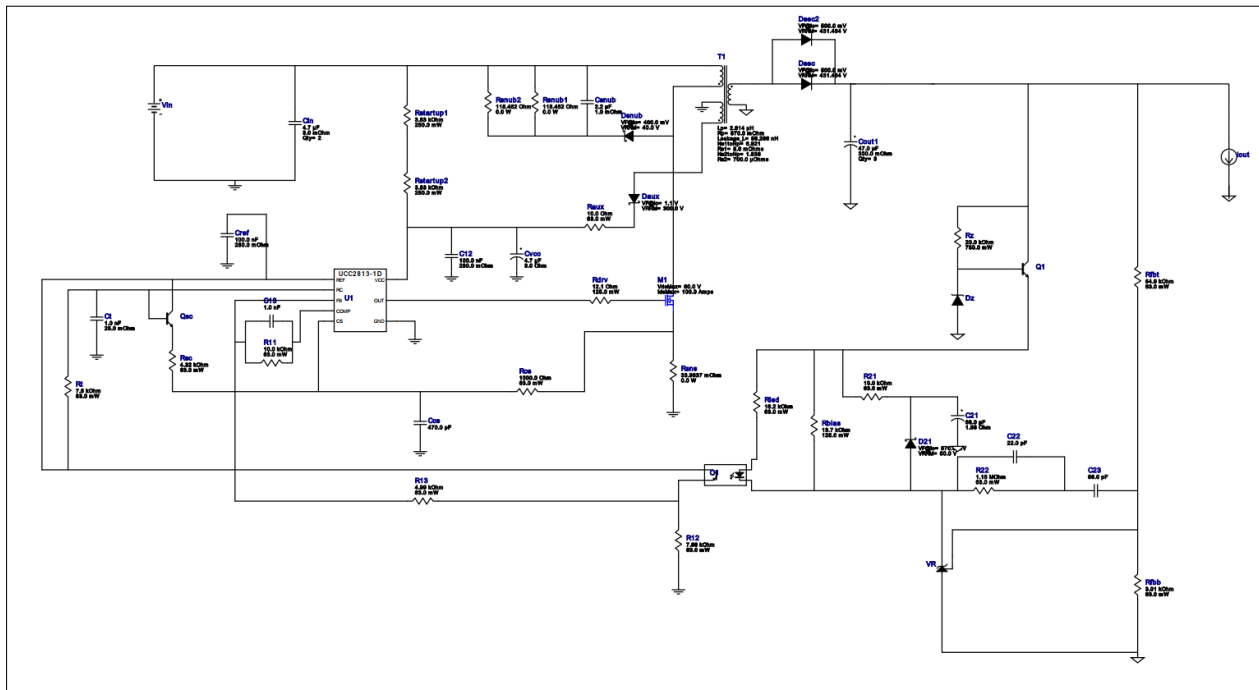

Figure 1: TI Webench design

Magnetic Design

a) The duty range of the converter is selected as [0.278 – 0.336] to match the design by the Ti Webench. According to the duty range determination, the turn ratio is calculated via the MATLAB code below.

```
clearvars
syms d turnsRatio
v_o = 48
d_min = 0.278; v_d_minduty = 18;
d_max = 0.366; v_d_maxduty = 12
turnsRatio_minduty = ( (d_min/(1-d_min)) * (v_d_minduty/v_o) )^-1
turnsRatio_maxduty = ( (d_max/(1-d_max)) * (v_d_maxduty/v_o) )^-1
```

According to the code above, the transformer turns ratio (N_s/N_p) is calculated as 6.93.

b)
1. The available cores and coil formers are investigated. Firstly, due to its available stock number is high, PCB5530-FA is selected as the coil former. Therefore, the compatible core 0P45530EC is selected as the transformer core. However, after calculations, it is seen that this core is overkill. Afterward, **79440A7 toroidal core is selected** due to its high stock number and wide window area. A wide window area makes the wounding procedure easier.
2. Using the MATLAB code below, the primary turn number is 13, while the secondary turn number is 87. The magnetizing inductance is 8 uH.

```
U_o = v_o;
v_t = d_max;
f_sw = 100e3;
i_out = 1;
i_avgSec = i_out/(1-v_t);
xformerCurrRipple = 0.5; % percent
L_sec = (U_o*(1-v_t))/(xformerCurrRipple*i_avgSec*f_sw)
L_pri = L_sec/(turnsRatio_maxduty^2)
% (turnsRatio_maxduty^2)*2.814e-6
```

```
syms priTurns secTurns
AL = 51e-9 % nH/T^2; minimal
priTurns = double(solve(L_pri == AL*priTurns^2))
secTurns = double(solve(L_sec == AL*secTurns^2))
% make sure core is not saturated
ampTurns = i_out*secTurns
```

3. According to the AWG table, the secondary should be wounded using 5 parallel 28 AWG wires. The primary, on the other hand, 18 parallel 28 AWG wires will be used.
4. According to the code below, the fill factor is 12.53%, which is reasonable.

```
windowArea_mm2 = 427;
priTurns = ceil(priTurns(priTurns>0))
secTurns = ceil(secTurns(secTurns>0))
num_of_paralles_pri = ceil(num_of_paralles_pri)
num_of_paralles_sec = ceil(num_of_paralles_sec)
cableArea_mm2 = 0.080;
primaryArea_mm2 = priTurns*num_of_paralles_pri*cableArea_mm2
secondaryArea_mm2 = secTurns*num_of_paralles_sec*cableArea_mm2
totalCableArea_mm2 = primaryArea_mm2 + secondaryArea_mm2
fillFactor_perc = 100*totalCableArea_mm2/windowArea_mm2
```

5. Cable resistance calculation is done by the code below:

```
windingLengthPerTurn_mm = 68.2
ohms_per_meter = 212.872 / 1e3
primaryLength_m = windingLengthPerTurn_mm * priTurns * 1e-3
secondaryLength_m = windingLengthPerTurn_mm * secTurns * 1e-3
primary_DC_resistance_ohm = ohms_per_meter * primaryLength_m /
num_of_paralles_pri
secondary_DC_resistance_ohm = ohms_per_meter * secondaryLength_m /
num_of_paralles_sec
```

The DC and AC resistances of the transformer are assumed equal thanks to the skin depth being greater than the radius.

Primary Resistance: 10.5 mOhm

Secondary Resistance: 252 mOhm

6. Copper losses are calculated by the code below:

```
diameter_mm = vpa(0.32004*u.mm)
radius_mm = diameter_mm/2
skinDepth_cm = vpa(7.5/sqrt(f_sw)*u.cm)
skinDepth_mm = unitConvert(skinDepth_cm, u.mm)
% skin depth is greater than radius.
% Therefore, AC reistance equals DC resistance
DC_to_AC_ratio = 1
primary_AC_resistance_ohm = primary_DC_resistance_ohm*DC_to_AC_ratio
secondary_AC_resistance_ohm = secondary_DC_resistance_ohm*DC_to_AC_ratio
resistancePri_ohm = vpa(primary_AC_resistance_ohm * u.Ohm)
resistanceSec_ohm = vpa(secondary_AC_resistance_ohm * u.Ohm)
copperLossPri = vpa(unitConvert((i_in_max*u.A)^2 * resistancePri_ohm, u.W))
copperLossSec = vpa(unitConvert((i_out*u.A)^2 * resistanceSec_ohm, u.W))
copperLoss_W = copperLossPri + copperLossSec
```

Total Copper Losses: 0.42 W

7. Core losses are calculated by the code below:

```
permeability = 26;
mu_zero = 1.25663706212e-6;
pathLength_m = 107e-3;
fluxDensity_Tesla = mu_zero * permeability * ampTurns / pathLength_m
% using graph above, 0.03 Tesla @ 100 kHz corresponds to
wattLoss_mW_cm3 = 60*u.mW/u.cm^3
volume_mm3 = 21300;
volume_cm3 = vpa(unitConvert(volume_mm3*u.mm^3, u.cm^3))
coreLoss_w = vpa(unitConvert(wattLoss_mW_cm3 * volume_cm3, u.W))
```

Core Loss: 1.27 W

The core loss is comparable with the copper loss. Hence, the design is good. No need to iterate more.

c) The open-loop flyback design is simulated on Simulink as shown in Figure 2. The circuit is simulated at its edges, namely, 12V input voltage and 0.366 duty and 18V input voltage and 0.278 duty. The simulation results are shown in Figures 3-6 for 0.278 duty and Figures 7-10 for 0.366 duty.
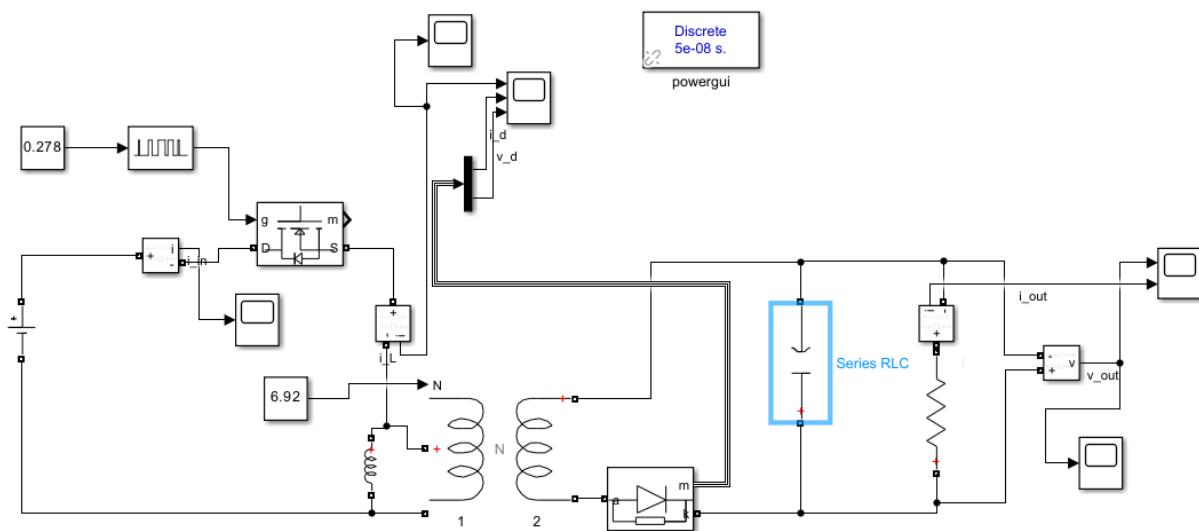

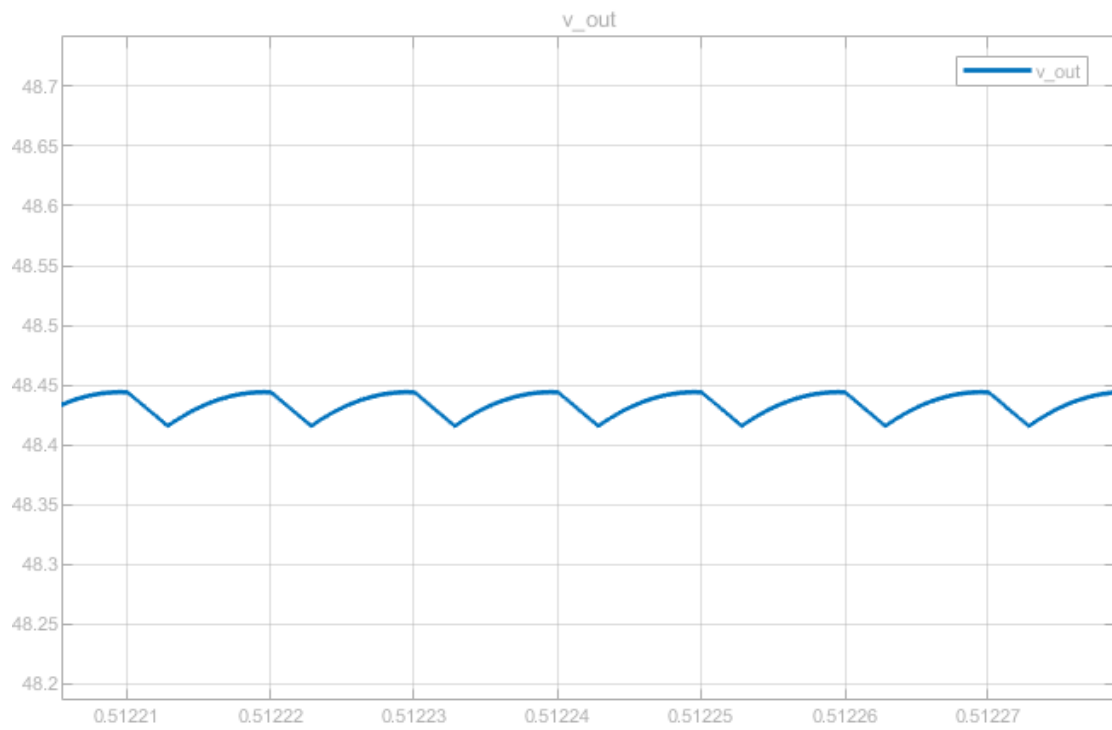Figure 2: The Flyback converter in Simulink
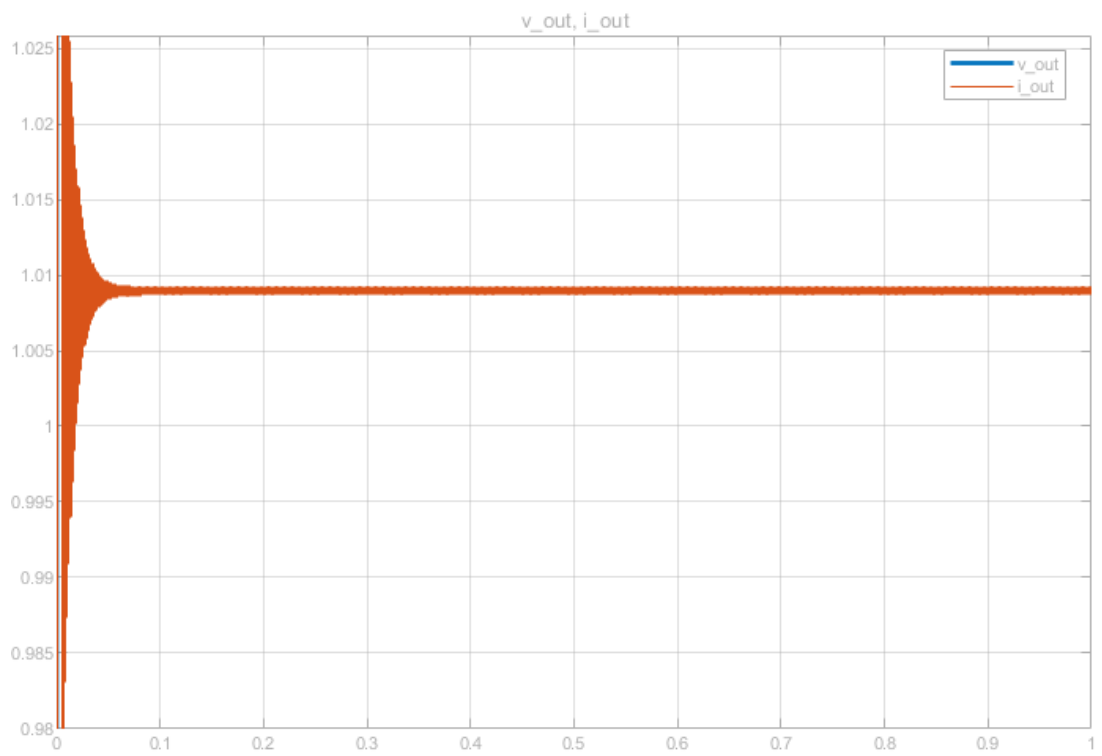
Figure 3: Output voltage ripple for 0.278 duty

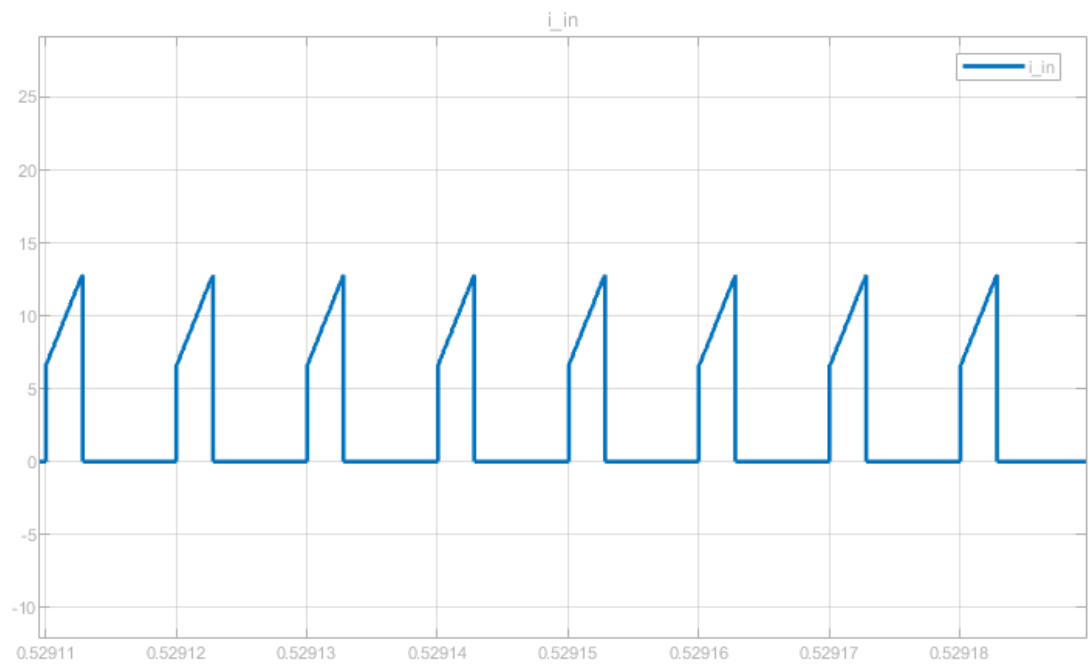*Figure 4: Output current waveform for 0.278 duty*

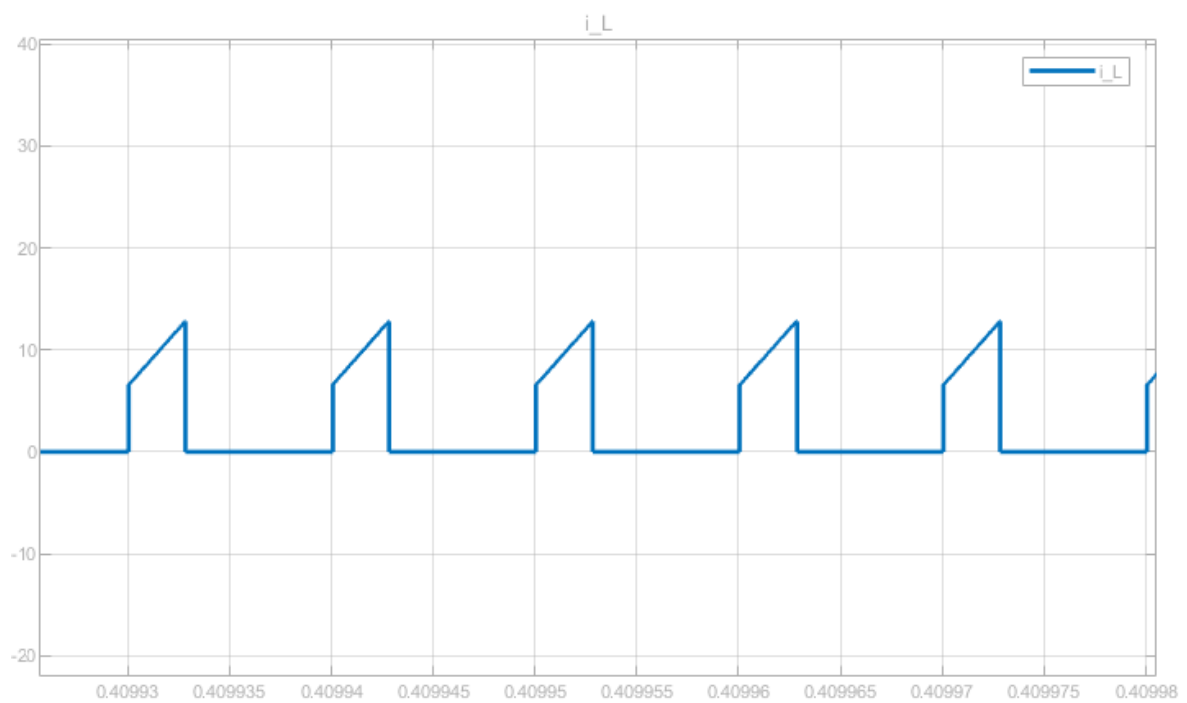*Figure 5: Input current waveform for 0.278 duty*

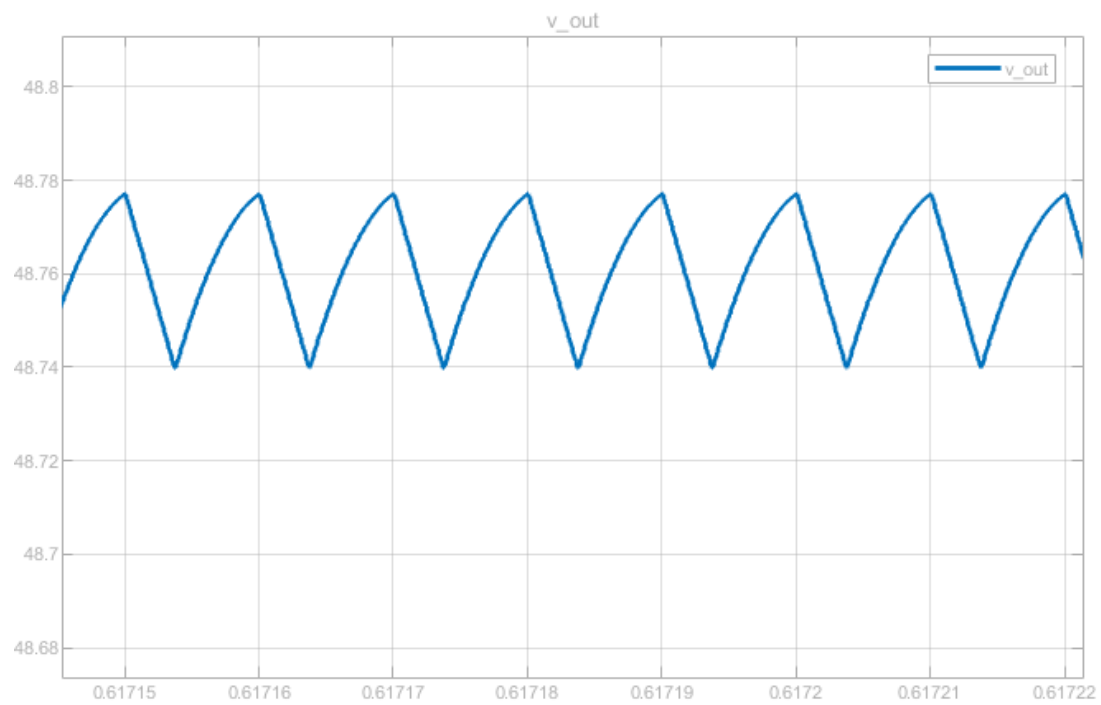*Figure 6: Transformer primary current waveform for 0.278 duty*

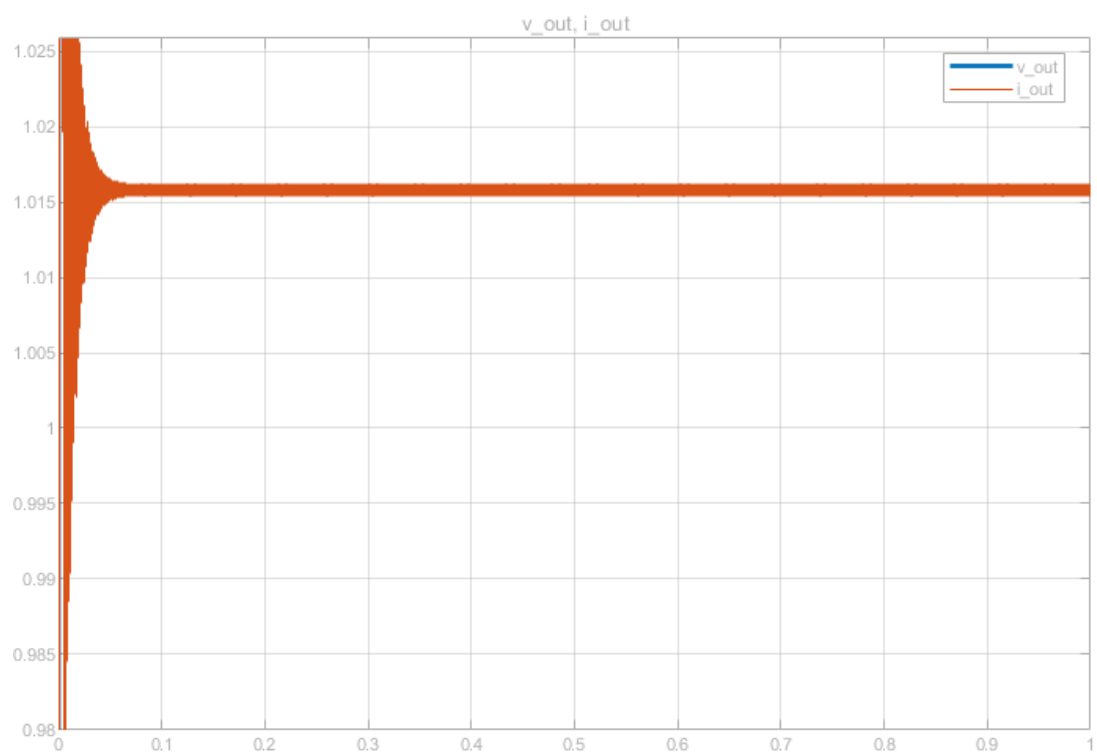*Figure 7: Output voltage ripple for 0.366 duty*

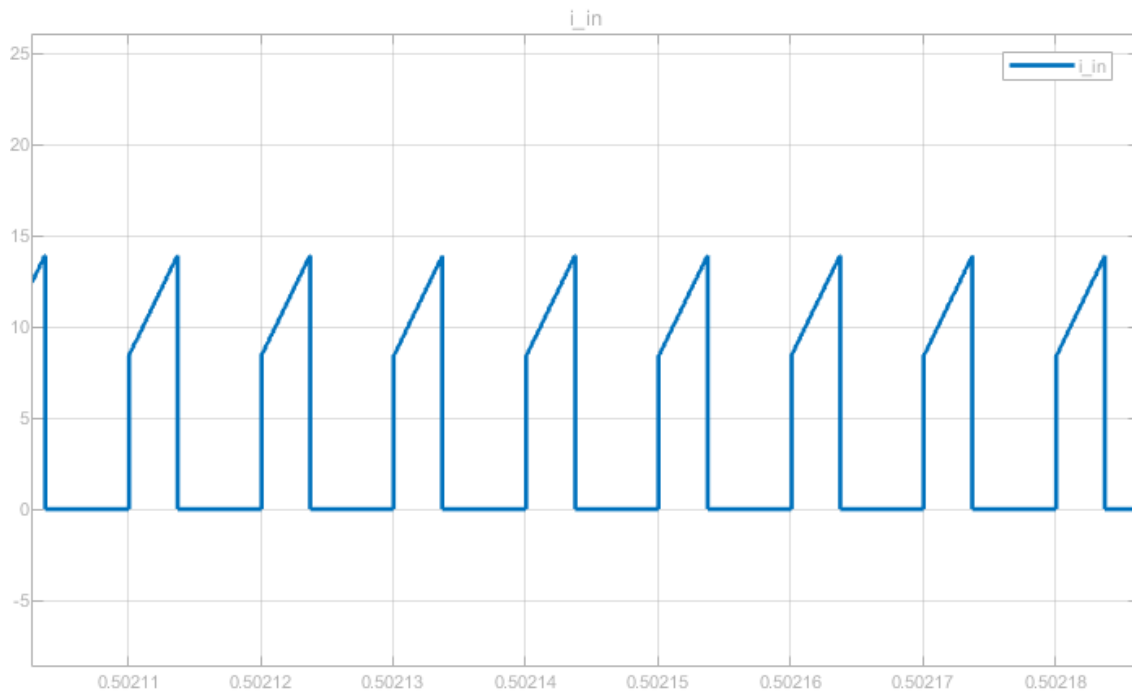*Figure 8: Output current waveform for 0.366 duty*

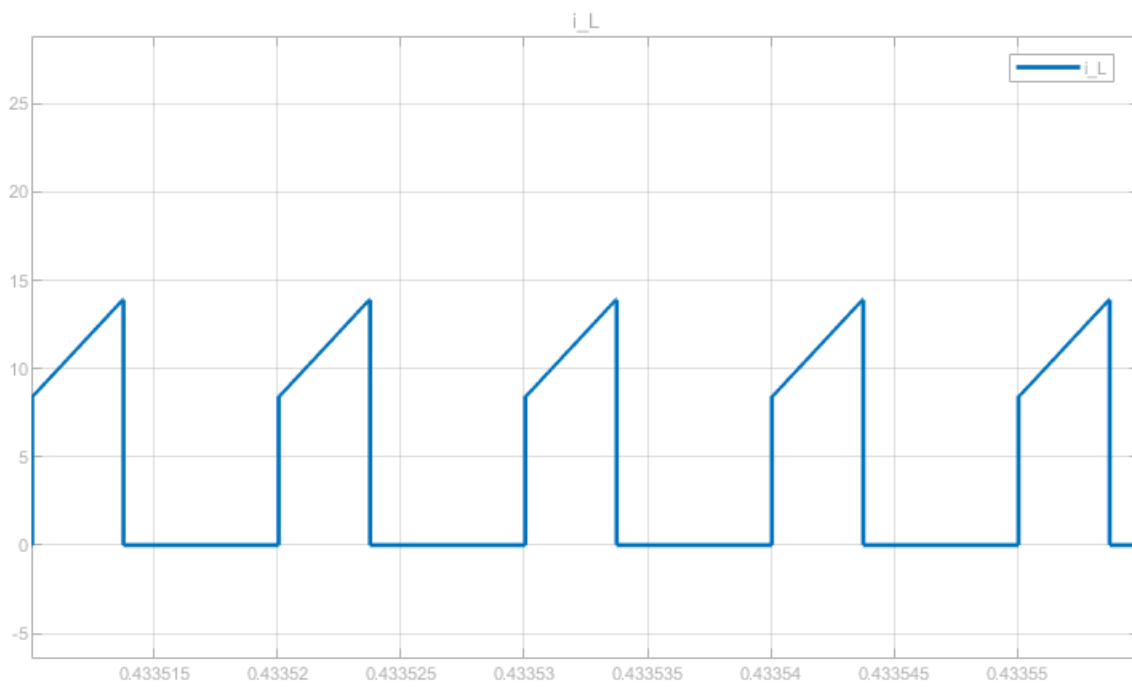*Figure 9: Input current waveform for 0.366 duty*

Figure 10: Transformer primary current waveform for 0.366 duty

d) The minimum load current to avoid from DCM is calculated with code below:

```
Lm = 8*10^-6; f_sw = 100*10^3;

% DCM
% for Vs = 12V
Vs = 12; D = 0.366;
deltaI_lm = Vs*D/(Lm*f_sw);
P_min = Vs^2 * D^2 / (2*Lm*f_sw);
I_load_min = P_min / 48

% for Vs = 18V
Vs = 18; D = 0.278;
deltaI_lm = Vs*D/(Lm*f_sw);
P_min = Vs^2 * D^2 / (2*Lm*f_sw);
I_load_min = P_min / 48
```

Minimum load current to operate in CCM when input is 12V = 0.251mA
Minimum load current to operate in CCM when input is 18V = 0.326mA

The maximum current that can flow through transformer is calculated with code below:

```
% max I_Lm current occurs when input voltage is 12V and at 100% load
Vs = 12; D = 0.366;
turnsRatio = 6.92; R = 48;
deltaI_lm = Vs*D/(Lm*f_sw);
P_out = Vs^2 * D^2 * turnsRatio^2 / ((1-D)^2 * R);
I_Lm_max = deltaI_lm/2 + P_out/(Vs*D)
```

Current can rise up to the 13.645A while converter is working with 100% load and 12V input voltage.
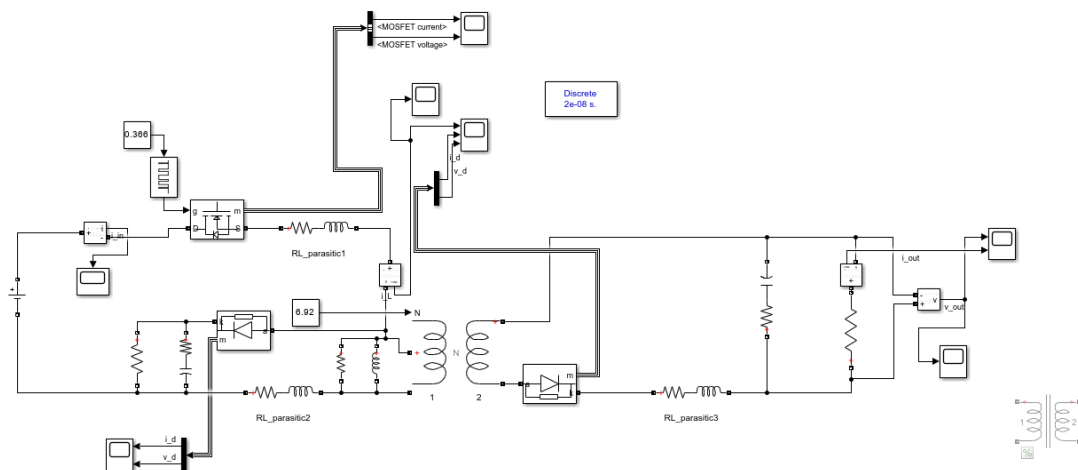
e)

Figure 11: Simulation of the converter with parasitic elements of transformer and switching device.
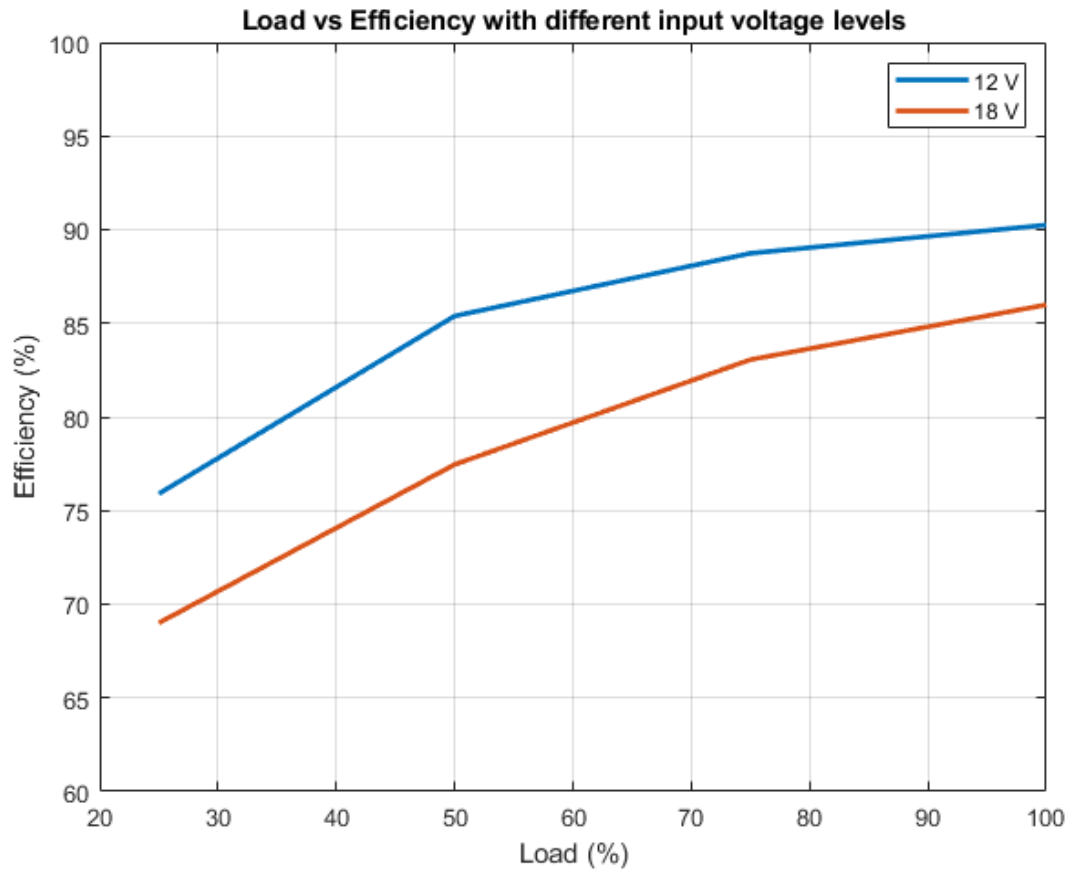
Figure 12: Voltage and current waveforms of MOSFET with parasitic elements.

In figure 12, it can be seen that, due to parasitic inductances, there are voltage spikes on MOSFET while switching. Because of leakage inductance, snubber must be used to discharge the leakage inductance. Snubber design is taken from the recommended design of Webench.

f)

The flyback converter is simulated with parasitic elements and non-ideal switching devices as shown in Figure 13.

Figure 13: Simulation design for efficiency test.

Figure 14: Efficiency vs Load curves for different voltage input levels.

Table 1: Simulation result of efficiency values for different input voltage and load conditions.

Load (%)	Efficiency (%)	
	12V	18V
25	75.9	69
50	85.39	77.46
75	88.74	83.06
100	90.25	85.99

Table 2: Calculated efficiency values without snubber losses.

Load (%)	Efficiency (%)	
	12V	18V
25	87.7	87.89
50	92.78	93.03
75	94.3	94.62
100	94.94	95.33

Efficiency of the flyback converter decreases with less load since core loss and snubber losses become dominant. Also, when the input voltage increased, the losses on switching device increase quadratically; thus, converter becomes less efficient with higher input voltage. Lastly, how inefficient is snubber can be seen by comparing two results.

Component Selection

Switching Device

Peak switching current and voltage can be calculated equations below:

```
V_sw = Vs + 1/turnsRatio*48
I_sw = 1./(1-duty).*turnsRatio.*I_out_avg + 1/turnsRatio.*
       (1-duty)./2./L_pri./f_sw*48
```

Switching voltages calculated as 18.94V and 24.94V, respectively with 12V and 18V input voltage, and maximum switching current is calculated as 13.65A. However, due to leakage inductances and parasitic elements, there are voltage spikes while switching. Thus, also it can be seen in Webench design, a mosfet with 80V rated voltage and 100A rated current is selected. For less rated voltages it is easy and cheap to find high current rated mosfets which also results in less losses on Mosfet due to less Rds value.

Secondary Diode:

```
V_d_max = Vs*turnsRatio + 48
I_d_max = I_sw./turnsRatio
```

By using above equations, maximum voltage on diode is found as 131.04V and 172.56V, respectively with 12V and 18V input voltage, and maximum current is calculated as 1.976A. Voltage rating of the diode should be select higher because the effect of voltage spikes increases with turns ratio at secondary side. Thus, diode is selected with 431

Output Capacitor:

Maximum allowed voltage ripple at output is 3%.

```
C_min = duty/f_sw/R/ripple
```

Minimum capacitance value of the output capacitor is found as 2.54µF with equation above. However, output voltage is 48V and to be safe rated voltage of capacitor should be higher. High voltage rated capacitor is found as aluminum capacitor which has high ESR values compared with other types. Found capacitors in market have high voltage ratings, so they have also high ESR values. Because ESR values become dominant on output ripple, capacitor with high capacitances is selected. The selected capacitor has 47µF capacitance and 2Ω ESR. Effect of ESR can be calculated equation below:

```
V_ESR = ESR * I_out_avg
```

The ripple due to ESR can be around 2V when single capacitor is used. Thus, four of the selected capacitors must connected in parallel.

Controller IC:

UC3843AN is selected which is appropriate for Webench's design. It is a current-mode PWM controller that can drive the gate of the mosfet with respect to sensed current and output voltage.

Transformer:

The detailed calculation of the transformer's turn ratio, cable parameters, core, magnetizing inductance etc. is given in magnetic design section.
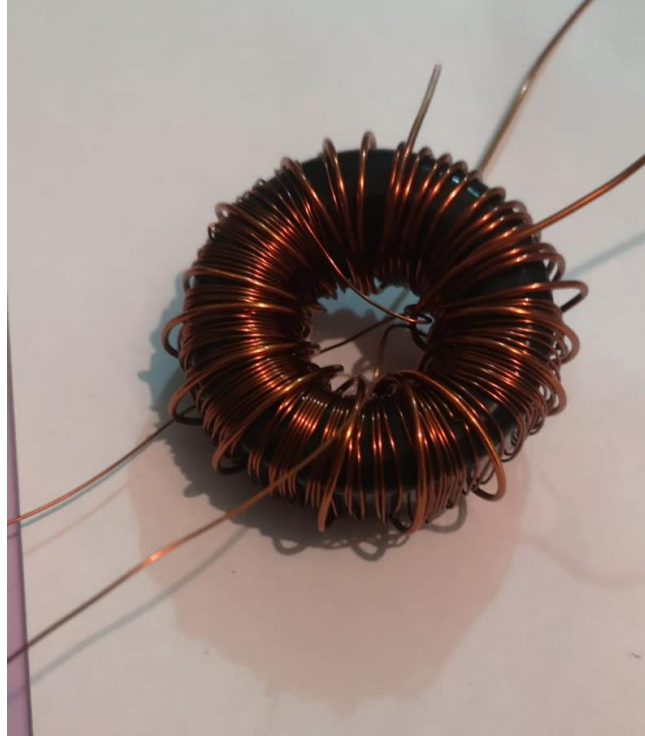
Experimental results of transformer on first try:

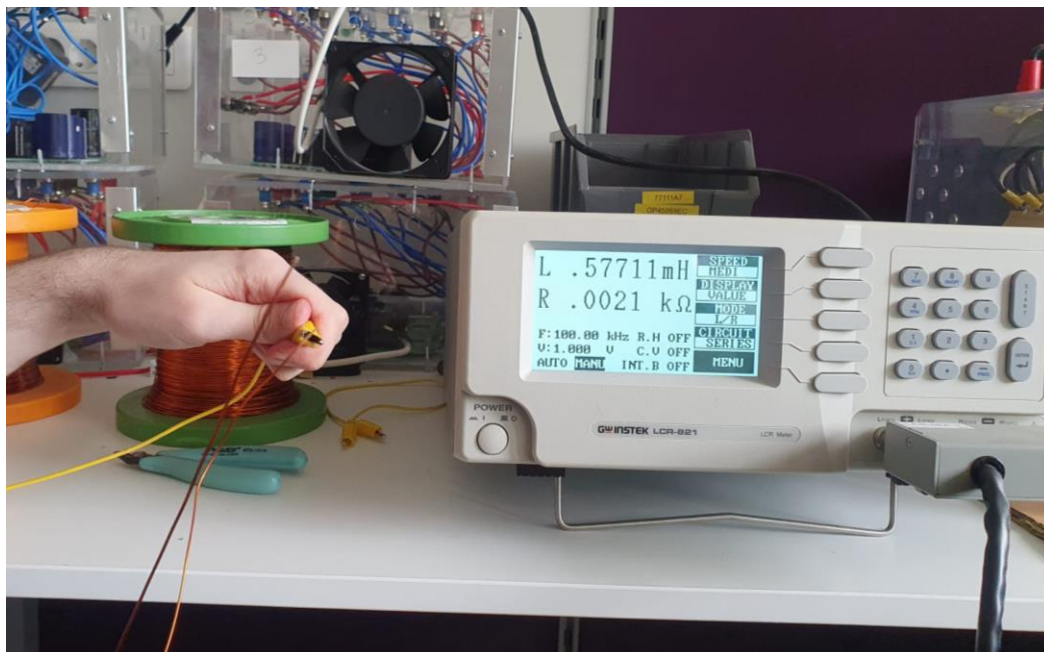

Figure 15: Wound transformer for initial experiments.

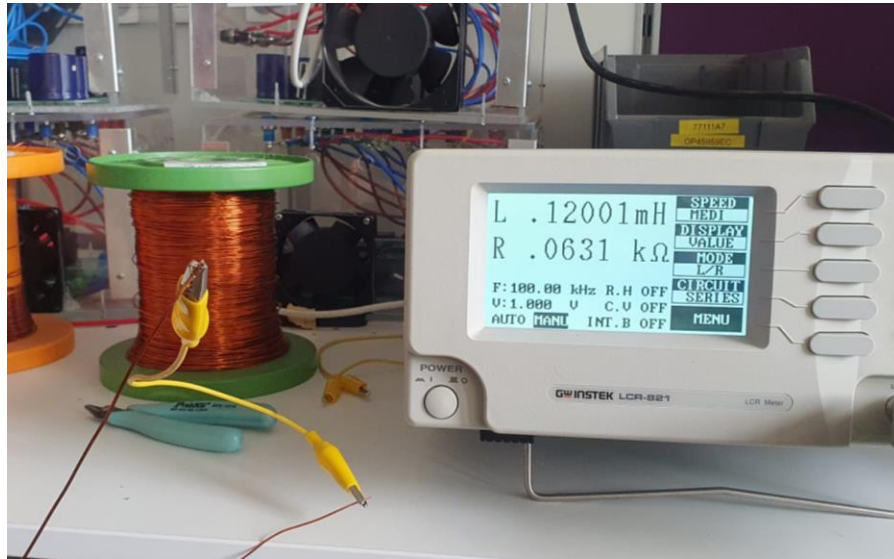*Figure 16: Primary is open circuited to measure leakage + magnetizing inductance at secondary.*

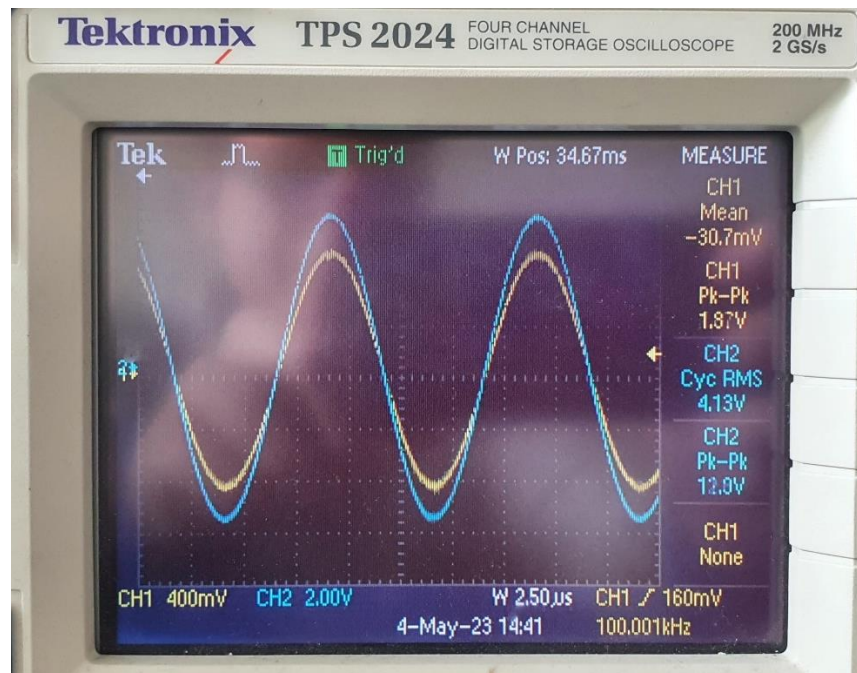*Figure 17: Primary is short circuited to measure leakge inductance at secondary.*

Figure 18: Input and output voltage ratio to observe turns ratio.

The leakage inductance at secondary is measured as 120µH and by substracting this value from the total inductace measured as 577µH, magnetizing inductance is measured as 457µH. Also, turns ratio, which is ratio of output and input voltage, is measured as 6. It can be seen that the leakage inductance is too high than the expected values. This may be caused by the toroid core because winding around a toroid core is difficult and results in high leakage which can be seen also Figure 15.

Conclusion