LAB 7. Adjustable Counter

A1)(50 pts)Implement a one-digit BCD counter as given in Fig. 1. It should count from 0 to 9 at**1 Hz**. It should also have a reset input, which resets the counter to go back to 0.

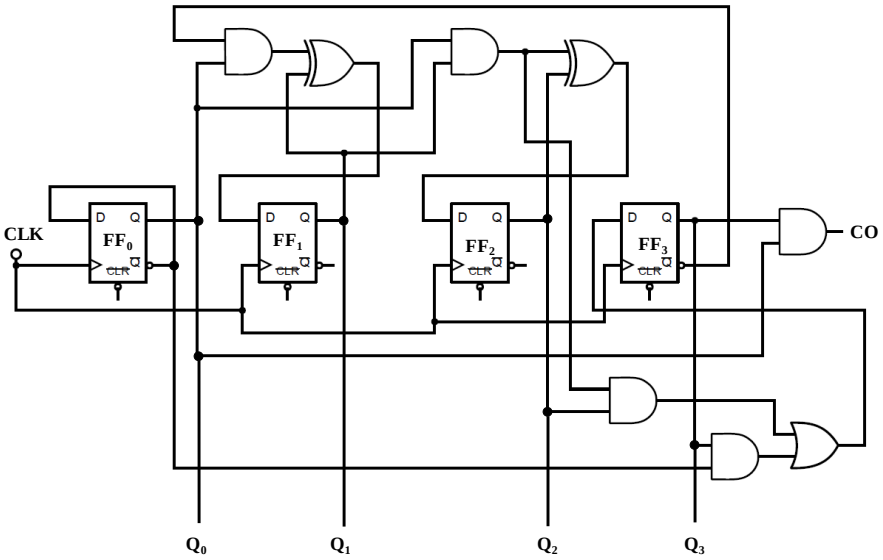

Figure 1.A BCD counter circuit.

Test the design by simulation. The simulation should consist of 3 times of repetition for counting from 0000 to 1001. After 1001, it should start from 0000 again to continue counting. Figure 2 shows the simulation input/output order. You must arrange the inputs/outputs in this order.

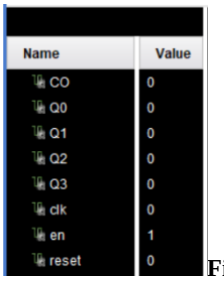

Figure 2. Input/output order in simulation.

Submission requirements;

1. Circuit design file in PDF. DO NOT submit as an image file such as TIFF, JPG, etc. To save the design as a pdf file, right click in the block design and save it as a pdf file.
2. Simulation result screen. This can be an image file.

A2)(50 pts)**Modify**the circuitof A1) so that the upper limit of the counter can be adjusted by the user input (in binary, i_3, i_2, i_1& i_0). i_3 is MSB. This upper limit should be between 1 (0001) and 9 (1001). For instance, if $i_3i_2i_1i_0$is 1000, the counter should count from 0 to 8, return to 0, and then count again. It should also have a reset input which resets the counter to 0.

Test the design by simulation.

1. User input will be 8(1000). This counting should repeat 2 times.
2. Then, user input will be 1.This counting should repeat 3 times.
3. Next, user input will be 5.This counting should repeat 2 times.
4. Finally, user input will be 3.This counting should repeat 2 times.

Figure 3 shows the simulation input/output order. You must arrange the inputs/outputs in this order.

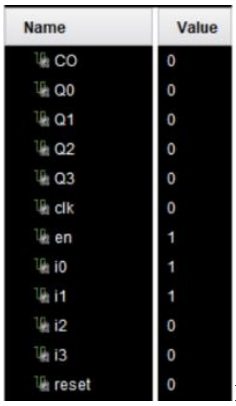

Figure 3. Input/output order in simulation.

Submission requirements;

1. Circuit design file in PDF. DO NOT submit as an image file such as TIFF, JPG, etc. To save the design as a pdf file, right click in the block design and save it as a pdf file.
2. Simulation result screen. This can be an image file.

Hint:XOR gates can be used for comparison.