Lab 6. Priority Encoder

An encoder is one of the basic combinational logic devices. Encoders are often used to control interrupt requests. A priority encoder is a standard encoder with some priorities. A standard encoder produces erroneous outputs if more than one inputs are HIGH. Also, when all inputs are LOW, the output becomes all zero, which is designated for another input. A priority encoder is a solution to these problems. It overcomes those problems by prioritizing the inputs. The priority encoder's output corresponds to the active input with the highest priority.

Truth Table of Priority Encoder

Inputs				Outputs		
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

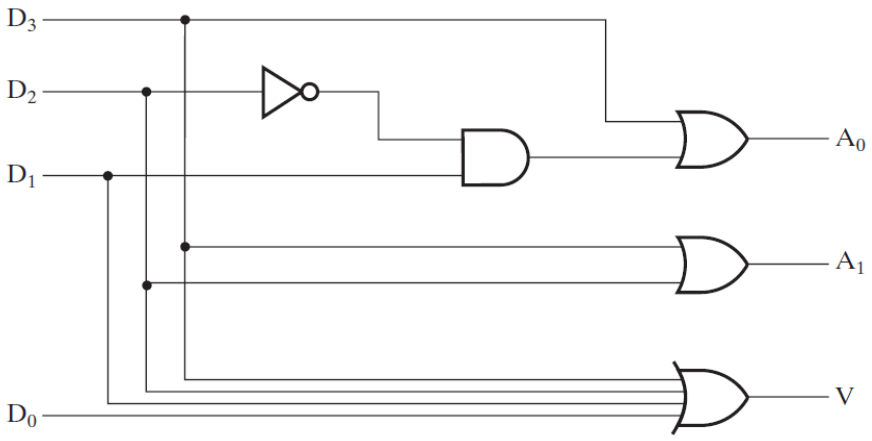


Figure 1. Standard 4-bit priority encoder. (Top) truth table. (Bottom) Gate-level implementation.

1) Build a 4-bit priority encoder as shown in Fig. 1. Test your circuit according to the following input sequence. (40 pts)

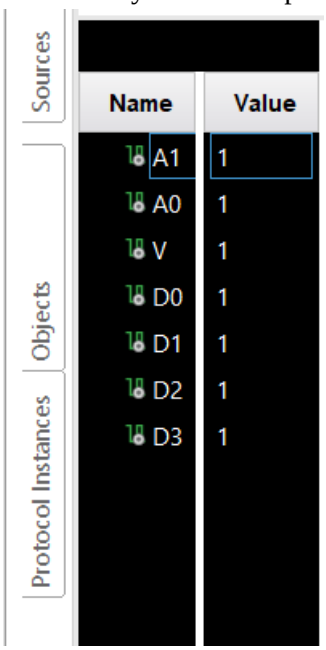
Table 1: Input squences to test

D3	D2	D1	D0
0	**0**	**0**	**0**
1	**1**	**0**	**0**
0	**1**	**1**	**1**
0	**0**	**1**	**0**
0	**0**	**0**	**1**

1	**1**	**1**	**1**

IMPORTANT

In addition, in below you can see in which order my inputs and outputs are seen in simulation part. Also make yours the same as mine one. (Note : You can easily change the order in simulation by selecting input/output then dragging and dropping it which place you want to put.) This part is very important while we are checking, so be careful about this part. Otherwise you can lose points.



2) By using two 4-bit priority encoders of part 1) and some auxiliary gates, design an 8-bit priority encoder. Use the encoder of part 1) as an IP in this part. Test your circuit according to the following input sequence. (60 pts)

Note: Filling out the truth table below can give you a hint.

Input								**4-bit encoder output**						**Output**			
D7	D6	D_5	D_4	D_3	D_2	D_1	D_0	a1	a0	v	a1	a0	v	A_2	A_1	A_0	V
0	0	0	0	0	0	0	0							X	X	X	0
0	0	0	0	0	0	0	1							0	0	0	1
0	0	0	0	0	0	1	X							0	0	1	1
0	0	0	0	0	1	X	X							0	1	0	1
0	0	0	0	1	X	X	X							0	1	1	1
0	0	0	1	X	X	X	X							1	0	0	1
0	0	1	X	X	X	X	X							1	0	1	1
0	1	X	X	X	X	X	X							1	1	0	1
1	X	X	X	X	X	X	X							1	1	1	1

Table 2: Input squences to test

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1
0	0	1	0	1	0	1	0
0	0	0	1	1	1	1	1
0	0	0	0	1	0	0	0
0	0	0	0	0	1	1	1
0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1

IMPORTANT

In addition, in below you can see in which order my inputs and outputs are seen in simulation part. Also make yours the same as mine one. (Note : You can easily change the order in simulation by selecting input/output then dragging and dropping it which place you want to put.) This part is very important while we are checking, so be careful about this part. Otherwise you can lose points.