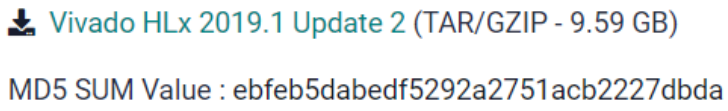
Lab 3. Block Design with IPs

In this lab, you will learn how to create a circuit in Vivado through block design by using intellectual properties (IPs), especially with the Xilinx University Program (XUP) Library.

Note:

- If your machine already has Vivado and XUP library installed, you can jump to step 2.
- If you want to install Vivado on your own machine, you may follow steps 1 and 2.

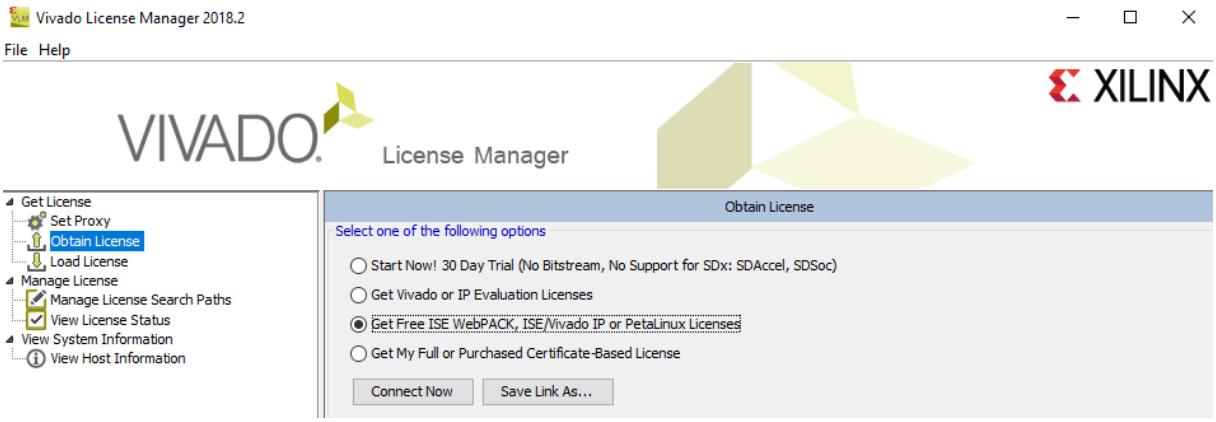
Step 1. Download Vivado Design Suite WebPack Edition from https://www.xilinx.com/support/download.html.



When you click on the edition above, Xilinx will ask you to create an account. After creating your account, click next button, then you can start the self-installer file.

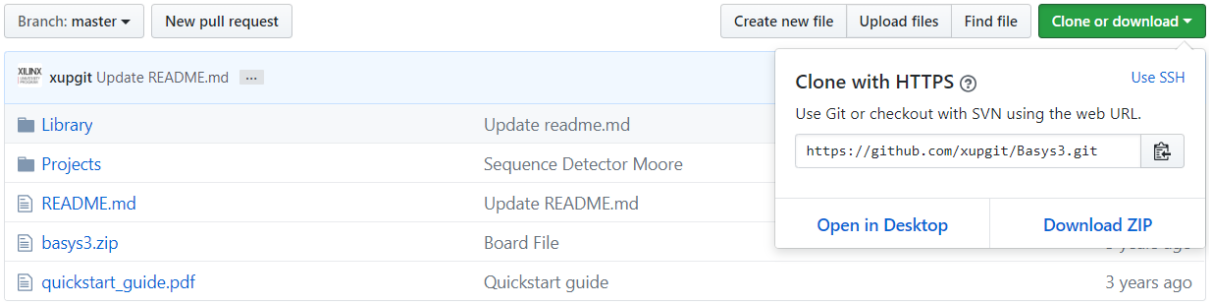
(The figure above is the screenshot from the 2018.2 version.)

Make sure that you have a required operating system. Next, it will ask you to log in with your account to download the program. To complete the download, you have to activate the license.

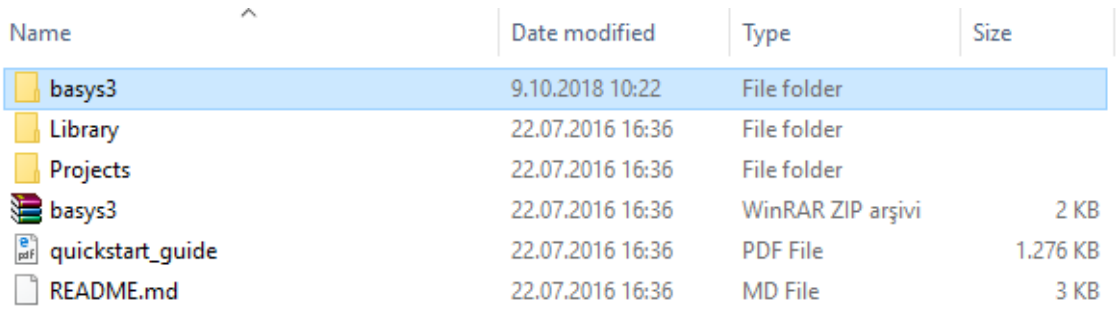


Step 2. Obtain the XUP library.

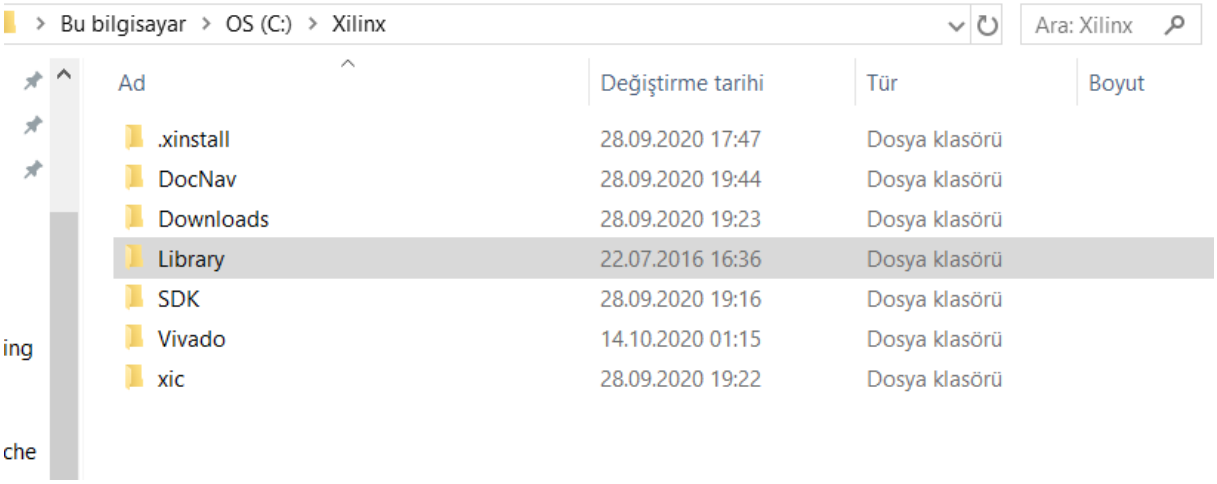
Visit https://github.com/xupgit/Basys3. Log in to GitHub with your account (you will have to create one if you do not have one). Click on clone or download.



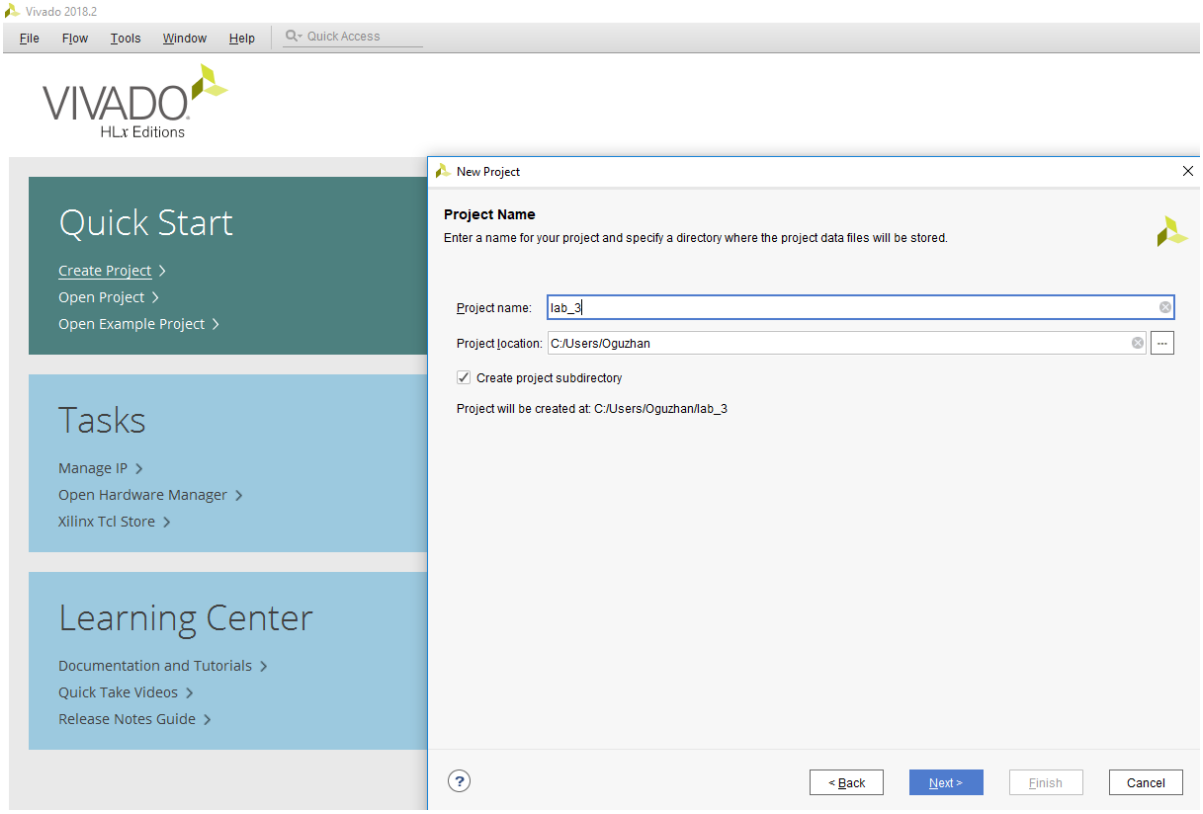
Extract the zip files.

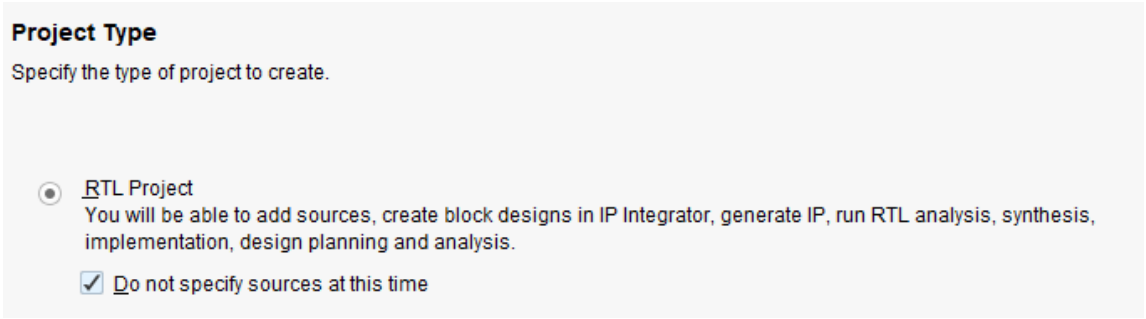


Now copy the Library folder to C:\Xilinx

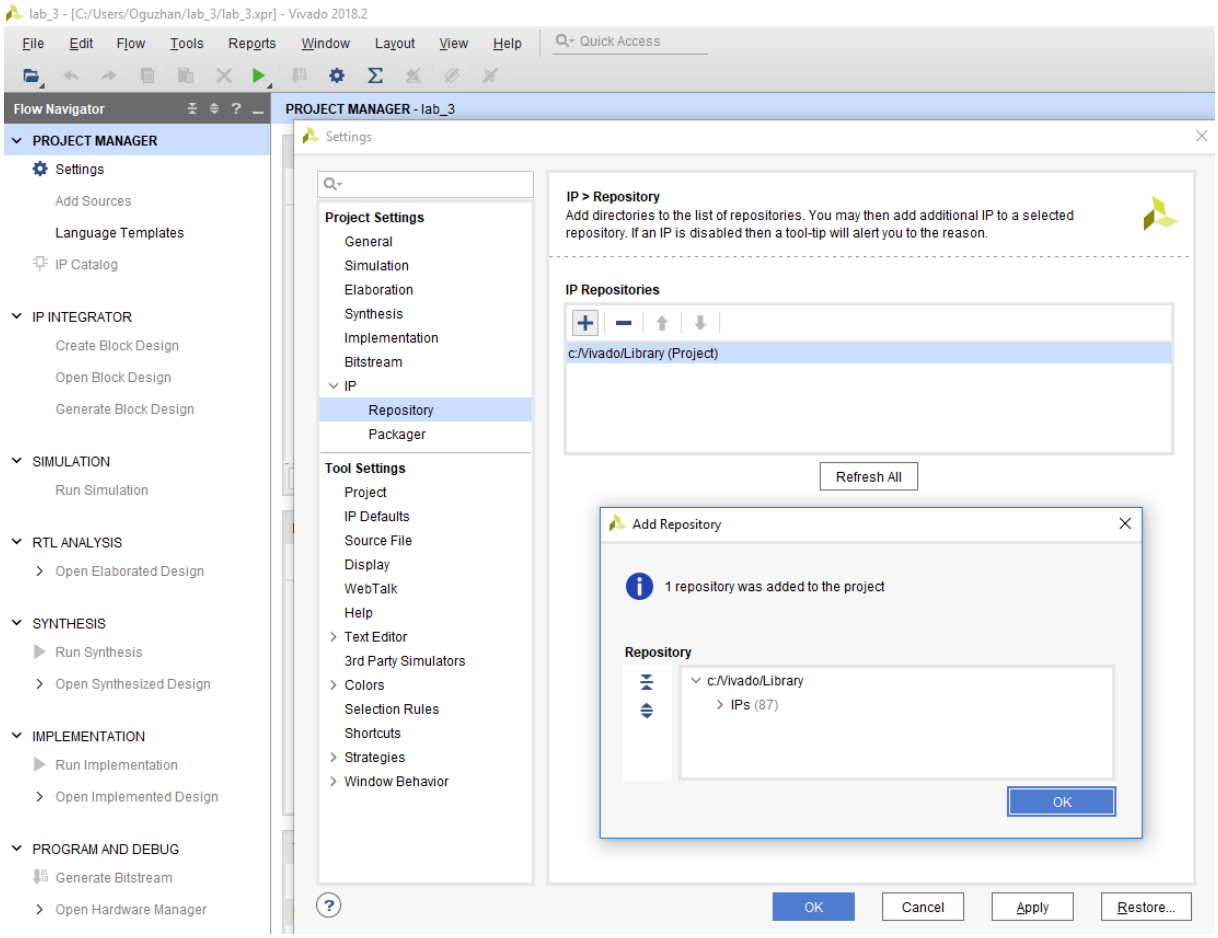


Step 3. Open the Vivado program and create a new project. Choose RTL project.

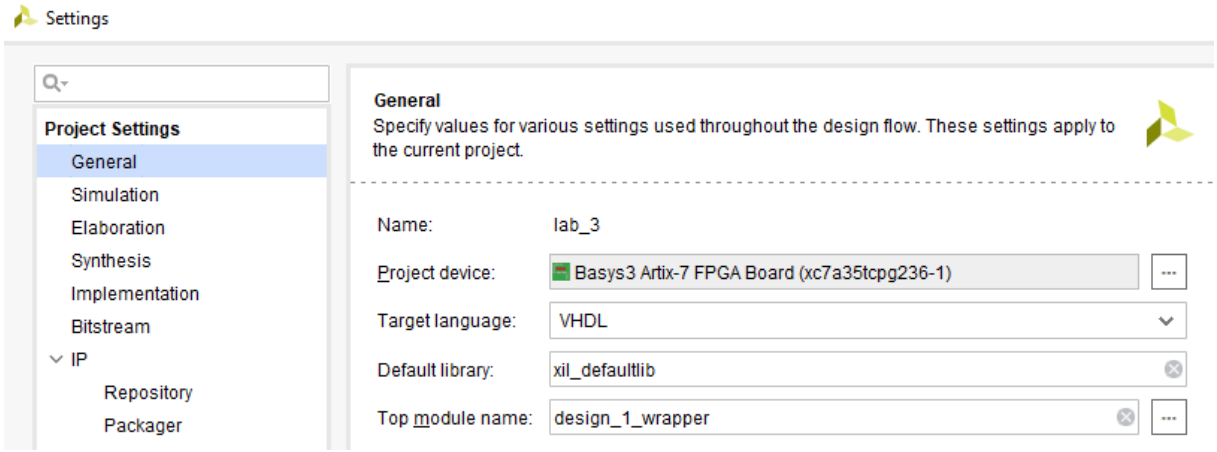




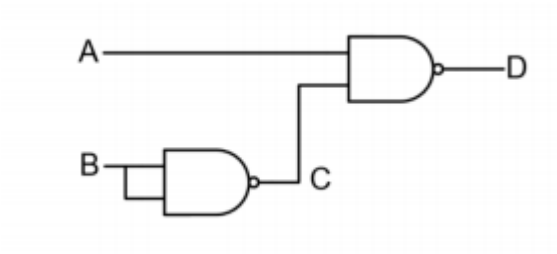
Step 4. Under the Project Manager, open the Project settings. Find IP and open Repository. Click on add (+) button and choose Library obtained from GitHub.



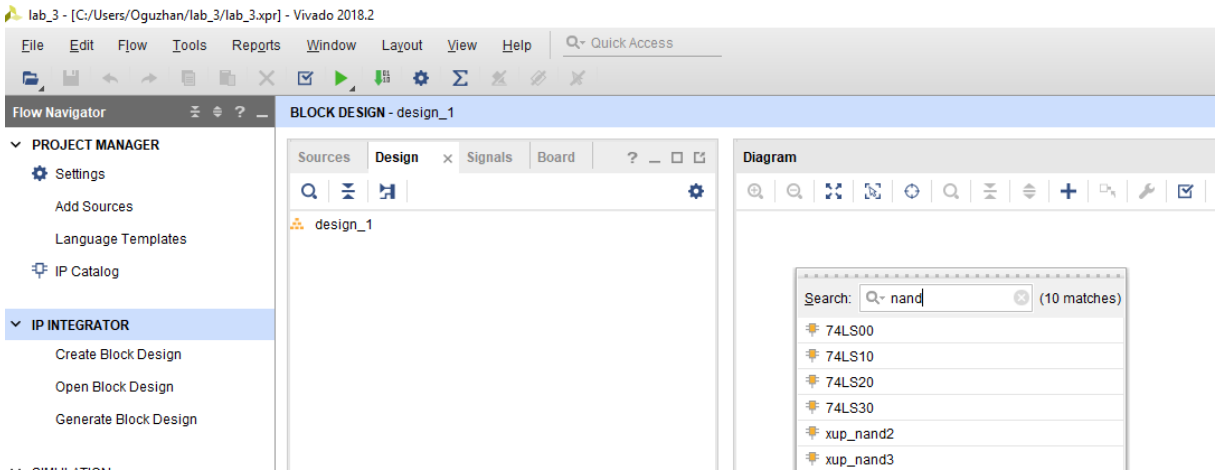
Make sure that in the General setting, language is defined as VHDL, not Verilog.

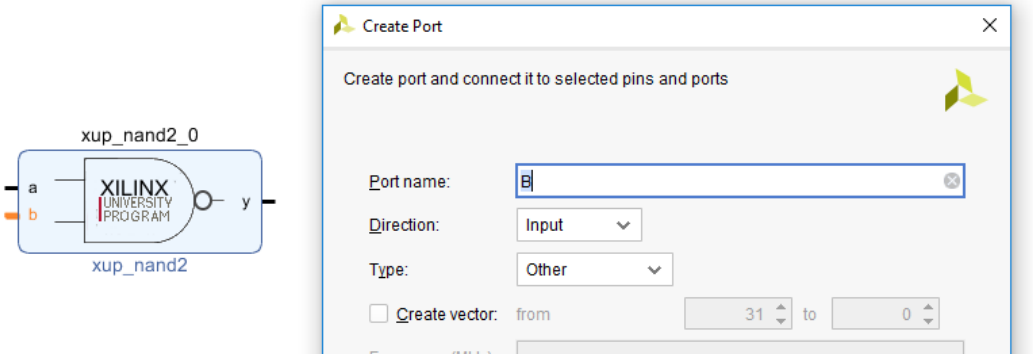


Step 5. Now we are ready to create a circuit. Click on Create Block Design. Continue with default options.



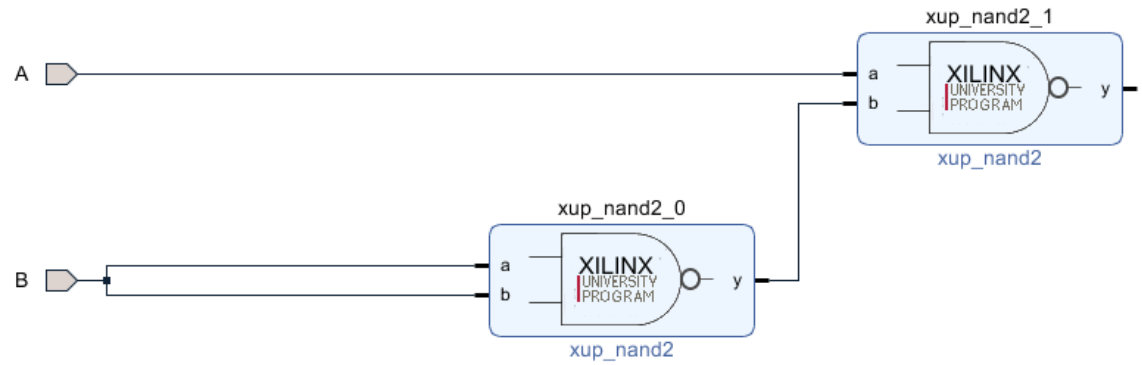
From the Diagram window, press the add (+) button to add an IP. Search for NAND2. Choose xup_nand2. Right click over the gate and choose Create Port. Change the port name to ‘B’.



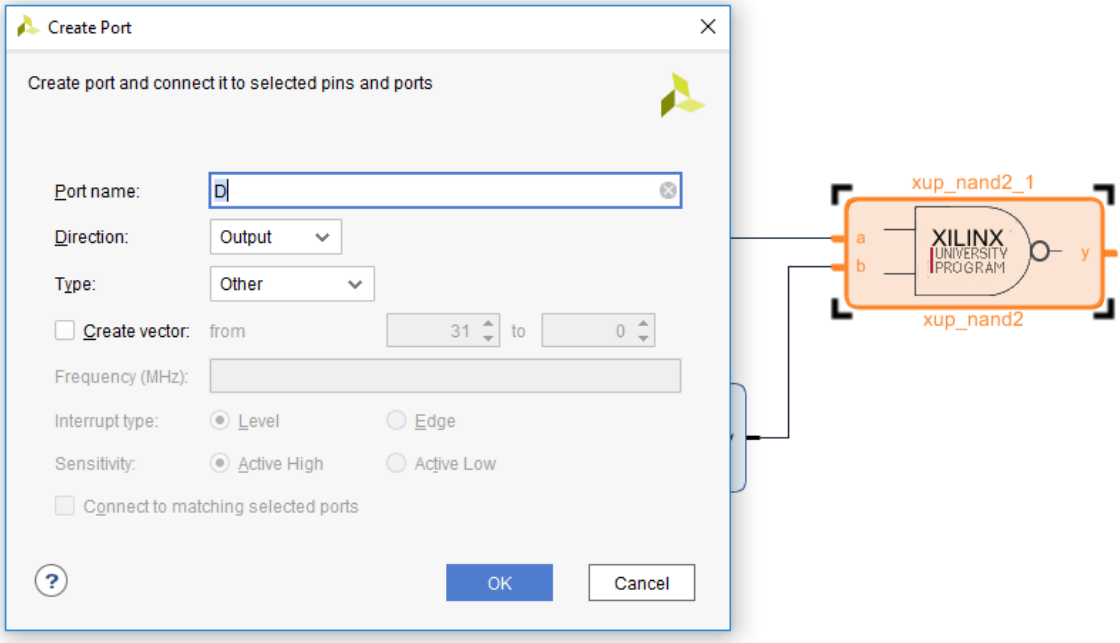


When a mouse pointer comes close to input, a pen will appear. Use the pen to draw connections as below.

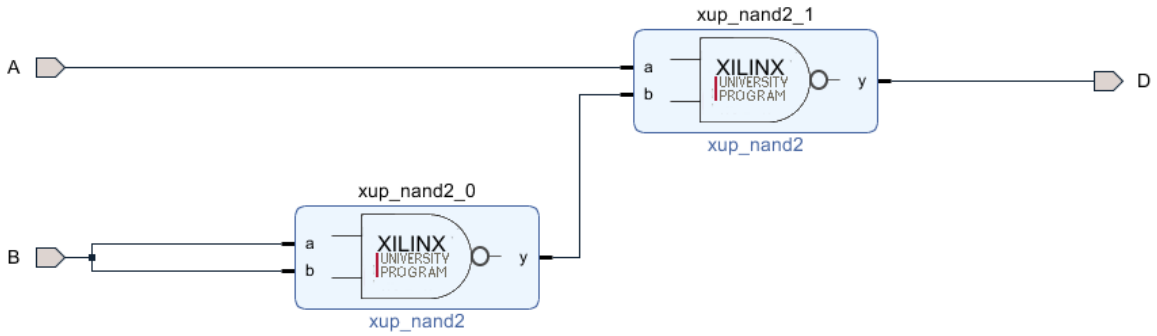
Add one more 2-input NAND gate and create a port A. Connect the output of the first NAND2 to one of the inputs of the second NAND2.



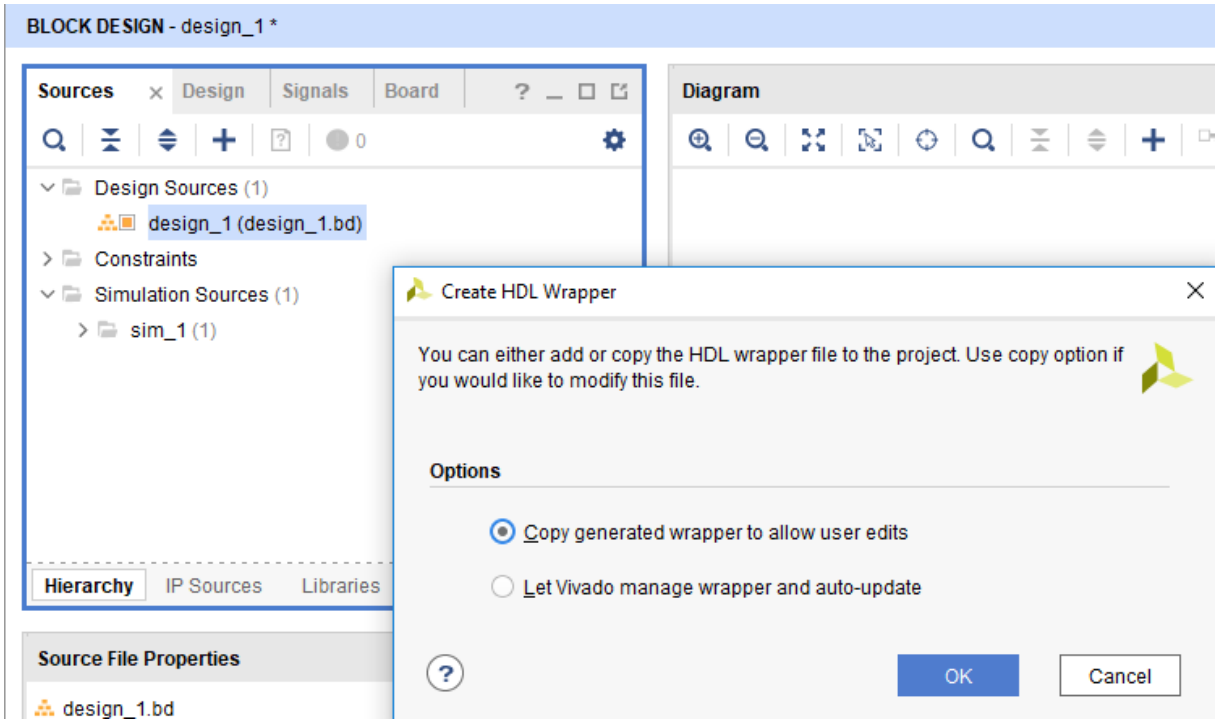
Create a circuit output port. Right click on the second NAND2 and choose Create Port. Give the port name as ‘D’. Choose the direction as Output.

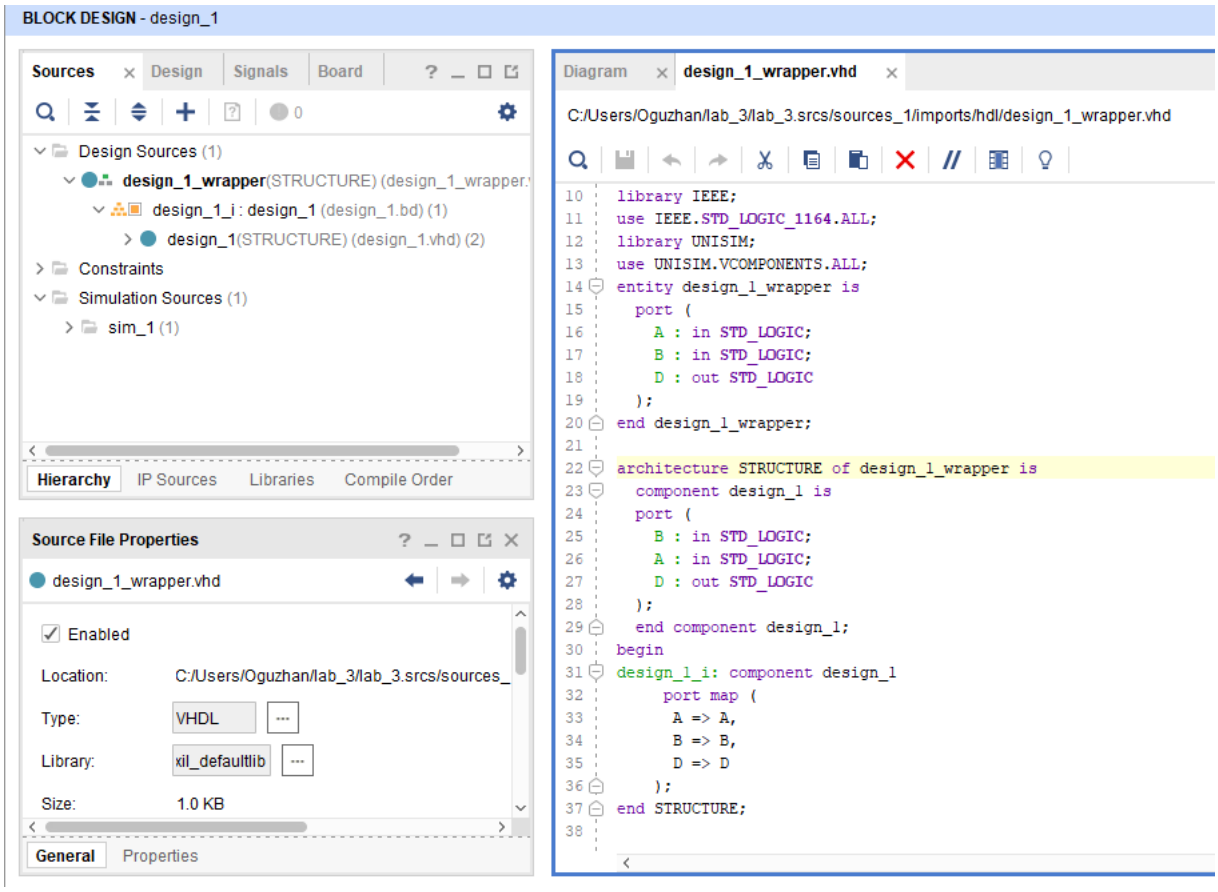


Now you should have completed the circuit as below.

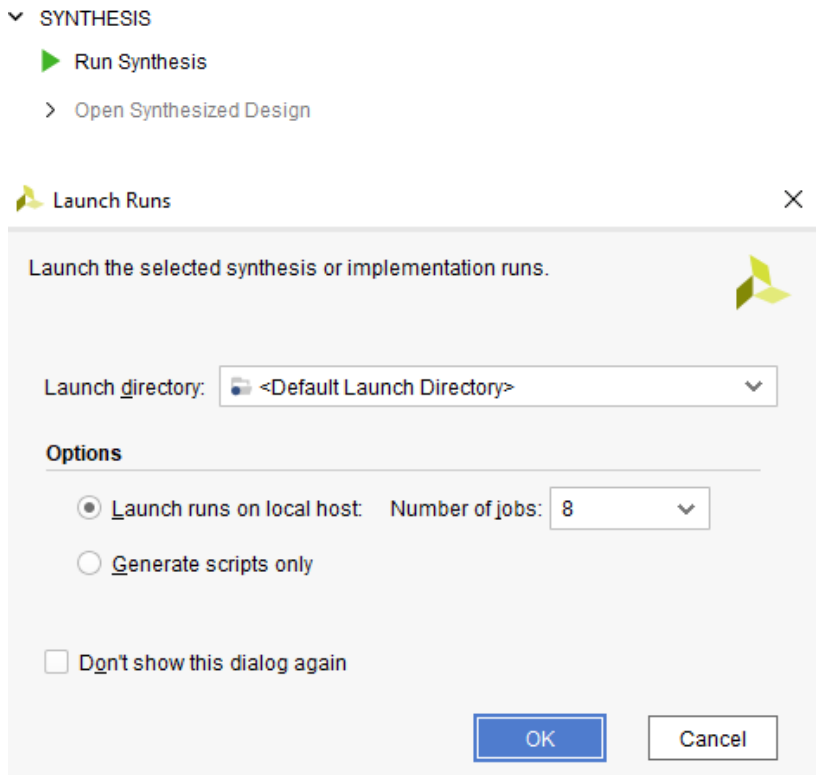


Step 6. Now we are ready to observe the VHDL code of this design. In Sources tab, right click on your design and choose Create HDL Wrapper. Now, you can see the VHDL code of the design.

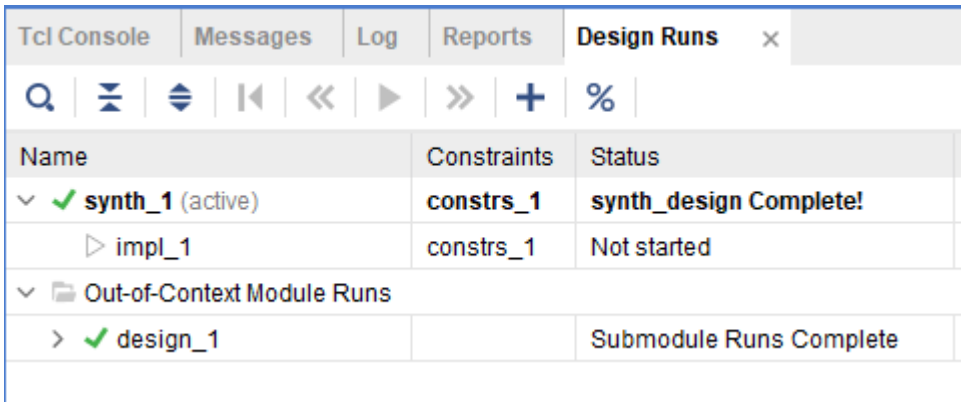




Step 7. After creating a VHDL code, first step is to run synthesis. Synthesis is the process of transforming an RTL-specified design into a gate-level representation.

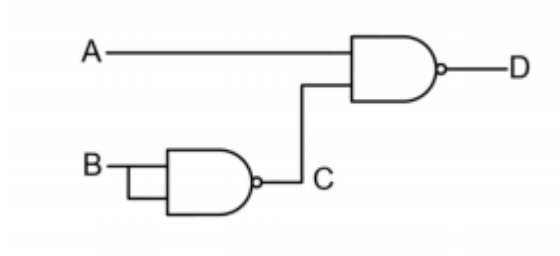


You can follow the progress from the Design Runs tab.



After synthesis is completed, we will add simulation source and run it.

Truth Table For Below Circuit



A	B	D
0	0	1
0	1	1
1	0	0
1	1	1