LAB #01. LOGIC GATES

Objective

To learn how to generate a design with Vivado software using simple logic gates and to examine the design through Simulation.

Submission Rules

Select your group member by yourself.

Just one submission for one group is enough. While you are submitting, write your name and your group member's name at the submission page in Canvas.

Submit your (1) elaborated design and (2) simulation result pictures.

Main-lab

1) Generate a behavioral VHDL code to design a circuit given in Figure 2. Module0 (M0, Figure 1) has 6 inputs and inverts all inputs. M1 is a 3-input AND gate, and M2 is a 3-input OR gate. M3 is a 2-input OR gate. M4 as an entire circuit has a 6-bit input and a single bit output.

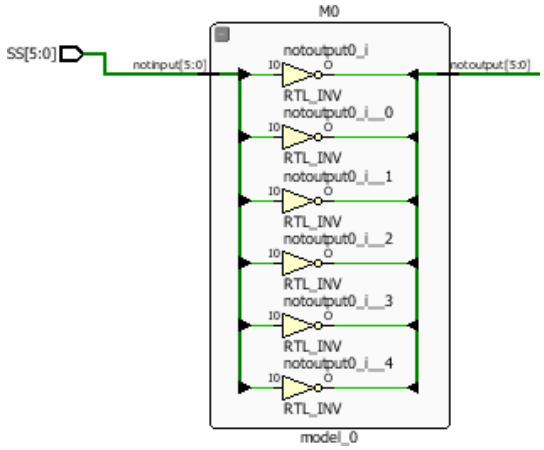

Figure 1. Schematic diagram of M0

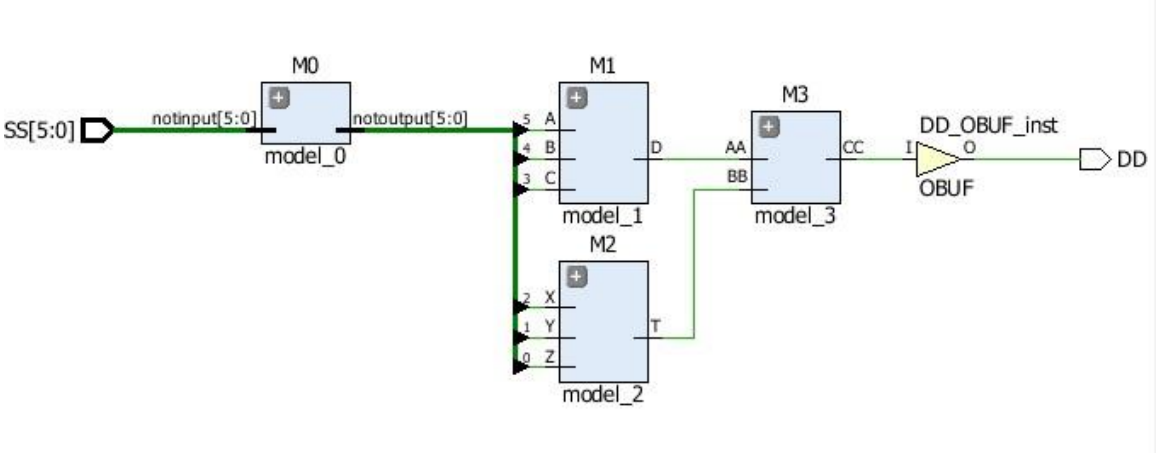

Figure 2. Schematic diagram of an entire circuit.

2) Synthesize your design and take a picture of the elaborated design.

3) Simulate the design with the input sequence combinations given below. (**Note:** The order of this input sequence is very important because we will check your simulation results according to this order. If you fail to follow this input sequence, you will not receive any credit.) Then take a picture of the simulation results. Finally, submit the pictures of both elaborated design and simulation results to Canvas.

Sequence	SS[5:0]
1	000000
2	000001
3	100111
4	100000
5	111111

Tips:

- Use components to combine the modules. Define internal signals to connect outputs of M1 and M2 to M3.