Lab 5. Decoder Design – Create Your Own IP

1) In this part, you will create an IP of a 2-to-4 decoder with enable, and then build a 3-to-8 decoder using the IP. (Total: 100 pts)

a. Create a block design of a 2-to-4 decoder with enable, of which truth table is given in Figure 1. Package the design as a new IP (refer to the tutorial). **Do not forget** to give a proper name to the IP. If you use the same name for two different IPs, it will cause an error. Show your result on simulation with given inputs, within given order. Submit both design picture and simulation result picture (50 pts).

Tablo 1: Input combinations to try

EN	A1	A2
0	**0**	**0**
1	**0**	**0**
1	**0**	**1**
1	**1**	**0**
1	**1**	**1**
0	**0**	**1**

EN	A_1	A_0	D_0	D_1	D_2	D_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

X means don't care.

Figure 1. Truth table of a 2-to-4 decoder with enable.

b. Create a 3-to-8 decoder (without enable) by using the IP of a 2-to-4 decoder (with enable) you generated in part (a).
Show your result on simulation with given inputs, within given order. Use given input and output names like in the table and be careful about MSB and LSB bits. Submit both design picture and simulation result picture(30 pts).

Tablo 2: Input combinations to try

X0(MSB)	X1	X2(LSB)	Output(Y0(LSB) Y1 Y2 Y3 Y4 Y5 Y6 Y7(MSB))
0	**0**	**0**	**10000000**
1	**0**	**0**	**00001000**
1	**0**	**1**	**…**
1	**1**	**0**	**…**
1	**1**	**1**	**…**
0	**0**	**1**	**…**

c. Create a 3-to-8 decoder **with** enable by slightly modifying the design created in part (b).

Show your result on simulation with given inputs, within given order. Use given input and output names like in the table and be careful about MSB and LSB bits. Submit both design picture and simulation result picture (20 pts).

Tablo 3: Input combinations to try

EN	X0(MSB)	X1	X2(LSB)	Output(Y0(LSB) Y1 Y2 Y3 Y4 Y5 Y6 Y7(MSB))
0	**0**	**0**	**0**	**00000000**
1	**1**	**0**	**0**	**00001000**
1	**1**	**0**	**1**	**…**
1	**1**	**1**	**0**	**…**
0	**1**	**1**	**1**	**…**
1	**1**	**1**	**1**	**…**