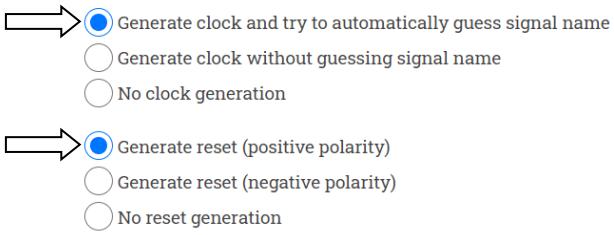
LAB-7 TUTORIAL

This tutorial is about clock generation for simulation.

1. First complete your design and create HDL wrapper.
2. Copy your wrapper and paste it to online generator.



This time click lines shown with arrows. Then generate testbench, copy and paste it to simulation part.

3. Then, go to your testbench. You will see below part. You need to edit this part. 1Hz is 1000 ms (milisecond), you need to change that part.

```
constant TbPeriod : time := 1000 ns; -- EDIT Put right period here
signal TbClock : std_logic := '0';
signal TbSimEnded : std_logic := '0';
```

4. For reset part of testbench which is generated automatically, give your time period like in below;

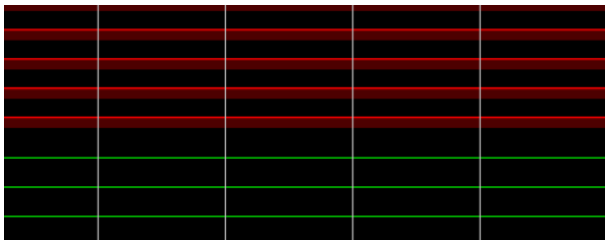
```
-- Reset generation
-- EDIT: Check that reset is really your reset signal
reset <= '1';
wait for TbPeriod;
reset <= '0';
wait for TbPeriod;
```

5. Then you will give your inputs one by one. How many clock you want to wait with given inputs?
   For example with given inputs, to be able to see all results you need to wait for 3 clocks. This time you can do like below;

```
-- EDIT Add stimuli here
en <= '1';
i0 <= '0';
i1 <= '0';
i2 <= '0';
i3 <= '1';
wait for 3* TbPeriod;
```

This means that inputs will be given for 3 clocks.

6. Finally, all the input combinations will be completed one by one and you will finish.
7. Another note I want to mention that when you run simulation, you may see red lines as below.



8. This time you need to restart and run simulation again is shown by arrows. With this way you can see the correct results.