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Release 14.7 Trace  (nt64)

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C:\xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 3

-n 3 -fastpaths -xml core_m.twx core_m.ncd -o core_m.twr core_m.pcf


Design file:              core_m.ncd

Physical constraint file: core_m.pcf

Device,package,speed:     xc6slx9,tqg144,C,-3 (PRODUCTION 1.23 2013-10-13)

Report level:             verbose report


Environment Variable      Effect

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NONE                      No environment variables were set

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INFO:Timing:2698 - No timing constraints found, doing default enumeration.

INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).

INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths

   option. All paths that are not constrained will be reported in the

   unconstrained paths section(s) of the report.

INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on

   a 50 Ohm transmission line loading model.  For the details of this model,
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and for more information on accounting for different loading conditions,

please see the device datasheet.

Data Sheet report:

All values displayed in nanoseconds (ns)

Setup/Hold to clock aclk

Source	Max Setup to Clock (edge)	Process Corner	Max Hold to clock (edge)	Process Corner	Internal Clock(s)	Phase
s_axis_data_tdata<0>	1.221(R)	SLOW	-0.288(R)	SLOW	aclk_BUFGP	0.000
s_axis_data_tdata<1>	1.049(R)	SLOW	-0.123(R)	SLOW	aclk_BUFGP	0.000
s_axis_data_tdata<2>	1.018(R)	SLOW	-0.094(R)	SLOW	aclk_BUFGP	0.000
s_axis_data_tdata<3>	0.750(R)	SLOW	0.158(R)	SLOW	aclk_BUFGP	0.000
s_axis_data_tdata<4>	0.683(R)	SLOW	0.218(R)	SLOW	aclk_BUFGP	0.000
s_axis_data_tdata<5>	0.559(R)	SLOW	0.336(R)	SLOW	aclk_BUFGP	0.000
s_axis_data_tdata<6>	0.665(R)	SLOW	0.235(R)	SLOW	aclk_BUFGP	0.000
s_axis_data_tdata<7>	0.764(R)	SLOW	0.139(R)	SLOW	aclk_BUFGP	0.000

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s_axis_data_tdata<8> |    0.978(R)|      SLOW  |   -0.060(R)|
SLOW  |aclk_BUFGP         |   0.000|
s_axis_data_tdata<9> |    0.866(R)|      SLOW  |    0.044(R)|
SLOW  |aclk_BUFGP         |   0.000|
s_axis_data_tdata<10>|    0.624(R)|      SLOW  |    0.273(R)|
SLOW  |aclk_BUFGP         |   0.000|
s_axis_data_tdata<11>|    0.957(R)|      SLOW  |   -0.043(R)|
SLOW  |aclk_BUFGP         |   0.000|
s_axis_data_tdata<12>|    1.063(R)|      SLOW  |   -0.144(R)|
SLOW  |aclk_BUFGP         |   0.000|
s_axis_data_tdata<13>|    1.000(R)|      SLOW  |   -0.083(R)|
SLOW  |aclk_BUFGP         |   0.000|
s_axis_data_tdata<14>|    0.586(R)|      SLOW  |    0.298(R)|
SLOW  |aclk_BUFGP         |   0.000|
s_axis_data_tdata<15>|    1.793(R)|      SLOW  |   -0.775(R)|
FAST  |aclk_BUFGP         |   0.000|
s_axis_data_tvalid   |    2.151(R)|      SLOW  |   -0.960(R)|
FAST  |aclk_BUFGP         |   0.000|
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Clock aclk to Pad

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                     |Max (slowest) clk|  Process   |Min (fastest)
clk|  Process   |                 | Clock  |
Destination          |  (edge) to PAD  |   Corner   |  (edge) to PAD
|   Corner   |Internal Clock(s) | Phase  |
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m_axis_data_tdata<0> |         8.451(R)|      SLOW  |
4.539(R)|      FAST  |aclk_BUFGP         |   0.000|
m_axis_data_tdata<1> |         8.595(R)|      SLOW  |
4.624(R)|      FAST  |aclk_BUFGP         |   0.000|
m_axis_data_tdata<2> |         8.839(R)|      SLOW  |
4.768(R)|      FAST  |aclk_BUFGP         |   0.000|
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m_axis_data_tdata<3>	8.582(R)	SLOW	4.605(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<4>	8.896(R)	SLOW	4.769(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<5>	8.854(R)	SLOW	4.726(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<6>	8.958(R)	SLOW	4.854(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<7>	8.813(R)	SLOW	4.754(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<8>	8.791(R)	SLOW	4.801(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<9>	9.120(R)	SLOW	5.003(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<10>	8.913(R)	SLOW	4.818(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<11>	9.102(R)	SLOW	4.936(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<12>	8.804(R)	SLOW	4.758(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<13>	8.698(R)	SLOW	4.718(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<14>	8.689(R)	SLOW	4.673(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<15>	8.739(R)	SLOW	4.678(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<16>	8.876(R)	SLOW	4.783(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<17>	8.559(R)	SLOW	4.592(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<18>	8.740(R)	SLOW	4.729(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<19>	8.752(R)	SLOW	4.736(R)	FAST	aclk_BUFGP	0.000
m_axis_data_tdata<20>	8.843(R)	SLOW	4.845(R)	FAST	aclk_BUFGP	0.000

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m_axis_data_tdata<21>|         8.751(R)|      SLOW  |
4.751(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<22>|         9.079(R)|      SLOW  |
4.993(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<23>|         9.293(R)|      SLOW  |
5.165(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<24>|         9.820(R)|      SLOW  |
5.446(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<25>|         9.241(R)|      SLOW  |
5.098(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<26>|         9.220(R)|      SLOW  |
5.133(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<27>|         9.413(R)|      SLOW  |
5.191(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<28>|         9.253(R)|      SLOW  |
5.069(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<29>|         9.358(R)|      SLOW  |
5.131(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<30>|         9.258(R)|      SLOW  |
5.107(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<31>|         9.535(R)|      SLOW  |
5.289(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<32>|         8.812(R)|      SLOW  |
4.793(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tdata<33>|         7.833(R)|      SLOW  |
4.193(R)|      FAST  |aclk_BUFGP        |   0.000|
m_axis_data_tvalid   |         8.215(R)|      SLOW  |
4.370(R)|      FAST  |aclk_BUFGP        |   0.000|
s_axis_data_tready   |         8.004(R)|      SLOW  |
4.218(R)|      FAST  |aclk_BUFGP        |   0.000|
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Clock to Setup on destination clock aclk

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               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
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Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
aclk	2.902			

Analysis completed Sat Jun 23 18:58:44 2018

Trace Settings:

Trace Settings

Peak Memory Usage: 4572 MB