Release 14.7 par P.20131013 (nt64)

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DESKTOP-KU30KCB:: Thu Jun 21 17:34:16 2018

par -w -intstyle ise -ol high -mt off optimizedSourceFIRfilter_map.ncd optimizedSourceFIRfilter.ncd optimizedSourceFIRfilter.pcf

Constraints file: optimizedSourceFIRfilter.pcf.

Loading device for application Rf_Device from file '6slx9.nph' in environment C:\xilinx\14.7\ISE_DS\ISE\.

"optimizedSourceFIRfilter" is an NCD, version 3.2, device xc6slx9, package tqg144, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)

Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par

-x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all

internal clocks in this design. Because there are not defined timing requirements, a timing score will not be

reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.

Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.23 2013-10-13".

Device Utilization Summary:

Slice Logic Utilization:

Number of Slice Registers:	285	out of	11,440	2%
Number used as Flip Flops:	285			
Number used as Latches:	0			
Number used as Latch-thrus:	0			
Number used as AND/OR logics:	0			
Number of Slice LUTs:	1,081	out of	5,720	18%
Number used as logic:	1,002	out of	5,720	17%
Number using O6 output only:	966			
Number using O5 output only:	2			
Number using O5 and O6:	34			
Number used as ROM:	0			
Number used as Memory:	7	out of	1,440	1%
Number used as Dual Port RAM:	0			
Number used as Single Port RAM:	0			
Number used as Shift Register:	7			
Number using O6 output only:	3			
Number using O5 output only:	0			
Number using O5 and O6:	4			
Number used exclusively as route-thrus:	72			
Number with same-slice register load:	68			
Number with same-slice carry load:	4			
Number with other load:	0			

Slice Logic Distribution:

Number of occupied Slices:	337	out of	1,430	23%

Number of MUXCYs used:	1,140	out of	2,860	39%
Number of LUT Flip Flop pairs used:	1,172			
Number with an unused Flip Flop:	959	out of	1,172	81%
Number with an unused LUT:	91	out of	1,172	7%
Number of fully used LUT-FF pairs:	122	out of	1,172	10%
Number of slice register sites lost to control set restrictions:	0	out of	11,440	0%

A LUT Flip Flop pair for this architecture represents one LUT paired with one Flip Flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element.

The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

IO Utilization:

Number of bonded IOBs:	36	out of	102	35%

Specific Feature Utilization:

Number of RAMB16BWERs:	0	out of	32	0%
Number of RAMB8BWERs:	0	out of	64	0%
Number of BUFIO2/BUFIO2_2CLKs:	0	out of	32	0%
Number of BUFIO2FB/BUFIO2FB_2CLKs:	0	out of	32	0%
Number of BUFG/BUFGMUXs:	1	out of	16	6%
Number used as BUFGs:	1			
Number used as BUFGMUX:	0			
Number of DCM/DCM_CLKGENs:	0	out of	4	0%
Number of ILOGIC2/ISERDES2s:	0	out of	200	0%
Number of IODELAY2/IODRP2/IODRP2_MCBs:	0	out of	200	0%

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  Number of OLOGIC2/OSERDES2s:                  0 out of     200    0%
  Number of BSCANs:                             0 out of       4    0%
  Number of BUFHs:                              0 out of     128    0%
  Number of BUFPLLs:                            0 out of       8    0%
  Number of BUFPLL_MCBs:                        0 out of       4    0%
  Number of DSP48A1s:                           1 out of      16    6%
  Number of ICAPs:                              0 out of       1    0%
  Number of MCBs:                               0 out of       2    0%
  Number of PCILOGICSEs:                        0 out of       2    0%
  Number of PLL_ADVs:                           0 out of       2    0%
  Number of PMVs:                               0 out of       1    0%
  Number of STARTUPs:                           0 out of       1    0%
  Number of SUSPEND_SYNCs:                      0 out of       1    0%


Overall effort level (-ol):   High
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 3 secs
Finished initial Timing Analysis.  REAL time: 3 secs

Starting Router


Phase  1  : 3810 unrouted;      REAL time: 3 secs

Phase  2  : 3542 unrouted;      REAL time: 4 secs

Phase  3  : 472 unrouted;      REAL time: 7 secs
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Phase 4 : 472 unrouted; (Par is working to improve performance) REAL time: 7 secs

Updating file: optimizedSourceFIRfilter.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Par is working to improve performance) REAL time: 8 secs

Phase 6 : 0 unrouted; (Par is working to improve performance) REAL time: 8 secs

Phase 7 : 0 unrouted; (Par is working to improve performance) REAL time: 8 secs

Phase 8 : 0 unrouted; (Par is working to improve performance) REAL time: 8 secs

Phase 9 : 0 unrouted; (Par is working to improve performance) REAL time: 8 secs

Phase 10 : 0 unrouted; (Par is working to improve performance) REAL time: 9 secs

Total REAL time to Router completion: 9 secs

Total CPU time to Router completion: 9 secs

Partition Implementation Status

No Partitions were found in this design.

Generating "PAR" statistics.

INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.

Timing Score: 0 (Setup: 0, Hold: 0)

Asterisk (*) preceding a constraint indicates it was not met.

   This may be due to a setup or hold violation.

Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
Autotimespec constraint for clock net tem	SETUP	N/A	27.462ns	N/A	0
p_BUFG	HOLD	0.317ns		0	0

All constraints were met.

INFO:Timing:2761 - N/A entries in the Constraints List may indicate that the

   constraint is not analyzed due to the following: No paths covered by this

   constraint; Other constraints intersect with this constraint; or This

   constraint was disabled by a Path Tracing Control. Please run the Timespec

   Interaction Report (TSI) via command line (trce tsi) or Timing Analyzer GUI.

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 9 secs
Total CPU time to PAR completion: 9 secs

Peak Memory Usage: 4521 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file optimizedSourceFIRfilter.ncd

PAR done!