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Release 14.7 Trace  (nt64)

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C:\xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v
3 -s 3

-n 3 -fastpaths -xml optimizedSourceFIRfilter.twx
optimizedSourceFIRfilter.ncd

-o optimizedSourceFIRfilter.twr optimizedSourceFIRfilter.pcf


Design file:              optimizedSourceFIRfilter.ncd

Physical constraint file: optimizedSourceFIRfilter.pcf

Device,package,speed:     xc6slx9,tqg144,C,-3 (PRODUCTION 1.23 2013-
10-13)

Report level:             verbose report


Environment Variable      Effect

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NONE                      No environment variables were set

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INFO:Timing:2698 - No timing constraints found, doing default
enumeration.

INFO:Timing:3412 - To improve timing, see the Timing Closure User
Guide (UG612).

INFO:Timing:2752 - To get complete path coverage, use the
unconstrained paths

   option. All paths that are not constrained will be reported in the

   unconstrained paths section(s) of the report.

INFO:Timing:3339 - The clock-to-out numbers in this timing report are
based on
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a 50 Ohm transmission line loading model. For the details of this model,

and for more information on accounting for different loading conditions,

please see the device datasheet.

Data Sheet report:

All values displayed in nanoseconds (ns)

Setup/Hold to clock aclk

Source	Max Setup to Clock (clk edge)	Process Corner	Max Hold to Clock (clk edge)	Process Corner	Internal Clock(s)	Phase
s_axis_data_tdata<0>	28.225(R)	SLOW	1.396(R)	SLOW	temp_BUFG	0.000
s_axis_data_tdata<1>	27.074(R)	SLOW	0.261(R)	SLOW	temp_BUFG	0.000
s_axis_data_tdata<2>	27.721(R)	SLOW	1.762(R)	SLOW	temp_BUFG	0.000
s_axis_data_tdata<3>	27.922(R)	SLOW	1.758(R)	SLOW	temp_BUFG	0.000
s_axis_data_tdata<4>	27.849(R)	SLOW	1.751(R)	SLOW	temp_BUFG	0.000
s_axis_data_tdata<5>	27.497(R)	SLOW	-0.146(R)	SLOW	temp_BUFG	0.000
s_axis_data_tdata<6>	28.288(R)	SLOW	1.151(R)	SLOW	temp_BUFG	0.000

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s_axis_data_tdata<7> |   27.727(R)|      SLOW  |    1.610(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<8> |   27.884(R)|      SLOW  |    1.813(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<9> |   28.140(R)|      SLOW  |    1.770(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<10>|   27.945(R)|      SLOW  |    1.767(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<11>|   27.112(R)|      SLOW  |    2.056(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<12>|   27.069(R)|      SLOW  |    0.597(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<13>|   27.991(R)|      SLOW  |    1.997(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<14>|   27.167(R)|      SLOW  |    1.689(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<15>|   27.418(R)|      SLOW  |    1.790(R)|
SLOW  |temp_BUFG         |   0.000|

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Setup/Hold to clock s_axis_data_tvalid

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                     |Max Setup to|  Process   |Max Hold to |  Process
|                  | Clock  |

Source               | clk (edge) |   Corner   | clk (edge) |   Corner
|Internal Clock(s) | Phase  |

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s_axis_data_tdata<0> |   28.260(R)|      SLOW  |    1.359(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<1> |   27.109(R)|      SLOW  |    0.224(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<2> |   27.756(R)|      SLOW  |    1.725(R)|
SLOW  |temp_BUFG         |   0.000|
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s_axis_data_tdata<3> |   27.957(R)|      SLOW  |    1.721(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<4> |   27.884(R)|      SLOW  |    1.714(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<5> |   27.532(R)|      SLOW  |   -0.183(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<6> |   28.323(R)|      SLOW  |    1.114(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<7> |   27.762(R)|      SLOW  |    1.573(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<8> |   27.919(R)|      SLOW  |    1.776(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<9> |   28.175(R)|      SLOW  |    1.733(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<10>|   27.980(R)|      SLOW  |    1.730(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<11>|   27.147(R)|      SLOW  |    2.019(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<12>|   27.104(R)|      SLOW  |    0.560(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<13>|   28.026(R)|      SLOW  |    1.960(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<14>|   27.202(R)|      SLOW  |    1.652(R)|
SLOW  |temp_BUFG         |   0.000|

s_axis_data_tdata<15>|   27.453(R)|      SLOW  |    1.753(R)|
SLOW  |temp_BUFG         |   0.000|

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Clock aclk to Pad

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                    |Max (slowest) clk|  Process   |Min (fastest)
clk|  Process   |                  | Clock  |

Destination         |  (edge) to PAD  |   Corner   |  (edge) to PAD
|   Corner   |Internal Clock(s) | Phase  |
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m_axis_data_tdata<0> |        10.762(R)|      SLOW  |
6.102(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<1> |        10.302(R)|      SLOW  |
5.814(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<2> |        10.325(R)|      SLOW  |
5.868(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<3> |        10.200(R)|      SLOW  |
5.784(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<4> |        10.120(R)|      SLOW  |
5.709(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<5> |        10.381(R)|      SLOW  |
5.892(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<6> |        10.267(R)|      SLOW  |
5.851(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<7> |         9.997(R)|      SLOW  |
5.655(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<8> |         9.575(R)|      SLOW  |
5.332(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<9> |         9.532(R)|      SLOW  |
5.315(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<10>|         9.582(R)|      SLOW  |
5.365(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<11>|         9.553(R)|      SLOW  |
5.348(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<12>|         9.947(R)|      SLOW  |
5.666(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<13>|         9.728(R)|      SLOW  |
5.488(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<14>|         9.838(R)|      SLOW  |
5.621(R)|      FAST  |temp_BUFG         |   0.000|

m_axis_data_tdata<15>|         9.845(R)|      SLOW  |
5.654(R)|      FAST  |temp_BUFG         |   0.000|

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Clock s_axis_data_tvalid to Pad

Destination	Max (slowest) clk (edge) to PAD	Process Corner	Min (fastest) clk (edge) to PAD	Process Corner	Clock Internal Clock(s)	Phase
m_axis_data_tdata<0>	10.725(R)	SLOW	6.048(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<1>	10.265(R)	SLOW	5.760(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<2>	10.288(R)	SLOW	5.814(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<3>	10.163(R)	SLOW	5.730(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<4>	10.083(R)	SLOW	5.655(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<5>	10.344(R)	SLOW	5.838(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<6>	10.230(R)	SLOW	5.797(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<7>	9.960(R)	SLOW	5.601(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<8>	9.538(R)	SLOW	5.278(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<9>	9.495(R)	SLOW	5.261(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<10>	9.545(R)	SLOW	5.311(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<11>	9.516(R)	SLOW	5.294(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<12>	9.910(R)	SLOW	5.612(R)	FAST	temp_BUFG	0.000
m_axis_data_tdata<13>	9.691(R)	SLOW	5.434(R)	FAST	temp_BUFG	0.000

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m_axis_data_tdata<14>|         9.801(R)|      SLOW  |
5.567(R)|      FAST  |temp_BUFG         |   0.000|
m_axis_data_tdata<15>|         9.808(R)|      SLOW  |
5.600(R)|      FAST  |temp_BUFG         |   0.000|
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Clock to Setup on destination clock aclk
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                  | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock      |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
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aclk              |   27.462|         |         |         |
s_axis_data_tvalid|   27.462|         |         |         |
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Clock to Setup on destination clock s_axis_data_tvalid
------------------+---------+---------+---------+---------+
                  | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock      |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
------------------+---------+---------+---------+---------+
aclk              |   27.462|         |         |         |
s_axis_data_tvalid|   27.462|         |         |         |
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Analysis completed Thu Jun 21 17:34:31 2018
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Trace Settings:
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Trace Settings

Peak Memory Usage: 4590 MB