

Release 14.7 Trace (nt64)

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C:\xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v
3 -s 3

-n 3 -fastpaths -xml core_m.twx core_m.ncd -o core_m.twr core_m.pcf

Design file: core_m.ncd

Physical constraint file: core_m.pcf

Device,package,speed: xc6slx9,tqg144,C,-3 (PRODUCTION 1.23 2013-
10-13)

Report level: verbose report

Environment Variable	Effect
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NONE	No environment variables were set
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INFO:Timing:2698 - No timing constraints found, doing default
enumeration.

INFO:Timing:3412 - To improve timing, see the Timing Closure User
Guide (UG612).

INFO:Timing:2752 - To get complete path coverage, use the
unconstrained paths

option. All paths that are not constrained will be reported in the
unconstrained paths section(s) of the report.

INFO:Timing:3339 - The clock-to-out numbers in this timing report are
based on

a 50 Ohm transmission line loading model. For the details of this
model,

and for more information on accounting for different loading conditions,

please see the device datasheet.

Data Sheet report:

All values displayed in nanoseconds (ns)

Setup/Hold to clock aclk

		Max Setup to	Process	Max Hold to	Process
		Clock			
Source	clk (edge)	Corner	clk (edge)	Corner	
Internal Clock(s)	Phase				
-----+-----+-----+-----+-----					
---+-----+-----+-----+-----					
s_axis_data_tdata<0>	2.265 (R)	SLOW	-1.077 (R)		
FAST aclk_BUFGP	0.000				
s_axis_data_tdata<1>	2.025 (R)	SLOW	-0.929 (R)		
FAST aclk_BUFGP	0.000				
s_axis_data_tdata<2>	2.337 (R)	SLOW	-1.098 (R)		
FAST aclk_BUFGP	0.000				
s_axis_data_tdata<3>	2.349 (R)	SLOW	-1.101 (R)		
FAST aclk_BUFGP	0.000				
s_axis_data_tdata<4>	2.423 (R)	SLOW	-1.176 (R)		
FAST aclk_BUFGP	0.000				
s_axis_data_tdata<5>	2.276 (R)	SLOW	-1.060 (R)		
FAST aclk_BUFGP	0.000				
s_axis_data_tdata<6>	2.116 (R)	SLOW	-0.947 (R)		
FAST aclk_BUFGP	0.000				
s_axis_data_tdata<7>	1.997 (R)	SLOW	-0.830 (R)		
FAST aclk_BUFGP	0.000				

s_axis_data_tdata<8>		2.262 (R)		SLOW		-1.017 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tdata<9>		2.377 (R)		SLOW		-1.112 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tdata<10>		2.041 (R)		SLOW		-0.858 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tdata<11>		2.420 (R)		SLOW		-1.159 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tdata<12>		2.693 (R)		SLOW		-1.436 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tdata<13>		2.592 (R)		SLOW		-1.331 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tdata<14>		2.619 (R)		SLOW		-1.367 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tdata<15>		2.620 (R)		SLOW		-1.314 (R)	
FAST		aclk_BUFGP		0.000			
s_axis_data_tvalid		2.421 (R)		SLOW		-1.229 (R)	
FAST		aclk_BUFGP		0.000			

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Clock aclk to Pad

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clk	Process		Max (slowest) clk	Process		Min (fastest)
			Clock			
Destination			(edge) to PAD	Corner		(edge) to PAD
Corner	Internal Clock(s)		Phase			

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m_axis_data_tdata<0>		8.955 (R)		SLOW	
4.861 (R)		FAST		aclk_BUFGP	
				0.000	
m_axis_data_tdata<1>		9.024 (R)		SLOW	
4.910 (R)		FAST		aclk_BUFGP	
				0.000	
m_axis_data_tdata<2>		9.530 (R)		SLOW	
5.301 (R)		FAST		aclk_BUFGP	
				0.000	

m_axis_data_tdata<3>		9.356 (R)		SLOW	
5.189 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<4>		9.286 (R)		SLOW	
5.126 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<5>		8.968 (R)		SLOW	
4.909 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<6>		9.715 (R)		SLOW	
5.407 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<7>		9.574 (R)		SLOW	
5.313 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<8>		9.405 (R)		SLOW	
5.216 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<9>		9.387 (R)		SLOW	
5.236 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<10>		8.832 (R)		SLOW	
4.786 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<11>		8.572 (R)		SLOW	
4.637 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<12>		8.707 (R)		SLOW	
4.704 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<13>		7.694 (R)		SLOW	
4.105 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<14>		8.969 (R)		SLOW	
4.918 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tdata<15>		7.797 (R)		SLOW	
4.222 (R)		FAST		ac1k_BUFGP	
				0.000	
m_axis_data_tvalid		7.367 (R)		SLOW	
3.939 (R)		FAST		ac1k_BUFGP	
				0.000	
s_axis_data_tready		7.802 (R)		SLOW	
4.198 (R)		FAST		ac1k_BUFGP	
				0.000	

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Clock to Setup on destination clock ac1k

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

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Source	Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
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aclk		3.594			
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Analysis completed Sat Jun 23 20:30:10 2018

Trace Settings:

Trace Settings

Peak Memory Usage: 4572 MB