Encode: Given that we have direct communication available between the two processes we use cache access as a way to communicate. In order to encode the message, the protocol checks whether the given bit is 1 or 0. When the bit is 1, the sender will access a selected address location and if the bit 0 it does nothing. The given operation is defined in the sender.c using a loop in the main() to check the bit value and the make use of send\_bit() function to access the selected memory location. To assist the 8 bit encoding we select 8 cache sets from the entire L2 size cache and create an eviction set. Once that is done, we assign one set for each bit for the 8 bit message. For each bit we will access the entire set.

Receive: The receiver will record the amount of time (cycles) it takes to access an address from the same cache sets as defined in the sender code. To do so the receiver first selects a buffer of the size of L2 cache and using this creates an eviction buffer with the same addresses as selected in the sender code. Once that is done it will prime the L2 cache by accessing all of the address locations of the defined buffer. Now that the L2 cache will contain all of the receiver data, whenever a message bit 1 and the sender accesses the cache address, it will evict the receiver lines. Since the lines will be evicted when we later try to access it again (in the decode phase) it will take a longer time since there will be a cache miss. Using this principle we establish communication.

Decode: When the receiver enters the decode phase, it will access all the addresses from the eviction set and record the access time using the measure\_one\_block\_access\_time() function and store it in an array. Once we have the latency numbers we will check each one of them against a threshold value. The threshold value was derived based on the Part1 Timing exercise. Basically we keep the threshold value to 50 cycles as most accesses to L2 and L1 caches take less than 50 cycles. Based on that, if 3 (just a threshold chosen) of the latency numbers for each set are above the threshold value we know that receiver evicted few of the sender cache lines and the message bit will be 1, else it will be considered as 0. Both thresholds need to be tweaked and tested multiple times to get a good success rate.