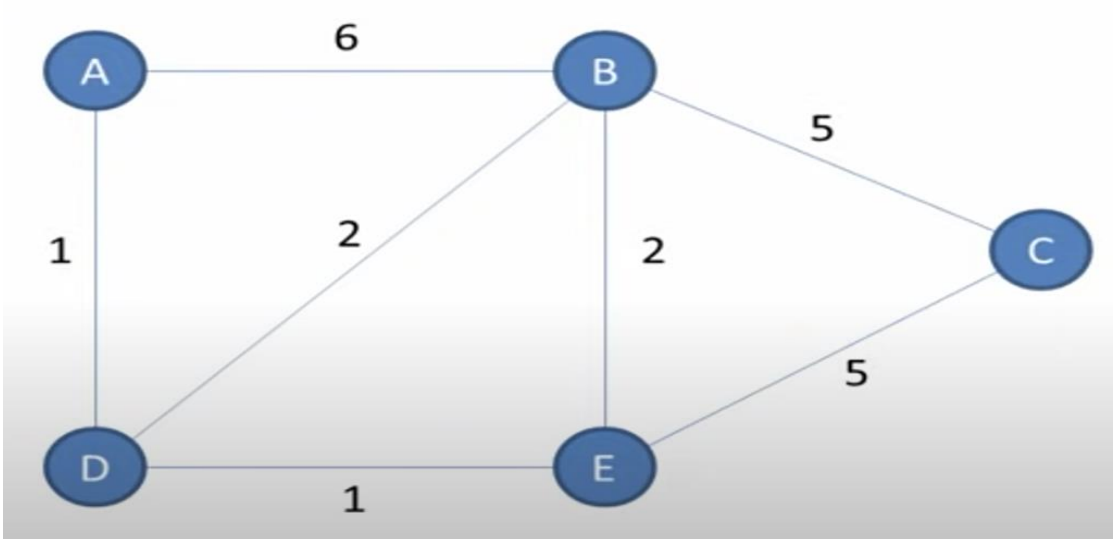
DIJKSTRA ALGORITHM USING DIGITAL ELECTRONICS

Dijkstra Algorithm – It is a greedy algorithm that helps us to find the shortest paths from the source to all vertices in a given graph.

Let us take an example of a graph so that it is easy for us to understand.



(Here, consider A, B, C, D, and E as 0,1,2,3,4 for convenience)

➔ For the given graph, the ideal adjacency matrix (8x8) should be

Node no	0	1	2	3	4	5	6	7
0	0	1	0	1	0	0	0	0
1	1	0	1	1	1	0	0	0
2	0	1	0	0	1	0	0	0
3	1	1	0	0	1	0	0	0
4	0	1	1	1	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0

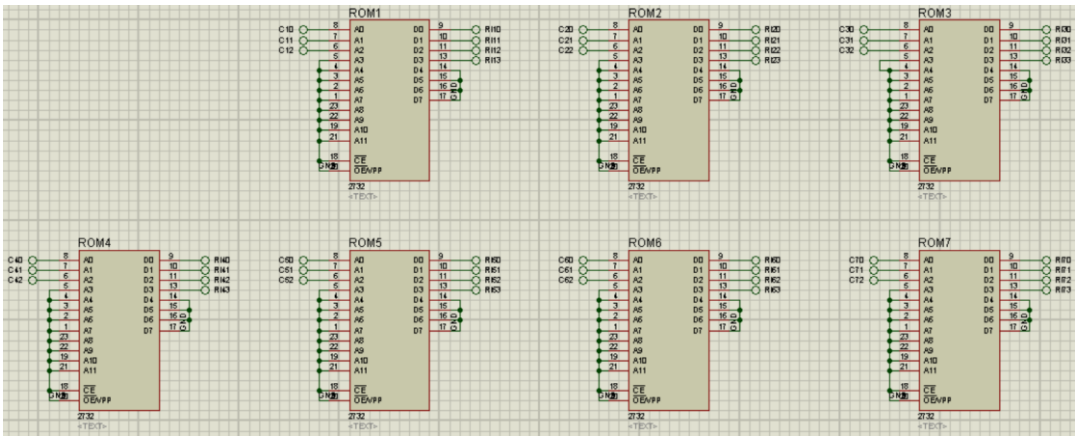
➔ To modify the adjacency matrix, we will replace the ones with the distance between two consecutive nodes and will replace the zeros with infinite distance, which in this particular digital circuit is 15. So the modified adjacency matrix will be: -

Node no	0	1	2	3	4	5	6	7
0	15	6	15	1	15	15	15	15
1	6	15	5	2	2	15	15	15
2	15	5	15	15	5	15	15	15
3	1	2	15	15	1	15	15	15
4	15	2	5	1	15	15	15	15
5	15	15	15	15	15	15	15	15
6	15	15	15	15	15	15	15	15
7	15	15	15	15	15	15	15	15

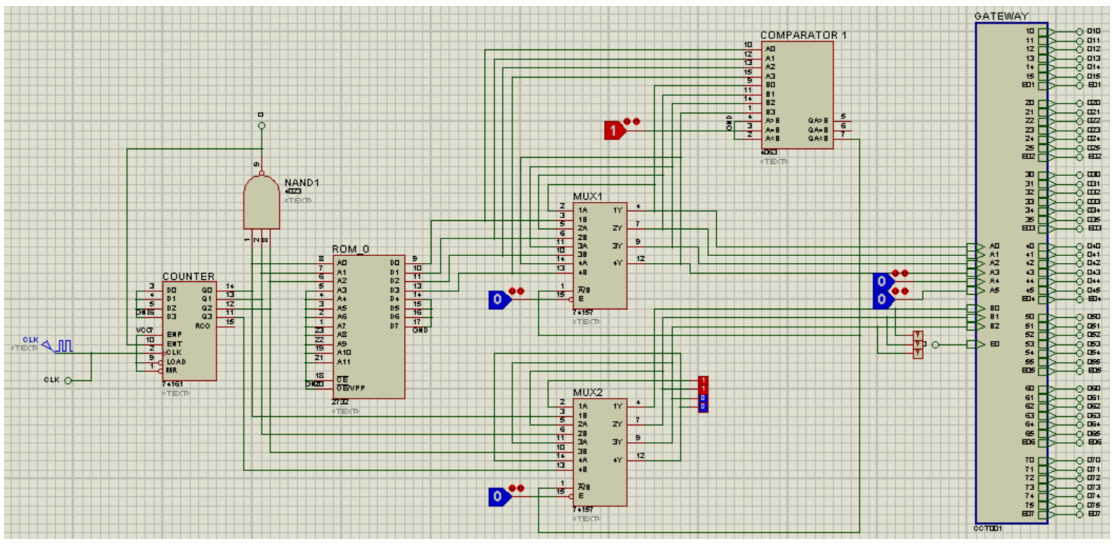
➔ After the adjacency matrix is modified, we will take each row and make its binary file, which is given as input to the ROM. (The python code for making binary files and the binary files are provided in the repository)

CIRCUIT EXPLANATION

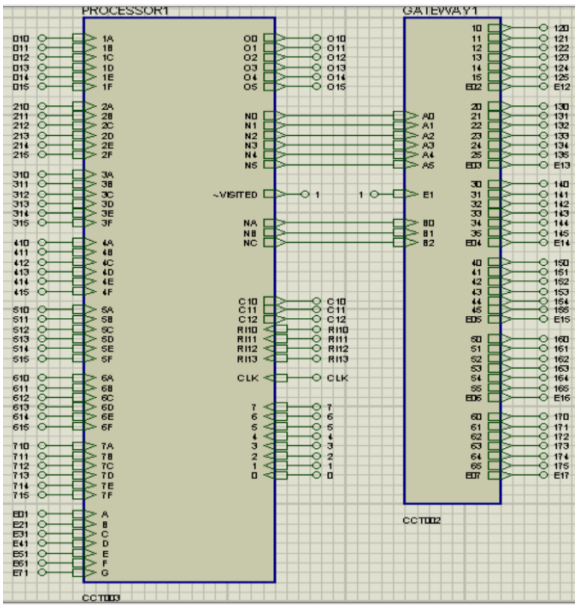
- **Input**: - We have used ROM (IC2732) and counters(IC74161) for input.



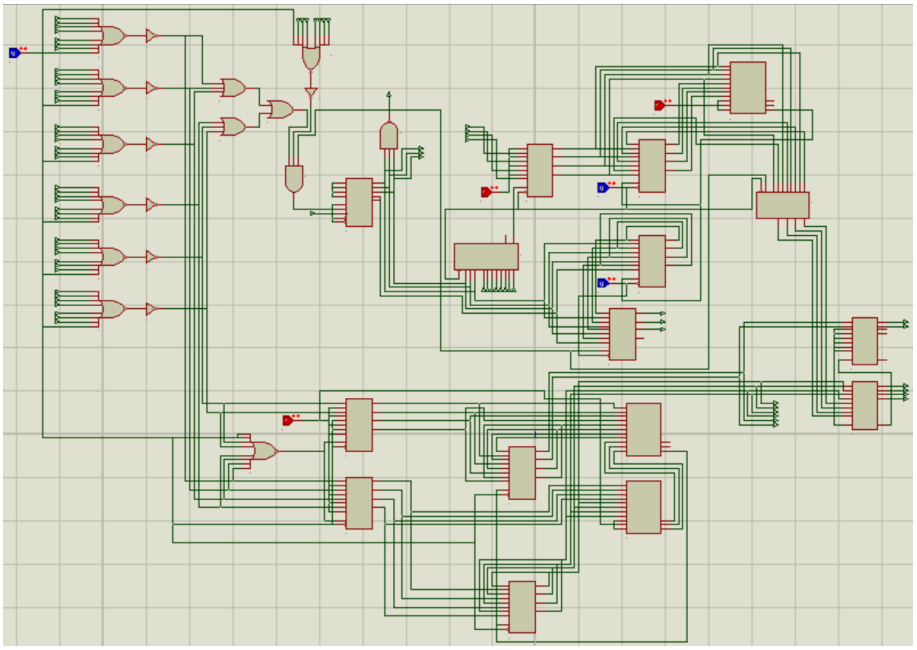
- **Source Node**: - The circuit finds the node along with the minimum distance from it and assigns it as the next node, and the gateway takes the distance value to the required node.



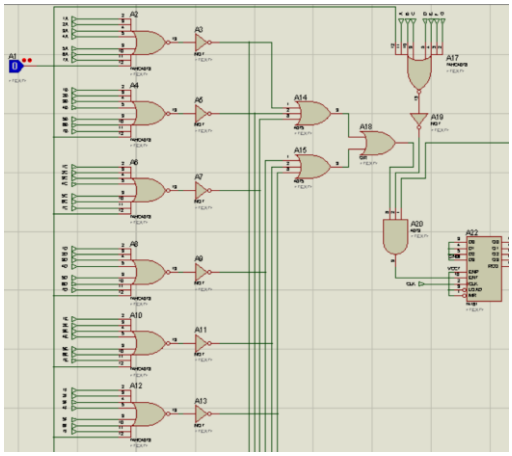
- The remaining circuit mainly consists of two parts: - Processor and Gateway



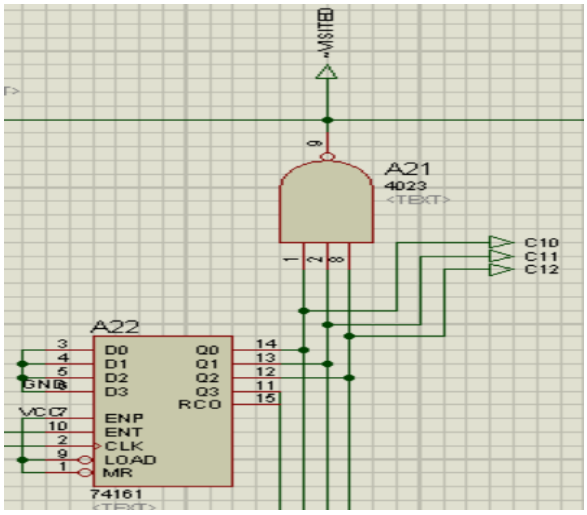
  - ❖ The function of the **processor** is to do the calculation, i.e., find the minimum distance of the current node from the source node and find the next node at the minimum distance from it.
  - ❖ The function of the **gateway** is to receive the next node and its minimum distance from the source node and take the values to the next node.
- **Processor**: - The basic layout of the processor is as follows



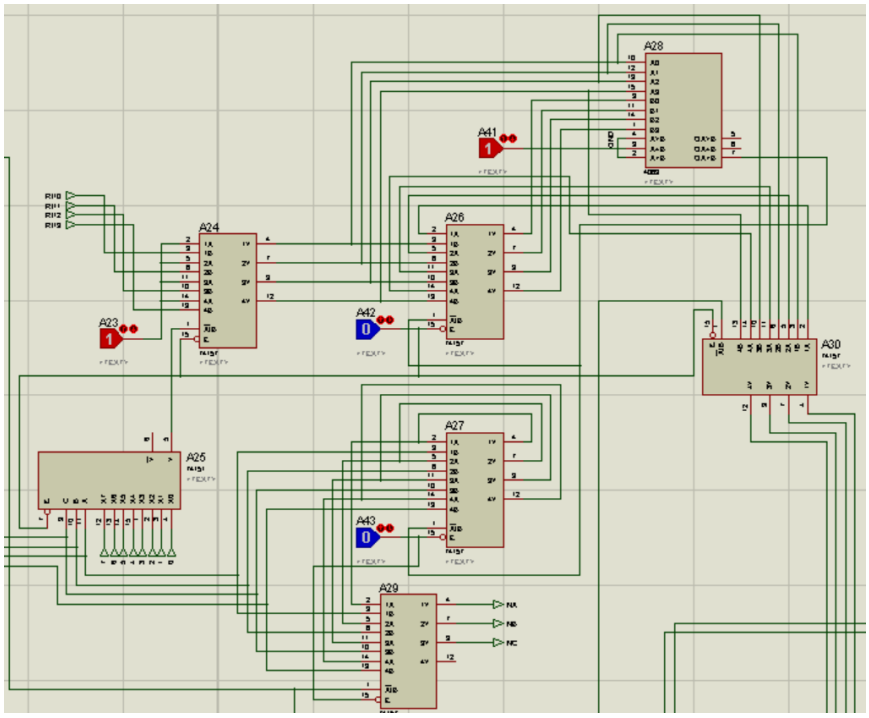
  - ❖ First, it receives the minimum distance from the previous node, and when it gets the enable bit, it starts behaving as the current node.



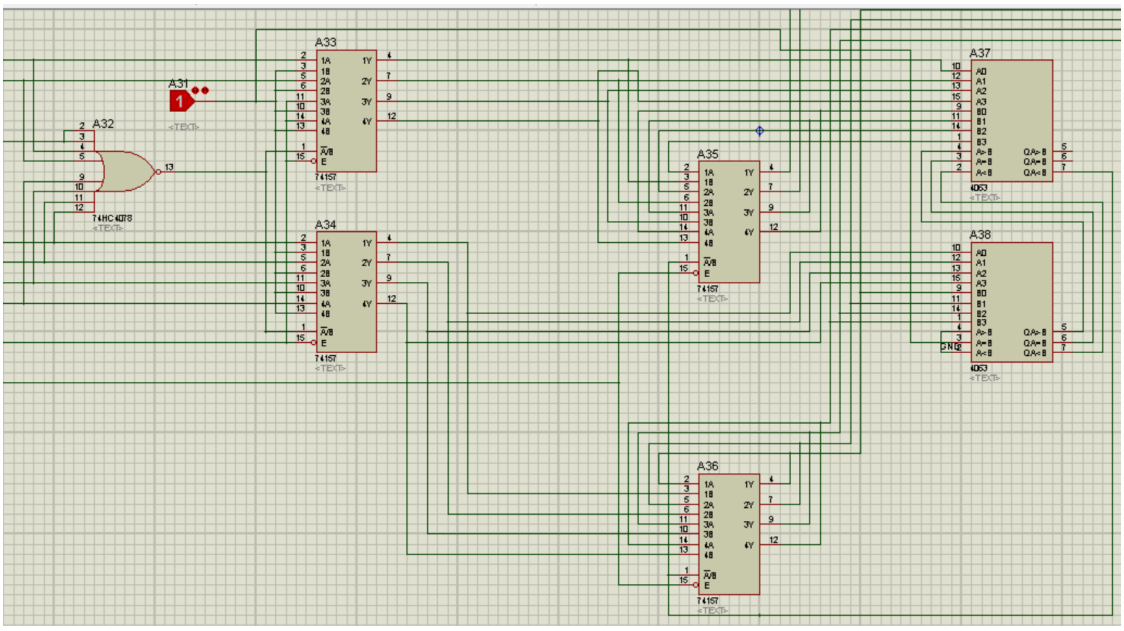
- Then, the counters start counting from 0 to 7, which is fed into the ROM to extract the data.



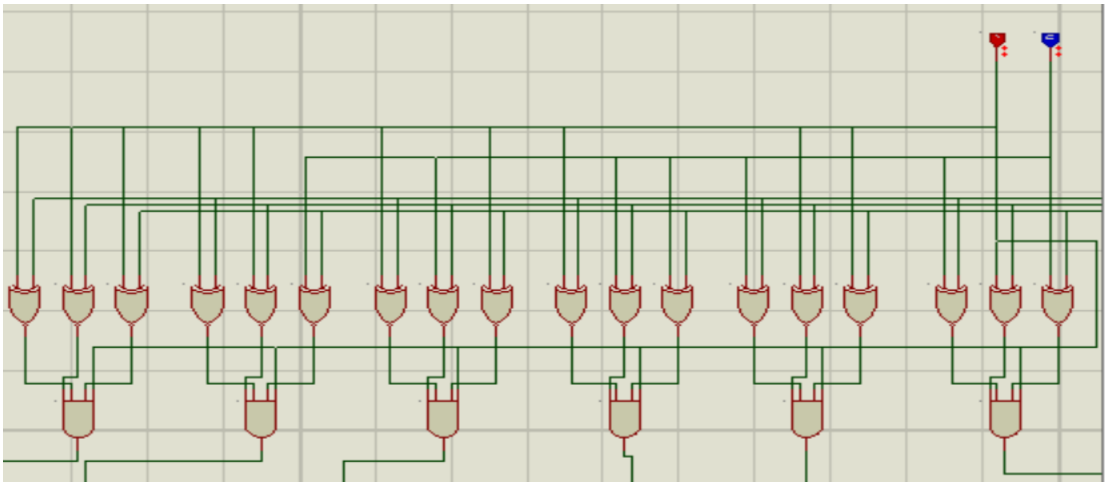
- The next part finds the minimum distance of the next node from the current node and ensures that it is not visited earlier.



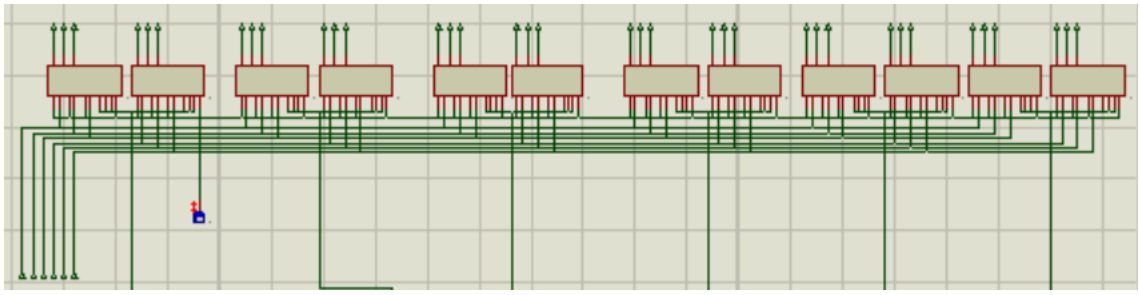
- The bottom part of the circuit finds the minimum distance of the current node from the source node through all possible paths received.



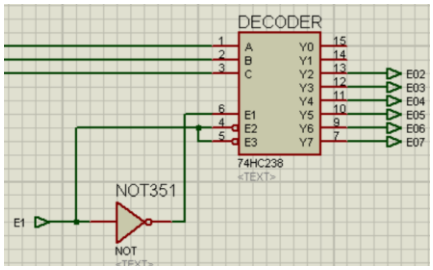
- **Gateway**: - It consists of three parts
  - ❖ XNOR gates for bit matching to channel the distance value to the next node by providing the select line for the 6x3 multiplexers.



  - ❖ 6x3 Multiplexers are present whose output is the distance whenever it is in state one else output is 0.



  - ❖ 3x8 decoder provides the enable bit for the processor of the next node.



Output: - The output is shown using logic probes and only checks the nodes for which the graph is made (for other unused nodes, it gives garbage value).