DIGISIM PS-1 PART 2

EXPLANATION

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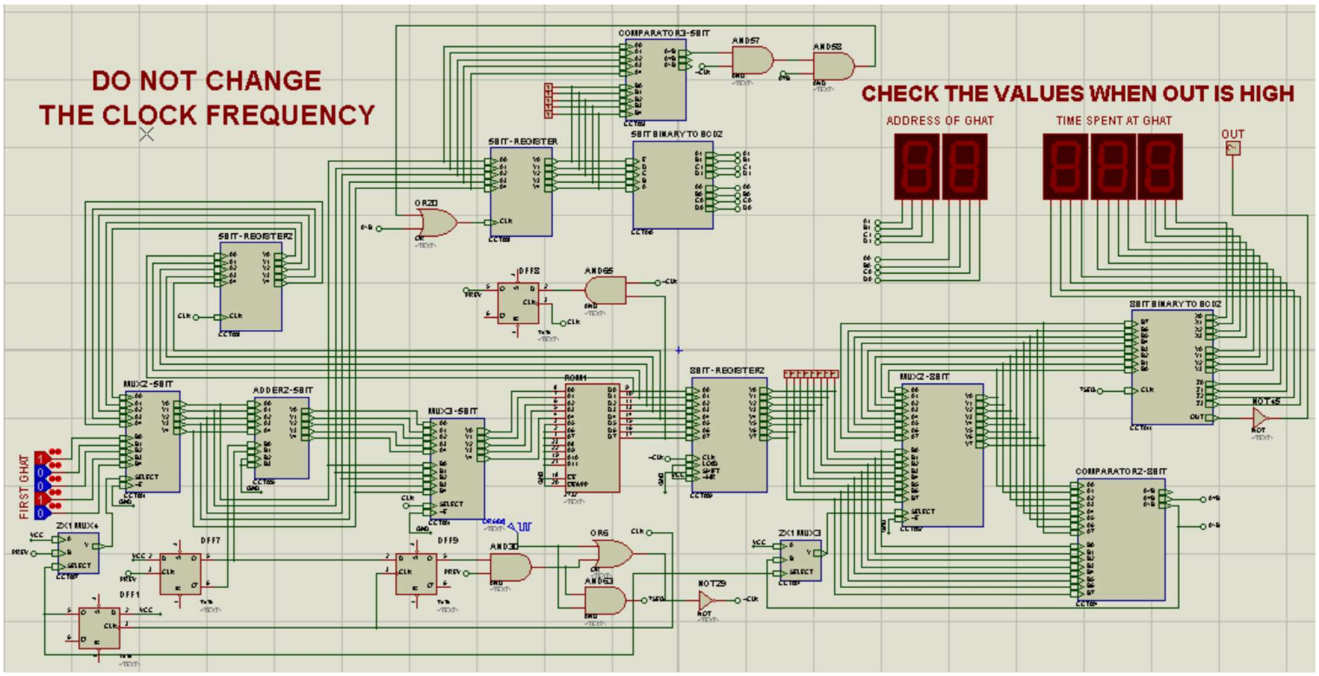
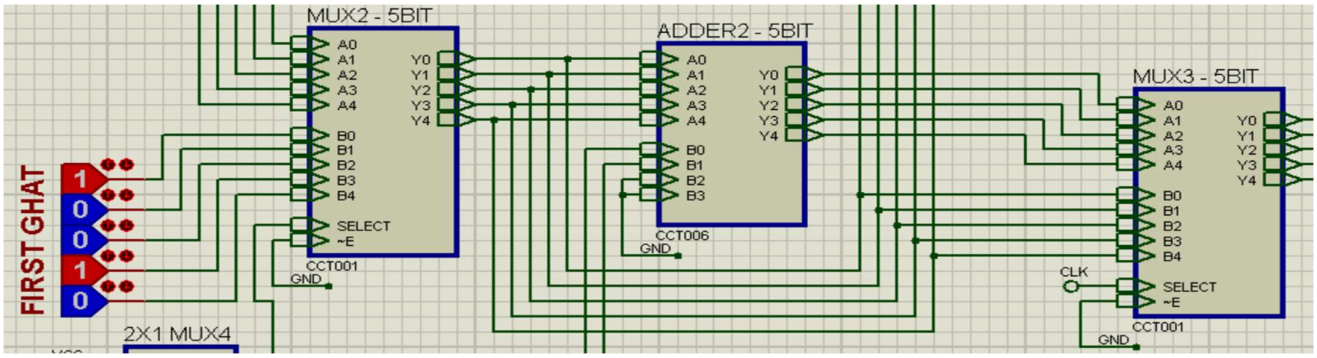
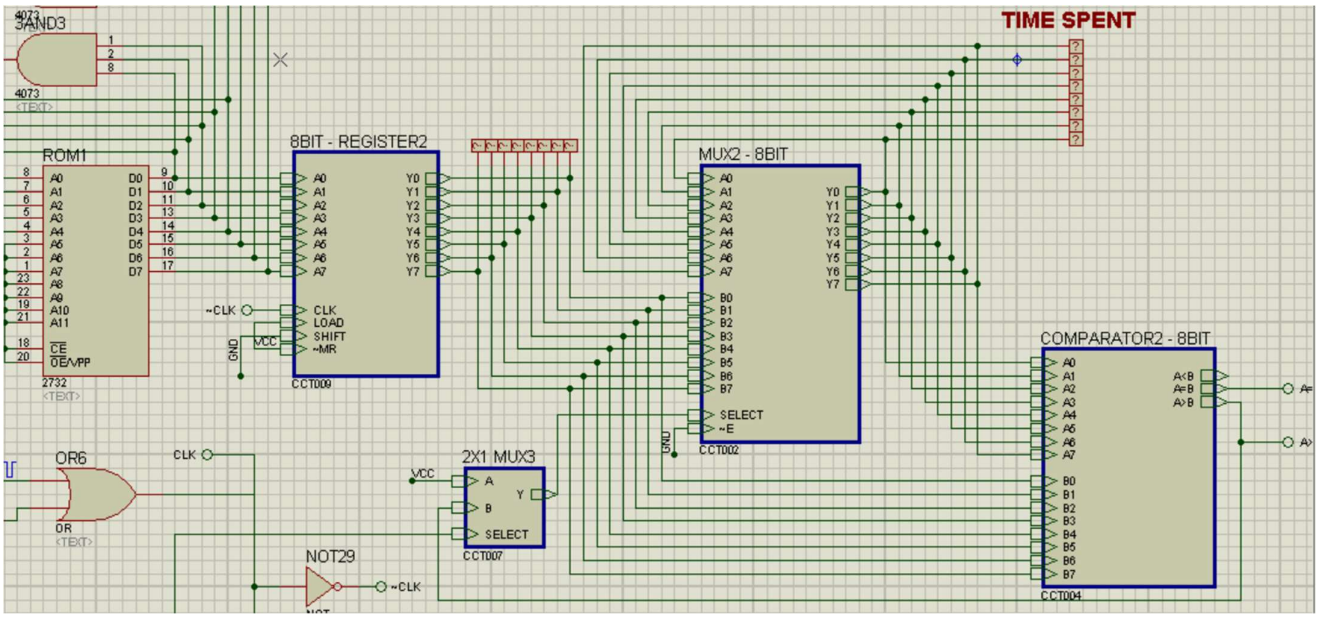
Circuit Diagram:



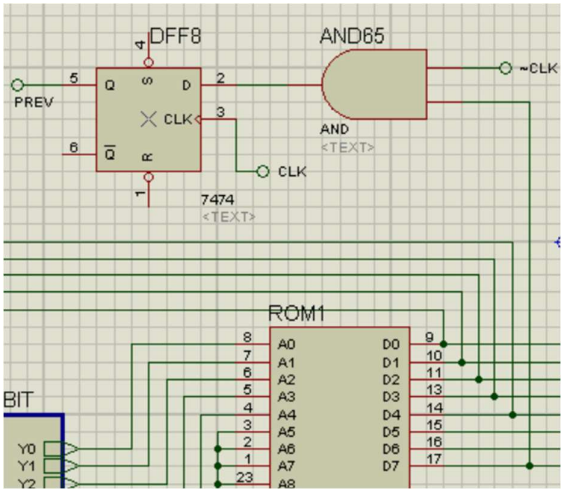
EXPLANATION:



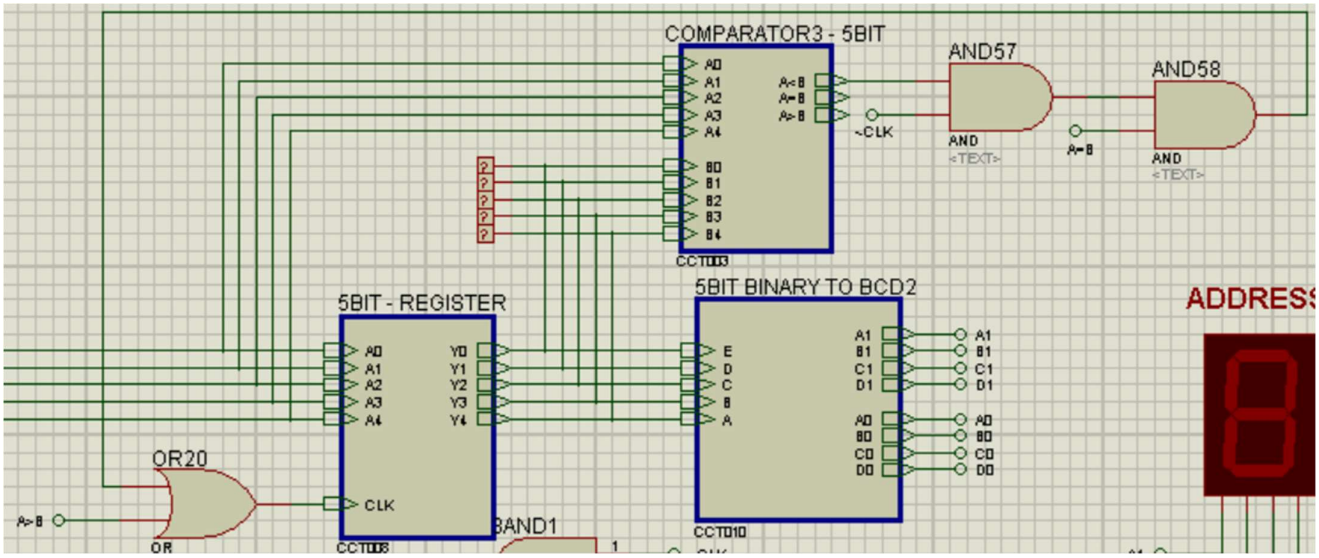
- First, we take input which is the address of the first ghat from where Manali and her friends are starting using a Multiplexer, which initially takes the address of the first node and then gives the output of the next node
- Then, we feed the output of the multiplexer to an adder that adds 1, which is used to find the address of the next node.
- The output of the adder and the initial multiplexer is fed to another multiplexer that has a clock as its select line, which means it selects the output from the adder when the clock is zero. It takes the address of the current node when the clock is one.
- Then, the address is fed into the ROM, which gives the output according to the binary file stored in it.



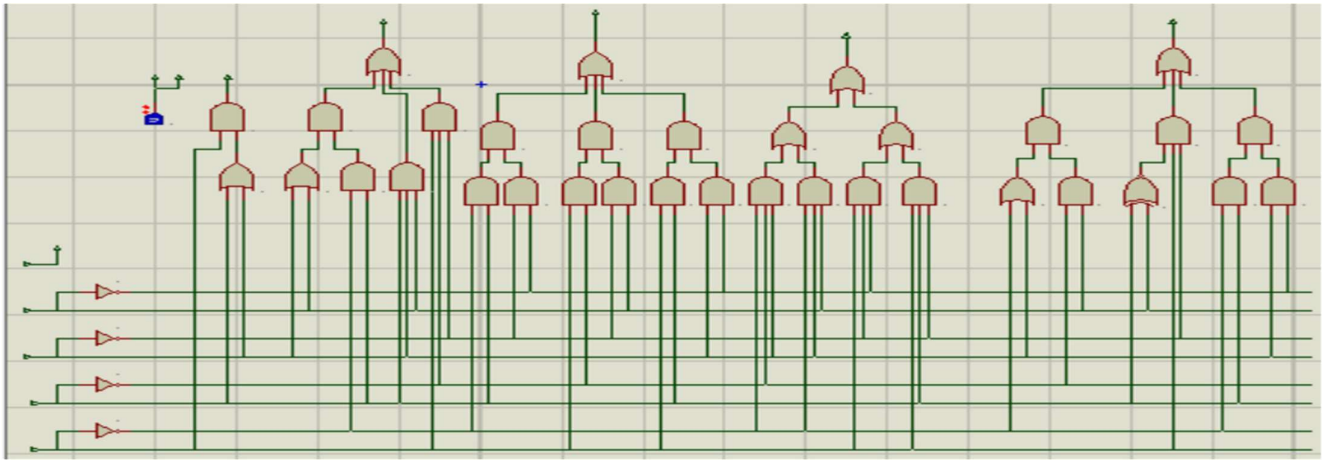
- Then, we have an 8-bit register which is negative edge triggered. So, it will store the data (which will be the time spent at a particular ghat) given to it at the falling edge of the clock.
- Following the register is an 8-bit multiplexer and an 8-bit comparator which are used to find out the lowest and store it.
- We also have used a 5-bit register (positive edge triggered) to store the address of the next node.



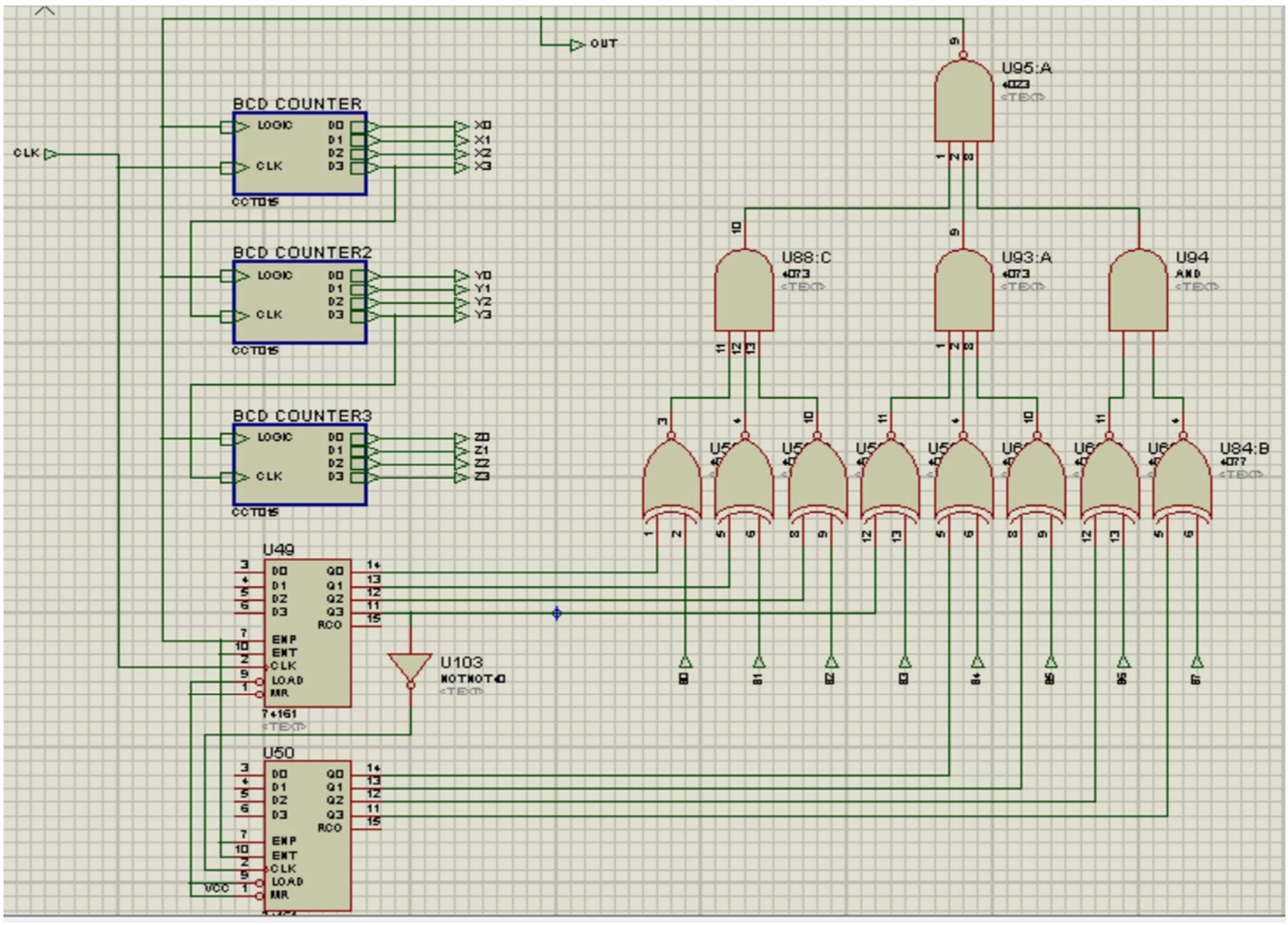
- Next, we have used an AND gate and a flip flop so that when the address of the next node is 255, we can reverse or stop the circuit.



- Then, we used a 5-bit register to store the address of the node where the minimum data is found. Also, we have used the comparator to find the minimum value of the address in case minimum data is found at two addresses.
- We also made a 5-bit BINARY TO BCD converter to display the output binary numbers in BCD (Made using K-Map).



- We also made an 8-bit BINARY to BCD converter using a BCD counter to display the minimum time spent at a ghat on 7 segment display (Picture on next page). (Though it takes more time to display the final answer but it is cost effective)



Components used in Circuit:

1. ROM (2732) – 1
2. Clock – 1
3. 4-bit Magnitude Comparator (7485) – 3
4. 4-bit Universal Shift Register (74179) – 4
5. 4-Counter (74161) – 5
6. 4-bit Binary Adder (74283) – 1
7. D Flip Flop (7474) – 6
8. 3 Input AND Gates – 9
9. 3 Input NAND Gates – 1
10. 3 Input OR Gates – 3
11. 2 Input AND Gates – 65
12. 2 Input NAND Gates – 3
13. 2 Input OR Gates – 28
14. NOT Gates – 13
15. 2 Input XOR Gates – 1
16. 2 Input XNOR Gates – 10

Total Cost of Circuit: **161.6**