wave forms

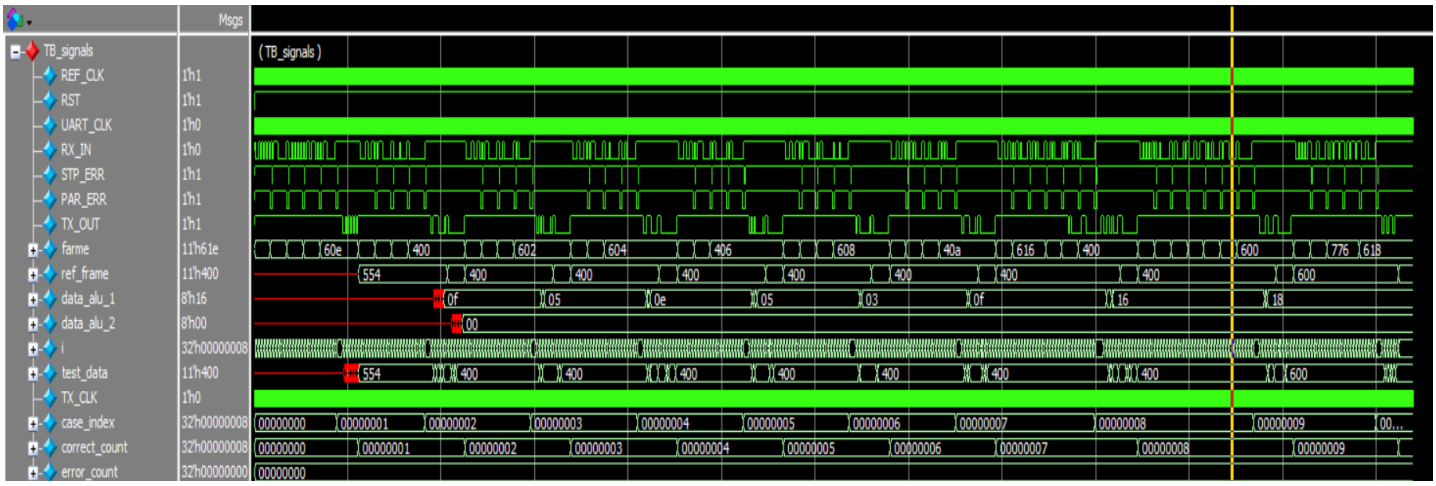

Figure 1 : TB SIGNALS

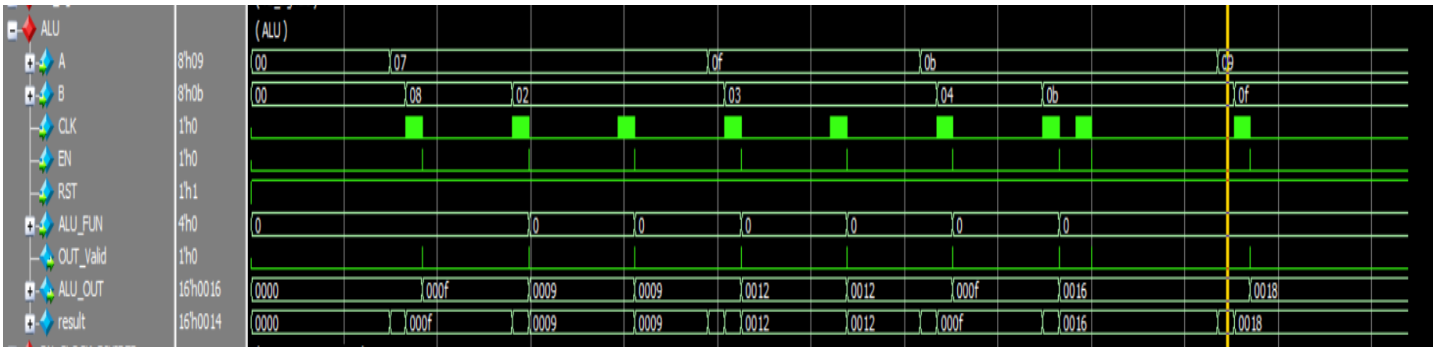

Figure 2: ALU signals

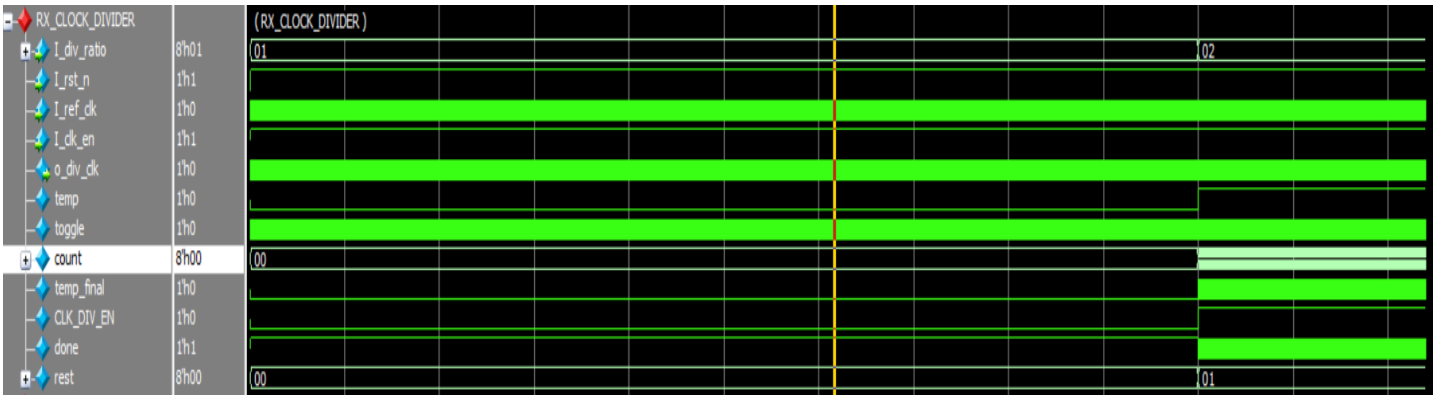

Figure 3: RX_CLOCK_DIVIDER signals

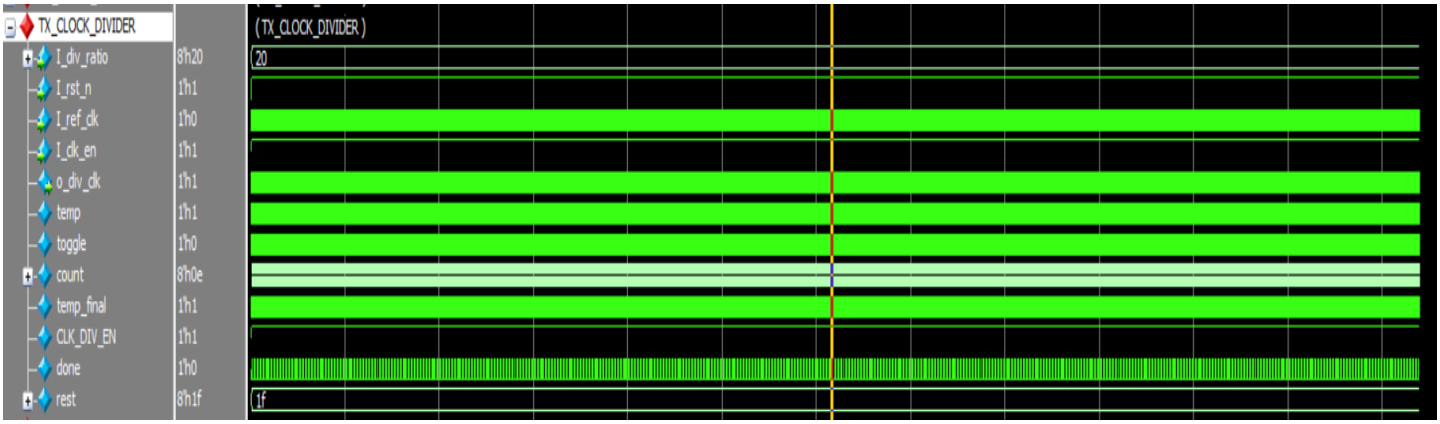

Figure 4: TX_CLOCK_DIVIDER

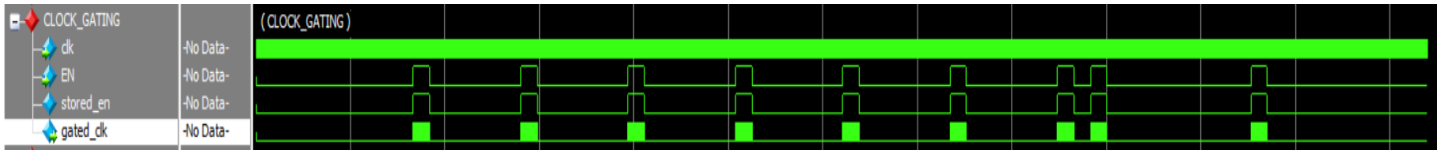

Figure 5 clock gating signals

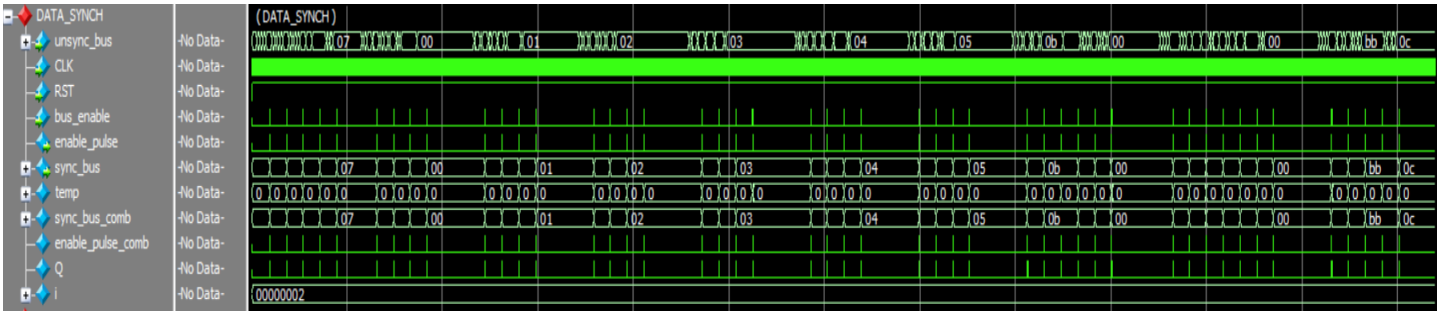

Figure 6: data synchronizer signals

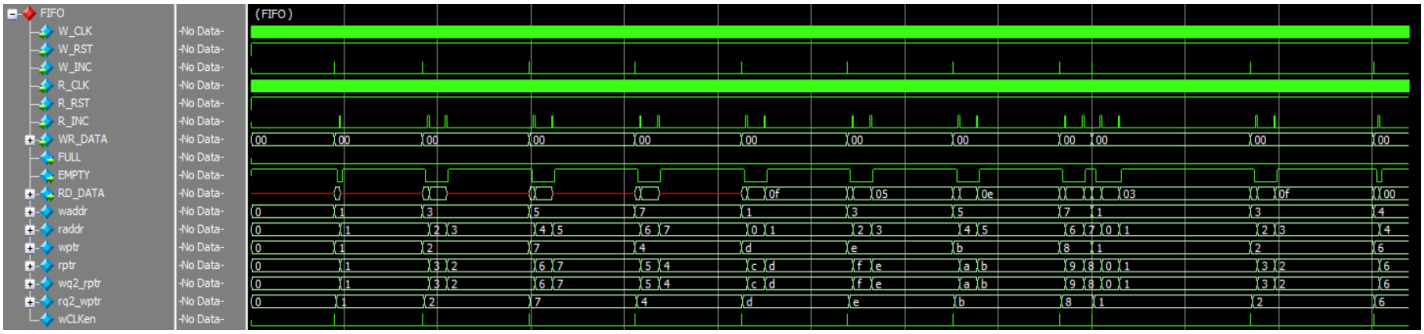

Figure 7 FIFO signals

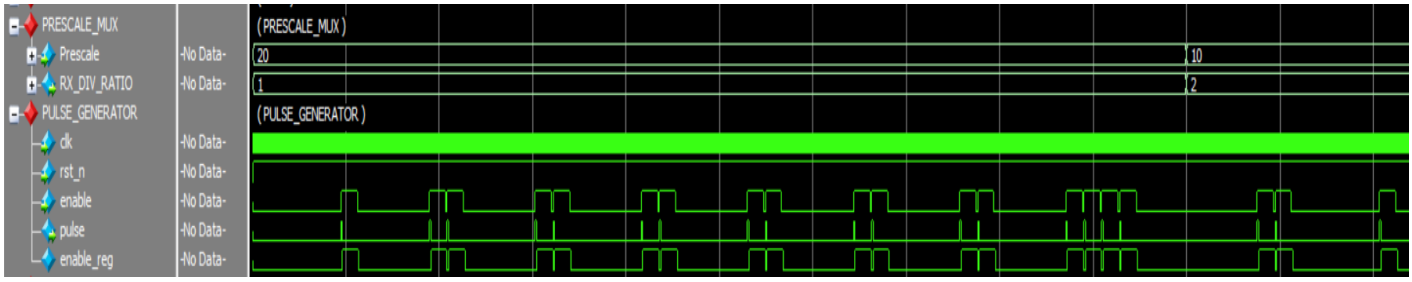

Figure 8: PULSE GENERATOR AND PRESCALE MUX signals

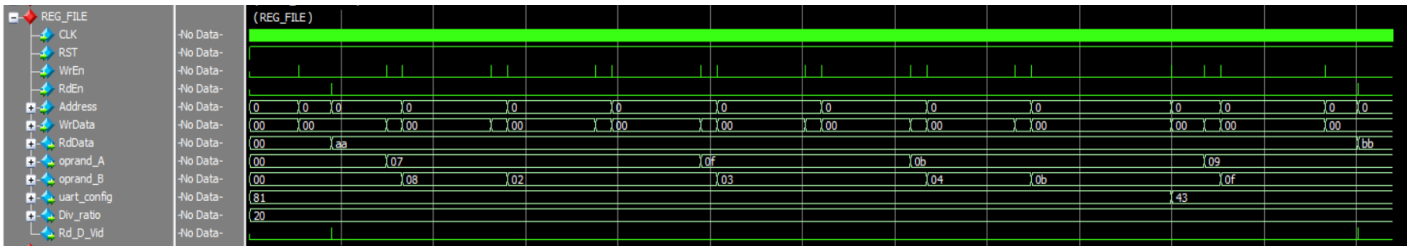

Figure 9: register file signals

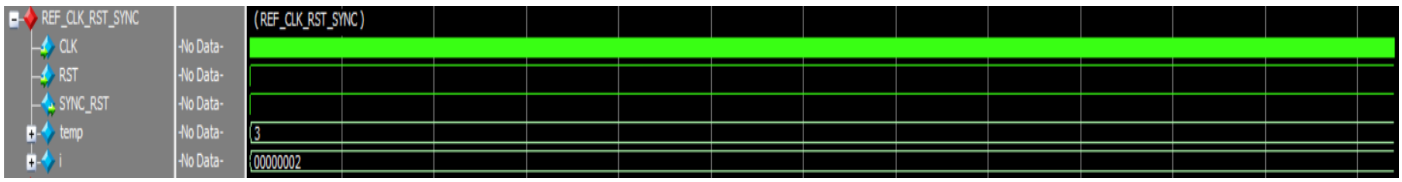

Figure 10: reference clock Reset synchronizer signals

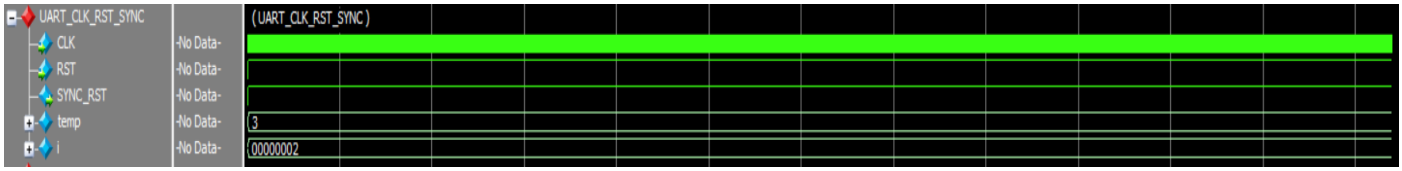

Figure 11: UART clock Reset synchronizer signals

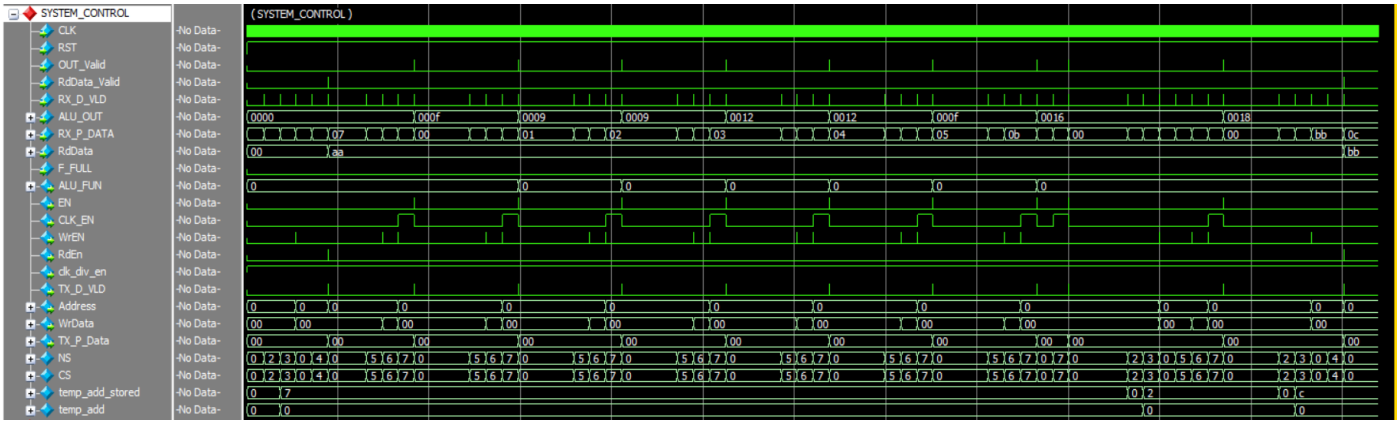

Figure 11: SYSTEM CONTROL Signals

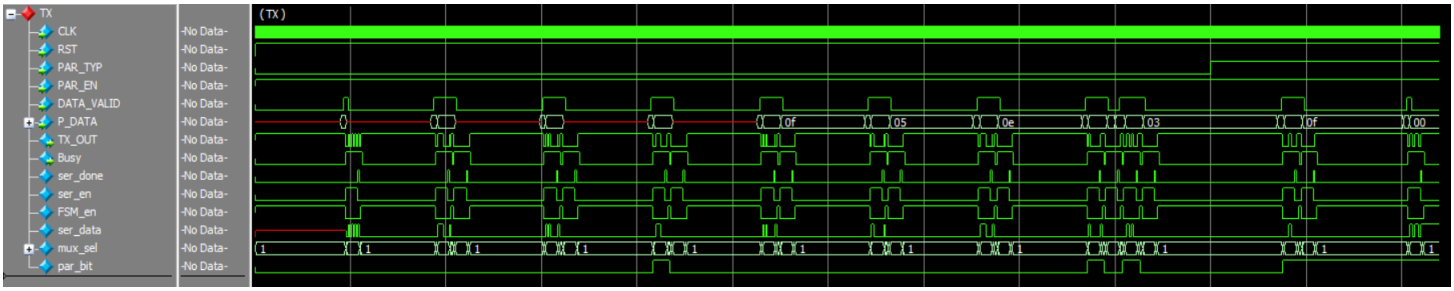

Figure 13: TX signals

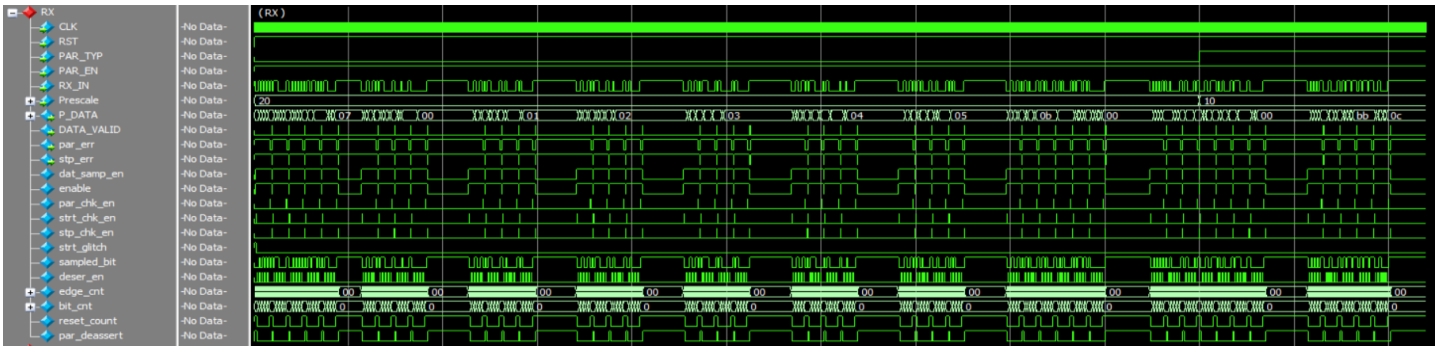

Figure 14: RX signals

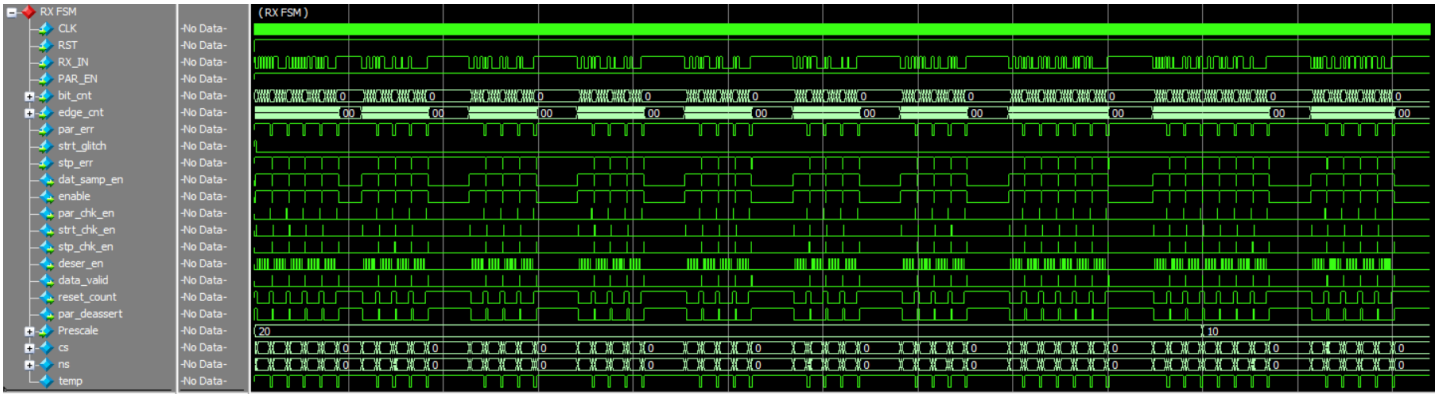

Figure 15: RX FSM signals

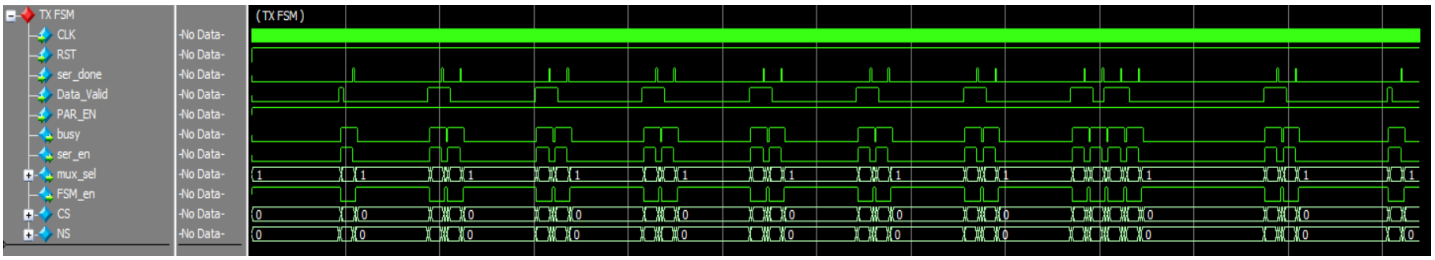

Figure 16: TX FSM

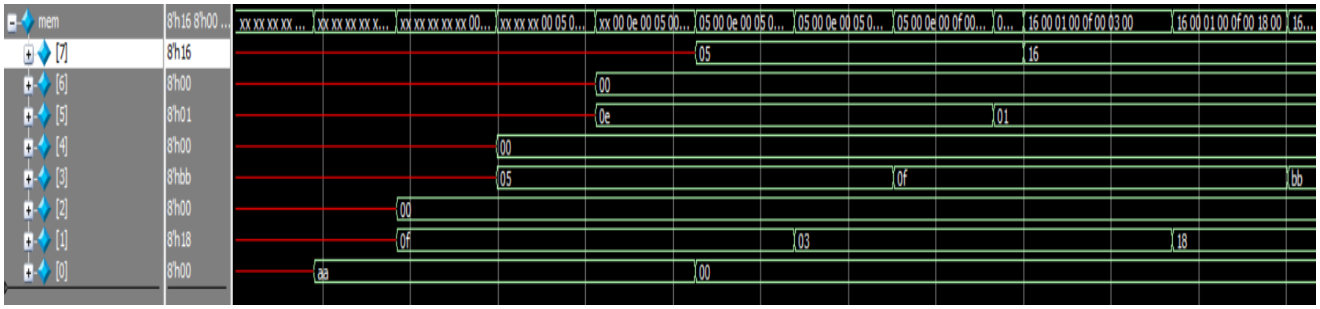

Figure 17: FIFO BUFFER

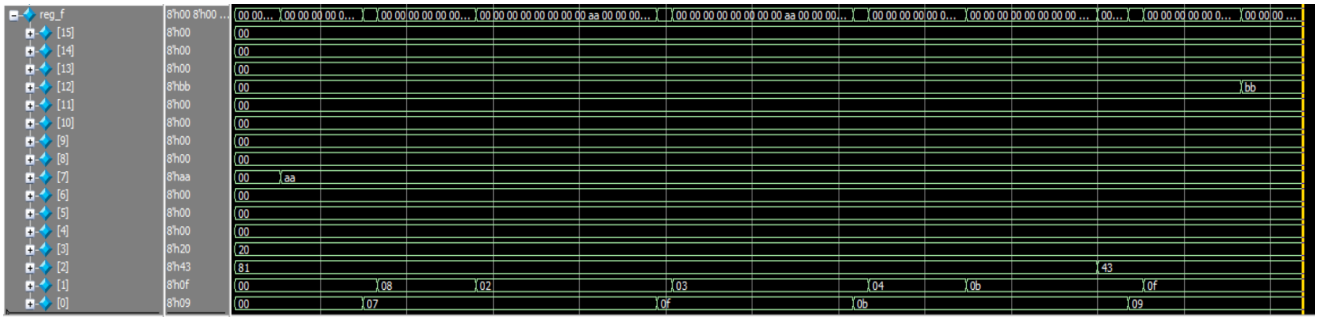

Figure 18: register file memory

TRANSCRIPT

```
VSIM 14> run -all
# reset assertion :)
# the design is reseted :)
# ////////////////////case_ 1 ////////////////////
# case 1 :read_operaton_succeded :)
# ////////////////////case_ 2 ////////////////////
# case 2 : read_ALU_succeded_FIRST_FRAME :)
# case 2 :read_ALU_succeded_SECOND_FRAME :)
# case 2 :read_alu total value:)
# ////////////////////case_ 3 ////////////////////
# case 3 : read_ALU_succeded_FIRST_FRAME :)
# case 3 :read_ALU_succeded_SECOND_FRAME :)
# case 3 :read_alu total value:)
# ////////////////////case_ 4 ////////////////////
# case 4 : read_ALU_succeded_FIRST_FRAME :)
# case 4 :read_ALU_succeded_SECOND_FRAME :)
# case 4 :read_alu total value:)
# ////////////////////case_ 5 ////////////////////
# case 5 : read_ALU_succeded_FIRST_FRAME :)
# case 5 :read_ALU_succeded_SECOND_FRAME :)
# case 5 :read_alu total value:)
# ////////////////////case_ 6 ////////////////////
# case 6 : read_ALU_succeded_FIRST_FRAME :)
# case 6 :read_ALU_succeded_SECOND_FRAME :)
# case 6 :read_alu total value:)
# ////////////////////case_ 7 ////////////////////
# case 7 : read_ALU_succeded_FIRST_FRAME :)
# case 7 :read_ALU_succeded_SECOND_FRAME :)
# case 7 :read_alu total value:)
# ////////////////////case_ 8 ////////////////////
# case 8 : read_ALU_succeded_FIRST_FRAME :)
# case 8 :read_ALU_succeded_SECOND_FRAME :)
# case 8 :read_alu total value:)
#  ////////////////////CHANGING UART CONFIGERATIONS//////////////////////////////
#  PRESCALE = 16 PAR_TYPE=1 PAR_EN = 1
# ////////////////////case_ 9 ////////////////////
# case 9 : read_ALU_succeded_FIRST_FRAME :)
# case 9 :read_ALU_succeded_SECOND_FRAME :)
# case 9 :read_alu total value:)
# ////////////////////case_ 10 ////////////////////
# case 10 :read_operaton_succeded :)
# testbench is ended
# number of wrong cases is 0
# number of correct cases is 10
# ** Note: $stop    : TB.v(194)
#    Time: 6200 us  Iteration: 1  Instance: /FINAL_sys_tb
# Break in Module FINAL_sys_tb at TB.v line 194
```