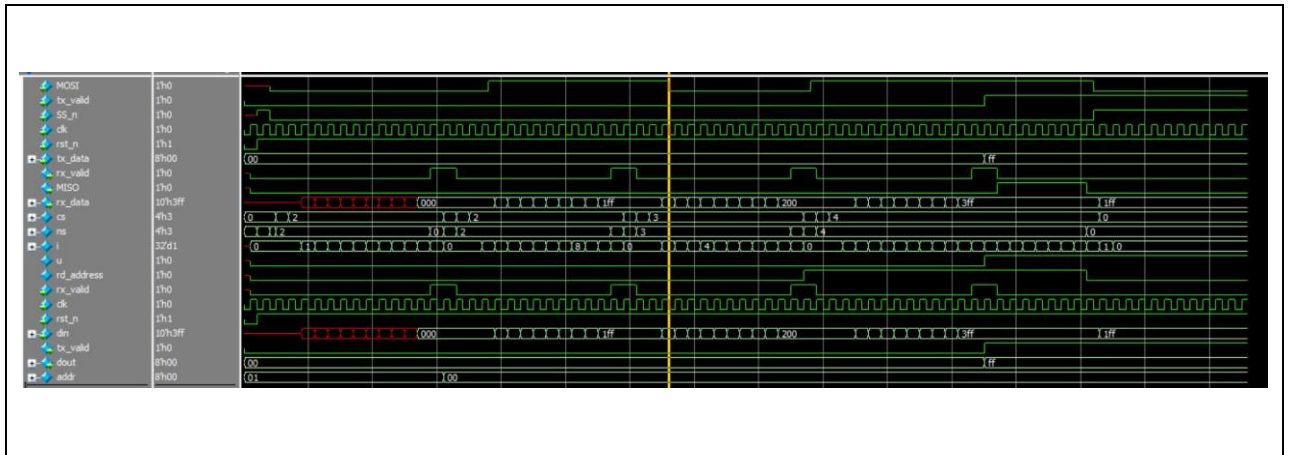
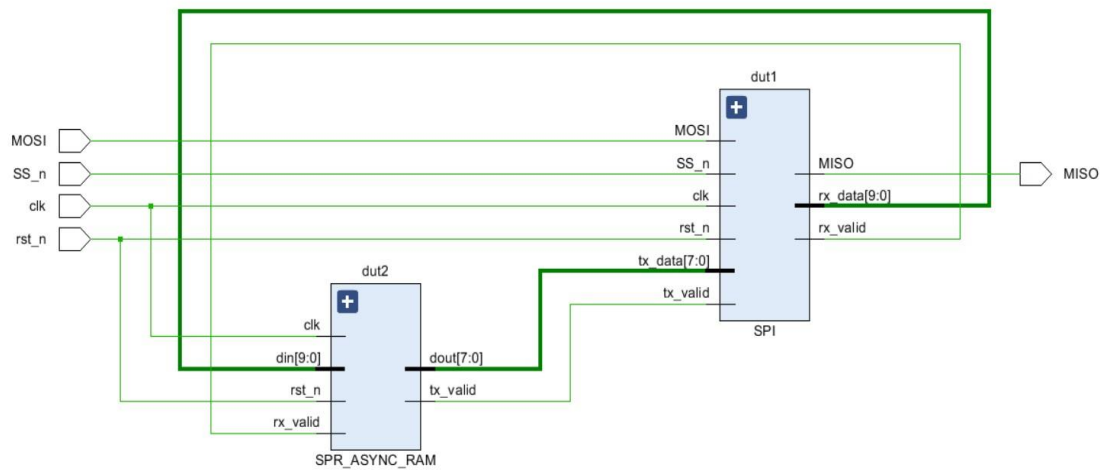


- *Questasim snippets*

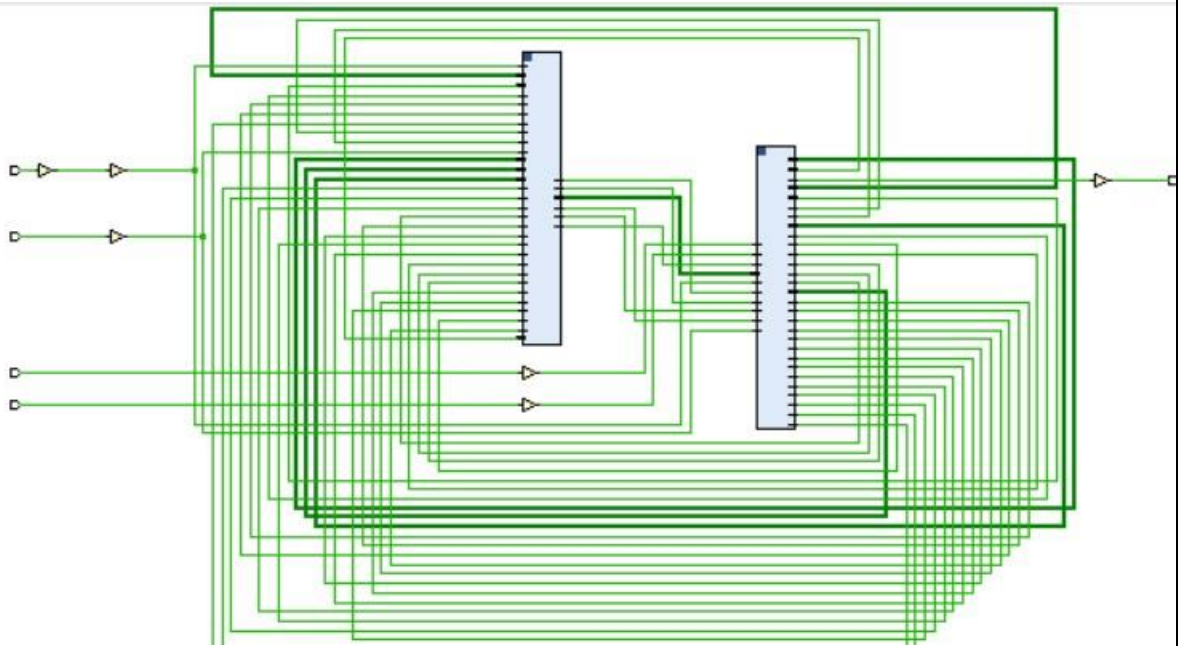


- *Gray encoding*



*Elaboration:*

## Synthesis:



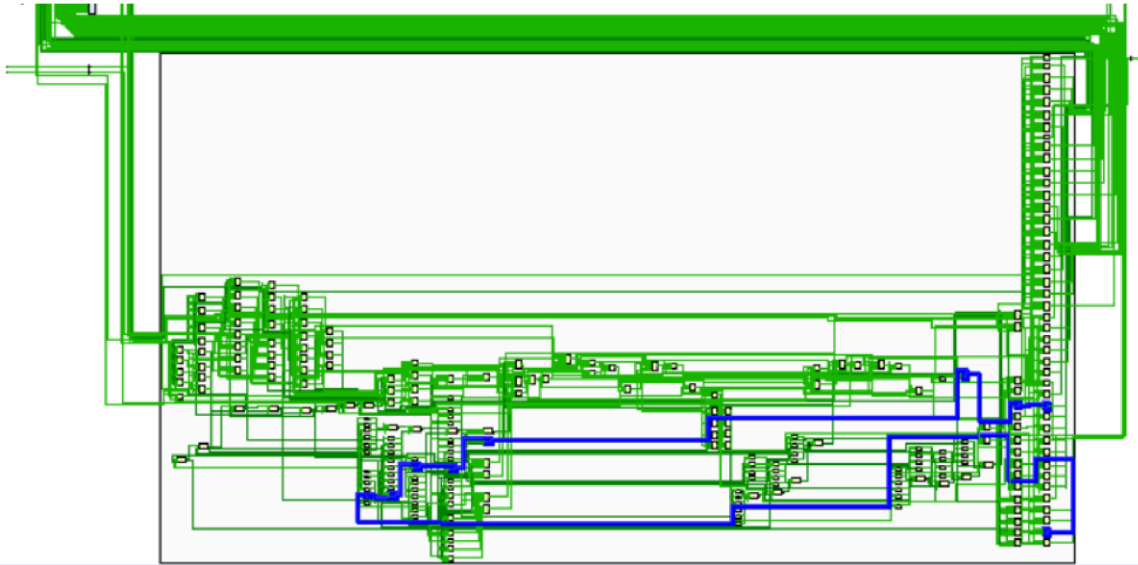
## The encoding

```
co
Parameter READ_DATA bound to: 4 - type: integer
INFO: [Synth 8-5534] Detected attribute (' fsm_encoding = "gray" ') [C:/Users/TECH SHOP/Desktop/TEST YA MEKKY.v:12]
INFO: [Synth 8-155] case statement is not full and has no default [C:/Users/TECH SHOP/Desktop/TEST YA MEKKY.v:28]
WARNING: [Synth 8-567] referenced signal 'MOSI' should be on the sensitivity list [C:/Users/TECH SHOP/Desktop/TEST YA MEKKY.v:1]
INFO: [Synth 8-6155] done synthesizing module 'SPI' (1#1) [C:/Users/TECH SHOP/Desktop/TEST YA MEKKY.v:1]
INFO: [Synth 8-6157] synthesizing module 'SPR_ASYNC_RAM' [C:/Users/TECH SHOP/Desktop/ram for SPI project.v:1]
Parameter MEM_DEPTH bound to: 256 - type: integer
```

## timing report

Design Timing Summary			
Clock Summary (1)			
Check Timing (16)			
Intra-Clock Paths			
sys_clk_pin			
Setup 5.229 ns (10)			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 5.229 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 4252	Total Number of Endpoints: 4252	Total Number of Endpoints: 2124	

## The critical path:



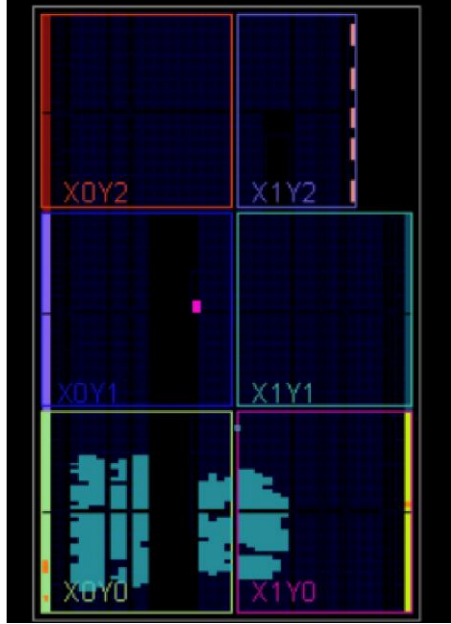
## Utilization report:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
▼ SPI_WRAPPER	1001	2126	268	134	797	1001	48	5	1
└ dut1 (SPI)	157	58	0	0	71	157	39	0	0
└ dut2 (SPR_ASYNC_RA...	844	2068	268	134	746	844	8	0	0

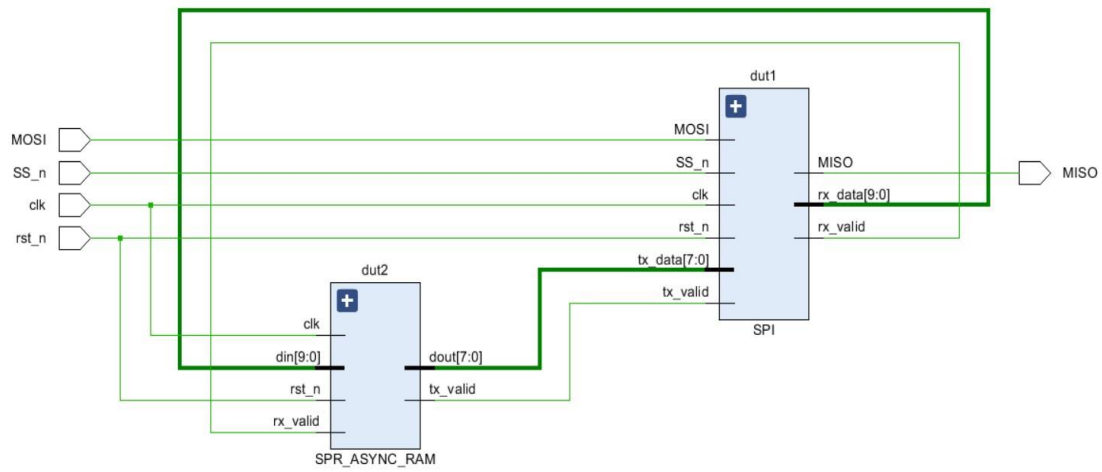
## Timing report (after implementation):

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.024 ns	Worst Hold Slack (WHS): 0.058 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4252	Total Number of Endpoints: 4252	Total Number of Endpoints: 2124
All user specified timing constraints are met.		

Device:

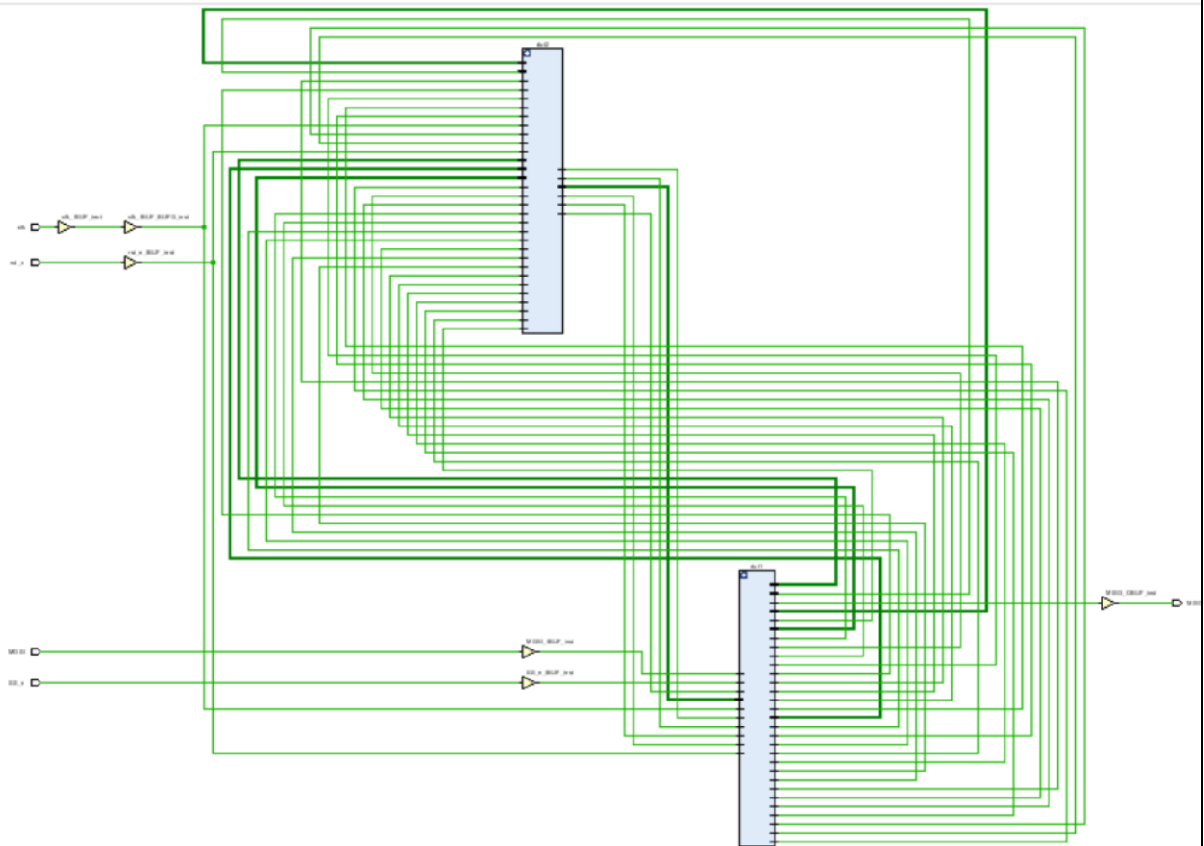


- *One-hot encoding*



*Elaboration:*

## Synthesis:



## The encoding

```
Parameter READ_ADD bound to: 3 - type: integer
Parameter READ_DATA bound to: 4 - type: integer
INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [C:/Users/TECH SHOP/Desktop/TEST YA MEKKY
INFO: [Synth 8-155] case statement is not full and has no default [C:/Users/TECH SHOP/Desktop/TEST YA MEKKY.v:28
WARNING: [Synth 8-567] referenced signal 'MOSI' should be on the sensitivity list [C:/Users/TECH SHOP/Desktop/TE
INFO: [Synth 8-6155] done synthesizing module 'SPI' (1#1) [C:/Users/TECH SHOP/Desktop/TEST YA MEKKY.v:1]
INFO: [Synth 8-6157] synthesizing module 'SPR_ASYNC_RAM' [C:/Users/TECH SHOP/Desktop/ram for SPI project.v:1]
```

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (34)

Intra-Clock Paths

sys\_clk\_pin

Setup 5.246 ns (10)

Setup

Worst Negative Slack (WNS): 5.246 ns

Total Negative Slack (TNS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 4250

Hold

Worst Hold Slack (WHS): 0.142 ns

Total Hold Slack (THS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 4250

Pulse Width

Worst Pulse Width Slack (WPWS): 4.500 ns

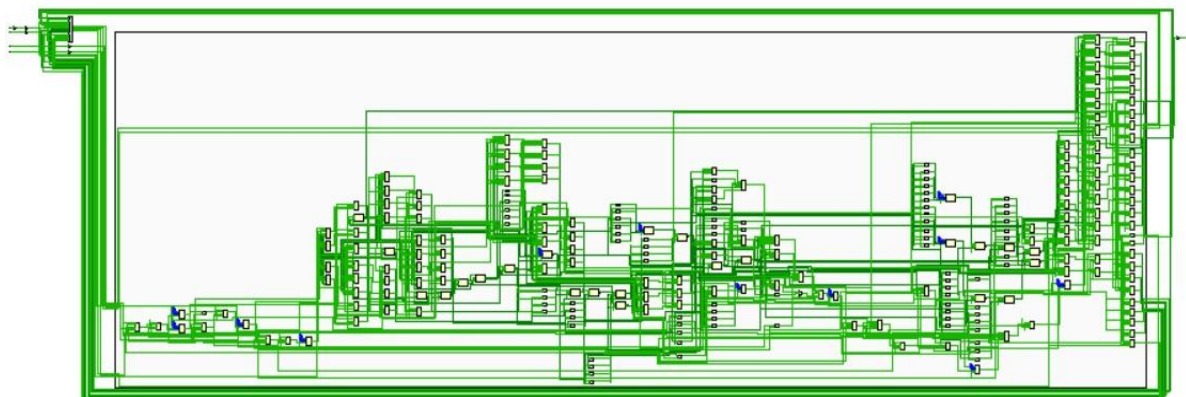
Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 2125

All user specified timing constraints are met.

timing report



The critical path:



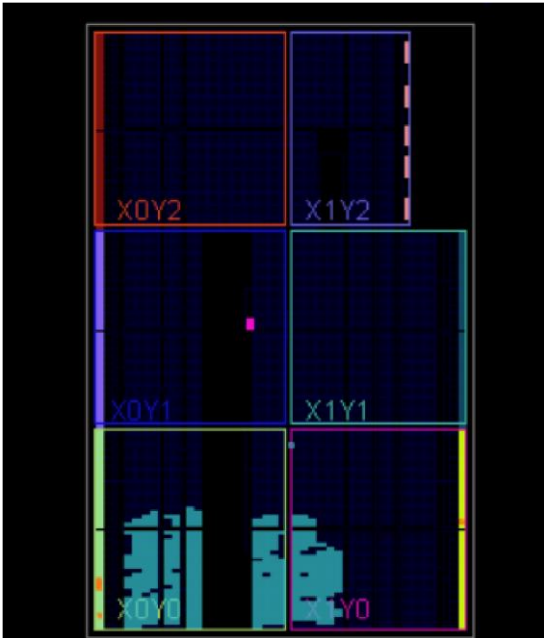
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_WRAPPER	994	2129	273	136	798	994	45	5	1
└ dut1 (SPI)	150	62	1	0	57	150	37	0	0
└ dut2 (SPR_ASYNC_RA...	844	2067	272	136	747	844	8	0	0

Utilization report:

Timing report (after implementation):

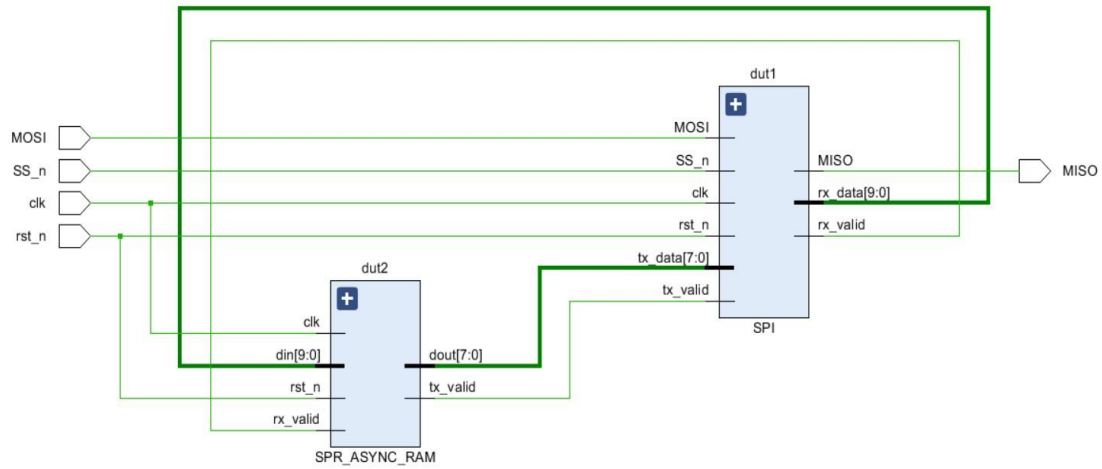
General Information	Setup	Hold	Pulse Width
Timer Settings			
Design Timing Summary	Worst Negative Slack (WNS): 0.415 ns	Worst Hold Slack (WHS): 0.189 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Clock Summary (1)	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Check Timing (34)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Intra-Clock Paths	Total Number of Endpoints: 4250	Total Number of Endpoints: 4250	Total Number of Endpoints: 2125
Inter-Clock Paths	All user specified timing constraints are met.		

Device:



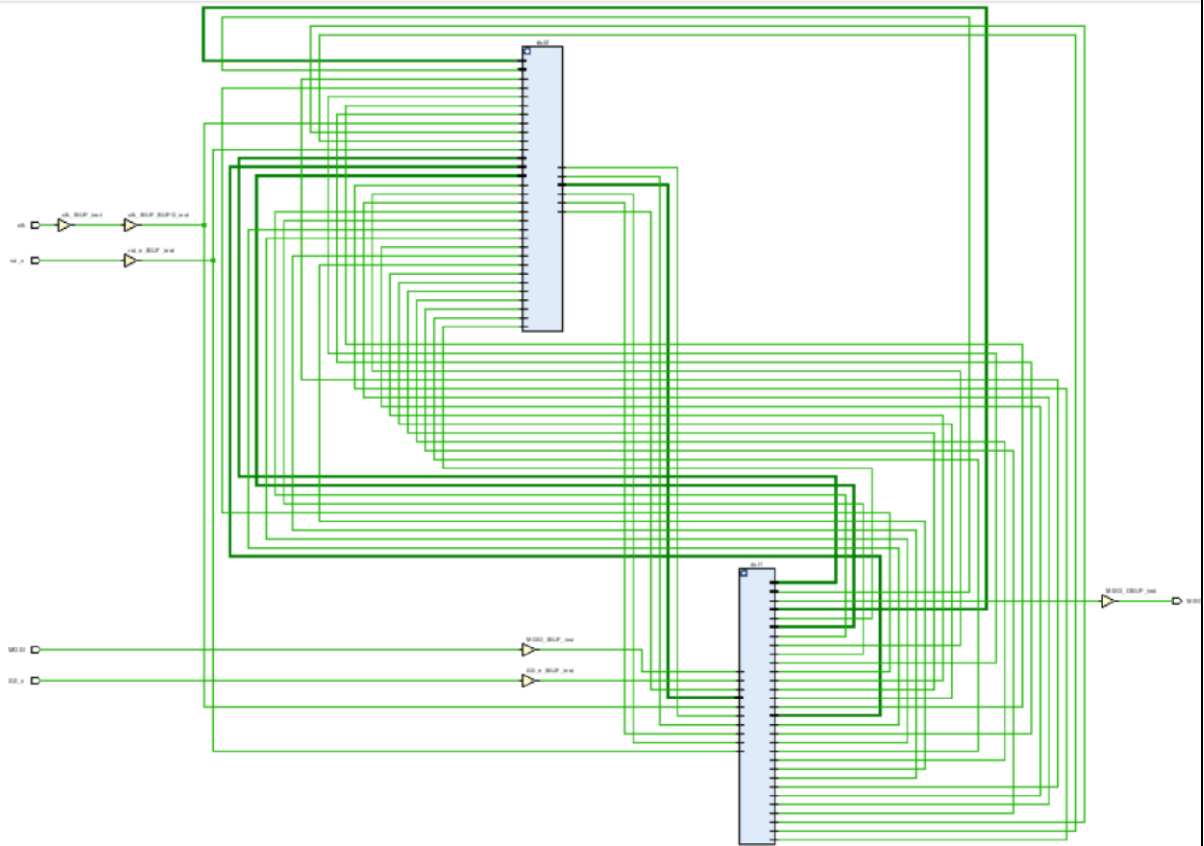


- binary



*Elaboration:*

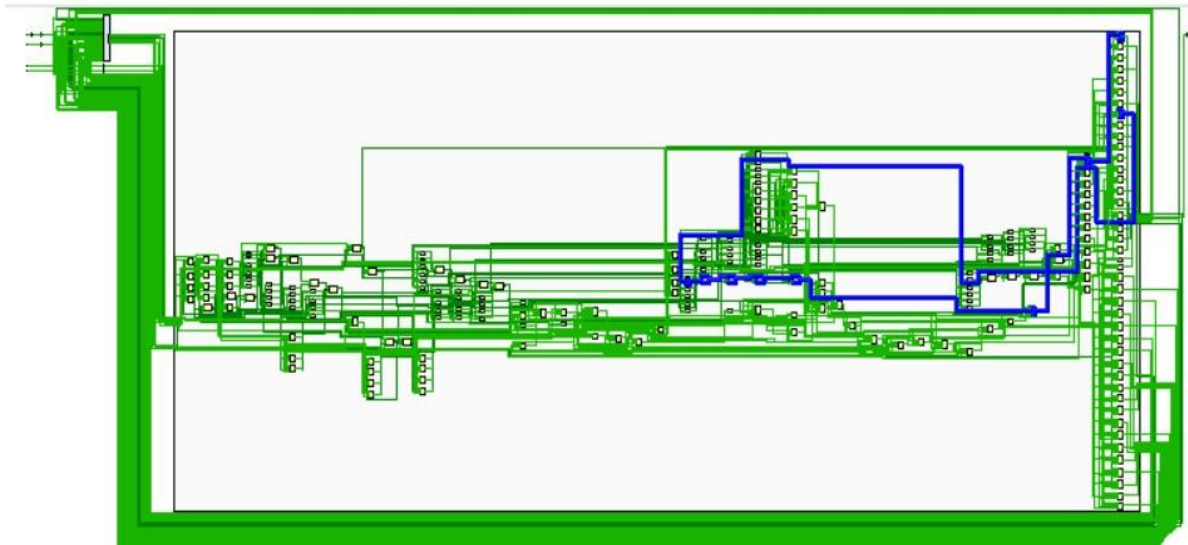
## Synthesis:



## The encoding

## timing report

## The critical path:



## Utilization report:

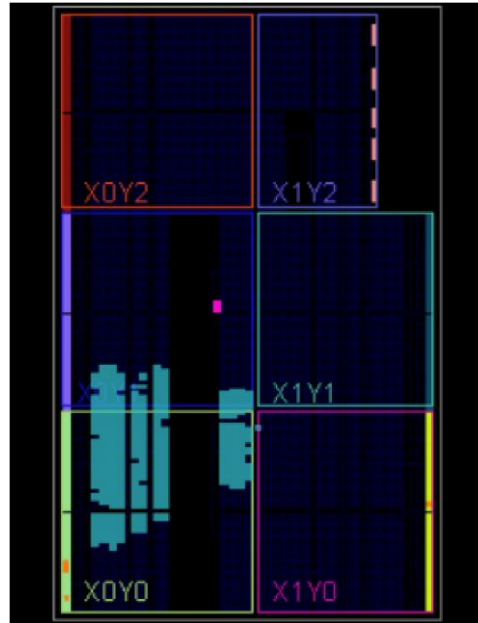
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_WRAPPER	971	2124	268	134	756	971	14	5	1
❏ dut1 (SPI)	128	58	0	0	53	128	5	0	0
❏ dut2 (SPR_ASYNC_RA...	843	2066	268	134	720	843	8	0	0

## Timing report (after implementation):

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.042 ns	Worst Hold Slack (WHS): 0.170 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4248	Total Number of Endpoints: 4248	Total Number of Endpoints: 2122

All user specified timing constraints are met.

Device:



- *MASSEGES:*

▼ Synthesis (6 warnings)

- [Synth 8-567] referenced signal 'MOSI' should be on the sensitivity list [TEST\_YA\_MEKKY.v:26]
- [Synth 8-5788] Register mem\_reg in module SPR\_ASYNC\_RAM is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code
- [Synth 8-4767] Trying to implement RAM 'mem\_reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
- [Synth 8-327] inferring latch for variable 'FSM\_gray\_ns\_reg' [TEST\_YA\_MEKKY.v:31]
- [Netlist 29-101] Netlist 'SPI\_WRAPPER' is not ideal for floorplanning, since the cellview 'SPR\_ASYNC\_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to floorplanning.
- [Constraints 18-5210] No constraint will be written out.

▼ Implementation (1 warning)

▼ Design Initialization (1 warning)

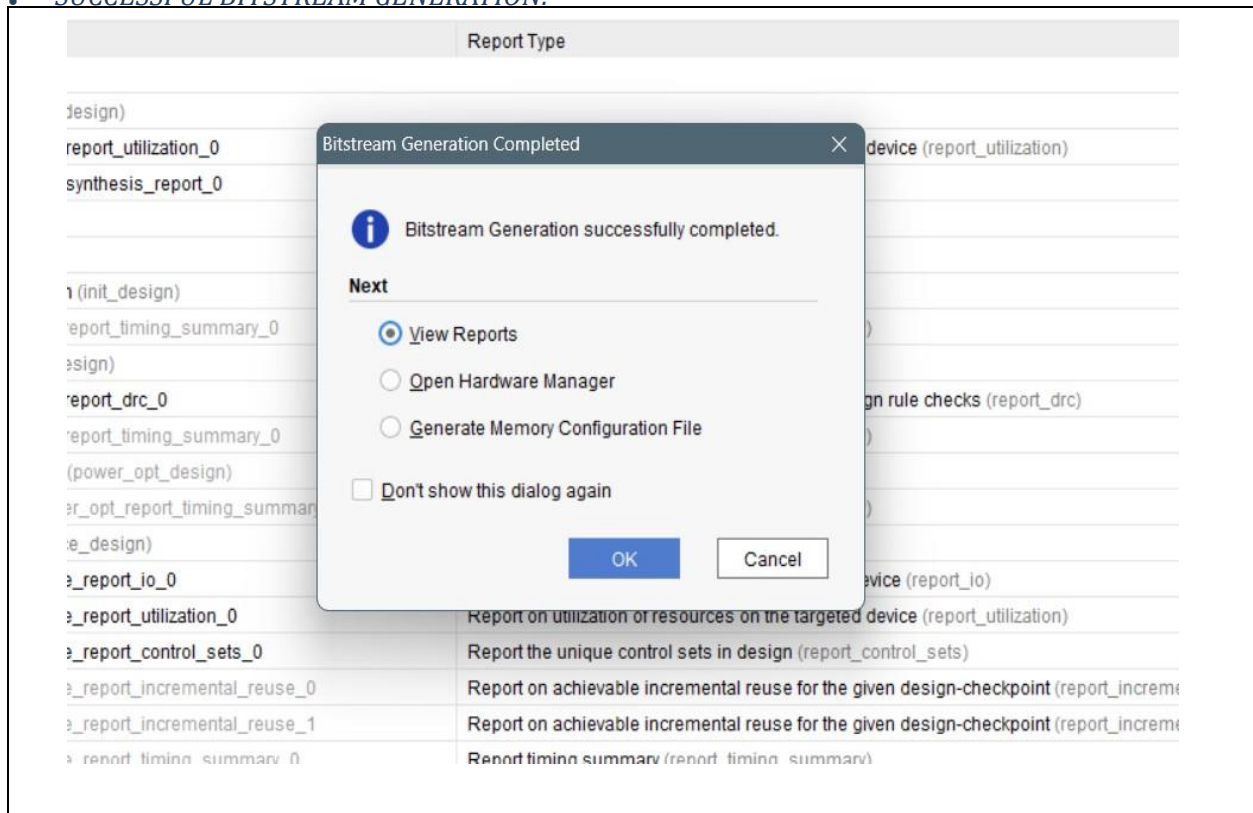
- [Netlist 29-101] Netlist 'SPI\_WRAPPER' is not ideal for floorplanning, since the cellview 'SPR\_ASYNC\_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to floorplanning.

▼ Implemented Design (1 warning)

▼ General Messages (1 warning)

- [Netlist 29-101] Netlist 'SPI\_WRAPPER' is not ideal for floorplanning, since the cellview 'SPR\_ASYNC\_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to floorplanning.

• *SUCCESSFUL BITSTREAM GENERATION:*





- *Setup and debugfor (one-hot) encoding (the best in timing report):*

