Final Project

Project (2)-RAM:

1. Verification plan

a) Asynchronous Reset functionality.

b) Testing writing operation in All Addresses of the memory by checking the waveform and compare to the golden model

c) Testing reading operation From All Addresses of the memory by checking dout in the waveform and compare to the golden model

d) Testing if rx_valid is low No operation is done the dout and the memory stayed stable or not.

e) Checking when Read the Functionality of tx_valid and if it still high or when read only.

Note:

-Reset randomization is closed during the first two loops to check all places in the memory and make sure every address in the memory wrote and read from it.

-addr_wr is not assigned a reset value which may cause a problem if the master started with the writing data operation.

2. Verification Document

Label	Description	Stimulus Generation	Functional Coverage	Functionality Check
RAM_1	Incase of rst_n high All memory places and dout should take 0	Randomization under constraints that rst_n is high almost all the time	no funcional coverage for this point	Output Checked against golden model
RAM_2	incase rx_valid low no writing or reading operation takes place in memory	Randomization under constraints that rx_valid is high almost all the time	no funcional coverage for this point	Output Checked against golden model
RAM_3	check the funcionality of din and if the ram reads write store the addresses right or now	No Randomization for din	Function coverage to check all values of din	Output Checked against golden model
RAM_4	Check the funcitonality of dout and that it stay the same during writing or rx_valid low.	No Randomization for dout	no funcional coverage for this point	Output Checked against golden model

3. Coverage reports:

Toggle Coverage is 100%

```
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         44        44         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /RAM_top/RAMif --

                                          Node      1H->0L      0L->1H  "Coverage"
                                          ----------------------------------------
                                           clk           1           1      100.00
                                       din[9-0]          1           1      100.00
                                      dout[7-0]          1           1      100.00
                                         rst_n           1           1      100.00
                                      rx_valid           1           1      100.00
                                      tx_valid           1           1      100.00

Total Node Count     =         22
Toggled Node Count   =         22
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (44 of 44 bins)
```

Branch Coverage is 87.5% as All values were handled no wrong branch in the design.

```
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         7         7         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\spi_ram_tb#dut

    Line         Item                     Count     Source
    ----         ----                     -----     ------
  File ram.v
------------------------------------IF Branch------------------------------------
    14                                    20242     Count coming in to IF
    14              1                       337        if (~rst_n) begin

    26              1                     18423        else if (rx_valid) begin

                                           1482     All False Count
Branch totals: 3 hits of 3 branches = 100.00%
```

Statement Coverage is 100%

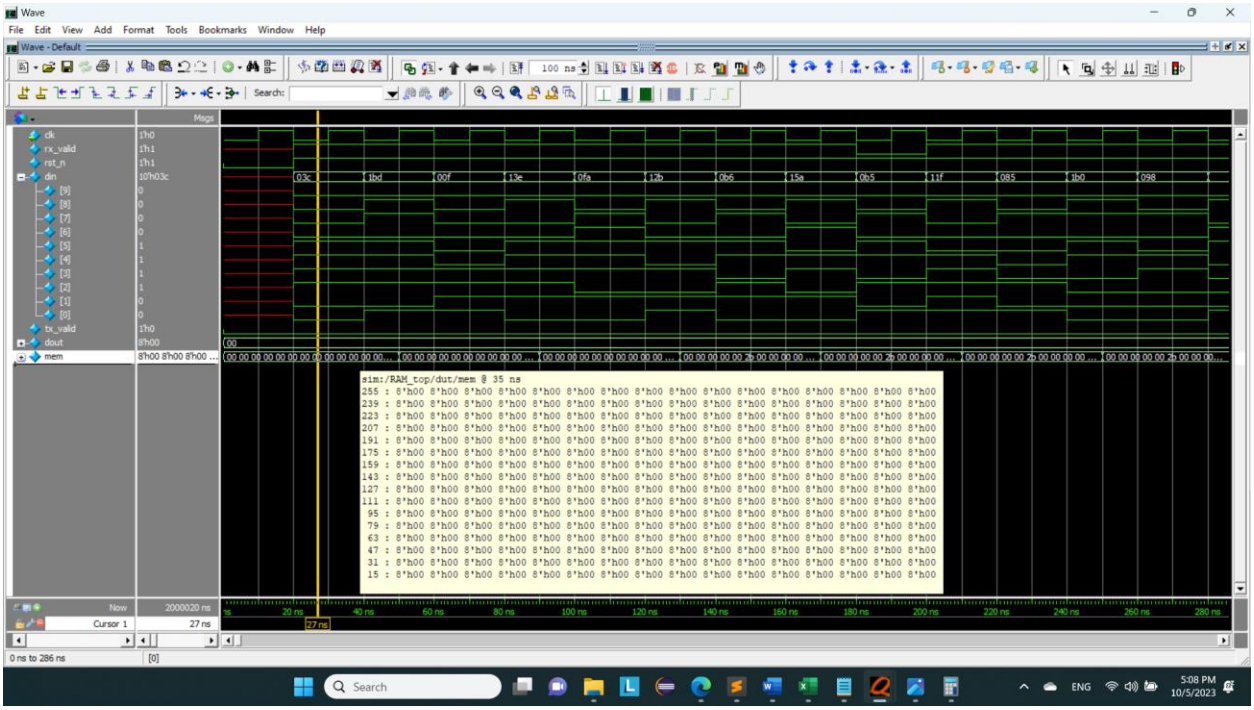
```
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      18        18         0   100.00%

================================Statement Details================================

Statement Coverage for instance /RAM_top/dut --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File ram.sv
    1                                                module project_ram(RAM_if.DESIGN ramif);
    2
    3                                                parameter MEM_DEPTH = 256;
    4                                                parameter ADDR_SIZE = 8;
    5
    6                                                logic rx_valid, clk, rst_n;
    7                                                logic [9:0] din;
    8                                                logic tx_valid;
    9                                                logic [7:0] dout;
    10
    11             1                          17803     assign rx_valid = ramif.rx_valid;
    12             1                         200003     assign clk = ramif.clk;
    13             1                           1141     assign rst_n = ramif.rst_n;
    14             1                         179658     assign din = ramif.din;
    15                                                   assign ramif.tx_valid= tx_valid;
    16                                                   assign ramif.dout = dout;
    17
    18                                                   reg [ADDR_SIZE-1:0] addr_rd, addr_wr;
    19                                                   reg [7:0] mem [MEM_DEPTH-1:0];
    20                                                   integer i = 0;
    21
    22             1                         100571     always @(posedge clk or negedge rst_n) begin
    23                                                      if (~rst_n) begin
    24             1                           1161                for (i = 0; i < MEM_DEPTH; i=i+1) begin
    24             2                         297216
    25             1                         297216                        mem [i] <= 1'b0;
    26             1                         297216                        dout <= 8'b0;
    27             1                         297216                        tx_valid <= 1'b0;
    28                                                               end
    29                                                      end
    30
    31                                                      else if (rx_valid) begin
    32                                                               if (din[9:8] == 2'b00) begin
    33             1                          22473                        addr_wr <= din[7:0];
    34             1                          22473                        tx_valid <= 0;
    35                                                               end
    36                                                               else if (din[9:8] == 2'b01) begin
    37             1                          22439                        mem [addr_wr] <= din[7:0];
    38             1                          22439                        tx_valid <= 0;
    39                                                               end
    40                                                               else if (din[9:8] == 2'b10) begin
    41             1                          22270                        addr_rd <= din[7:0];
    42             1                          22270                        tx_valid <= 0;
    43                                                               end
    44                                                               else if (din[9:8] == 2'b11) begin
    45             1                          22373                        dout <= mem[addr_rd];
    46             1                          22373                        tx_valid <= 1;
```

Function Coverage For din is 100% All values were reached

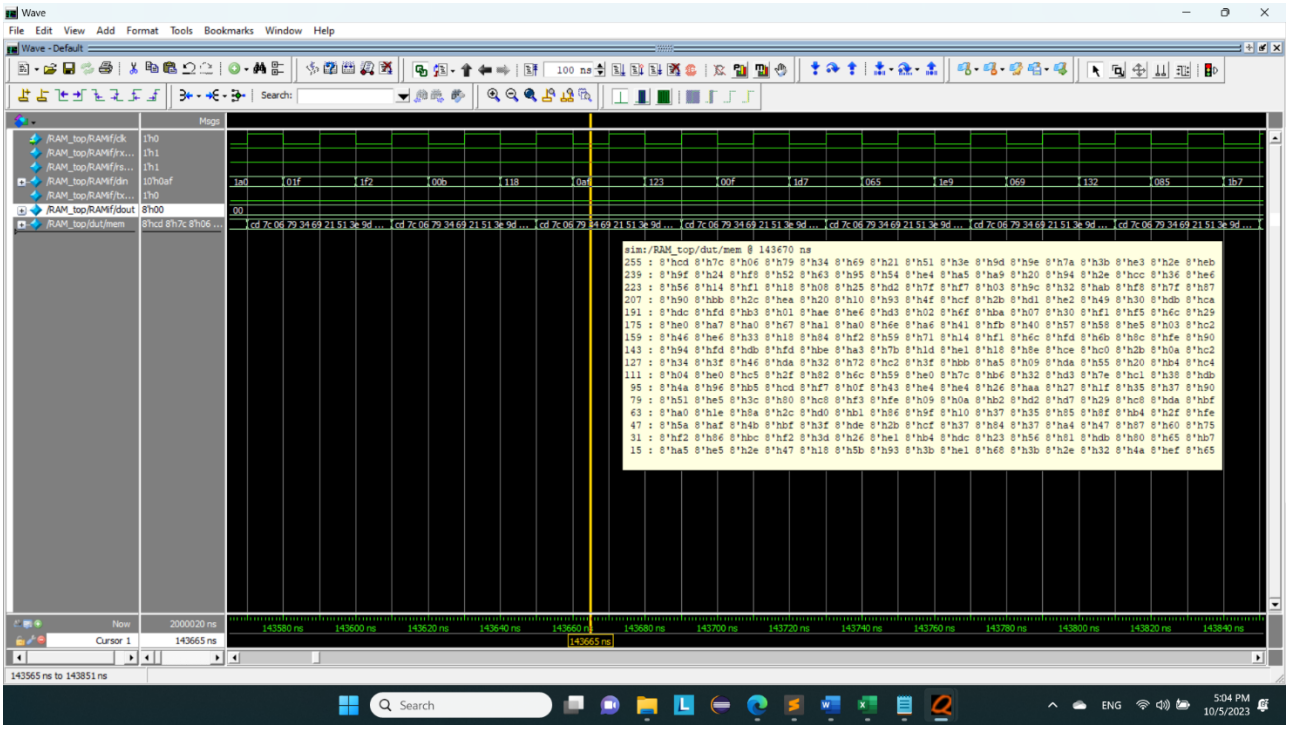
```
COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------------------
Covergroup                                                Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------------
 TYPE /RAM_package/RAM_transcation/CovCode               100.00%        100          -    Covered
    covered/total bins:                                       64         64          -
    missing/total bins:                                        0         64          -
    % Hit:                                                100.00%        100          -
    Coverpoint din_cp                                     100.00%        100          -    Covered
        covered/total bins:                                   64         64          -
        missing/total bins:                                    0         64          -
        % Hit:                                            100.00%        100          -
        bin auto[0:15]                                       1586          1          -    Covered
        bin auto[16:31]                                      1519          1          -    Covered
        bin auto[32:47]                                      1575          1          -    Covered
        bin auto[48:63]                                      1576          1          -    Covered
        bin auto[64:79]                                      1535          1          -    Covered
        bin auto[80:95]                                      1573          1          -    Covered
        bin auto[96:111]                                     1580          1          -    Covered
        bin auto[112:127]                                    1479          1          -    Covered
        bin auto[128:143]                                    1596          1          -    Covered
        bin auto[144:159]                                    1586          1          -    Covered
        bin auto[160:175]                                    1528          1          -    Covered
        bin auto[176:191]                                    1636          1          -    Covered
        bin auto[192:207]                                    1557          1          -    Covered
        bin auto[208:223]                                    1542          1          -    Covered
        bin auto[224:239]                                    1602          1          -    Covered
        bin auto[240:255]                                    1574          1          -    Covered
        bin auto[256:271]                                    1586          1          -    Covered
        bin auto[272:287]                                    1609          1          -    Covered
        bin auto[288:303]                                    1571          1          -    Covered
        bin auto[304:319]                                    1615          1          -    Covered
        bin auto[320:335]                                    1513          1          -    Covered
        bin auto[336:351]                                    1520          1          -    Covered
        bin auto[352:367]                                    1650          1          -    Covered
        bin auto[368:383]                                    1550          1          -    Covered
        bin auto[384:399]                                    1557          1          -    Covered
        bin auto[400:415]                                    1546          1          -    Covered
        bin auto[416:431]                                    1553          1          -    Covered
        bin auto[432:447]                                    1555          1          -    Covered
        bin auto[448:463]                                    1549          1          -    Covered
        bin auto[464:479]                                    1555          1          -    Covered
        bin auto[480:495]                                    1537          1          -    Covered
        bin auto[496:511]                                    1614          1          -    Covered
        bin auto[512:527]                                    1546          1          -    Covered
        bin auto[528:543]                                    1524          1          -    Covered
        bin auto[544:559]                                    1567          1          -    Covered
        bin auto[560:575]                                    1577          1          -    Covered
        bin auto[576:591]                                    1510          1          -    Covered
        bin auto[592:607]                                    1521          1          -    Covered
        bin auto[608:623]                                    1539          1          -    Covered
        bin auto[624:639]                                    1626          1          -    Covered
        bin auto[640:655]                                    1521          1          -    Covered
        bin auto[656:671]                                    1557          1          -    Covered
        bin auto[672:687]                                    1592          1          -    Covered
        bin auto[688:703]                                    1593          1          -    Covered
        bin auto[704:719]                                    1597          1          -    Covered
        bin auto[720:735]                                    1528          1          -    Covered
        bin auto[736:751]                                    1522          1          -    Covered
        bin auto[752:767]                                    1572          1          -    Covered
        bin auto[768:783]                                    1558          1          -    Covered
        bin auto[784:799]                                    1644          1          -    Covered
        bin auto[800:815]                                    1531          1          -    Covered
        bin auto[816:831]                                    1553          1          -    Covered
        bin auto[832:847]                                    1543          1          -    Covered
        bin auto[848:863]                                    1525          1          -    Covered
        bin auto[864:879]                                    1532          1          -    Covered
        bin auto[880:895]                                    1571          1          -    Covered
        bin auto[896:911]                                    1560          1          -    Covered
        bin auto[912:927]                                    1593          1          -    Covered
        bin auto[928:943]                                    1542          1          -    Covered
        bin auto[944:959]                                    1557          1          -    Covered
        bin auto[960:975]                                    1568          1          -    Covered
        bin auto[976:991]                                    1601          1          -    Covered
        bin auto[992:1007]                                   1487          1          -    Covered
        bin auto[1008:1023]                                  1619          1          -    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1
```

Some Questa Pic to Verify the RAM:

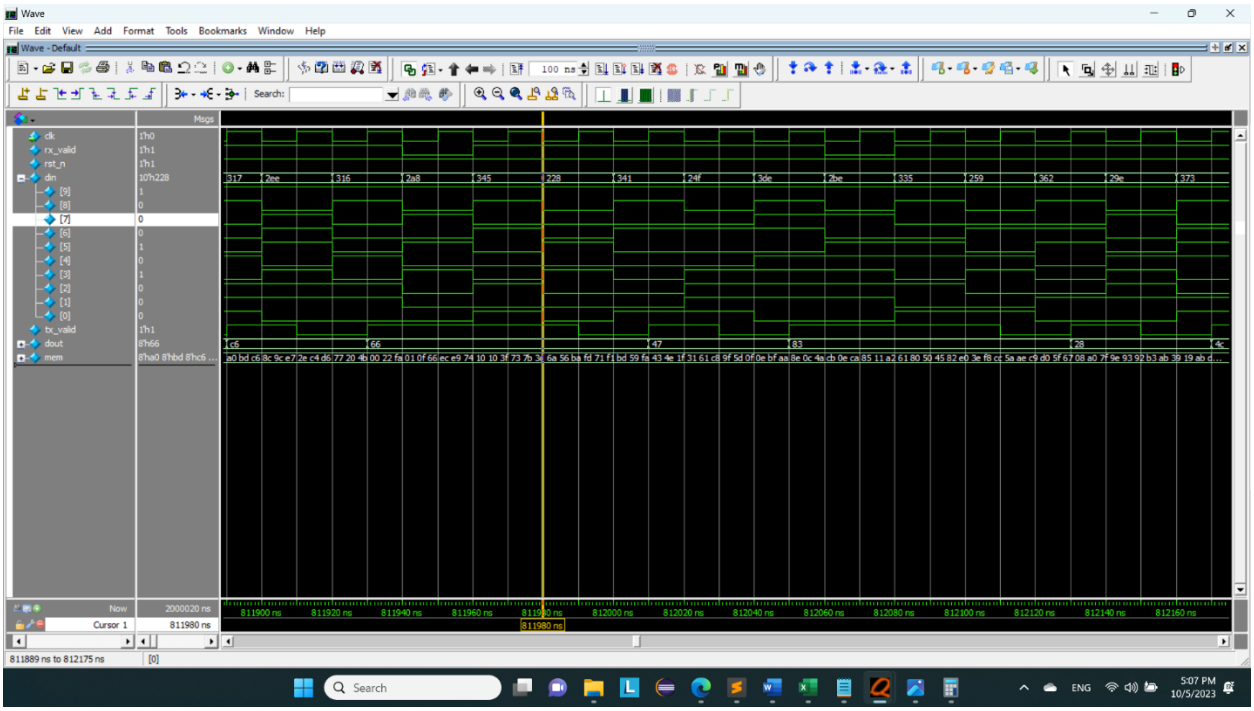
When rst_n =0 All ram values and dout = 0.



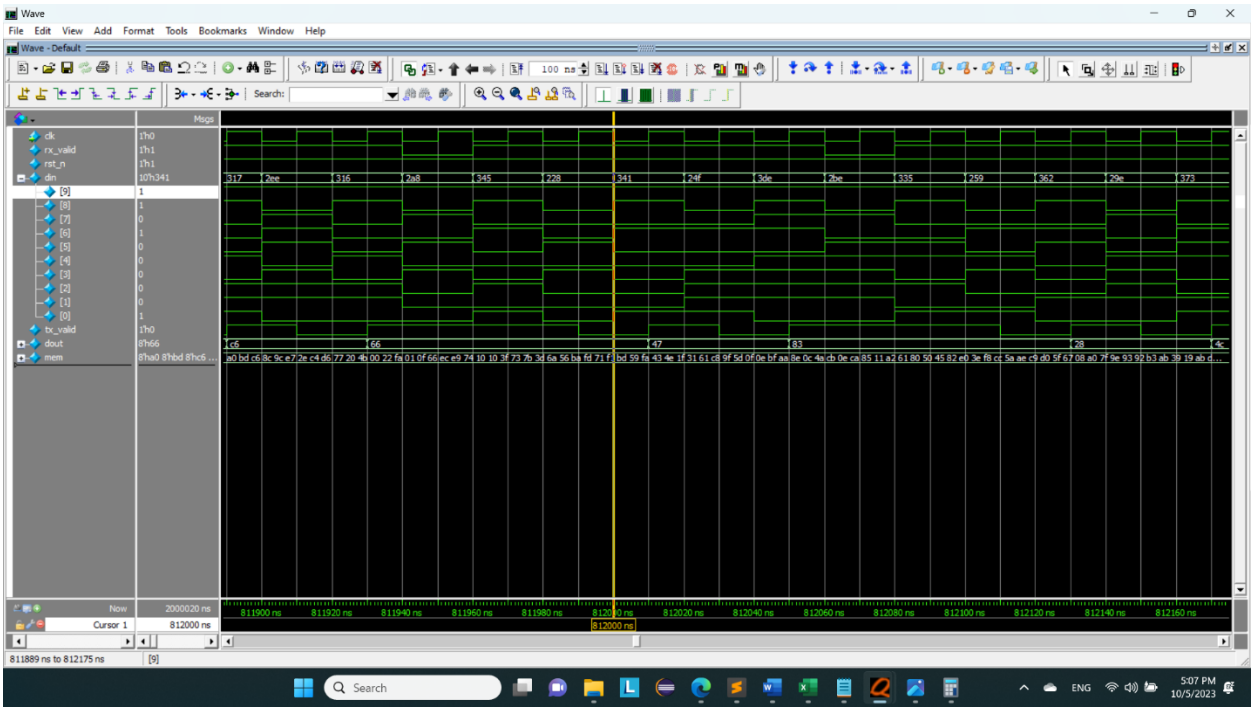
Writing in All Memory values.



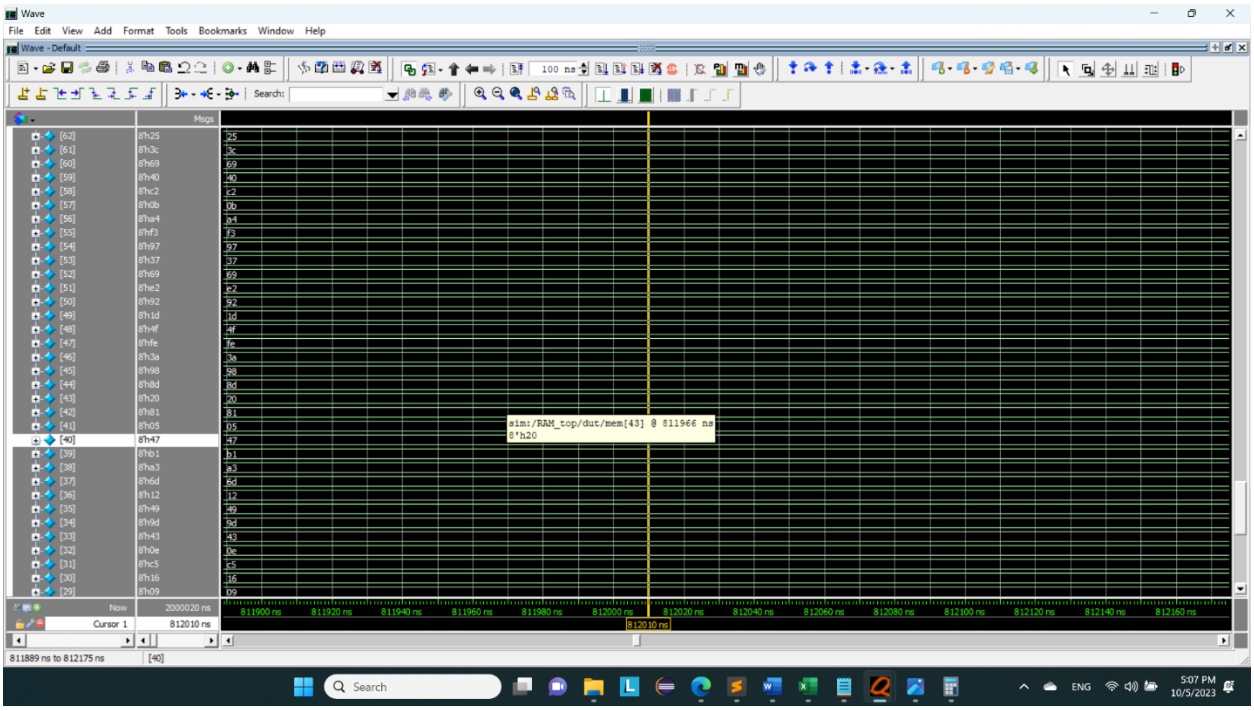
Example For checking Read:



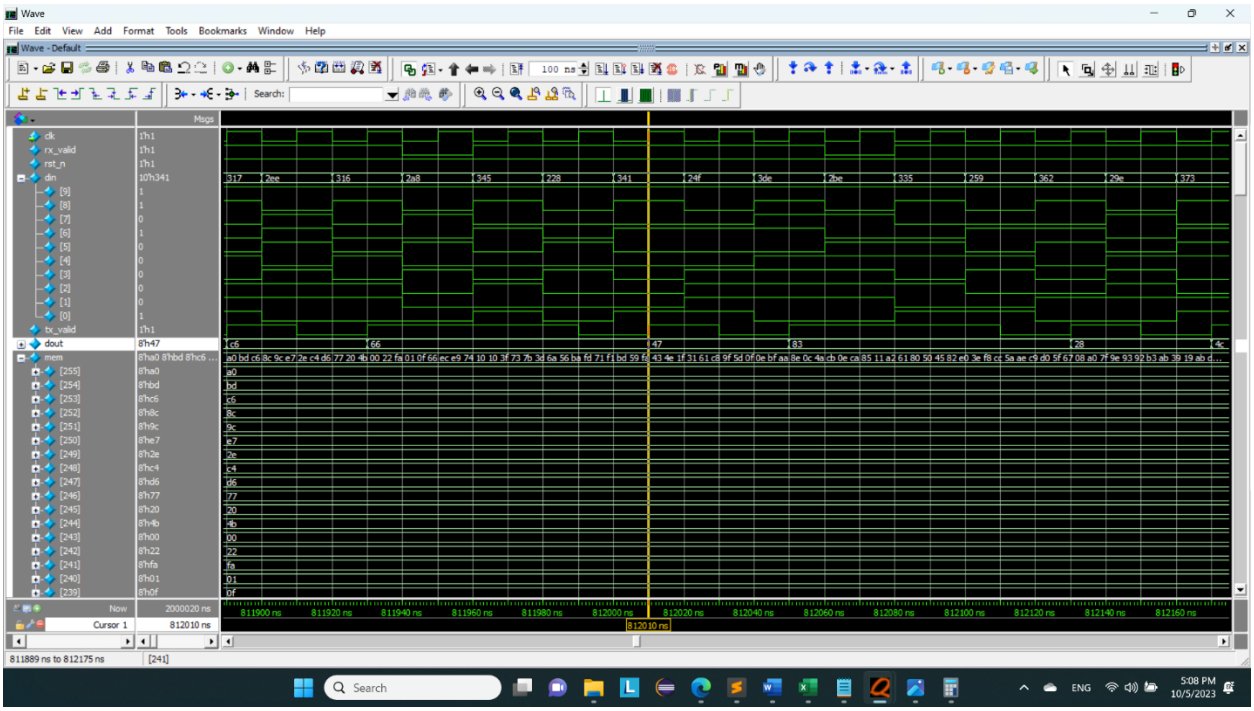
Din [9:8] is 10 so we will save 10100 in add_rd so we will check place 40 in memory.



After the Din[9:8] is 11 so it will go to address 40 to read and dout must = the value in memory [40].



In memory the address of 40 is = 8’h47 .



Dout is equal to the memory address 40 so read is true.

After examining the wave form and check all possible values for dout there is NO BUGS in the RAM memory.