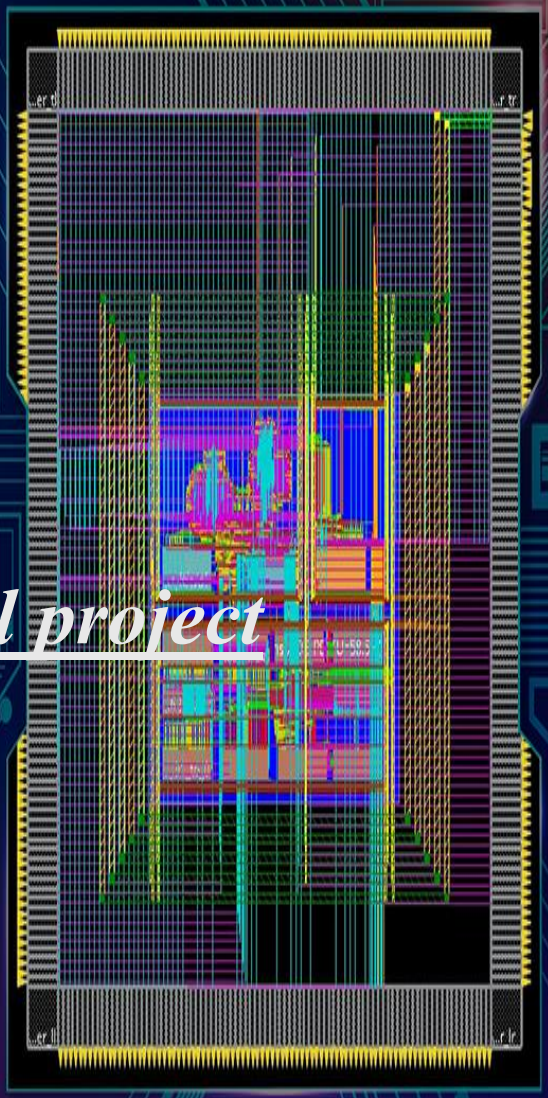


Internship final project

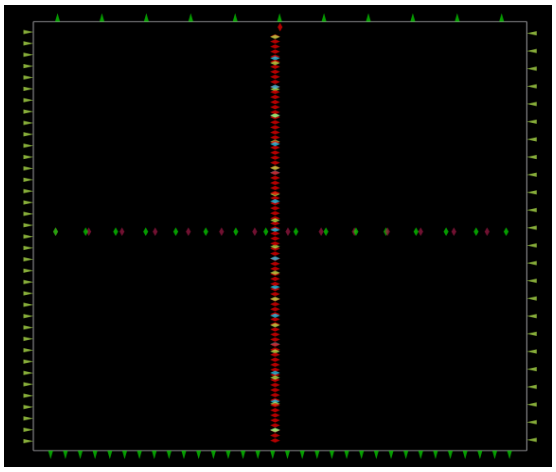
summited from:

Mustafa Magdy Ibrahim Mohamed

Power planning and floor planning

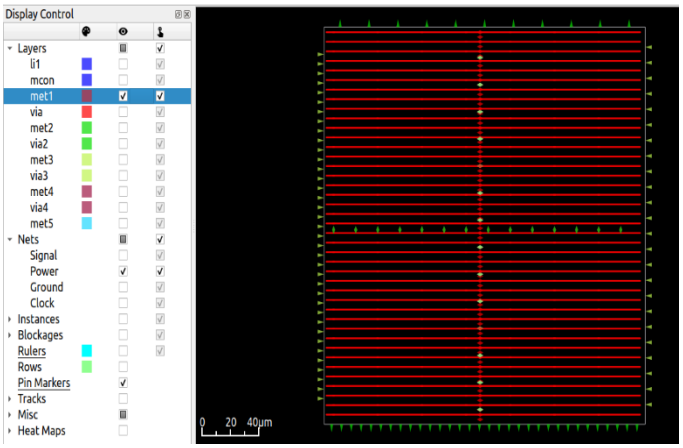
- ***floor planning***

using the pin configuration file to adjust the position of pins as required "all output pins at North and South" & all input pins at "West and East".

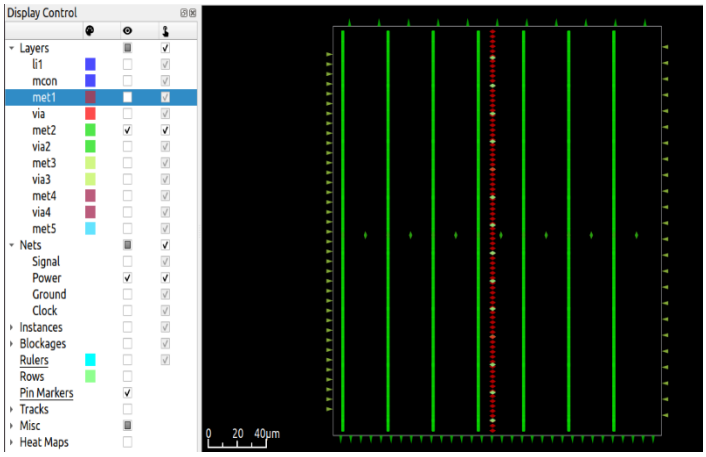


- ***PDN building:***

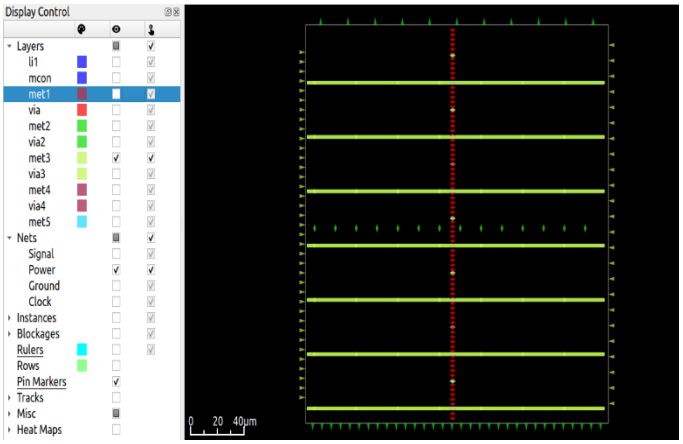
Metal 1:

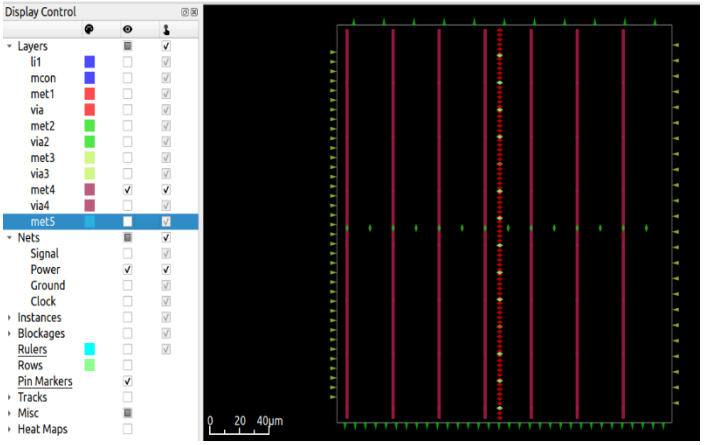


Metal 2:



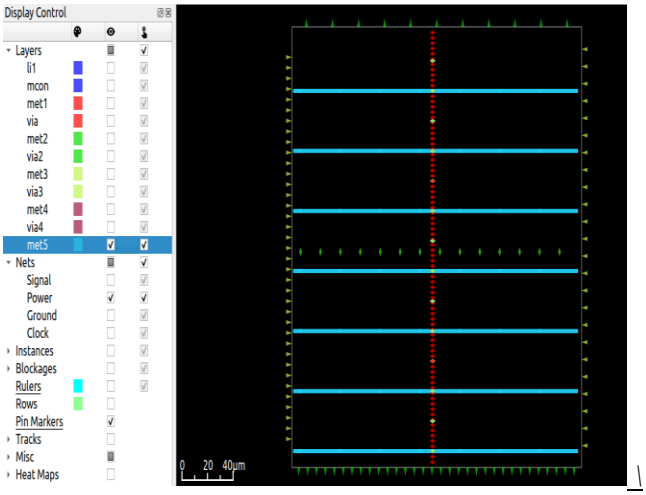
Metal 3:



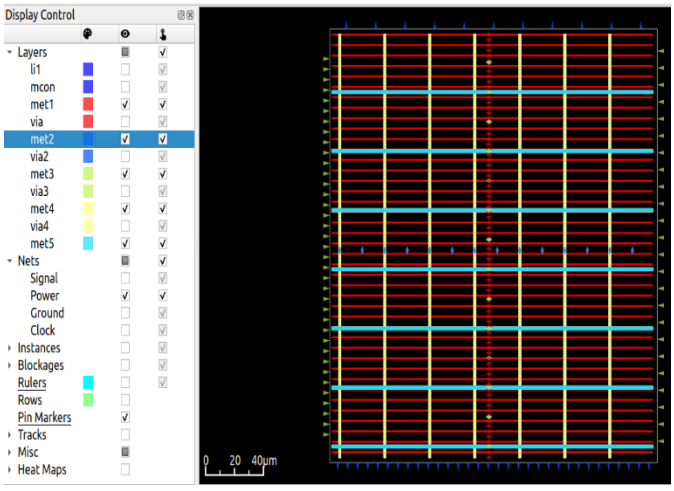


Metal 4:

Metal 5:



the whole PDN:

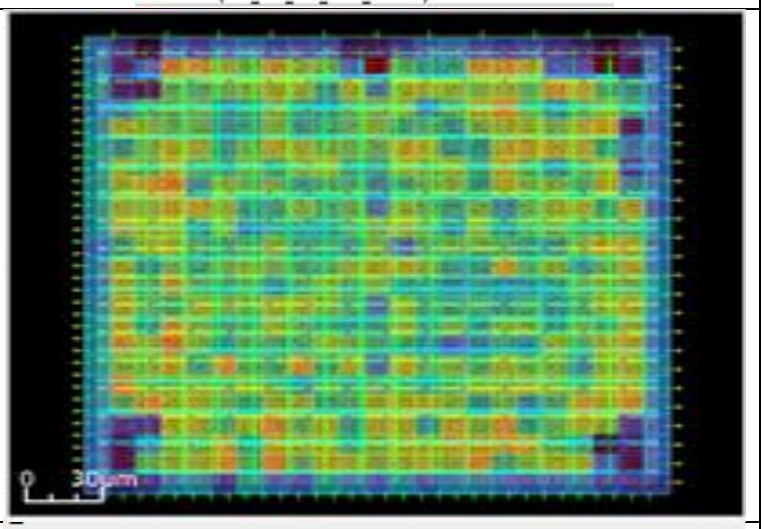


Comment: *as shown there are Stripes at metal layers "1,2,3,4 &5" to add the Vdd and Vss from the power rings to the core.*

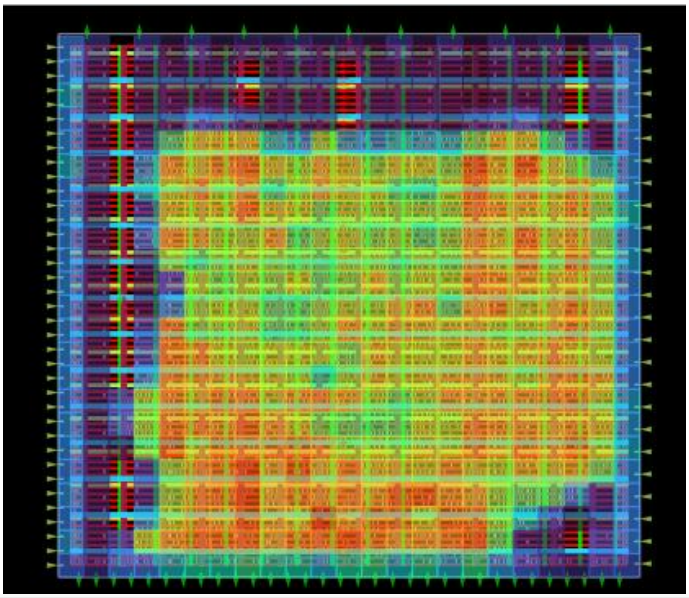
power rails in metal layer 1 to carry the Vss and Vdd from stipes to std cells exists in metal layer 1.

Placement and clock tree synthesis

Configuration 1:

Variables	``` #####################placement##################### set ::env(PL_TARGET_DENSITY) 0.47 set ::env(PL_ROUTABILITY_DRIVEN) 1 set ::env(PL_TIME_DRIVEN) 1 #####################################CTS######### set ::env(CLOCK_TREE_SYNTH) 1 set ::env(CTS_TARGET_SKEW) 2 set ::env(CTS_TOLERANCE) 50 set ::env(CTS_SINK_CLUSTERING_SIZE) 60 set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) 50 set ::env(CTS_REPORT_TIMING) 1 set ::env(CTS_CLK_MAX_WIRE_LENGTH) 0 ```
Congestion map	
Setup and hold worst Slack after CTS	``` 2 === 3 report_worst_slack -max (Setup) 4 === 5 worst slack 3.32 6 7 === 8 report_worst_slack -min (Hold) 9 === 0 worst slack 0.21 ```

Configuration 2:

Variables	``` ########################placement################################# set ::env(PL_TARGET_DENSITY) 0.8 set ::env(PL_ROUTABILITY_DRIVEN) 1 set ::env(PL_TIME_DRIVEN) 1 ##CTS######################### set ::env(CLOCK_TREE_SYNTH) 1 set ::env(CTS_TARGET_SKEW) 200 set ::env(CTS_TOLERANCE) 50 set ::env(CTS_SINK_CLUSTERING_SIZE) 80 set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) 90 set ::env(CTS_REPORT_TIMING) 1 set ::env(CTS_CLK_MAX_WIRE_LENGTH) 0 ```
Congestion map	
Setup and hold worst Slack after CTS	``` 1 2 === 3 report_worst_slack -max (Setup) 4 === 5 worst slack 3.15 6 7 === 8 report_worst_slack -min (Hold) 9 === 0 worst slack 0.20 ```

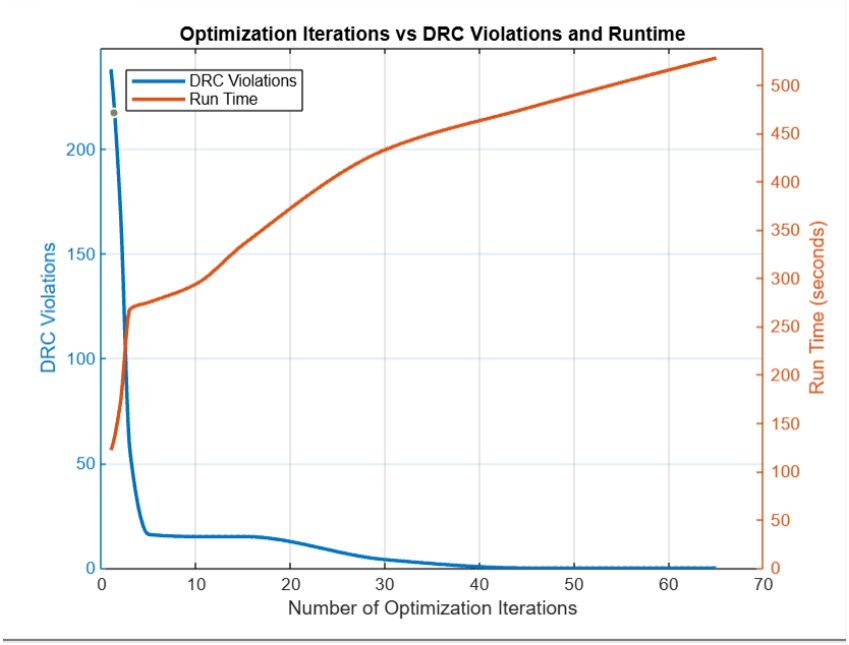
	Configuration 2	*Configuration 1*
congestion	*Higher*	*Lower*
Slacks	*worse*	*Better*

Tradeoff between reported DRCs and runtime

Number of opt iterations	*DRC violations*	*Run time*
1	*238*	*122 second*
2	*171*	*171 seconds*
3	*56*	*268 seconds*
5	*16*	*275 seconds*
10	*15*	*294 seconds*
15	*15*	*335 seconds*
30	*4*	*433 seconds*
45	*0*	*476 seconds*
65	*0*	*528 seconds*

Conclusion:

As we increase the number of iterations of optimization the number of violations decreases but also the run time increases too so it's a trade off as shown in MATLAB Figure.

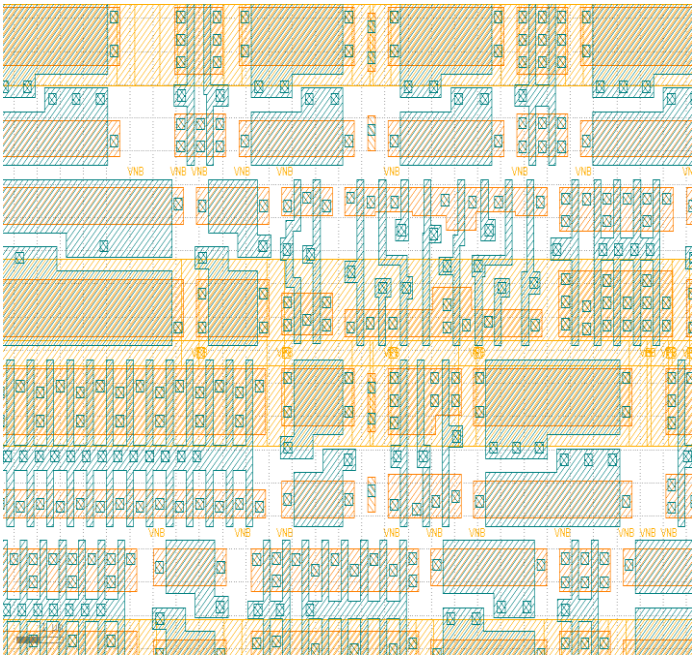


***Note that**: total number of violations depends also on congestion and placement we have done in previous steps in flow but the decaying of violations number across number of iterations is **almost** always follows the same behavior.*

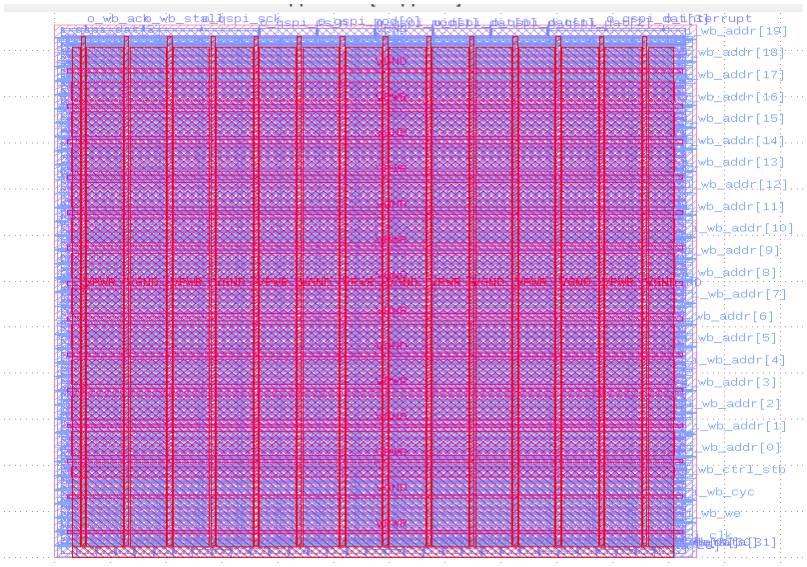
GDS and LEF views of the design

a) *GDS view:*

The view has all the information which exists in LEF file and information about transistors and diffusions and detailed geometric information, including polygons and paths for each layer of the IC as shown in figures below.

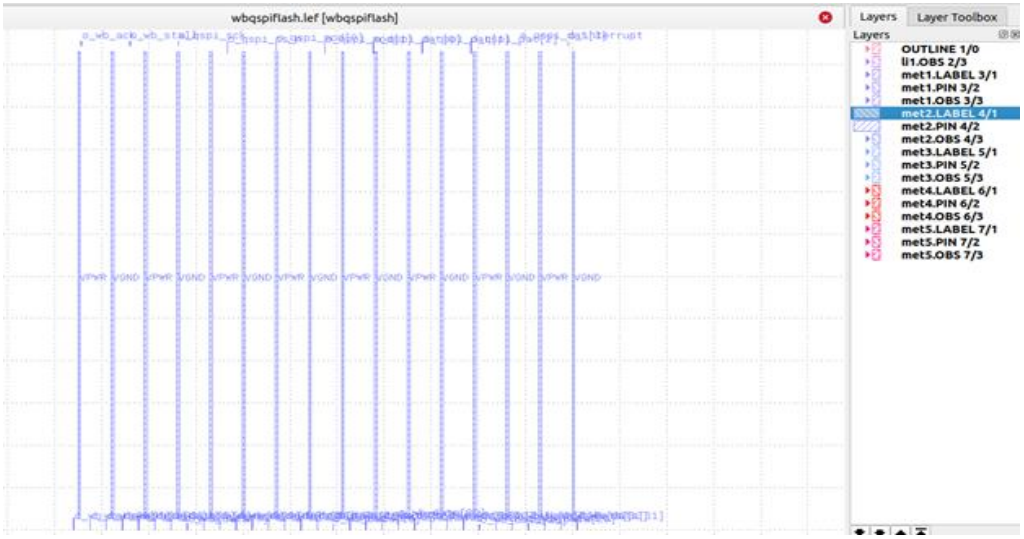


b) *LEF view:* *this view Includes physical dimensions, pin locations, metal layer usage, and routing blockages, without detailed geometry.*



validation of the metals used for pins creation.

as shown in figures below from. LEF view the output pins are on metal 2 and the input pins are on metal 3.

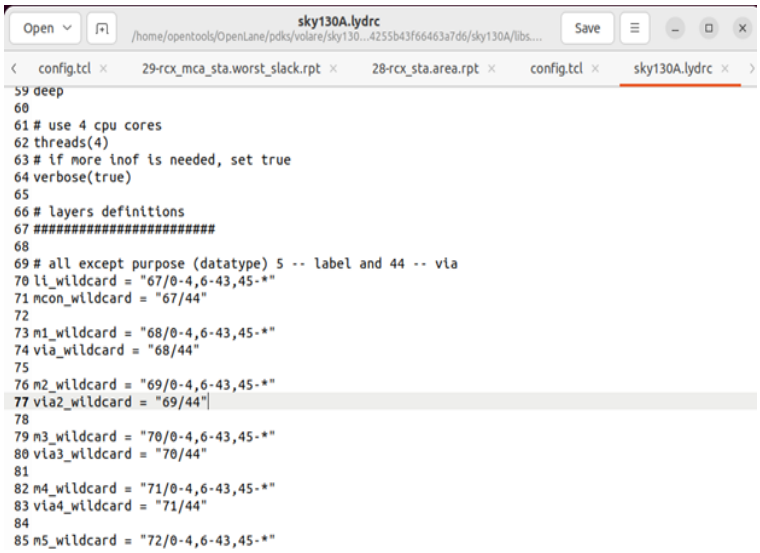


Metal layer mapping number

As shown in sky130A.lydrc file which is in the directory:

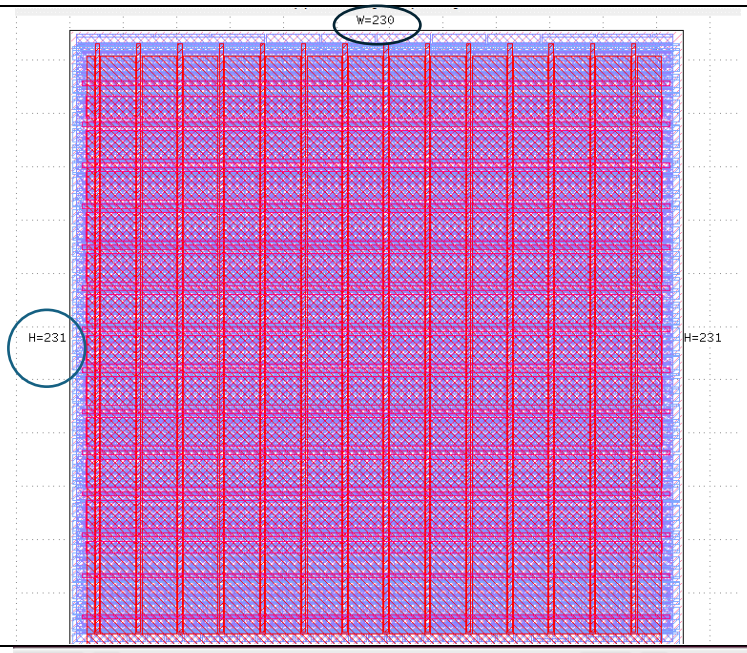
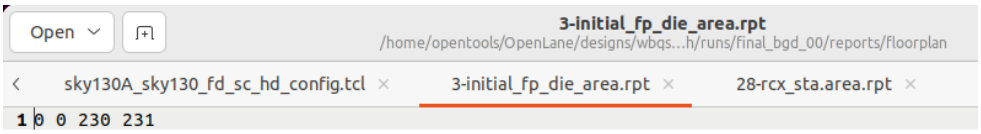
"/home/opentools/OpenLane/pdks/volare/sky130/versions/41c0908b47130d5675ff848 4255b43f66463a7d6/sky130A/libs.tech/klayout"

in this script we will see the metal layers mapping number.



Metal 2	*69/0-4,6-43,45 to max integer exist*
Metal 3	*70/0-4,6-43,45 to max integer exist*

validation of the metals used for pins creation.

LEF view	
FP configurations	
FP report	

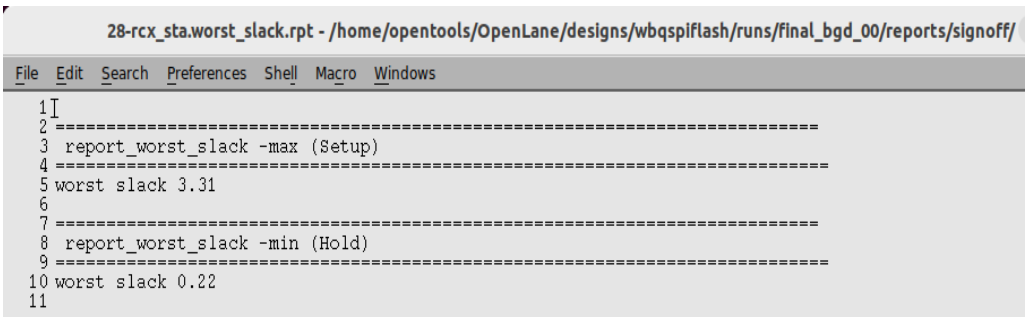
results of Sign off:

The target *was to get minimum period and violations clean design with minimum possible area.*

Result: *I have achieved clock period 6.6ns without setup or hold violations in* ***multi corner analysis*** *and total area of 46948 um^2 97% utilization. Clean without any type of violations and DRC in* ***signoff stage.***

Across multiple runs changing some switching values to force the tool to get its maximum optimization.

Screenshots for reports and terminal

The terminal output	
Worst slack report "for tt analysis"	

Worst slack report "for multi corner analysis"	29-rcx_mca_sta.worst_slack.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/final_... File Edit Search Preferences Shell Macro Windows 1 2 ========== 3 report_worst_slack -max (Setup) 4 ========== 5 worst slack 0.06 6 7 ========== 8 report_worst_slack -min (Hold) 9 ========== 10 worst slack 0.04 11
DRC report	drc.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/final_bgd_00/reports/signoff/ File Edit Search Preferences Shell Macro Windows 1 wbqspiflash 2 ---------- 3 [INFO]: COUNT: 0 4 [INFO]: Should be divided by 3 or 4 5
Area report	9-rcx_mca_sta.area.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/final_bgd_00.. File Edit Search Preferences Shell Macro Windows 1 2 ========== 3 report_design_area 4 ========== 5 Design area 46948 u^2 97% utilization. 6
Clock period from config file in the run folder	config.tcl - /home/opentools/OpenLane/designs/wbqspiflash/runs/final_bgd_00/ File Edit Search Preferences Shell Macro Windows 18 set ::env(CLOCK_PERIOD) {6.6} 19 set ::env(CLOCK_PORT) {i_clk} 20 set ::env(CLOCK_TREE_SYNTH) {1} 21 set ::env(CLOCK_WIRE_RC_LAYER) {met5} 22 set ::env(CONFIGS) {/home/opentools/OpenLane/configuration/placement.tcl 23 set ::env(CORE_AREA) {5 5 225 226}

The content of sky130A_sky130_fd_sc_hd_config.tcl I have added

```
# Adjusted Optimization Configuration Script

# Clock period and related settings
set ::env(CLOCK_PERIOD) 6.6             ;# Slightly relaxed clock period
```

```
set ::env(SYNTH_CLOCK_UNCERTAINITY) 0.1                    ;# Tight but not
overly aggressive clock uncertainty
set ::env(SYNTH_CLOCK_TRANSITION) 0.1                      ;# Tight clock
transition

# Synthesis strategy and fanout control
set ::env(SYNTH_STRATEGY) "AREA 3"                        ;# Balanced delay
optimization
set ::env(SYNTH_MAX_FANOUT) 30                           ;# Slightly increased
max fanout for better timing
set ::env(CLOCK_BUFFER_FANOUT) 15                         ;# Slightly increased
clock buffer fanout
set ::env(SYNTH_BUFFERING) 1                             ;# Enable buffering
set ::env(SYNTH_SIZING) 1                                  ;# Enable cell
sizing

# Capacitive load setting
set ::env(SYNTH_CAP_LOAD) 5                              ;# Standard capacitive
load

# Timing derating
set ::env(SYNTH_TIMING_DERATE) 0.00                        ;# No timing
derating

# Utilization and density settings
set ::env(FP_CORE_UTIL) 60                                ;# Balanced core
utilization
set ::env(PL_TARGET_DENSITY) [expr ($::env(FP_CORE_UTIL) + 10) / 100.0]
set ::env(IO_PCT) 0.1                                      ;# Tight I/O delays
# Synthesis tool and script settings
set ::env(SYNTH_BIN) yosys                                 ;# Yosys binary used
in the flow
set ::env(SYNTH_SCRIPT) ::env(SCRIPTS_DIR)/yosys/synth.tcl
set ::env(SYNTH_NO_FLAT) 0                                 ;# Flatten hierarchy
for better optimization
set ::env(SYNTH_FLAT_TOP) 1                                ;# Flatten the top
level during elaboration
set ::env(SYNTH_READ_BLACKBOX_LIB) 0                       ;# Do not read full
liberty file as blackbox
set ::env(SYNTH_SHARE_RESOURCES) 1                         ;# Enable resource
sharing for better area and timing
set ::env(SYNTH_ADDER_TYPE) "YOSYS"           ;# Use ripple carry adder for
balanced timing

# Extra mapping file and parameters
set ::env(SYNTH_EXTRA_MAPPING_FILE) ""                     ;# No extra techmap
file
set ::env(SYNTH_PARAMETERS) ""                             ;# No additional
parameters for Yosys

# Base SDC file for timing constraints
set ::env(BASE_SDC_FILE) $::env(OPENLANE_ROOT)/scripts/base.sdc
```

```
# Verilog includes and blackbox settings
set ::env(VERILOG_INCLUDE_DIRS) ""                          ;# No specific
Verilog include directories
set ::env(VERILOG_FILES_BLACKBOX) ""                        ;# No blackbox
Verilog files specified

##########################floorplan#############################################

# Floorplan defaults
#set ::env(FP_SIZING) realative
set ::env(FP_SIZING) absolute
set ::env(DIE_AREA) "0 0 230 231"
set ::env(CORE_AREA) "5 5 225 226"

set ::env(FP_CORE_UTIL) 60
set ::env(FP_CORE_MARGIN) 1
set ::env(FP_ASPECT_RATIO) 1

set ::env(FP_PDN_VOFFSET) 5.32
set ::env(FP_PDN_VPITCH) 30.94
set ::env(FP_PDN_HOFFSET) 5.65
set ::env(FP_PDN_HPITCH) 30.80

set ::env(FP_PDN_AUTO_ADJUST) 1

set ::env(FP_PDN_CORE_RING) 0
set ::env(FP_PDN_ENABLE_RAILS) 1

set ::env(FP_PDN_CHECK_NODES) 1
set ::env(FP_PDN_IRDROP) 1

set ::env(FP_IO_MODE) 1;#0matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 2
set ::env(FP_IO_VLENGTH) 2
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 1
set ::env(FP_IO_HTHICKNESS_MULT) 1
set ::env(FP_IO_MIN_DISTANCE) 5
set ::env(FP_IO_UNMATCHED_ERROR) 1

set ::env(BOTTOM_MARGIN_MULT) 4
set ::env(TOP_MARGIN_MULT) 4
set ::env(LEFT_MARGIN_MULT) 12
set ::env(RIGHT_MARGIN_MULT) 12

set ::env(FP_PDN_HORIZONTAL_HALO) 10
set ::env(FP_PDN_VERTICAL_HALO) $::env(FP_PDN_HORIZONTAL_HALO)
set ::env(FP_TAP_HORIZONTAL_HALO) 10
set ::env(FP_TAP_VERTICAL_HALO) $::env(FP_TAP_HORIZONTAL_HALO)
set ::env(FP_PDN_ENABLE_GLOBAL_CONNECTIONS) 1
```

```
set ::env(FP_PDN_ENABLE_MACROS_GRID) 1

set ::env(DESIGN_IS_CORE) 1


########################placement#################################
set ::env(PL_TARGET_DENSITY) 0.47
set ::env(PL_ROUTABILITY_DRIVEN) 1
set ::env(PL_TIME_DRIVEN) 1
set ::env(PL_RANDOM_GLB_PLACEMENT) 0
set ::env(PL_BASIC_PLACEMENT) 0
set ::env(PL_SKIP_INITIAL_PLACEMENT) 0
set ::env(PL_RANDOM_INITIAL_PLACEMENT) 0
set ::env(PL_ESTIMATE_PARASITICS) 1
set ::env(PL_RESIZER_DESIGN_OPTIMIZATIONS) 1
set ::env(PL_RESIZER_TIMING_OPTIMIZATIONS) 1
set ::env(PL_RESIZER_MAX_WIRE_LENGTH) 0
set ::env(PL_OPTIMIZE_MIRRORING) 1
set ::env(PL_RESIZER_BUFFER_INPUT_PORTS) 1
set ::env(PL_RESIZER_BUFFER_OUTPUT_PORTS) 1
set ::env(PL_RESIZER_MAX_SLEW_MARGIN) 20
set ::env(PL_RESIZER_MAX_CAP_MARGIN) 20
set ::env(PL_RESIZER_HOLD_SLACK_MARGIN) 0.2
set ::env(PL_RESIZER_TIE_SEPERATION) 0
set ::env(PL_RESIZER_SETUP_SLACK_MARGIN) 1
set ::env(PL_RESIZER_HOLD_MAX_BUFFER_PERCENT) 50
set ::env(PL_RESIZER_SETUP_MAX_BUFFER_PERCENT) 100
set ::env(PL_RESIZER_ALLOW_SETUP_VIOS) 0
set ::env(PL_RESIZER_ALLOW_HOLD_VIOS) 0
set ::env(PL_RESIZER_REPAIR_TIE_FANOUT) 1
set ::env(PL_MAX_DISPLACEMENT_X) 500
set ::env(PL_MAX_DISPLACEMENT_Y) 100
set ::env(PL_MACRO_HALO) {0 0}
set ::env(PL_MACRO_CHANNEL) {0 0}

########################CTS#################################
set ::env(CLOCK_TREE_SYNTH) 1
set ::env(CTS_TARGET_SKEW) 200
set ::env(CTS_TOLERANCE)  1
set ::env(CTS_SINK_CLUSTERING_SIZE) 60
set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER)  50
set ::env(CTS_REPORT_TIMING) 1
set ::env(CTS_CLK_MAX_WIRE_LENGTH) 0
```