EE313 PROJECT: DISCRETE OPAMP

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EE313-3

Introduction

From the given four options we decided to implement a Discrete OPAMP. An OPAMP is an operational amplifier that is used to amplify small electrical signals in order to not to lose the carried information on the signal. OPAMPs simply amplify the voltage difference between their input channels only using positive and negative DC power supplies. We used our differential amplifier knowledge to design and implement the discrete OPAMP. Our project had 2 steps: Software implementation and hardware implementation.

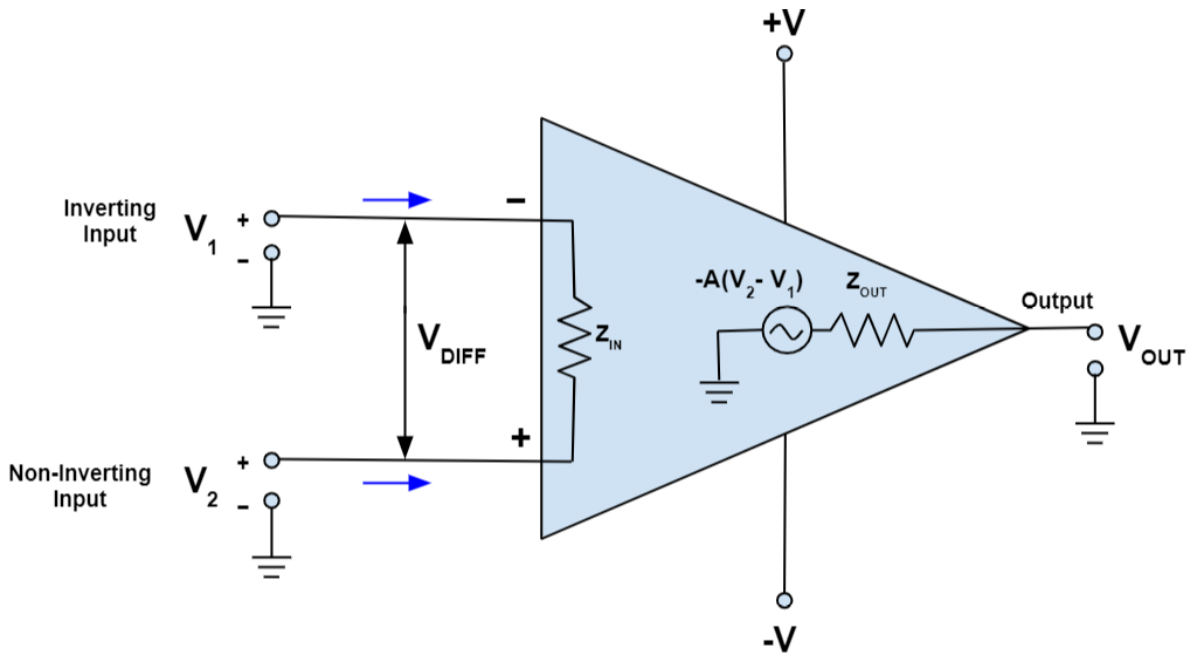

Figure 1: OPAMP schematic

While implementing the design the Project manual stated that we need to satisfy some requirements. In both software and hardware implementation we made sure that the following criteria are met:

- Dual power supplies (+/- V_{DD}) no more than +/-10V
- Power consumption should be less than 200mW.
- $A_V = V_{out}/(V_+ - V_-) > 500$
- An output stage that can drive a load resistance less than 1kΩ and the gain should not drop when the load resistance is connected.
- The circuit should generate its own biasing, if you need different voltages you should generate them from the supplies.
- Frequency compensation is not required, but you can implement it if you want to.

After satisfying these conditions, we are asked to connect a test circuit to observe that our OPAMP works as desired.

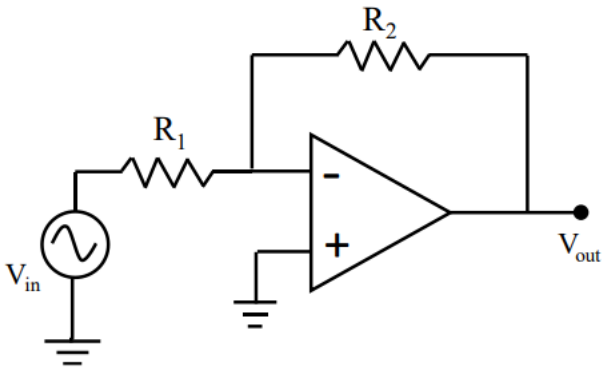

Figure 2: Test circuit

$V_{out} = -V_{in}$ should be observed in the circuit where R1 = R2 = 5KΩ.

Software Implementation and Analysis

There are 3 main stages in our discrete APAMP. The first stage is differential amplifier as input stage, second stage the level shifter which is a common emitter amplifier and the last part is a buffer circuit as the output stage.

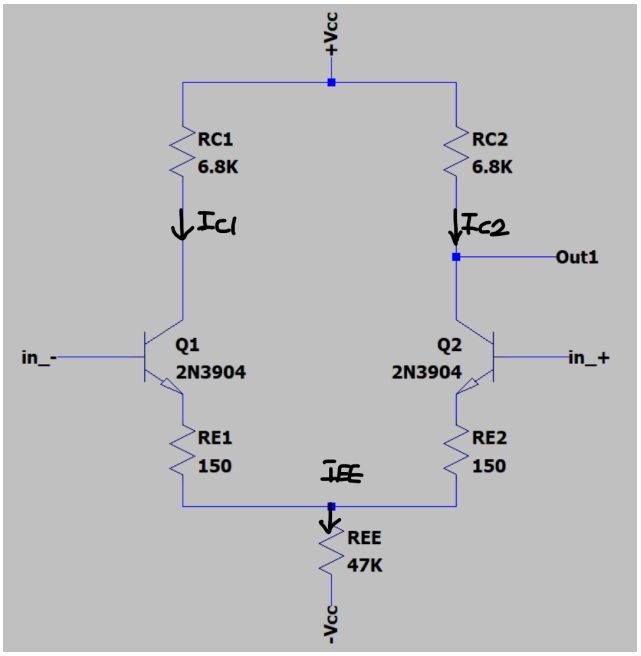

Figure 3: Differential amplifier circuit design

The input stage of a discrete OPAMP is most commonly a differential amplifier. In this stage it takes two inputs and it reduces the common noise significantly thus gives an overall better result in the following stages this stage also causes a 180-degree phase shit between the input and output. In this stage there is also smal signal gain but it is not much and also it is not the purpose of this stage. We used the basic differential amplifier design which we learned in the lectures. We could improve our results by changing the REE resistor with a BJT used as a current source but the software and hardware results meet the minimum requirements so we did not need any change in our design choice.

DC analysis:

For the simplicity and clarity, we assume collector currents same as the emitter currents ($\beta \tilde{=} \beta + 1$, since β is sufficiently large, $\beta \tilde{=} 200$) so by using KVL at emitter side

$$0 - V_{BE} - I_{E1}R_{E1} - I_{EE}R_{EE} = \quad - Vcc \; (eq. 1)$$

By plugging the numbers $V_{BE} = 0.62V$, $R_{E1} = 150ohms$, $I_{EE} = 2I_{E1}$, $R_{EE} = 47k\ ohms$, and $-V_{CC} = -10\ V$

we acquire $I_{E1} = 0.171\ mA$ and it gives us $V_{BE} = 0.62V\ and$ if we use this I_{E1} value in collector side we got

$$V_{CC} - I_{C1}R_{C1} = V_{C1}(eq.2)$$

it gives us $V_{CE} = 8.83V$, $V_{CE} > 0.2V$ so both of our transistors are forward active and nicely biased in this stage.

Small signal analysis:

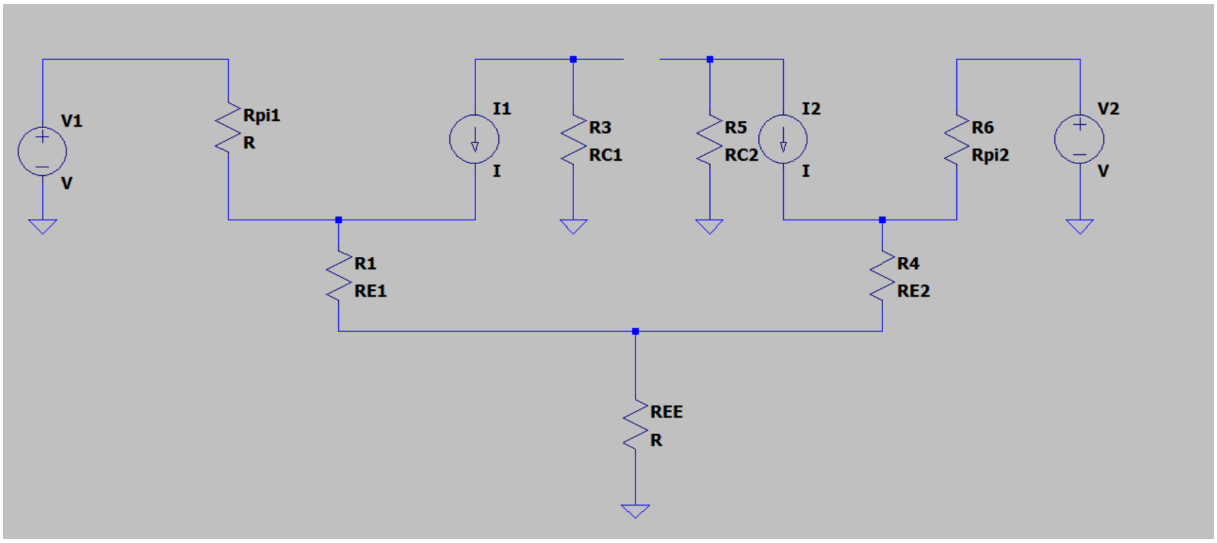

figure 4: small signal of the first stage

It gives as a differential mode gain of

$$\frac{V_{out}}{V_{In}} = \frac{-\beta R_{C2}}{R_{pi1}+(\beta+1)R_{E1}}$$

Which is approximately equals 45.333 and for the common mode gain it has:

$$\frac{V_{out}}{V_{In}} = \frac{-\beta R_{C2}}{R_{pi1}+(\beta+1)(R_{E1}+2REE)}$$

Which gives much smaller gain because of the REE term.

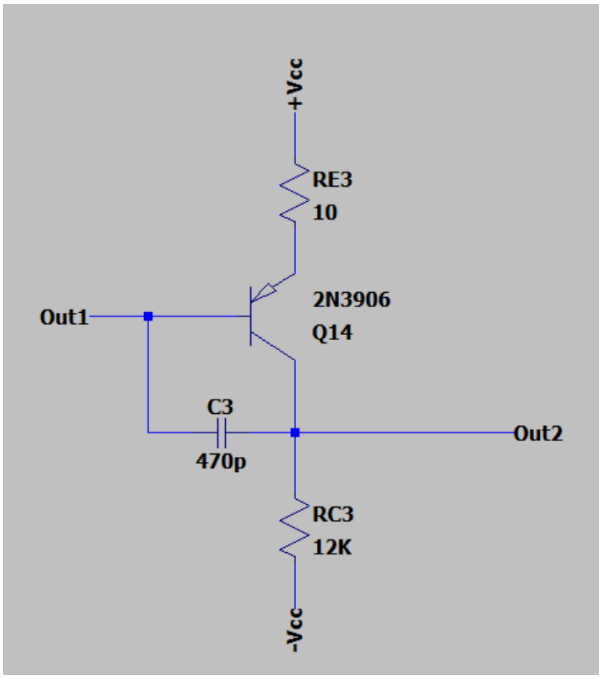

Figure 5: Common emitter BJT amplifier circuit design

This stage is the stage where most of the small signal amplification happens. For this purpose, we also used the basic common emitter design we learned in the lectures.

DC analysis:

We apply KVL for the emitter side

$$Vb - V_{BE} - I_{E3} R_{E3} = V_{CC} (eq. 3)$$

The Vb comes from the previous stage around 9.3V which gives us $I_{E3} = 0.838\, mA$. By assuming $I_{C3} = I_{E3}$ we obtain $V_{CE} = 9.59$ V so The BJT is forward active

Also we have $Rpi = \frac{V_T}{I_B} = \frac{0.026}{0.0008} \cong 32.5\, ohm$

Small Signal Analysis:

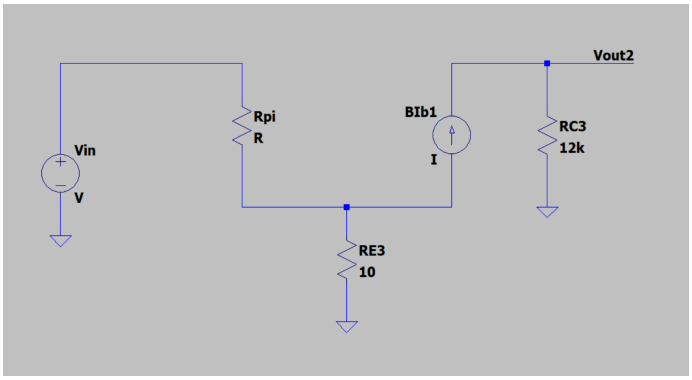

Figure 6: Common emitter BJT amplifier circuit small signal model

The gain equation is that

$$\frac{V_{out}}{V_{In}} = \frac{-\beta R_{C3}}{R_{pi}+(\beta+1)R_{E3}} \ (eq.\ 4)$$

So, when we plug the number, we get small signal gain of 1178.78 so it is approximately $\frac{R_{C3}}{R_{E3}}$ value.

The C3 capacitor is used for frequency compensation.

The last stage is the buffer stage. This stage causes some drop in the overall gain but it ensures that the circuit does not loses all of its gain to the smaller output load. This stage also ensures that the circuit has a smaller output resistance. For this purpose, we used the push-pull buffer design used in the lab 4.

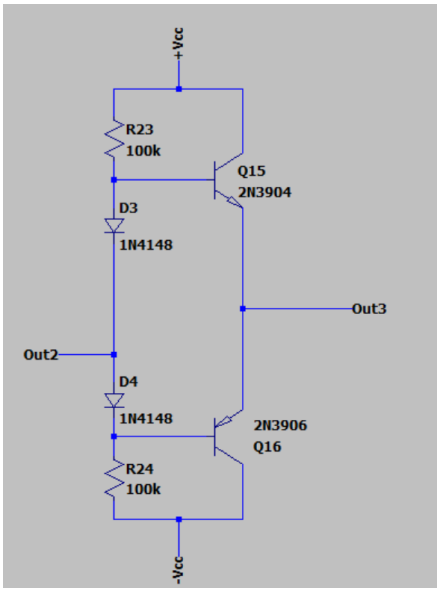

Figure 7: push-pull buffer design

In this stage diodes are making sure that the transistors are biased correctly all the time.

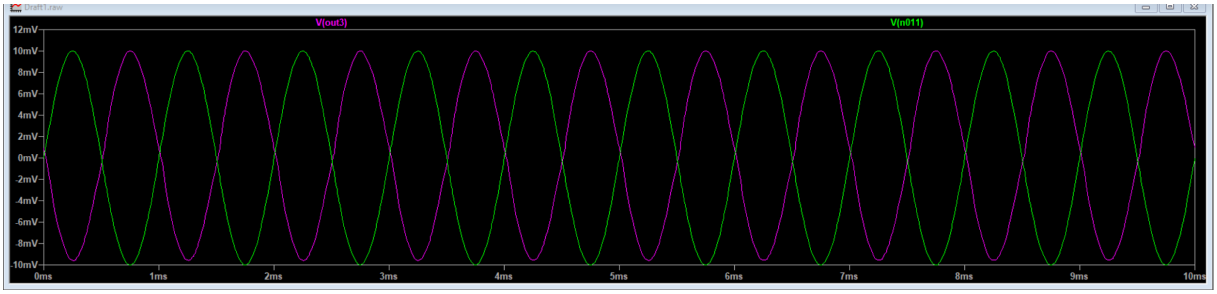

Figure 8: The test circuit results in the LT spice

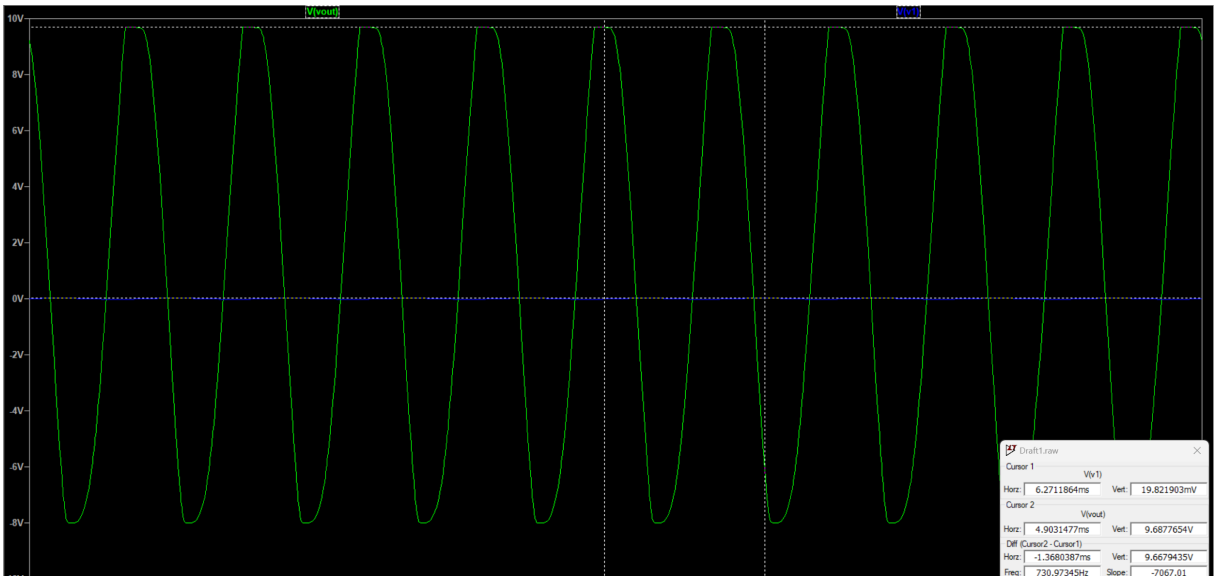

Figure 9: open circuit gain

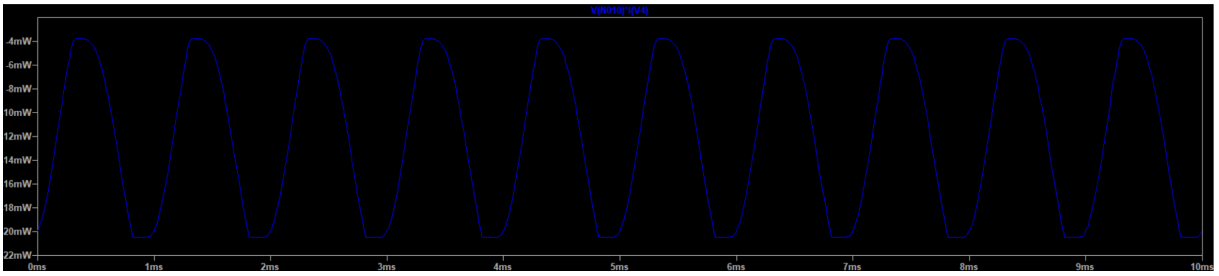

Figure 10: power consumption of the circuit

Hardware Implementation and analysis

While implementing the circuit on board, we used the buffer stage from fourth lab session and we bought 2N3904 and 2N3906 transistors to match with the software design exactly. Other components of the circuit are supplied from laboratory.

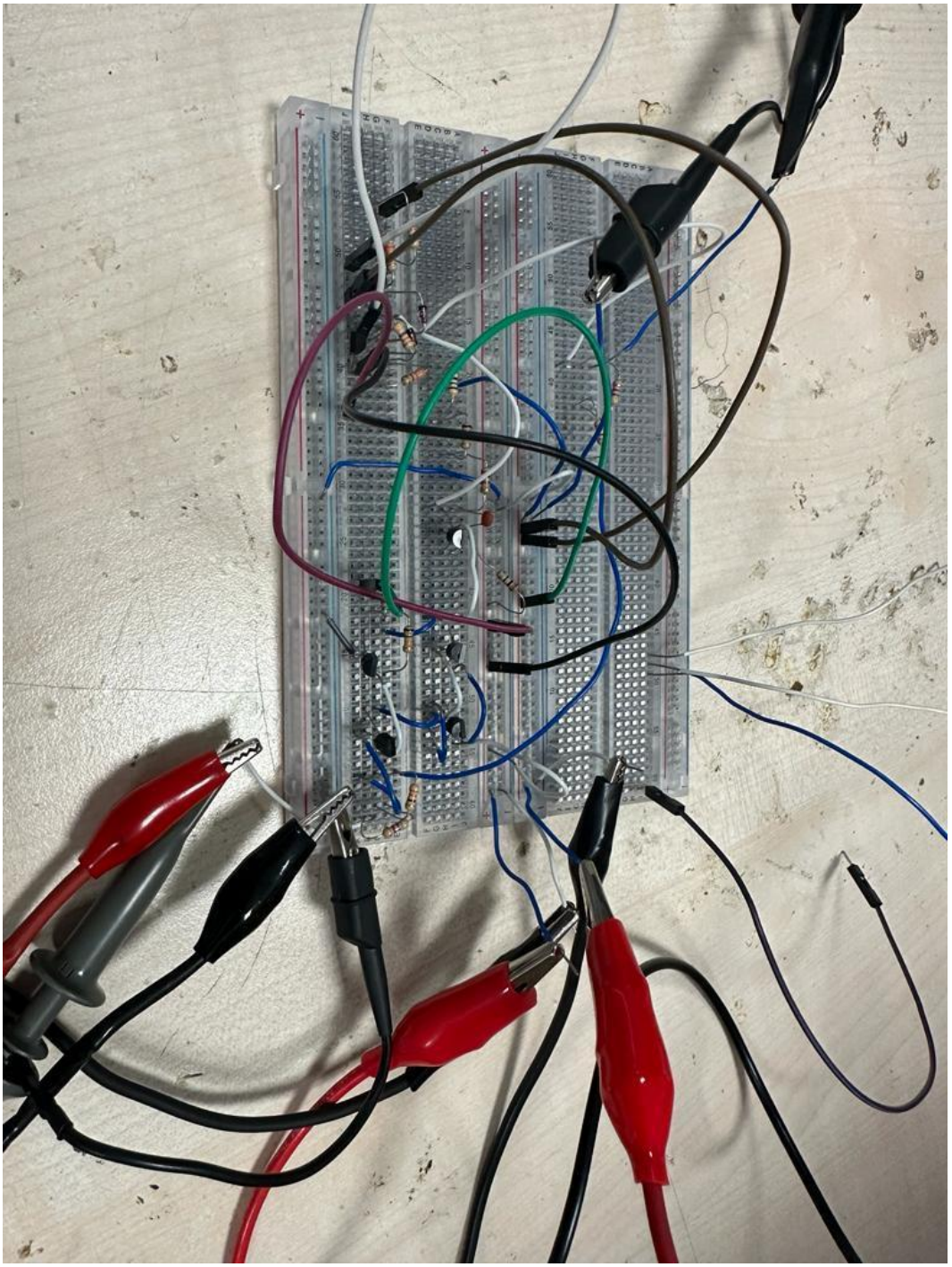

Figure 11: Breadboard implementation

First we measured the open loop gain. Our input was 10mV peak to peak with 1Khz. We observed our output as 16.2V peak to peak. Hence our gain is 675. The difference between the software and hardware gain is caused due to signal generators inability to apply 1mV sinusoidal input.

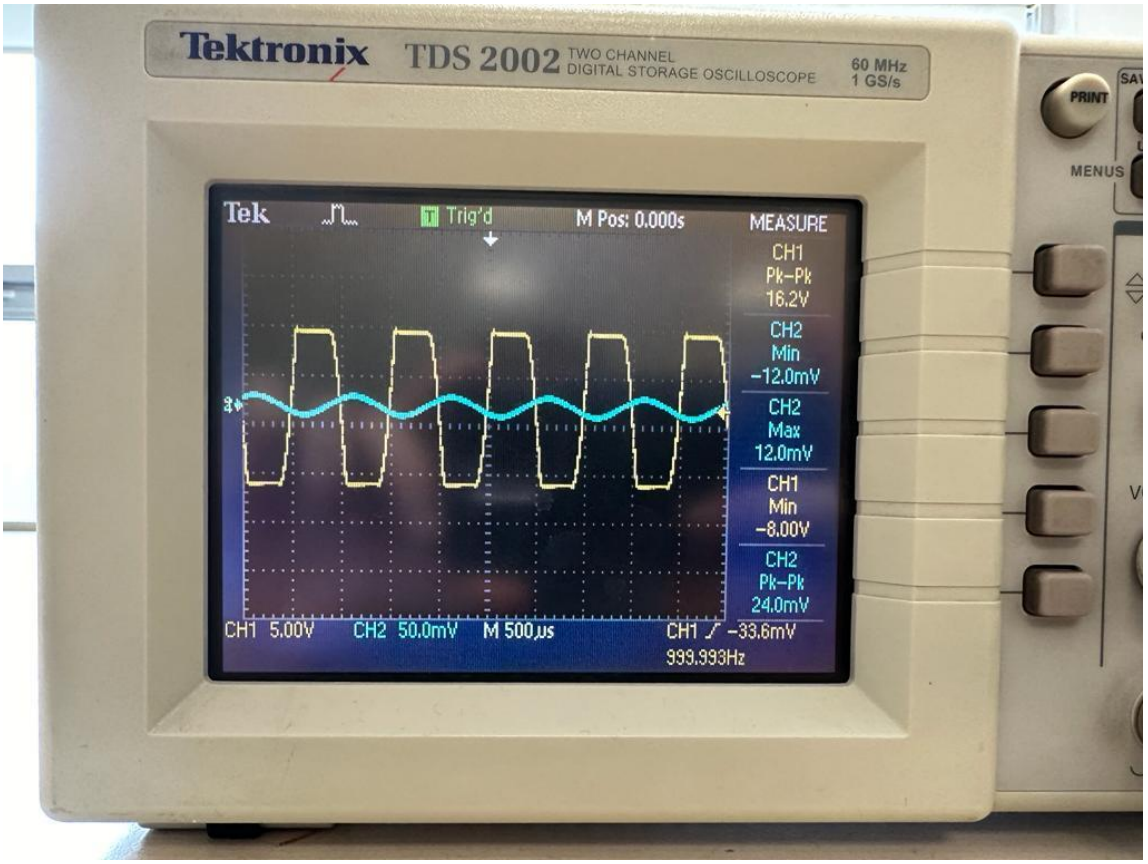

Figure 12: Open loop gain

Figure 13: Open loop gain and power consumption

From figure 13 it can be seen that 2mA current flows from supply hence the power consumption is 20mW from one supply. Also with the load resistance of 560Ω the open loop gain of the OPAMP did not change.

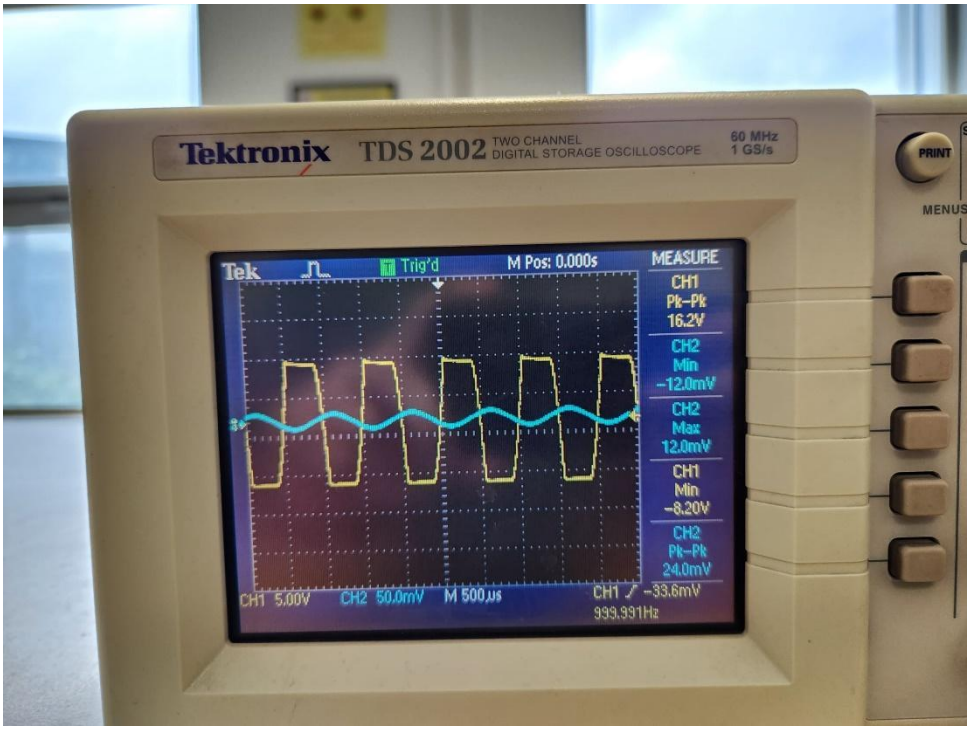

Figure 14: Open loop gain with load resistance

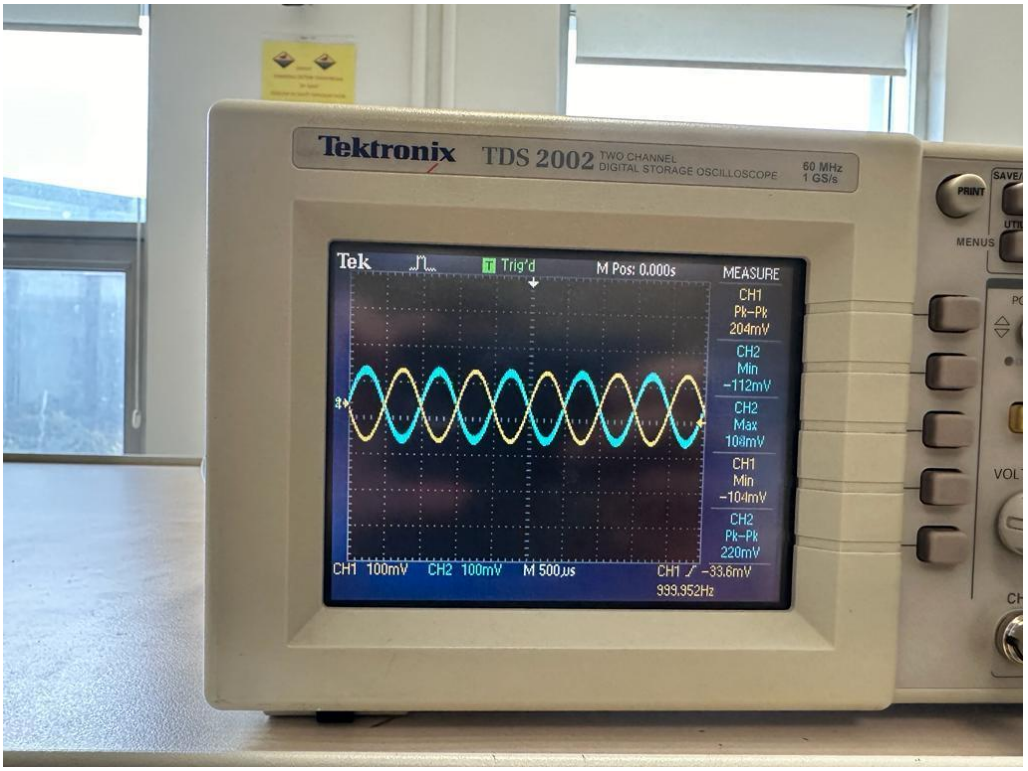

Figure 15: Test circuit result

As it can be seen from figure 15, our test circuit worked as we desired. The input signal is exactly inverted when the signal is 100mV peak to peak with 1Khz.

Conclusion

The main purpose of this Project was to design and implement a discrete OPAMP using the knowledge we got from the lecture. The OPAMP consists of 3 stages which are: differential amplifier, level shifter and buffer. The differential amplifier stage is used to differentiate the input signal from noise in order to not to amplify the noise. We used resistor design in the lecture notes instead of using a current mirror. Using resistors cost us some gain however, we were still able to meet the requirements for the open loop gain. Then with the level shifter stage, we get most of our gain and leveled the output around zero. Then we used a buffer stage to lower the output impedance of the circuit. We used fourth lab's buffer stage with same diodes and transistors. After completing the software design, we implemented the circuit on breadboard and used new bought 2N3904 and 2N3906 transistors to get a higher gain (due to beta values of these transistors). After analyzing the circuit on breadboard, we observed that our circuit meets the requirements of the project. Consequently, we implemented a Discrete OPAMP with an open loop gain higher than 500 and less power consumption than 200mW successfully.