

Part 1 Software Implementation

Introduction

The main purpose of this lab to design a band pass filter with central frequency(f_0) between 3MHz and 6MHz, passband width equal to $0.05f_0$, at least 3Db gain variation in the passband ,and 30 Db stopband attenuation. In order to fulfill the requirements a second order butterworth bandpass filter is implemented. f_0 selected as 3.58 MHz. The order selected as lowest possible and the frequency selected according to the available component values.

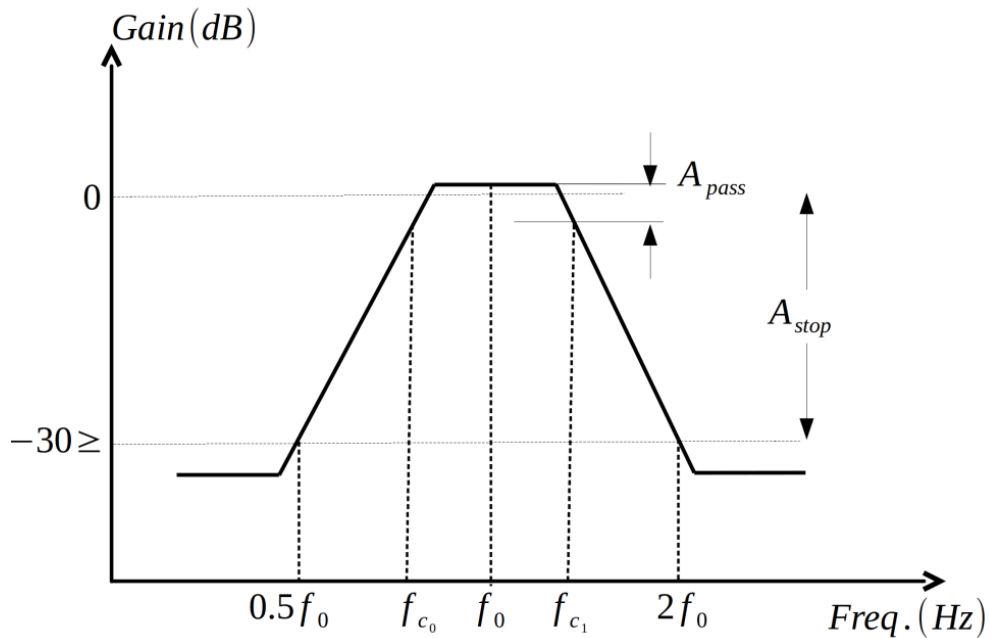


Figure 1: Frequency response of the filter

Central frequency: $3MHz \leq f_0 \leq 6MHz$

Passband width: $f_{c1} - f_{c0} = 0.05f_0$

Gain variation in the passband: $A_{pass} \leq 3dB$

Stopband attenuation: $A_{stop} \geq 30dB$

Analysis

Firstly the order of the band pass filter is determined from the equation

$$\frac{P_L}{P_A} = \frac{1}{1 + \left(\frac{f_0}{\Delta f}\right)^{2n} \left(\frac{f}{f_0} - \frac{f_0}{f}\right)^{2n}} \quad (\text{eq. 1.1})$$

for the values $f_1 = f_0 + \frac{\Delta f}{2}$ and $f_2 = f_0 - \frac{\Delta f}{2}$ The gain should be at least -3 Db in order to achieve this n should be bigger or equal than two and second order is selected since it is easier to implement in the hardware part.

For designing band pass filter Butterworth low pass filter with -3 Db cutt-of frequency equal to Δf is designed than it is elements tuned with LC circuits for f_0 .

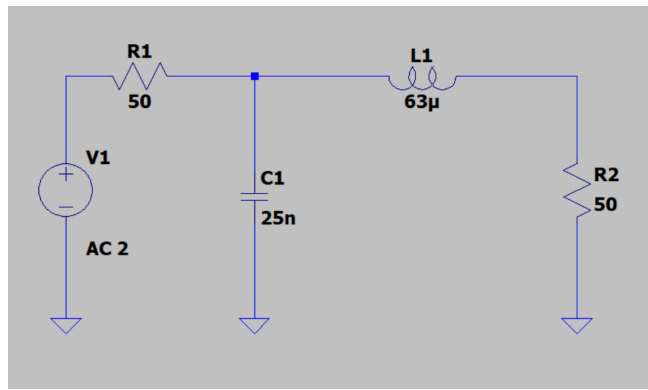


Photo 1: Butterworth low pass filter

For second order Butterworth low pass filter components selected according to

$$b_i = 2\sin\left(\frac{(2i-1)\pi}{2 \cdot 2}\right) \quad (\text{eq. 2.1})$$

$$L_2 = \frac{b_1 R}{2\pi \Delta f} \quad (\text{eq. 2.2})$$

$$C_1 = \frac{b_1}{2\pi R \Delta f} \quad (\text{eq. 2.3})$$

Inserting $b_1, b_2 = \sqrt{2}$, $R = 50 \text{ ohm}$ and $\Delta f = 179 \text{ KHz}$ we get

$$L_2 = 63 \text{ uH}$$

$$C_1 = 25 \text{ nF}$$

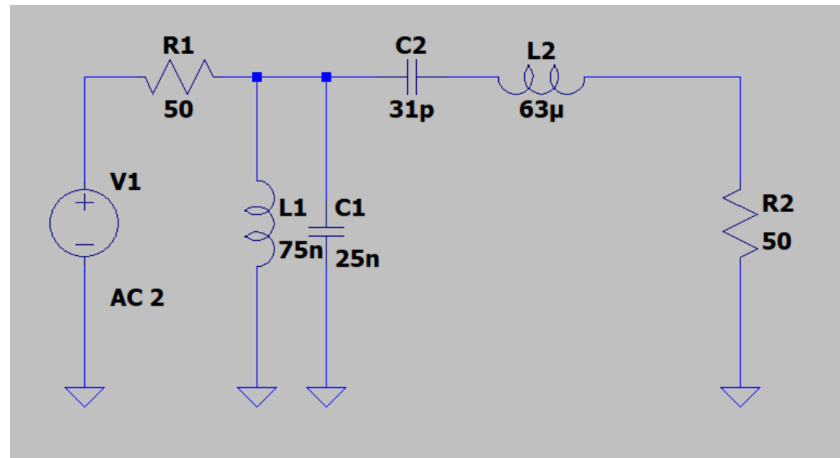


Photo 2: Butterworth band pass filter

For tuning capacitor C1 at f_0 we add parallel inductor with value

$$L_1 = \frac{1}{(2\pi f_0)^2 C_1} \text{ (eq. 2.4)}$$

Inserting C1 and $f_0 = 3.58 \text{ MHz}$ we get

$$L_1 = 75 \text{ nH}$$

For tuning L2 at f_0 we add series capacitor with value

$$C_2 = \frac{1}{(2\pi f_0)^2 L_2} \text{ (eq. 2.5)}$$

Inserting L2 and $f_0 = 3.58 \text{ MHz}$ we get

$$C_2 = 31 \text{ pF}$$

By taking $10\log$ of the the equation 1.1 we calculate the expected gain values

Gain at $f_0 = 0 \text{ Db}$, $f_{c_1} = -2.91 \text{ Db}$, $f_{c_0} = -3.12 \text{ Db}$

Simulations

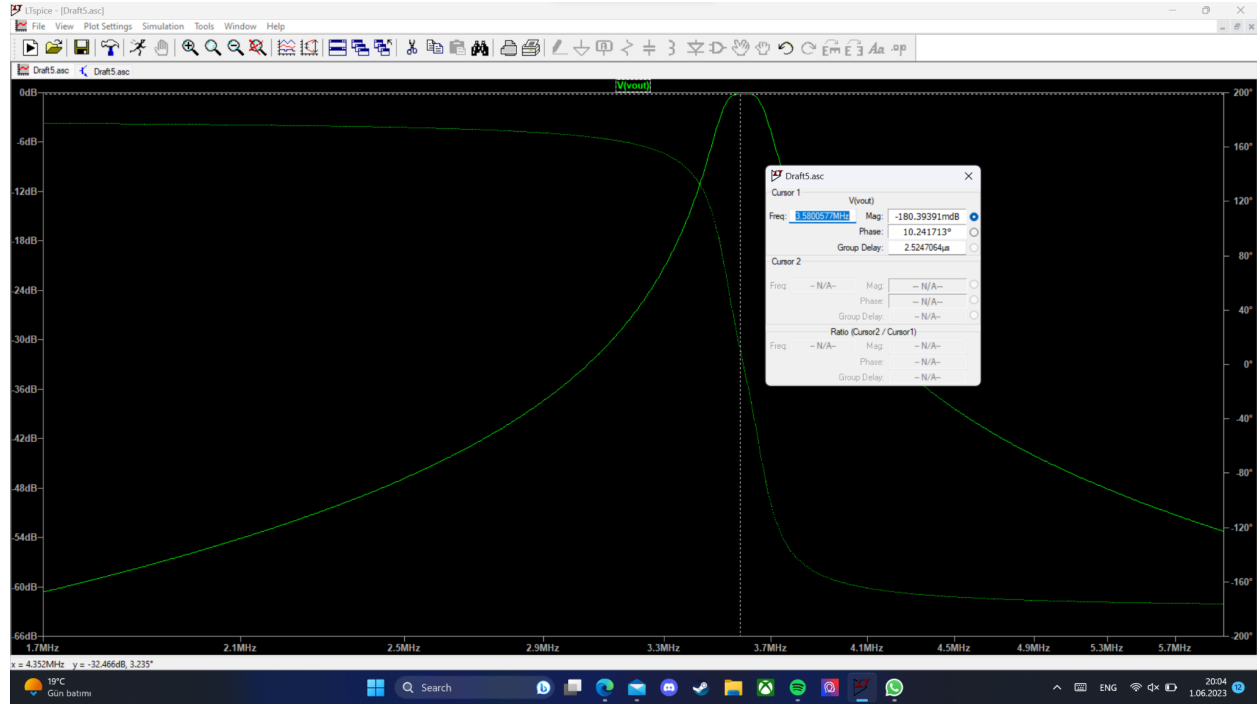


Photo 3: Simulation result of Butterworth bandpass filter

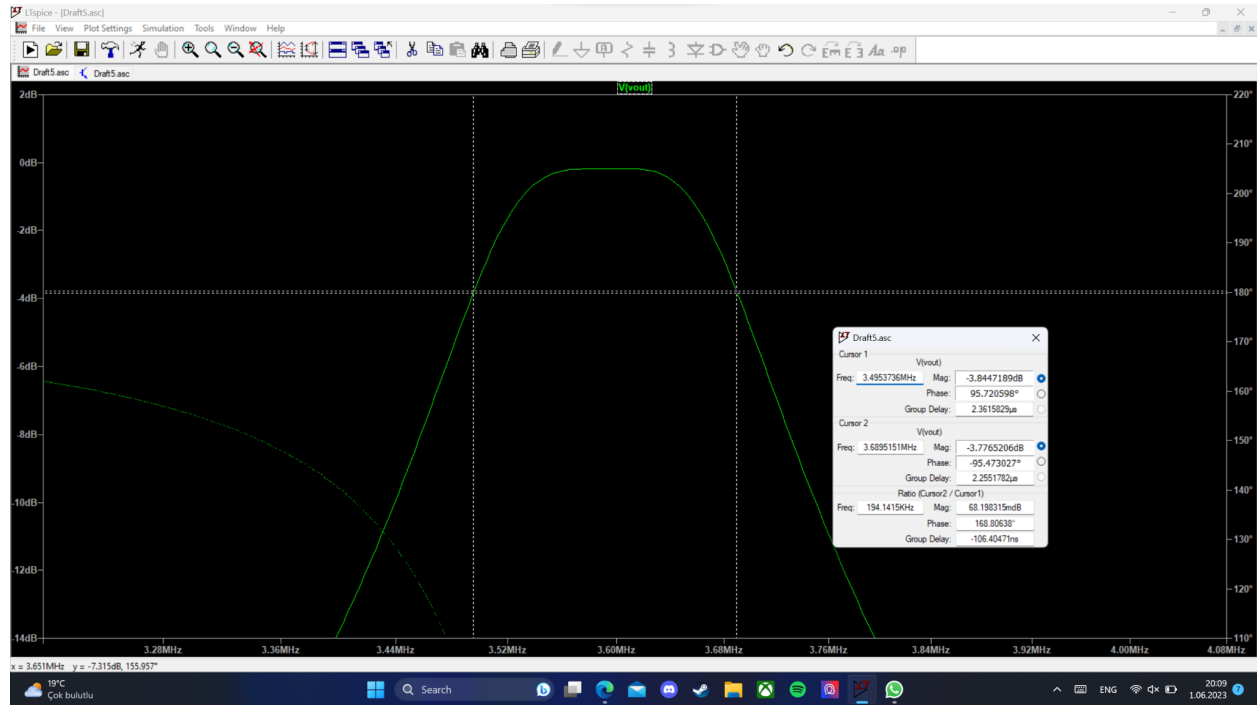


Photo 4: Simulation result of f_{c0} , f_{c1} values

EEE 202 Circuit Theory Lab 5
Melih Kutay Yagdereli 22002795
Section 1

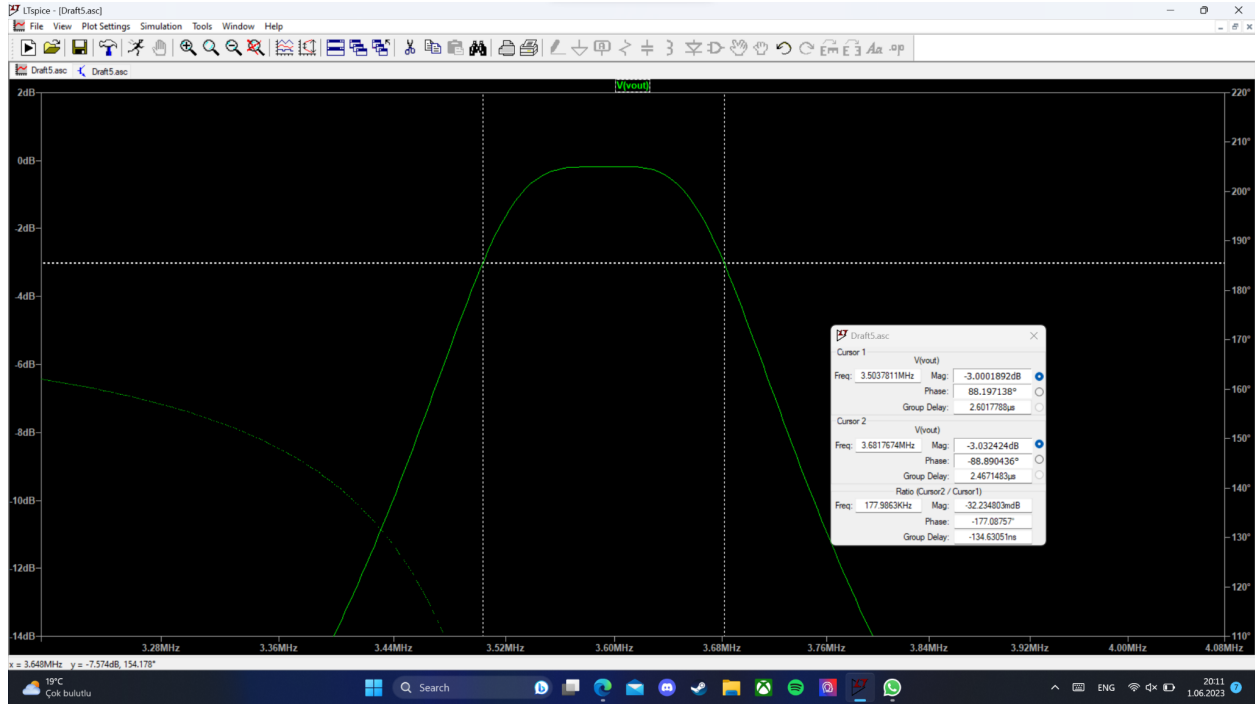


Photo 5: Simulation result of -3Db points

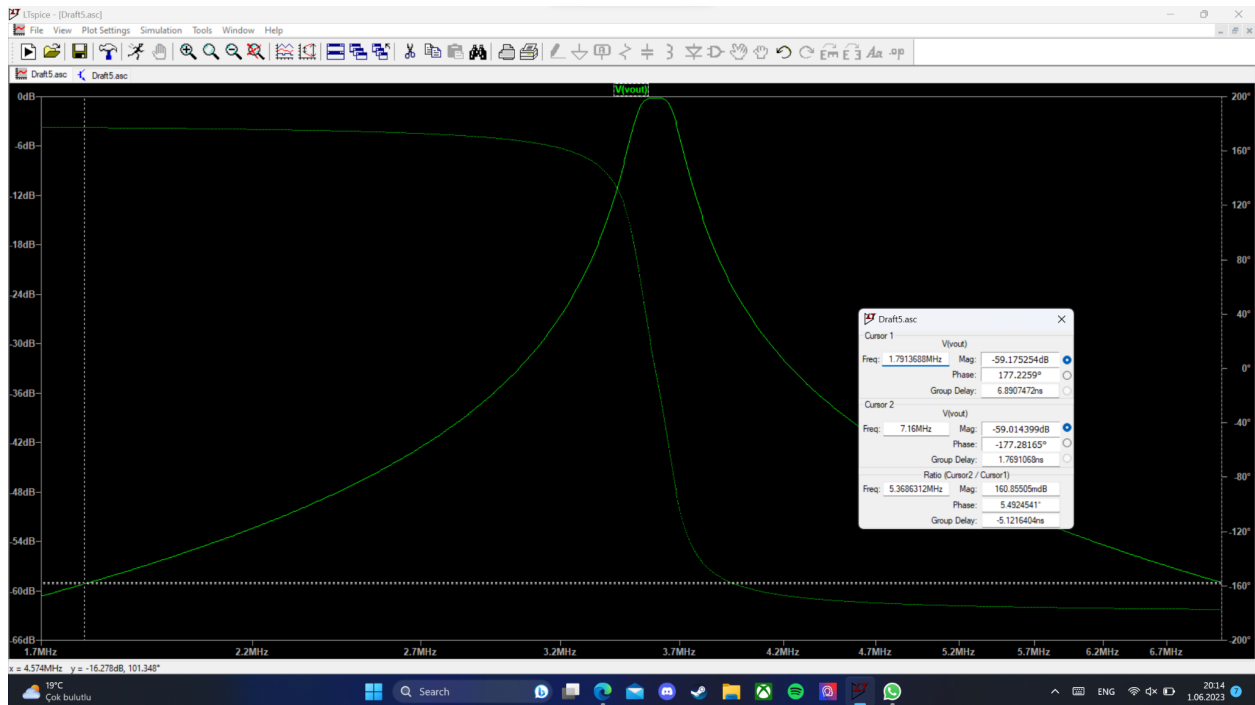


Photo 4: Simulation result of $0.5f_0$, $2f_0$ values

EEE 202 Circuit Theory Lab 5
Melih Kutay Yagdereli 22002795
Section 1

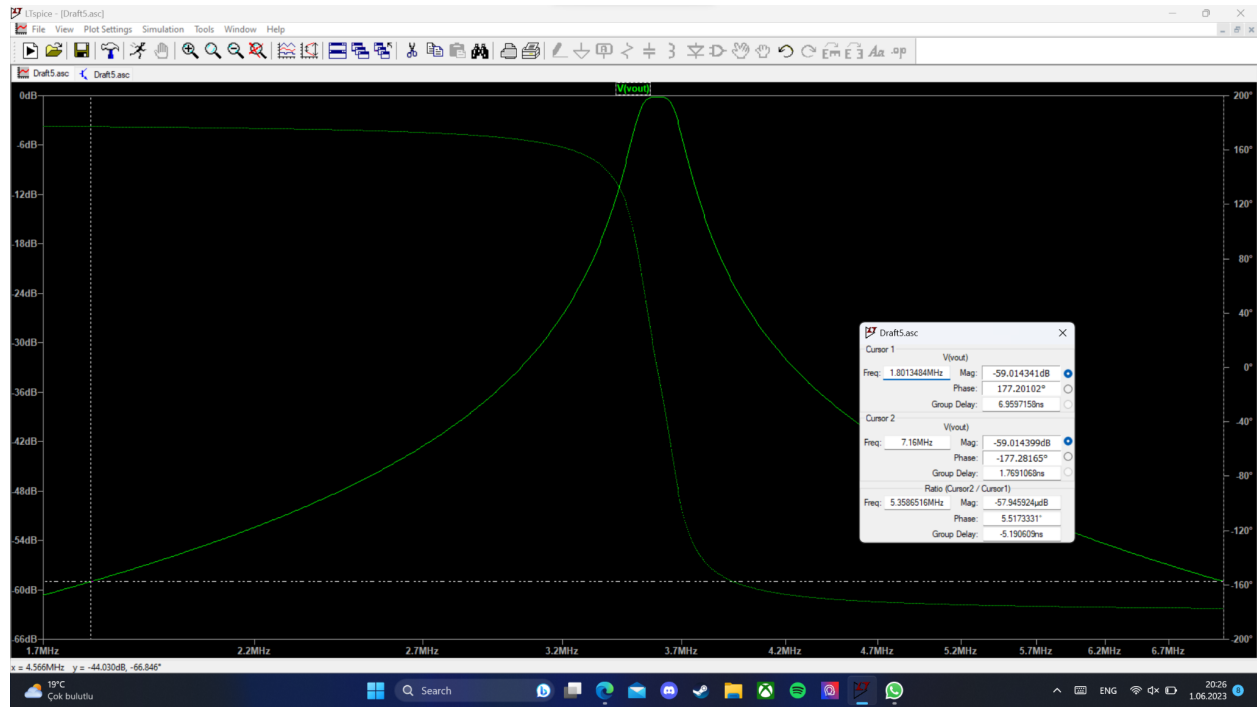


Photo 5: Simulation result of -59Db points

	Expected Value	Simulation Results	% Error
First -3Db point	3.571 MHz	3.503 MHz	1.9
Second -3Db point	3.359 MHz	3.681 MHz	9.59
First -59Db point	1.8 Mhz	1.79 Mhz	0.5
Second -59 Db point	7.16 Mhz	7.16 Mhz	0
Δf	179 Khz	177 KHz	1.1

Table 1: Errors of the simulation results

Δf value calculated from the values in the Photo 5

All of the errors are in the expected range. The reason for the errors is because values are selected according to the availability in labs and for easier implementation. In the hardware part which helped a lot in terms of applicability. Also inductor values vary according to the selected frequency.

Part 2 Hardware Implementation

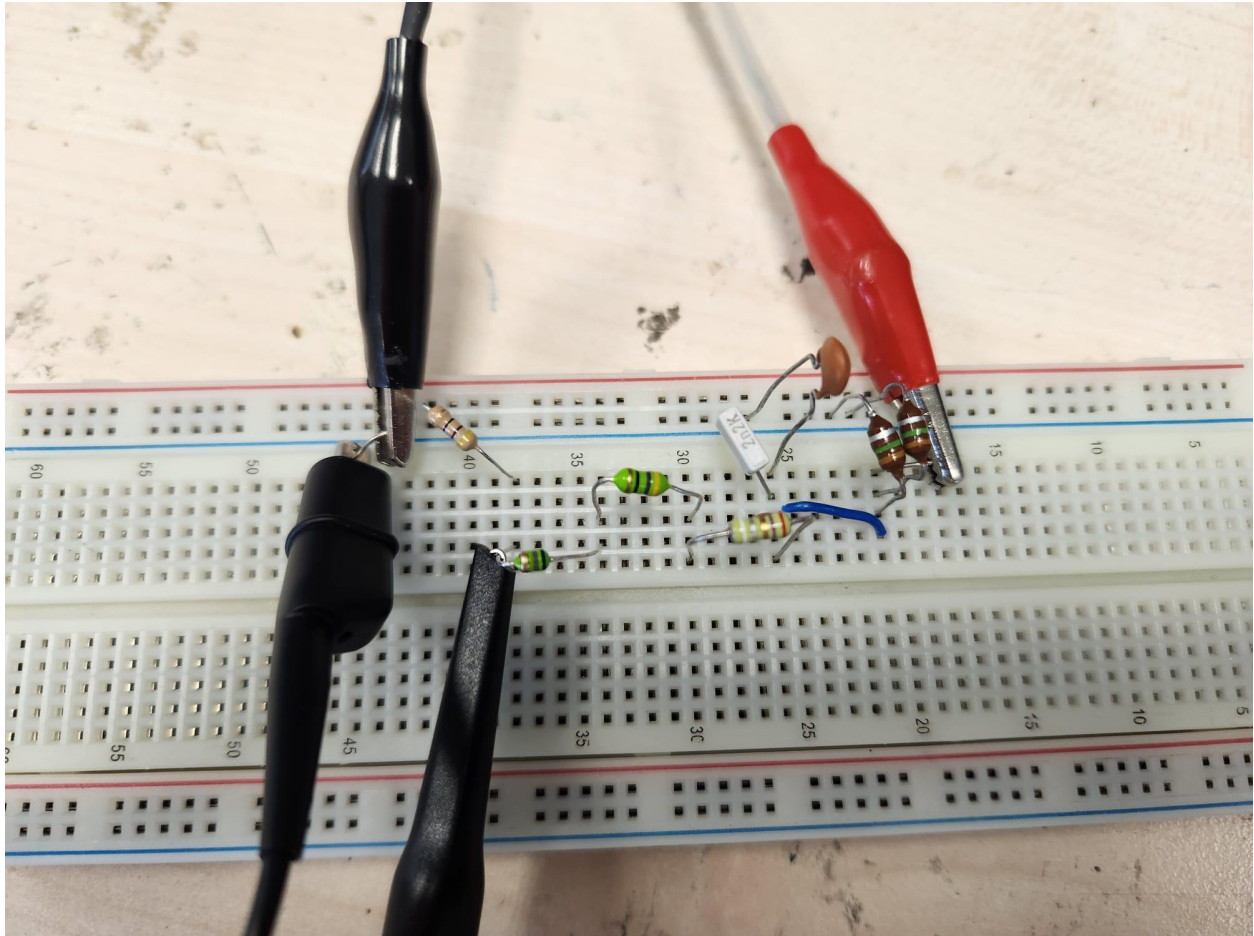


Photo 6: The implemented Butterworth bandpass filter circuit

EEE 202 Circuit Theory Lab 5
Melih Kutay Yagdereli 22002795
Section 1

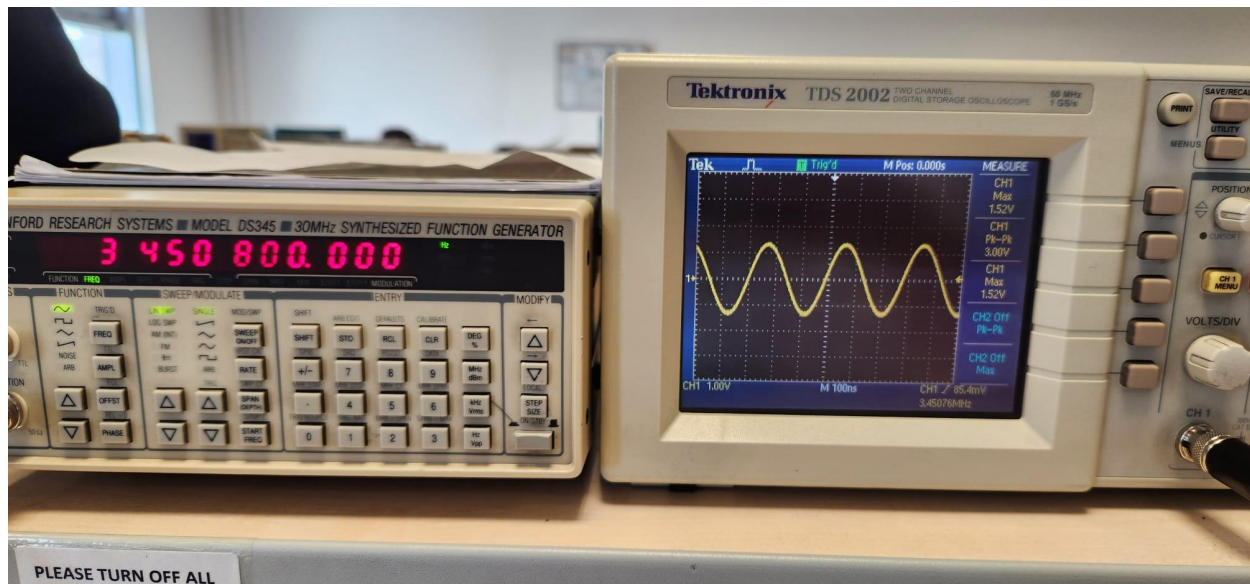


Photo 7: The Hardware result of the circuit for 3.45 MHz

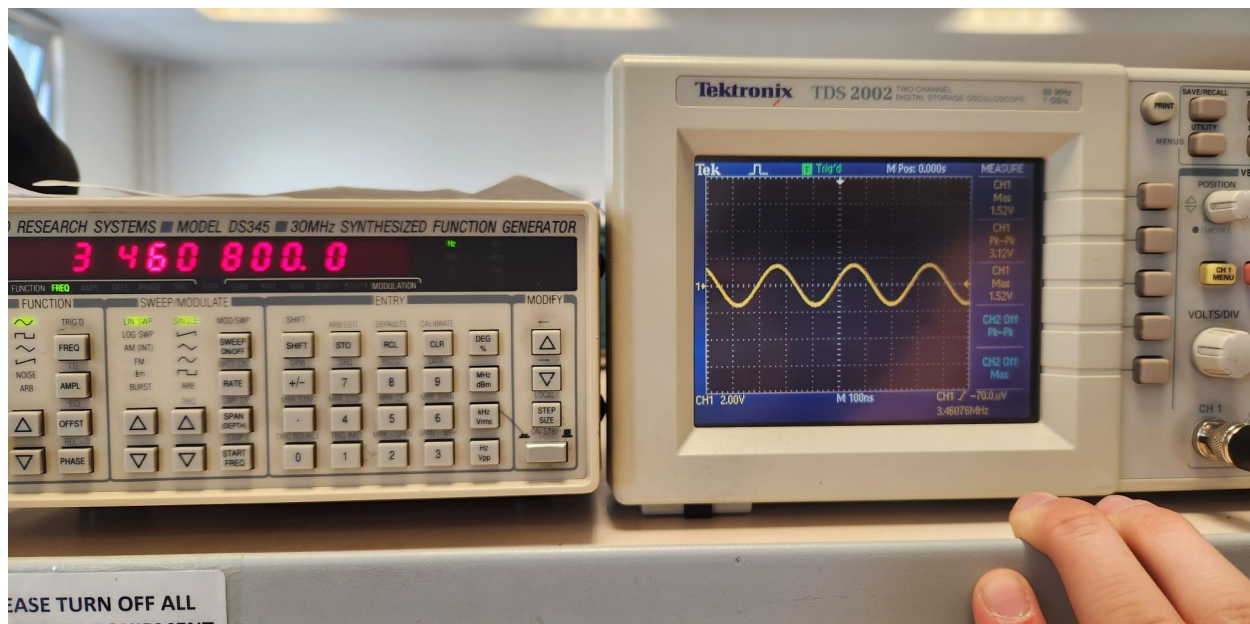


Photo 8: The Hardware result of the circuit for 3.46 MHz

EEE 202 Circuit Theory Lab 5
Melih Kutay Yagdereli 22002795
Section 1

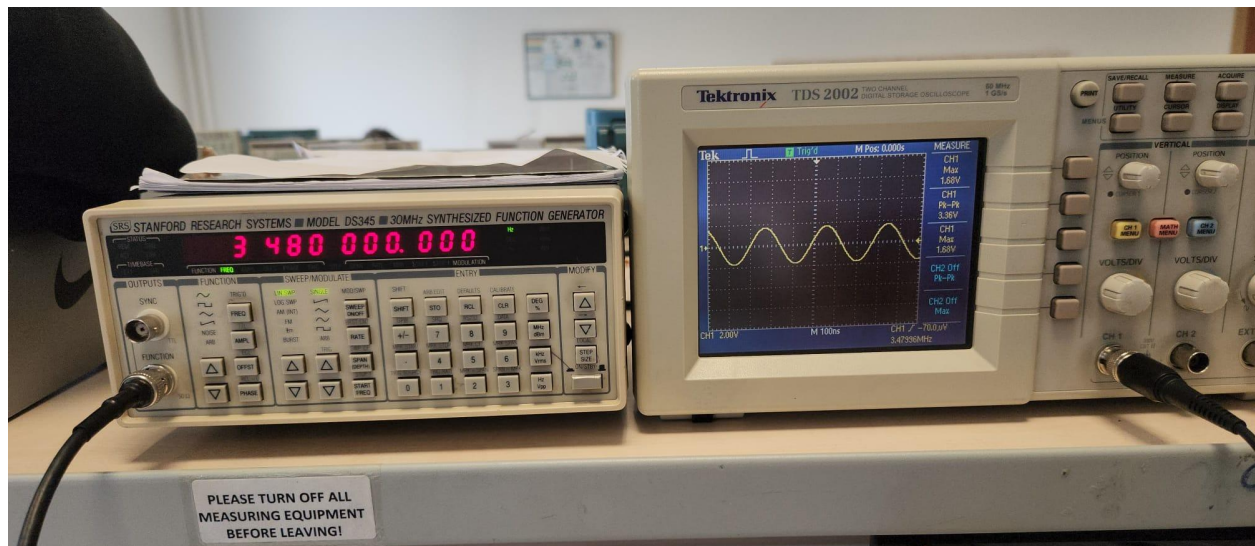


Photo 9: The Hardware result of the circuit for 3.48 MHz

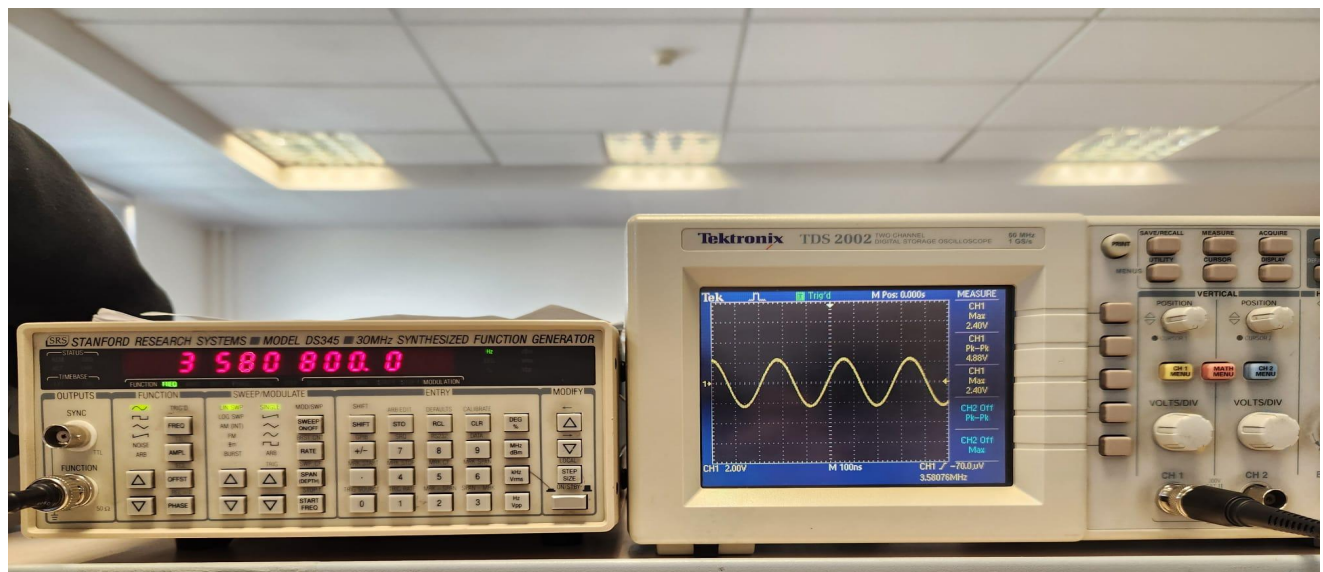


Photo 10: The Hardware result of the circuit for 3.58 MHz

EEE 202 Circuit Theory Lab 5
Melih Kutay Yagdereli 22002795
Section 1

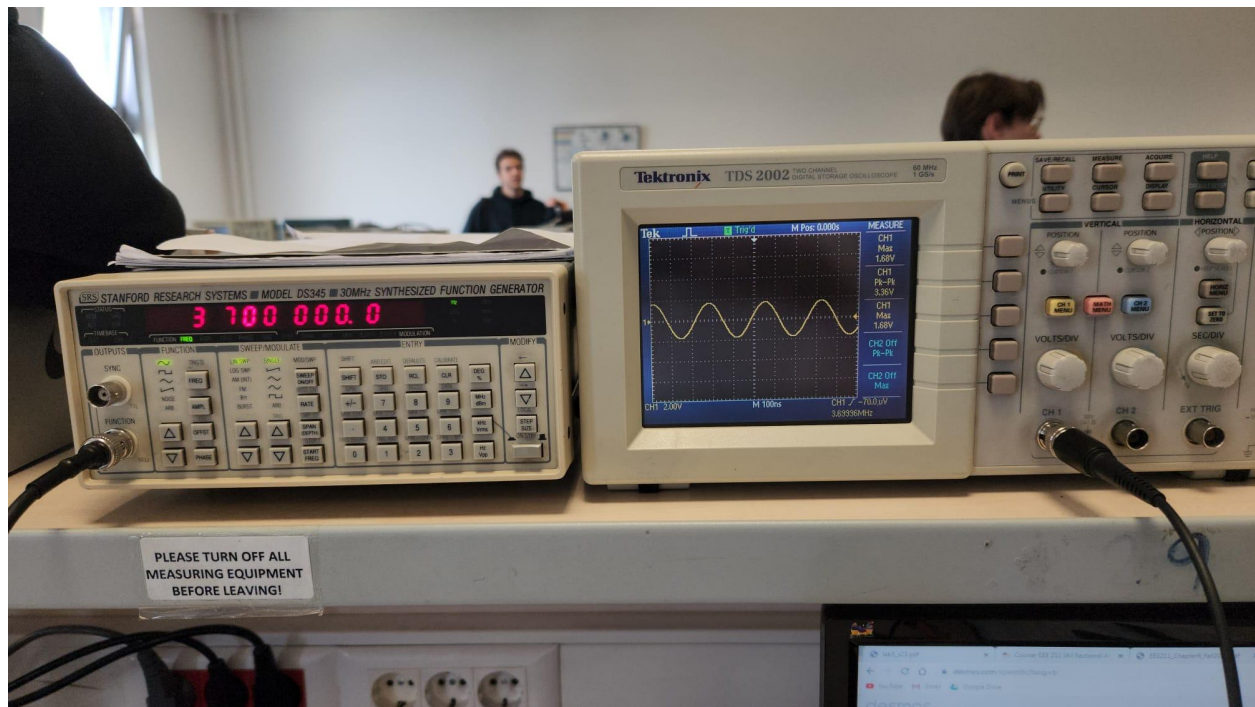


Photo 11: The Hardware result of the circuit for 3.700 MHz

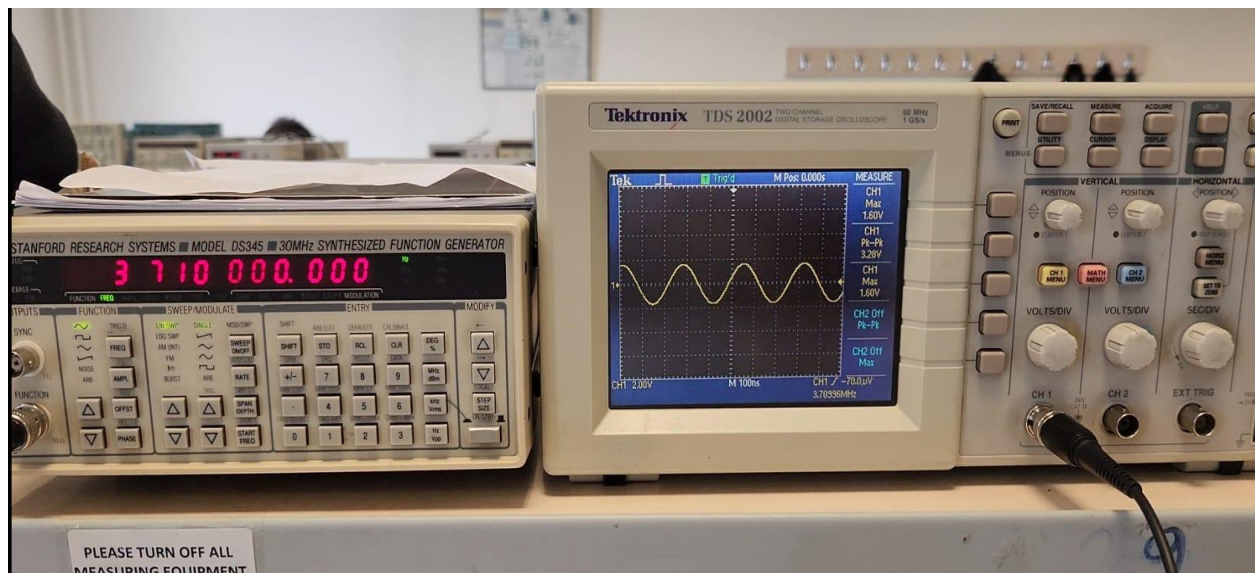


Photo 12: The Hardware result of the circuit for 3.71 MHz

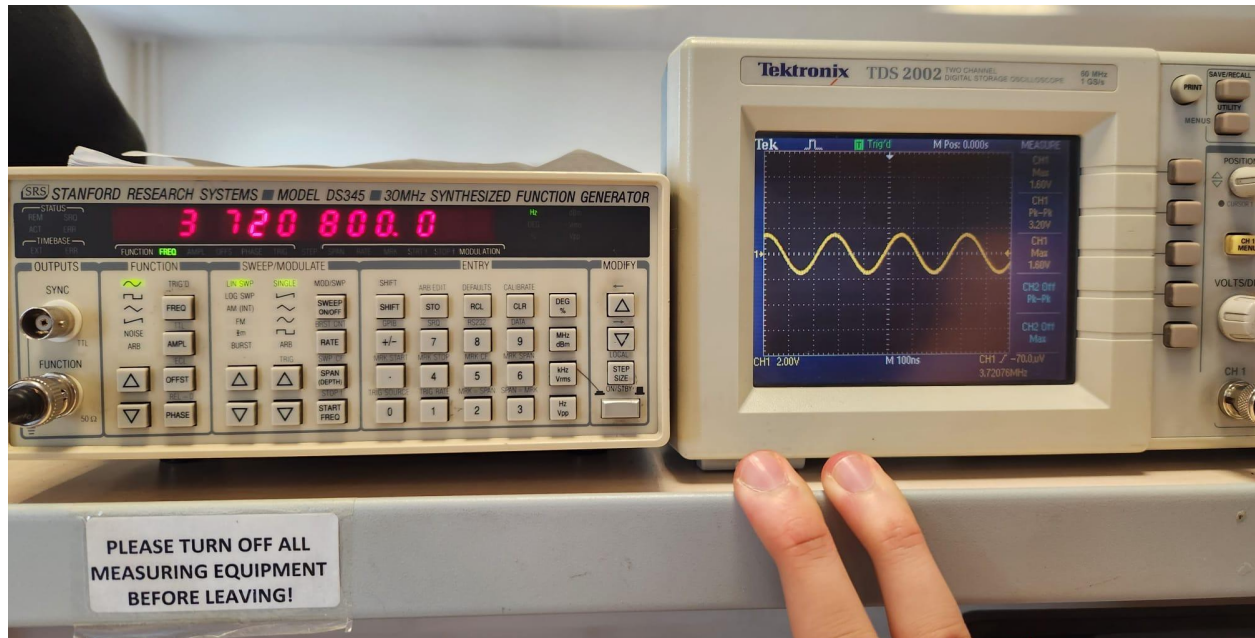


Photo 13: The Hardware result of the circuit for 3.72 MHz

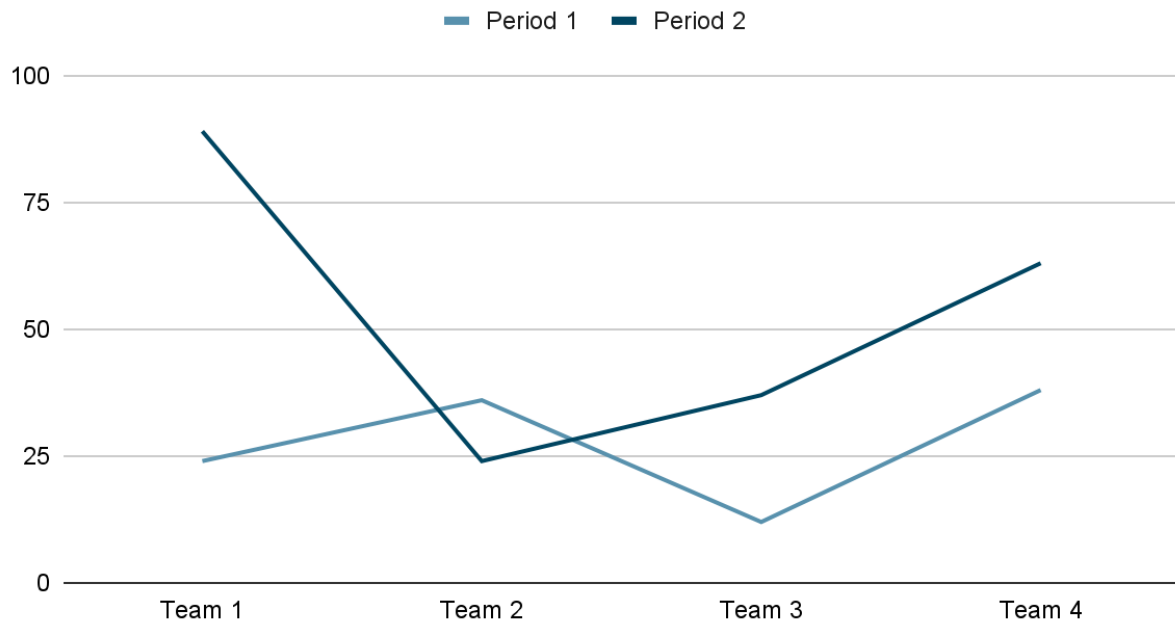
Frequency Values	Expected Value	Hardware Results	Simulation Results	% Error from Simulation value
3.450 Mhz	-7.63 Db	-4.44 Db	-5.37 Db	16.98
3.460 Mhz	-6.50 Db	-4.10 Db	-4.02 Db	1.99
3.480 Mhz	-4.23 Db	-3.45 Db	-3.44 Db	0.29
3.580 Mhz	0 Db	-0.21 Db	-0.069 Db	204
3.700 Mhz	-6.05 Db	-3.45 Db	-3.761 Db	8.24
3.710 Mhz	-7.11 Db	-3.66 Db	-4.37 Db	19.82
3.720 Mhz	-8.16 Db	-3.88 Db	-4.82Db	19.5

Table 2: Errors of the hardware results

The errors are below the accepted rate. This error shows that near the central frequency filter works better and as the frequency moves away from there filter deviates from the expected results. And the filter works better for low frequencies compared to

high frequencies. The %204 error at f_0 is caused because it is such small values that it is hard to measure with the lab equipment.

Points scored



Conclusion

The results came parallel to the analysis part but there are much higher error rates compared to other labs. This is mainly because it is a sensitive circuit. Using jumper cables and breadboard highly increased error rates. The simulation part follows the analysis part. In the hardware part the results still follow the expectation as shape but there is a high error. Hardware results showed that this filter works better with low frequencies and as the frequency goes to $2f_0$ or $1/2f_0$ the filter deviates from the expected values. This lab showed how to tune butterworth filters