

Part 1 Software Implementation

Introduction

The main purpose of this experiment is to design a circuit that transforms square wave input into a desired shaped wave benefiting OPAMP's and RC circuits properties. For this purpose two delay circuits, two integrator circuits and a subtractor circuit is implemented. In the delay circuits RC circuits are used to determine the delays Δt_0 , $\Delta(t_0 + t_1 + t_2)$ and OPAMP to amplify the voltage, in integrator circuit rc circuit and the opamp used for determining Δt_1 , Δt_3 , and creating ramp shapes. At last the subtractor OPAMP used for completing the total shape.

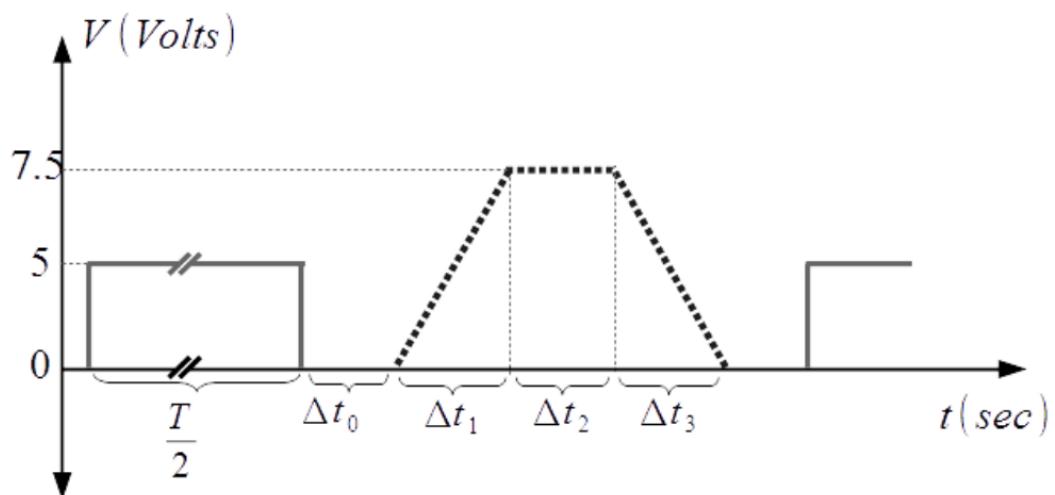


Figure 1

Analysis

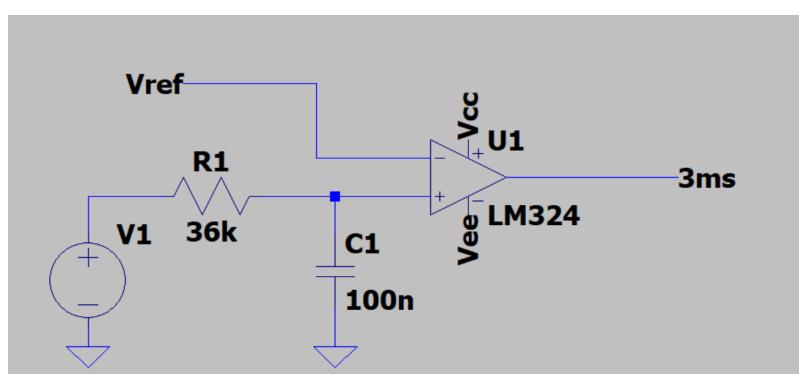


Photo 1: The delay circuit

As mentioned in the introduction part first the input will be shifted 3ms and 8ms in order to achieve this opamps are used in saturation mod to create the binary square shape. And the rc circuit part determines the delays. The delays calculated as

(By using KCL)

$$\frac{V_{C1} - V_{Input}}{R1} + C1 \cdot d\frac{V_{C1}}{dt} = 0 \quad (\text{eq. 1.1})$$

$$d\frac{V_{C1}}{dt} + \frac{V_{C1}}{R1 C1} = \frac{V_{Input}}{R1 C1} \quad (\text{eq. 1.2})$$

Eq 1.2 is a first order nonhomogeneous differential equation. For the Natural Response (homogeneous part) we found

$$d\frac{V_{C1}}{dt} + \frac{V_{C1}}{R1 C1} = 0 \quad (\text{eq. 1.3})$$

$$V_{C1(Homogeneous)}(t) = c_1 \cdot e^{-\frac{t}{R1 C1}} \quad (\text{eq. 1.4})$$

And for the forced response (Particular solution) we use candidate solution constant A $V_{C1(Particular)}(t) = A$ (Assume V_{Input} as constant 5 V).

$$d\frac{A}{dt} + \frac{A}{R1 C1} = \frac{5}{R1 C1} \quad (\text{eq. 1.5})$$

$$A = 5$$

So the general solution becomes

$$c_1 \cdot e^{-\frac{t}{R1 C1}} + 5 = 0 \quad (\text{eq. 1.6})$$

Inserting initial condition

$$V_{C1}(0) = c_1 \cdot e^{-\frac{0}{R1 C1}} + 5 = 0 \quad (\text{eq. 1.7})$$

$$c_1 = -5$$

$$V_{C1}(t) = 5 - 5 \cdot e^{-\frac{t}{R1 C1}} \quad (\text{eq. 1.8})$$

We want 3ms and 8ms delay so inserting t=3ms and t=8ms we reach

$$t=3\text{ms}; R1 \cdot C1 = 0.004328$$

$$R1 = 43\text{k ohm}, C1 = 100\text{n F}$$

$$t=8\text{ms}; R1 \cdot C1 = 0.0115$$

$$R1 = 5.6\text{k ohm}, C1 = 2.8\text{u F}$$

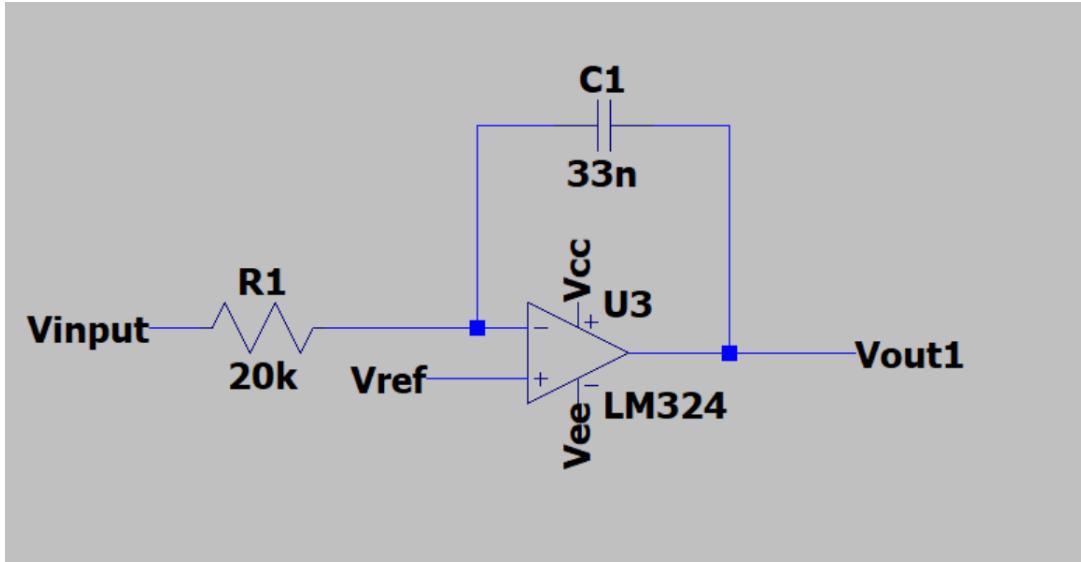


Photo 2: The integrator circuit

In the integrator part we use basic an integrating OPAMP circuit to create a skew line from the square wave input. For the 2ms duration we calculate the following equations

(By using KCL)

$$\frac{V_- - V_{Input}}{R1} + C1 \cdot d\frac{V_{C1}}{dt} = 0 \quad (\text{eq. 2.1})$$

$$d\frac{V_{C1}}{dt} = \frac{V_{Input} - V_-}{R1 C1} \quad (\text{eq. 2.2})$$

$$V_{C1}(t) = \frac{1}{R1 C1} \int (V_{Input} - V_-) dt \quad (\text{eq. 2.3})$$

$$V_{C1}(t) = \frac{t}{R1 C1} (V_{Input} - V_-) + C \quad (\text{eq. 2.4})$$

By using initial condition $V_{C1}(0) = 0$, $C = 0$. At $t=2\text{ms}$ we want 7.5 V so

$$\frac{2 \times 10^{-3}}{R1 C1} (2.5) = 7.5 \quad (\text{eq. 2.5})$$

$$R1 C1 = 6.66 \times 10^{-4} \quad (\text{eq. 2.6})$$

$$R1 = 20\text{k ohm} \quad C1 = 33\text{n F}$$

Since we want the same shape and the delay for the both sides, the same results are used for the both circuits.

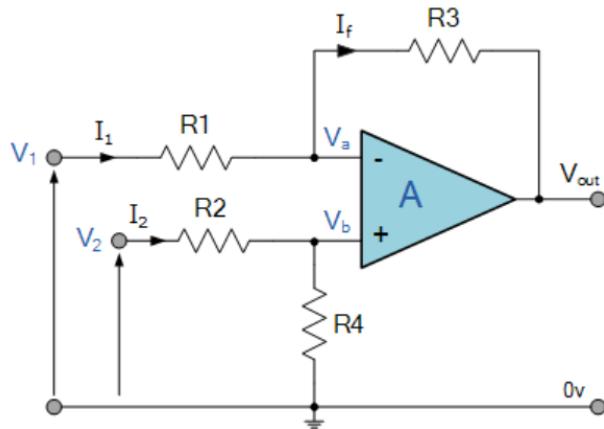


Photo 3: The Subtractor Circuit

At last for completing the total shape we used an basic subtractor OPAMP circuit the calculations for the resistance values are

$$\frac{V_1 - V_a}{R1} = \frac{V_a - V_{out}}{R3} \quad (\text{eq. 3.1})$$

$$V_- = \left(\frac{V_1}{R1} + \frac{V_{out}}{R3} \right) \cdot \frac{1}{\frac{1}{R3} + \frac{1}{R1}} \quad (\text{eq. 3.2})$$

$$\frac{V_2 - V_b}{R2} = \frac{V_b}{R4} \quad (\text{eq. 3.3})$$

$$\frac{V_b}{R4} + \frac{V_b}{R2} = \frac{V_2}{R4} \quad (\text{eq. 3.4})$$

$$V_b = \frac{V_2}{R2 \cdot \left(\frac{1}{R4} + \frac{1}{R2} \right)} \quad (\text{eq. 3.5})$$

Use $V_b = V_a$ in linear region

$$\frac{V_2}{R2 \cdot \left(\frac{1}{R4} + \frac{1}{R2} \right)} = \left(\frac{V_1}{R1} + \frac{V_{out}}{R3} \right) \cdot \frac{1}{\frac{1}{R3} + \frac{1}{R1}} \quad (\text{eq. 3.6})$$

Select all the resistor as equal to each other and the equation 3.6 simplifies to

$$V_2 - V_1 = V_{out} \quad (\text{eq. 3.7})$$

All resistor selected as 100k ohm

Simulations

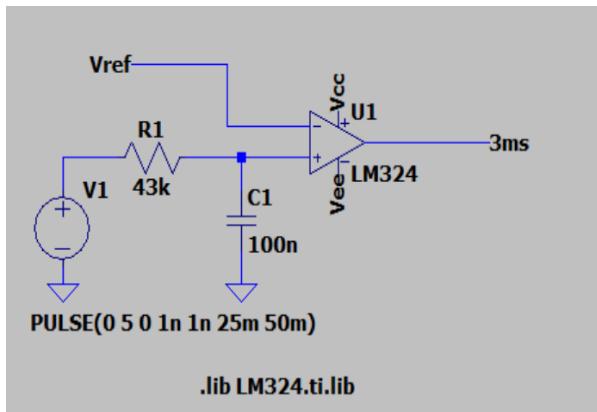


Photo 4: 3ms delay circuit

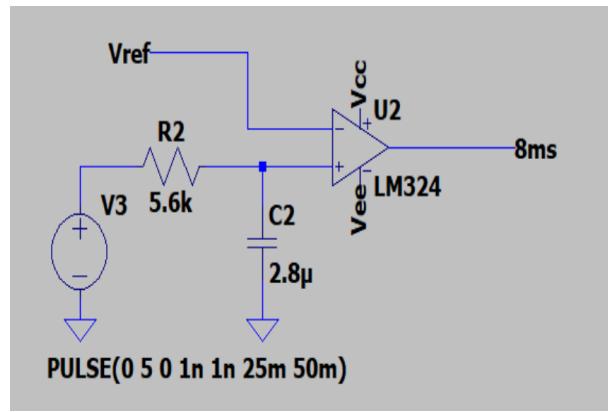


Photo 5: 8ms delay circuit

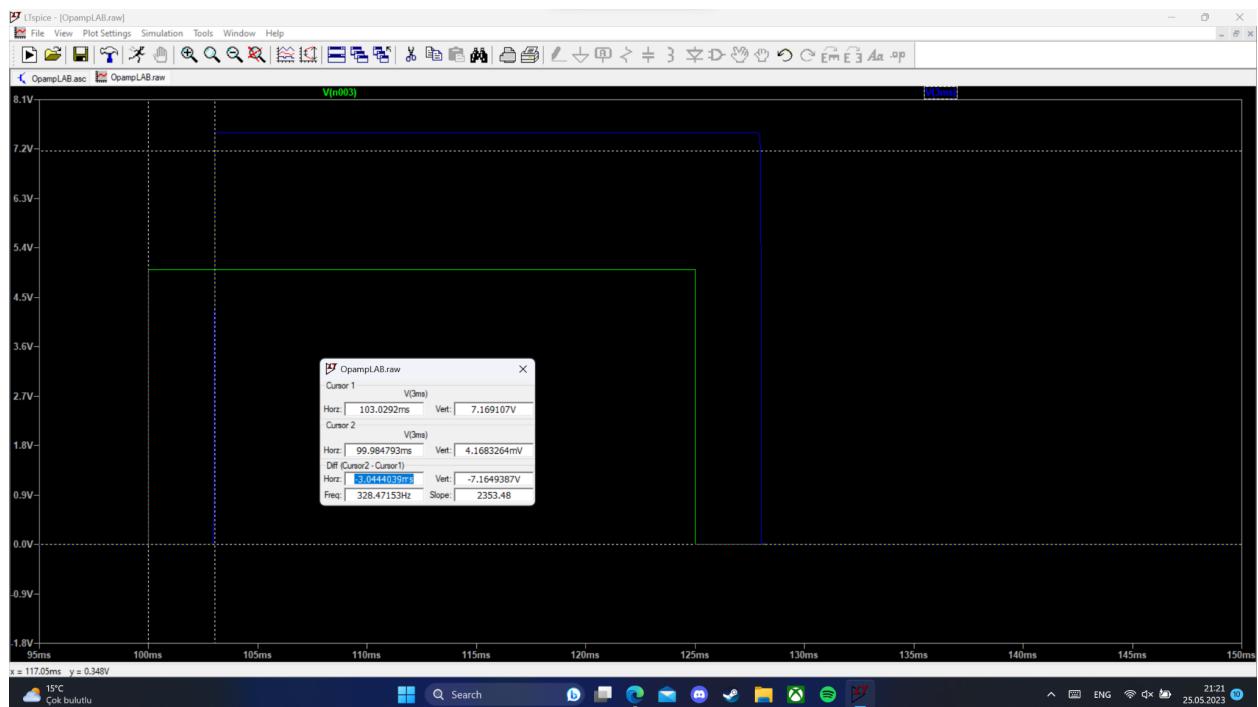


Photo 6: 3ms delay circuit simulation results

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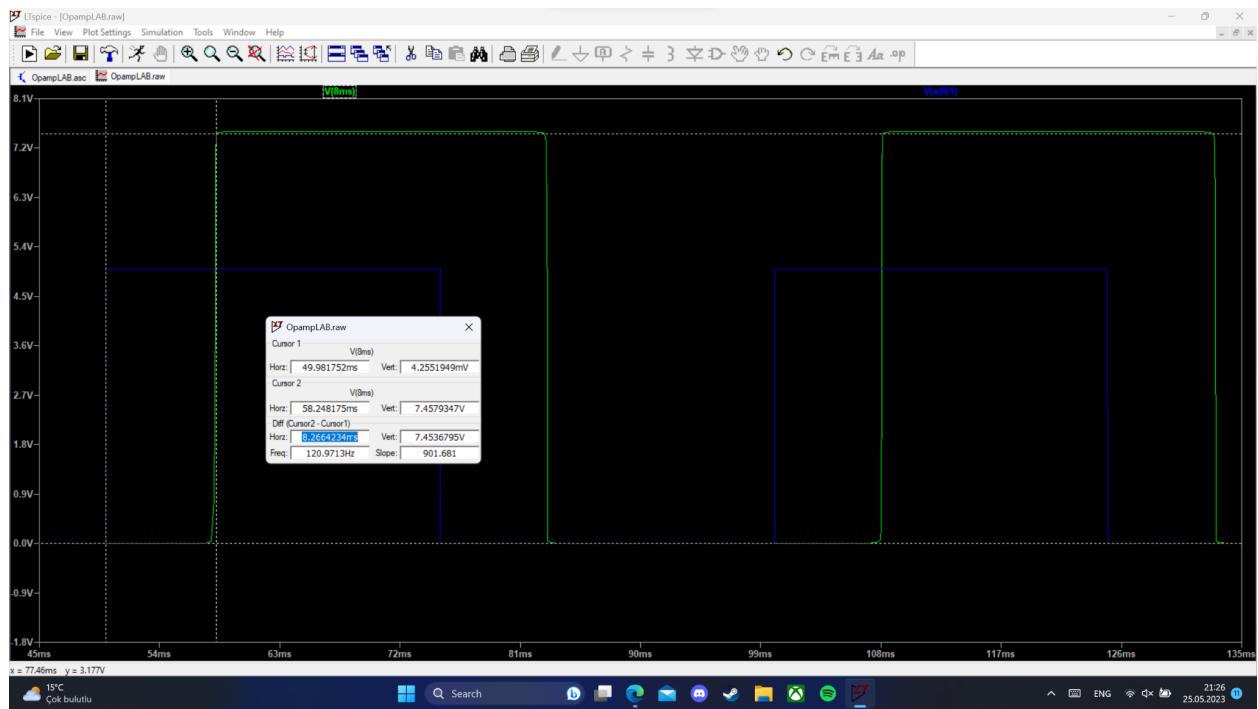


Photo 7: 8ms delay circuit simulation results

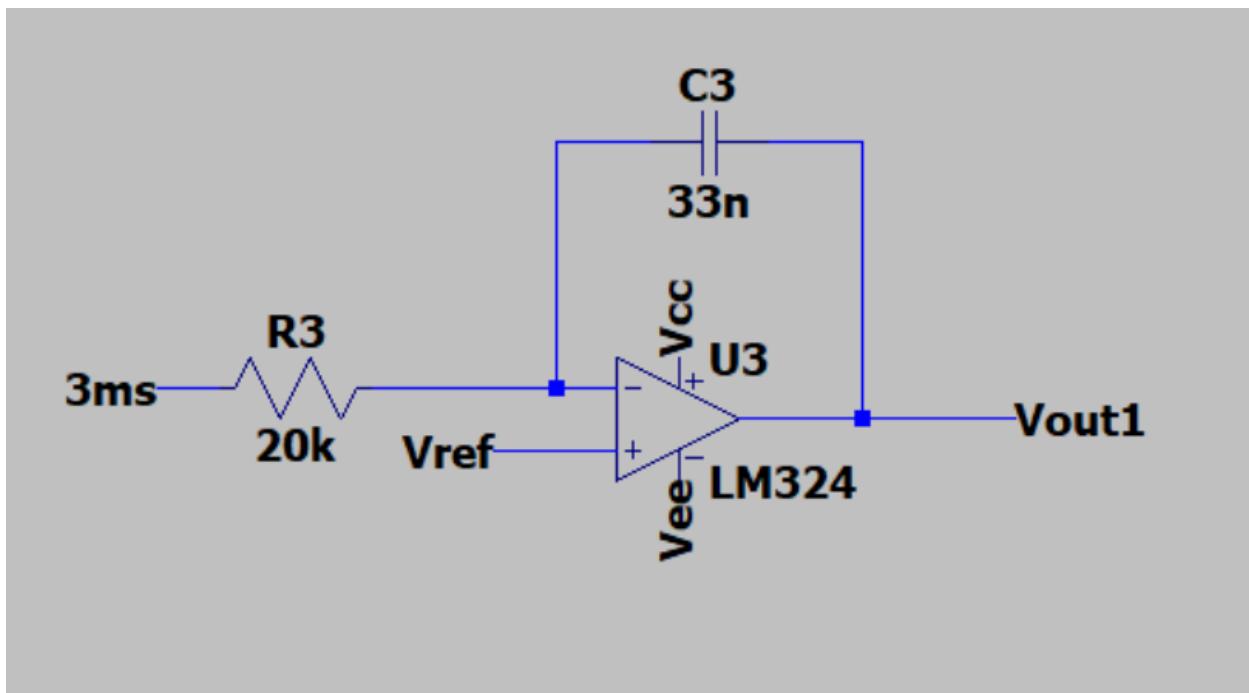


Photo 7: Integrator circuit

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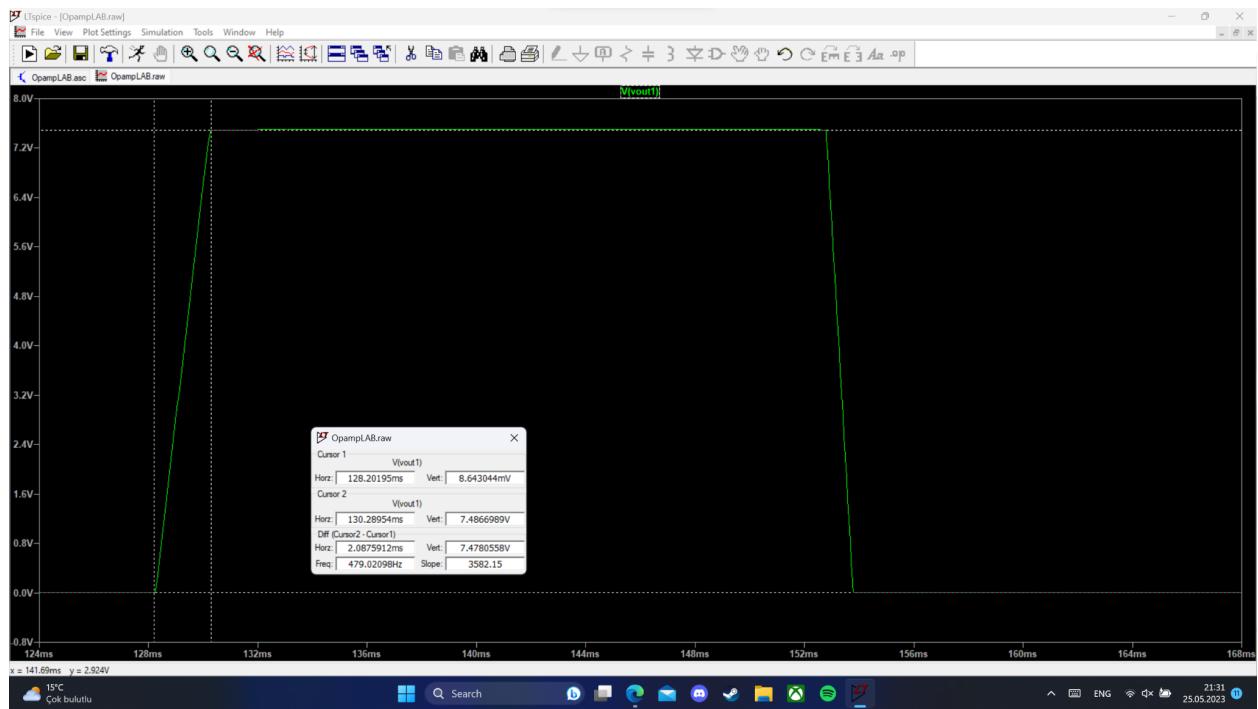


Photo 8: Integrator circuit simulation results

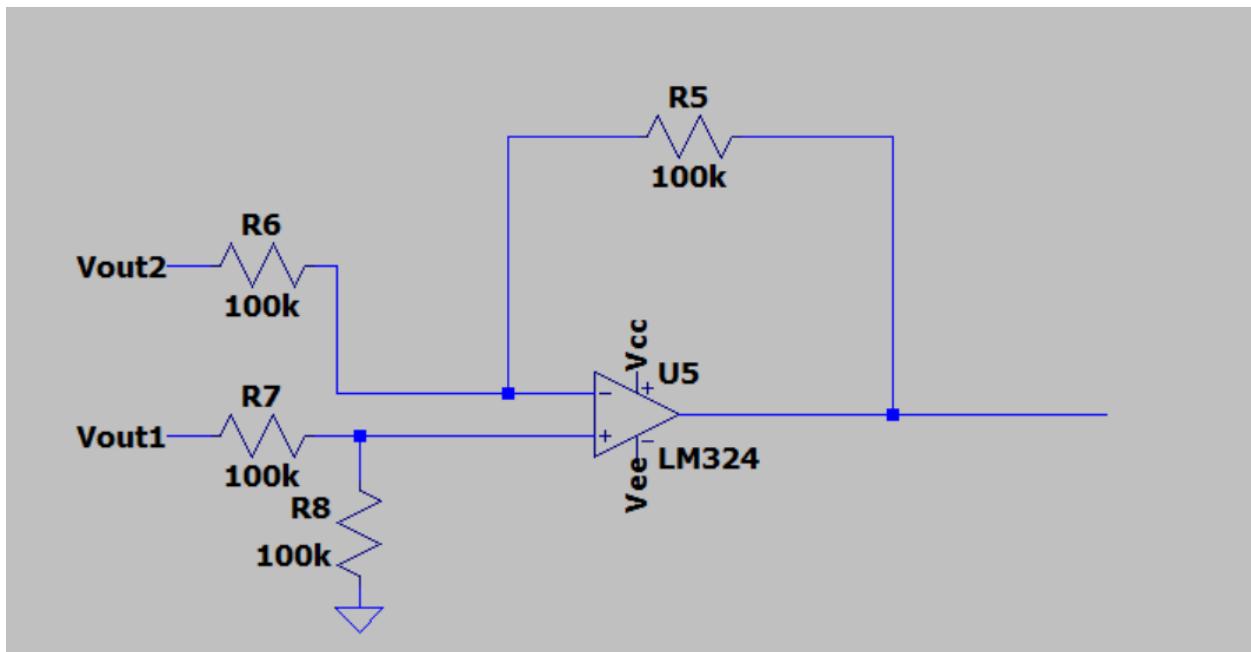


Photo 9: Subtractor circuit

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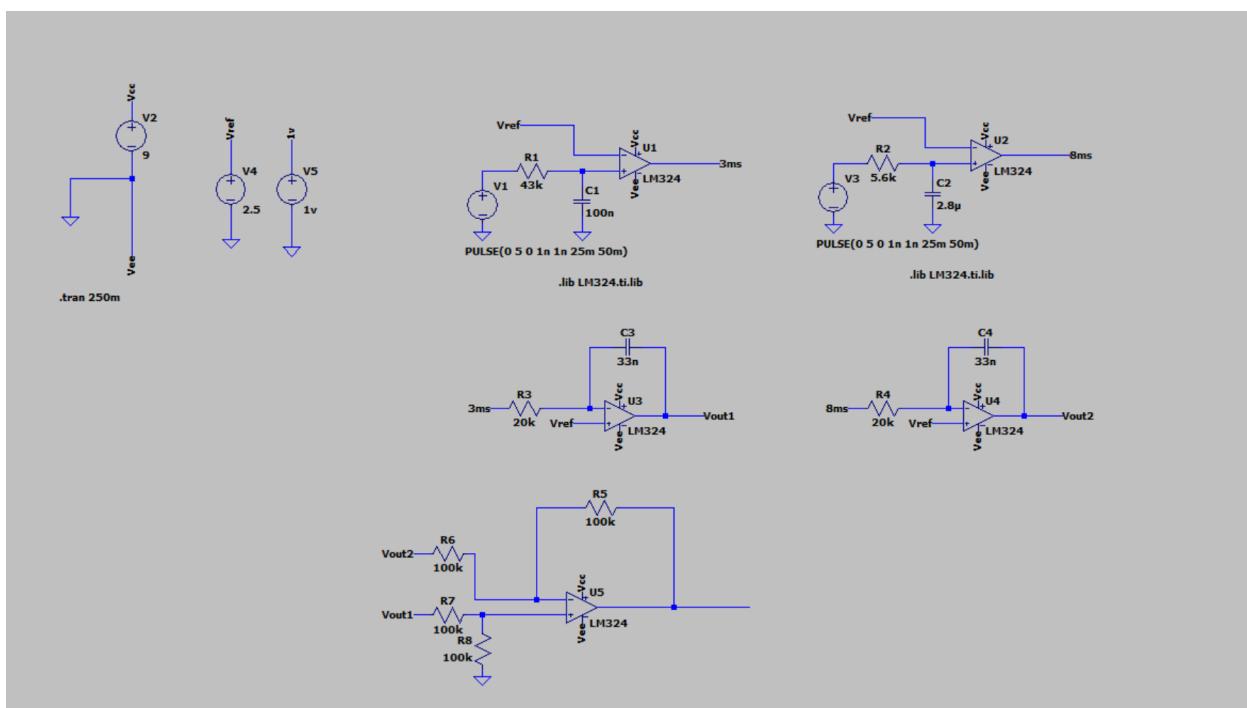


Photo 10: The complete circuit

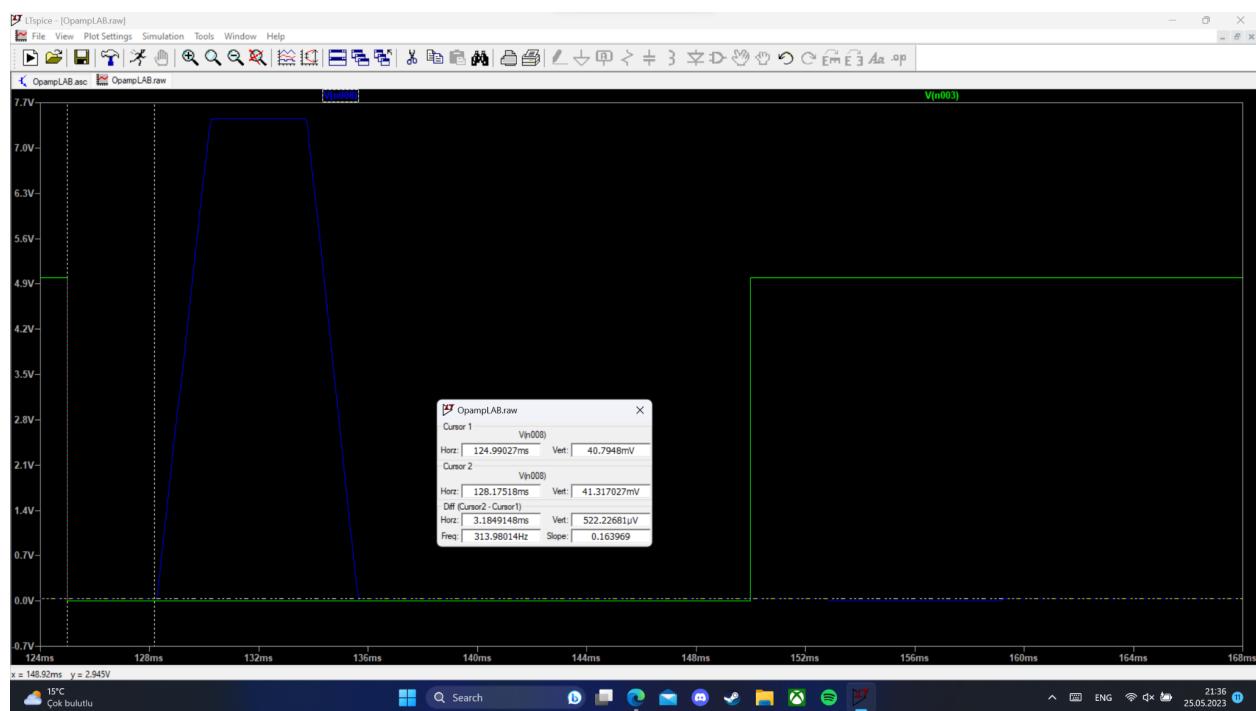


Photo 11: Δt_0 value in simulation

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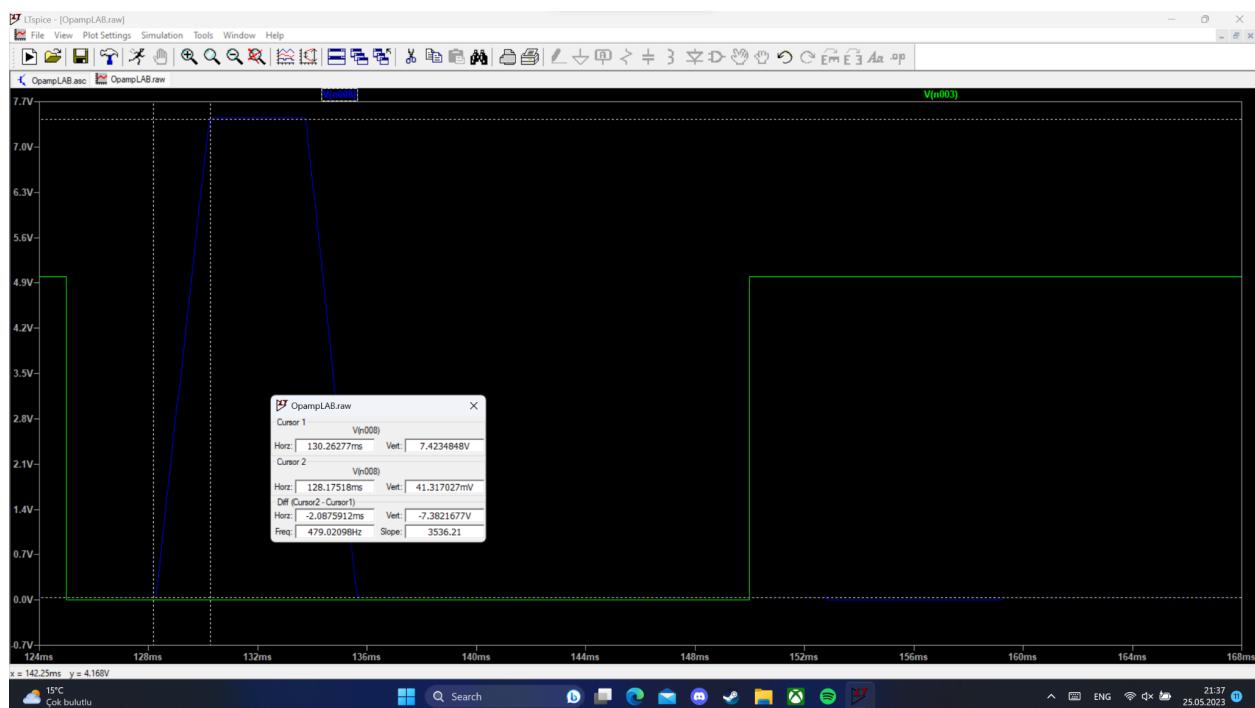


Photo 12: Δt_1 value in simulation₁

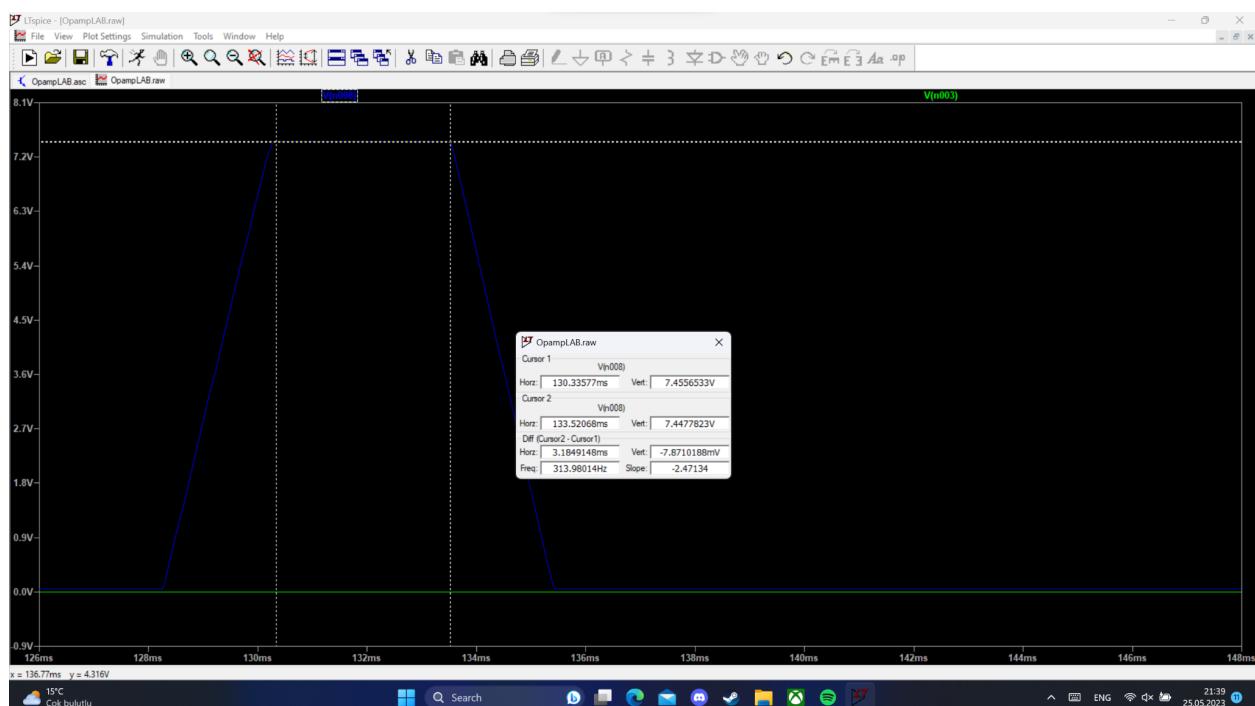
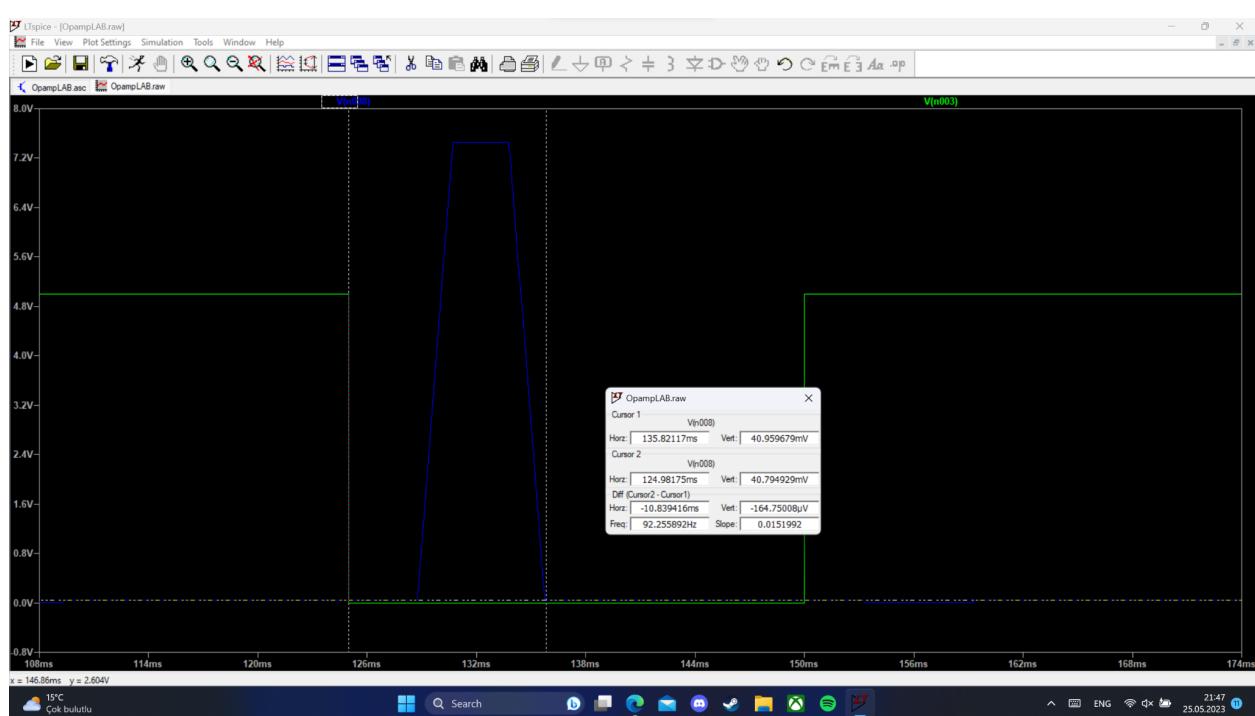
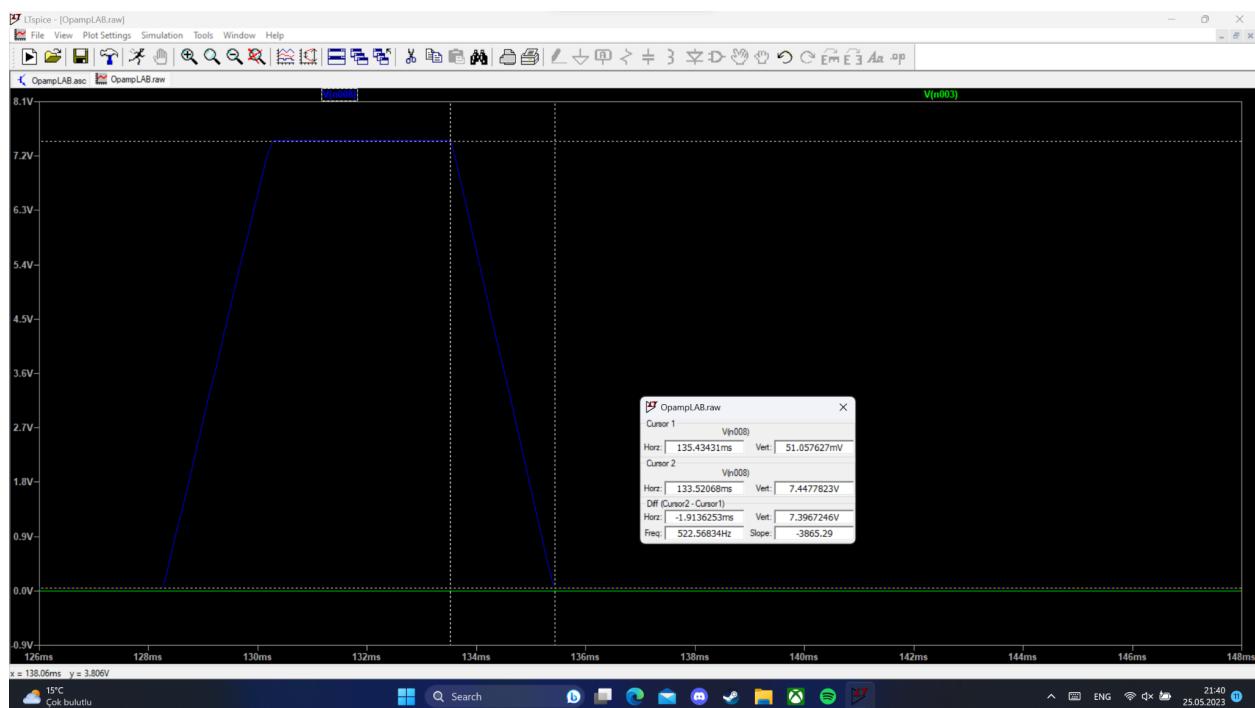


Photo 13: Δt_2 value in simulation₂

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	Expected Value	Simulation Results	% Error
Δt_0	3 ms	3.184 ms	6.13333
Δt_1	2ms	2.088 ms	4.4
Δt_2	3ms	3.184 ms	6.13333
Δt_3	2ms	1.913 ms	4.35
$\Delta t_0 + \Delta t_1 + \Delta t_2 + \Delta t_3$	10 ms	10.839 ms	8.39

Table 1: Errors of the simulation results

All of the errors are in the expected range. The reason for the errors is because values are selected according to the availability in labs and for easier implementation. In the hardware part which helped a lot in terms of applicability

Part 2 Hardware Implementation

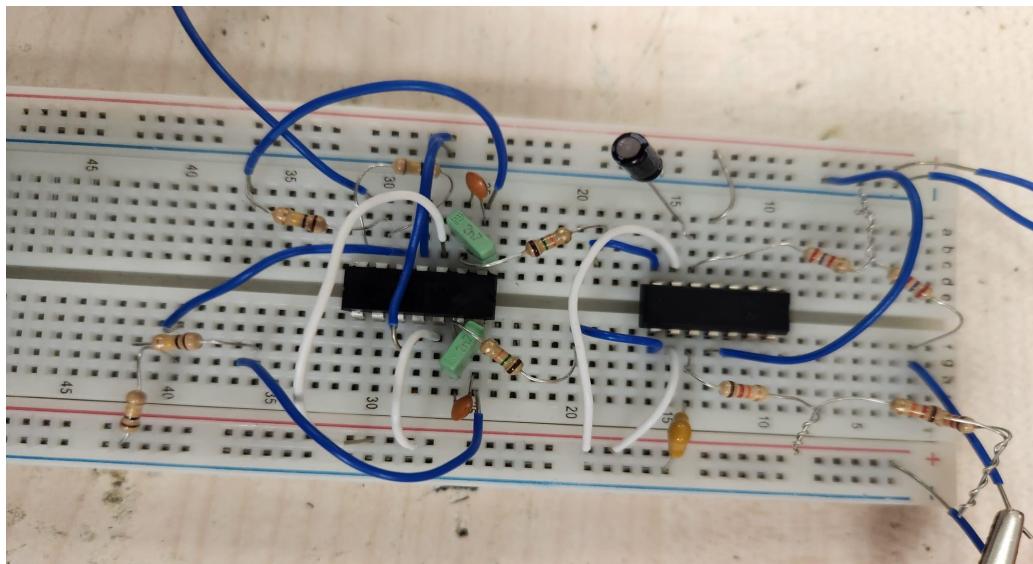


Photo 15: The implemented Circuit

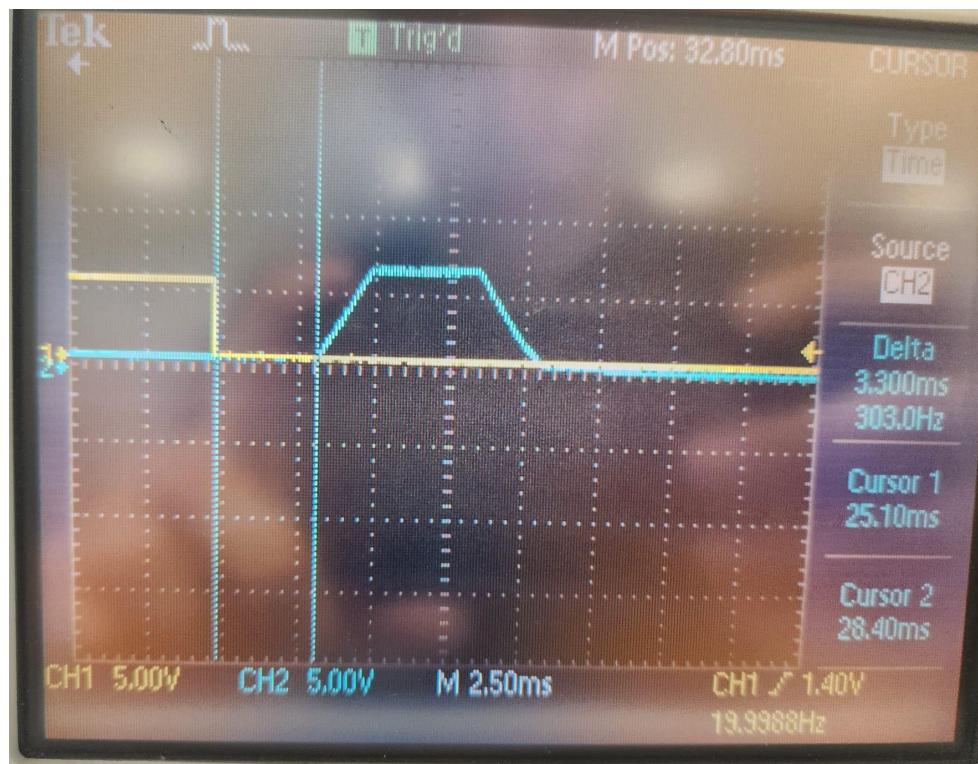


Photo 16: Δt_0 Value in Hardware

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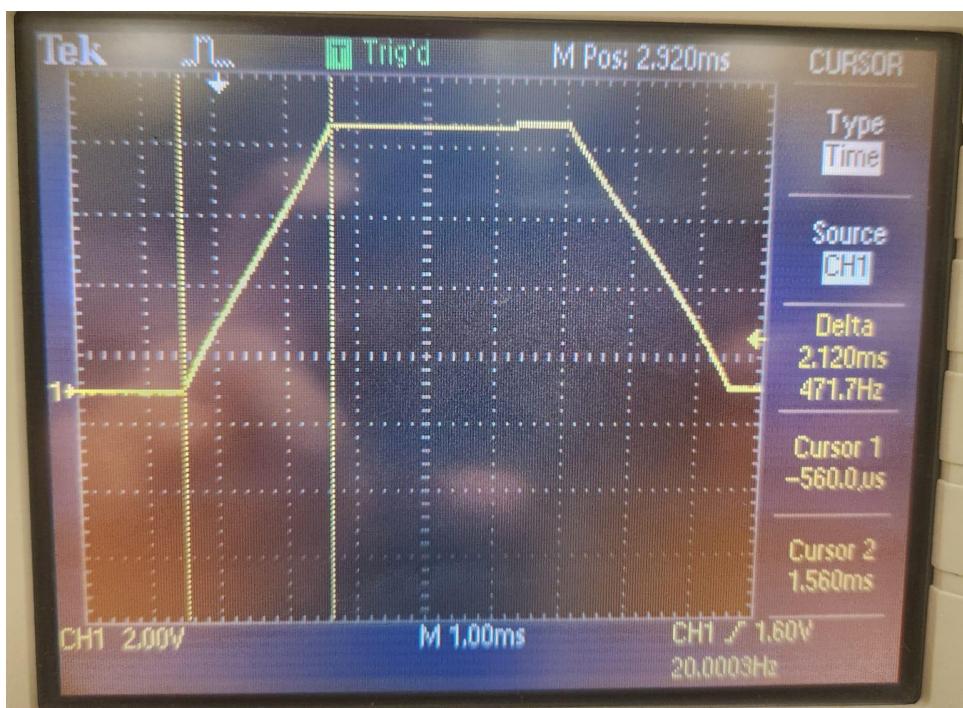


Photo 17: Δt_1 Value in Hardware

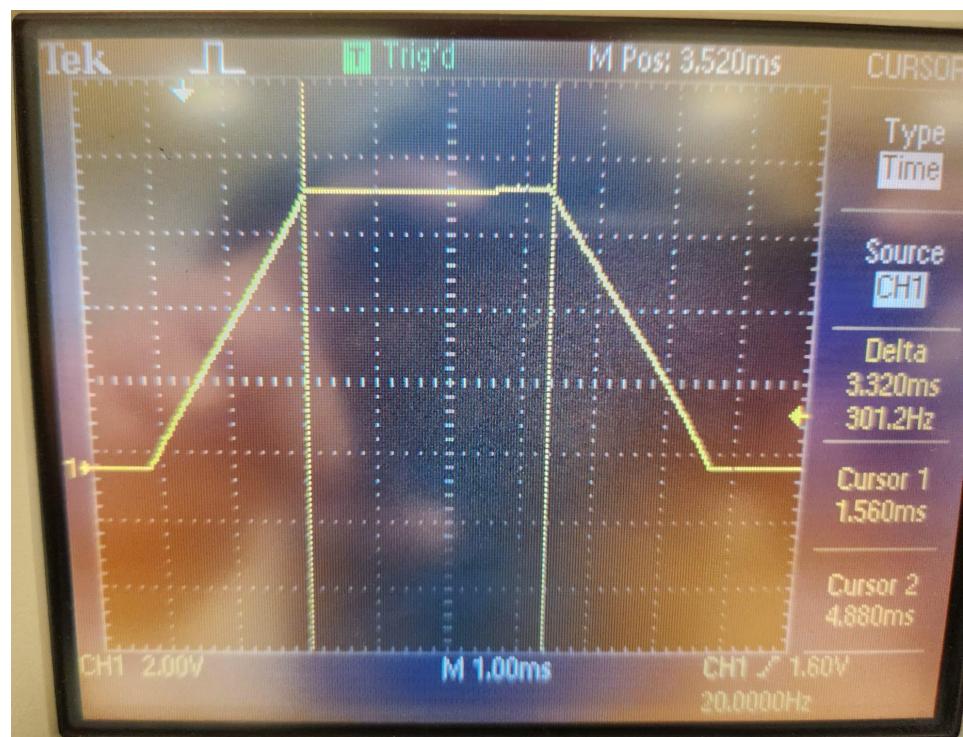


Photo 18: Δt_2 Value in Hardware

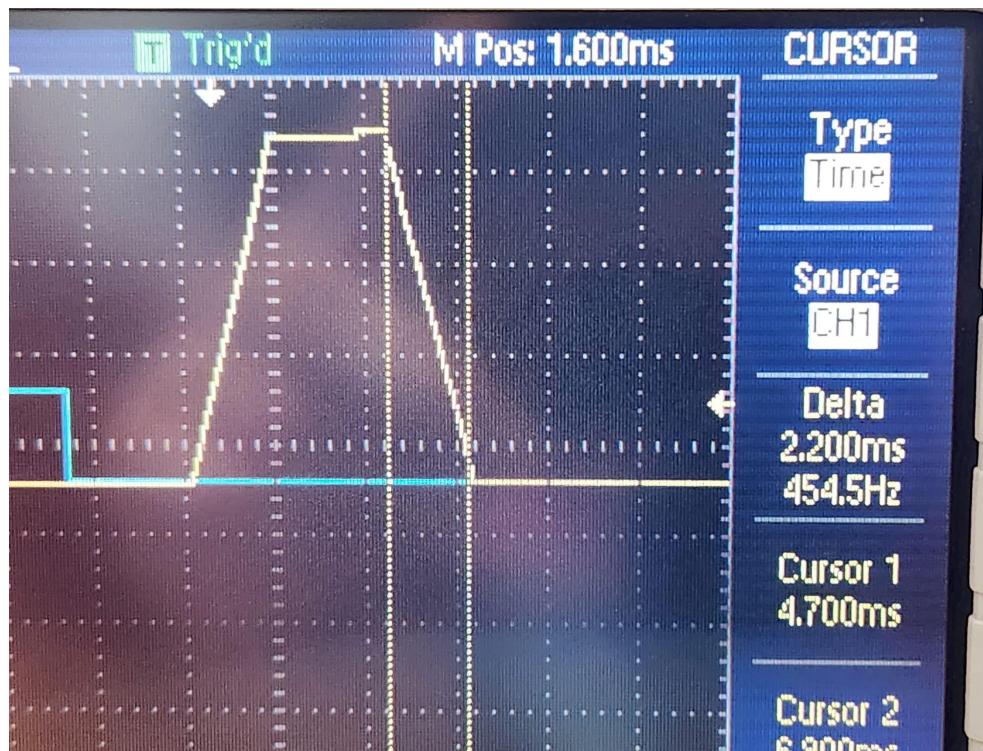


Photo 19: Δt_3 Value in Hardware

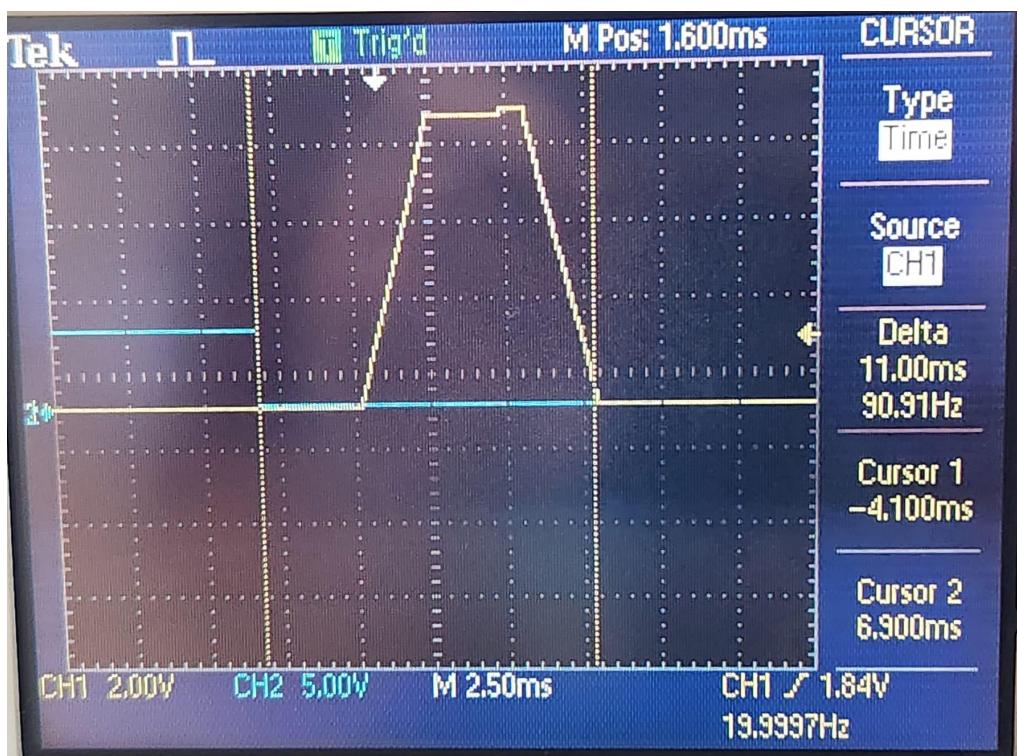


Photo 20: $\Delta t_0 + \Delta t_1 + \Delta t_2 + \Delta t_3$ Value in Hardware

All the parts are implemented on a breadboard. Signal generator used with 2.5 Vpp square wave input and 1.25vpp dc offset in order to offset the minus 2.5V part to 0 V. DC supply used for opamps with 9 volts and 0 volts.

	Expected Value	Hardware Results	% Error from simulation value	% Error from expected value
Δt_0	3 ms	3.3 ms	0.03643	10
Δt_1	2ms	2.120 ms	1.53256	6
Δt_2	3ms	3.320 ms	4.0963	10.666
Δt_3	2ms	2.200 ms	3.63636	10
$\Delta t_0 + \Delta t_1 + \Delta t_2 + \Delta t_3$	10 ms	11 ms	1.4853	10

Table 2: Errors of the hardware results

Conclusion

All of the results in the hardware part came as expected in the simulation part. Both the hardware part and the simulation part follow the calculations made in the analysis part. Not using jumper cables highly decreases the error rate and makes it easier to implement the circuit on the breadboard. The condition of the components and the opamps made insignificant errors which are acceptable. This lab showed how to use opamp in both saturation mode and in linear mode. It was a very useful lab to see how opamps used in order to create desired outputs as seen in creating delay part and manipulate the input wave seen in the integrator part and subtractor part. This lab showed how to use basic RC circuits with the opamps. Not using a breadboard can further improve the results in the hardware part. Implementing 5 different opamp circuit in one breadboard and connecting all of them was the most difficult part of this lab. Since it is hard to manage many components at the same time, and the outputs were impacting other parts outputs, error in only one part damages the whole circuit and results error cumulatively.