High-Voltage and Low-Leakage AlGaN/GaN Tri-Anode Schottky Diodes With Integrated Tri-Gate Transistors

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***Abstract*—We present AlGaN/GaN nanostructured Schottky barrier diodes (SBDs) on silicon substrate with high breakdown voltage (V_{BR}) and low reverse leakage current (I_R), based on a hybrid of tri-anode and tri-gate architectures. The fabricated SBDs presented a small turn-ON voltage (V_{ON}) of 0.76 ± 0.05 V, since the tri-anode architecture formed direct Schottky contact to the 2-D electron gas (2DEG). The reverse characteristic was controlled electrostatically by an embedded tri-gate transistor, instead of relying only on the Schottky barrier. This resulted in low I_R below 10 and 100 nA/mm at large reverse biases up to 500 and 700 V, respectively. In addition, these devices exhibited record V_{BR} up to 1325 V at I_R of 1 μA/mm, rendering an excellent high-power figure-of-merit (FOM) of 939 MW/cm^2 and demonstrating the significant potential of nanostructured GaN SBDs for future efficient power conversion.**

***Index Terms*—GaN, Schottky diode, tri-gate, tri-anode, breakdown, leakage current.**

I. Introduction

WITH the rapid development of GaN power transistors on silicon substrate, GaN lateral SBDs are attracting large attention [1]–[12] since they can be easily and monolithically integrated with such transistors, reducing parasitic inductances, which is highly desirable for future efficient and low-cost power converters. However, conventional AlGaN/GaN lateral SBDs suffer from high V_{ON}, large I_R, and poor V_{BR}. Sophisticated schemes have been proposed to overcome these issues such as recessed anodes [1] and field plates [2]. However, the reverse blocking performance of GaN SBDs, such as V_{BR} and I_R, is still much inferior than in state-of-the-art GaN transistors. These are general limitations of SBDs even in other semiconductors. When defining V_{BR} at a leakage current of 1 μA/mm, GaN-on-silicon transistors have presented values over 1400 V [13], while only a few SBDs with V_{BR} over 500 V have been reported [2], [4], [11], [12], and the highest value up to date is about 900 V [2].

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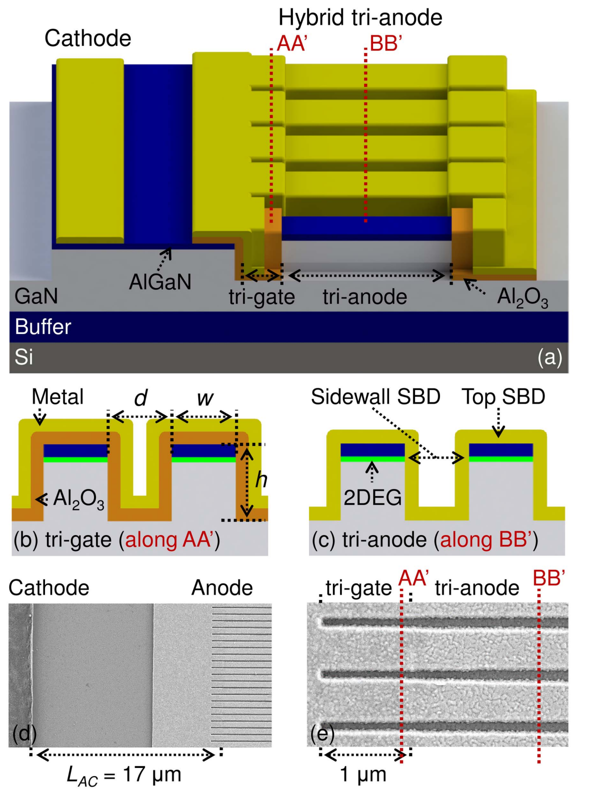

Fig. 1. (a) Schematic of a fabricated tri-anode SBD. Cross-sectional schematics of (b) the tri-gate region along line AA′ and (c) the tri-anode region along line BB′. (d) Top-view SEM image of a fabricated hybrid tri-anode SBD. (e) Zoomed-in SEM image of the tri-gate and tri-anode regions.

Novel nanostructured AlGaN/GaN SBDs based on a hybrid combination of tri-anode and tri-gate architectures have been proposed [14] and investigated in our previous studies [15], [16], which yielded a reduced V_{ON}, an improved ideality factor, a diminished I_R, and an enhanced heat dissipation of the SBDs, at the expense of a larger ON-resistance (R_{ON}) and a smaller current capability. In addition, the potential of this architecture for high-voltage power SBDs has not been presented. In this work, we demonstrate hybrid tri-anode power SBDs with state-of-the-art ON-state and reverse-blocking performances. The fabricated SBDs presented a small V_{ON} of 0.76 ± 0.07 V since tri-anode formed Schottky contact directly to the 2DEG. The integrated tri-gate transistor in the SBD largely improved the reverse

TABLE I

SUMMARY OF TRI-ANODE SBDS WITH DIFFERENT NANOWIRE WIDTHS

	w = 400 nm	w = 200 nm	w = 100 nm
V_{ON} (V, at 1 mA/mm)	0.76 ± 0.07	0.76 ± 0.05	0.73 ± 0.06
R_{ON} (Ω·mm)	10.3 ± 0.4	11.0 ± 0.6	13.1 ± 0.8
I_F (mA/mm, V = 5V)	355 ± 10	332 ± 13	275 ± 13
I_R (nA/mm, V = -10V)	3.03 ± 1.02	0.96 ± 0.81	0.15 ± 0.13

blocking performance of the device. A record V_{BR} of 1325 V (at $I_R = 1\ \mu$A/mm) among GaN lateral diodes on silicon was achieved, along with a high-power FOM of 939 MW/cm^2. The I_R of the SBDs was below 10 and 100 nA/mm at blocking voltages up to 500 and 700 V, respectively, which was more than 2 orders of magnitude smaller than up-to-date high-voltage GaN lateral SBDs.

II. DEVICE FABRICATION

The AlGaN/GaN epitaxy in this work consisted of 3.75 μm of buffer, 0.3 μm of un-doped GaN (u-GaN) channel, 23.5 nm of AlGaN barrier and 2 nm of u-GaN cap layer. A schematic of the hybrid tri-anode SBD is shown in Fig. 1(a). The anode was formed by a combination of a tri-gate transistor and a tri-anode SBD in series (cross-sectional schematics are shown in Fig. 1(b) and (c)). The device fabrication started with e-beam lithography to define the mesa and nanowires, which were then etched by Cl_2-based inductively coupled plasma and followed by ohmic metal deposition and rapid thermal annealing. The height (h) of the nanowires was 166 nm, and the width (w) varied from 100 to 1000 nm while the spacing (d) was fixed at 200 nm. Then 20 nm of Al_2O_3 was deposited by atomic layer deposition and selectively removed in tri-anode region. Finally the entire anode was formed by Ni/Au, which was later used as the mask for wet-etching of the Al_2O_3 in access and ohmic regions. Figure 1(d) and (e) show the top-view SEM images of the SBD and the hybrid tri-anode, respectively. The device characteristics such as R_{ON}, forward current (I_F) and I_R were normalized by device width (60 μm). The error bars presented in all results were determined from measurements on up to 10 separate devices of the same kind.

III. RESULTS AND DISCUSSION

The impact of w on the R_{ON} and I_R of the tri-anode SBDs is presented in Fig. 2(a). The observed reduction of R_{ON} with w increasing from 100 to 400 nm is mainly attributed to the increasing filling factor ($FF = w/(w + d)$), which preserved more 2DEG in the tri-gate region and hence reduced the resistance of the integrated tri-gate transistors. After w reached 400 nm (FF = 66.7%), the R_{ON} saturated regardless of the increasing w, or equivalently the FF, at about 10.2 ± 0.45 Ω·mm, and the I_R, taken at $V = -10$ V, kept reducing with decreasing w due to the enhanced gate depletion of the integrated tri-gate transistor with narrower nanowires.

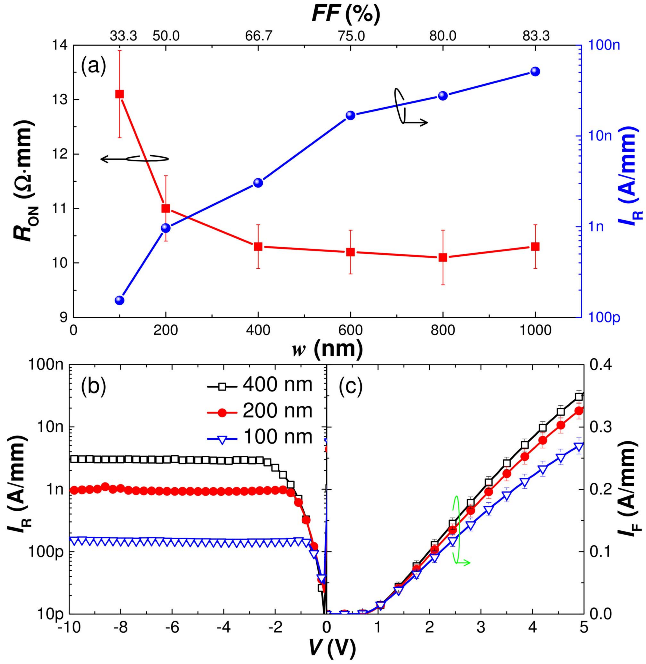

Fig. 2. (a) R_{ON} and I_R (at –10 V) of tri-anode SBDs with different w. (b) Reverse and (c) forward I-V characteristics of the tri-anode SBDs with w of 400, 200 and 100 nm, normalized by device width of 60 μm.

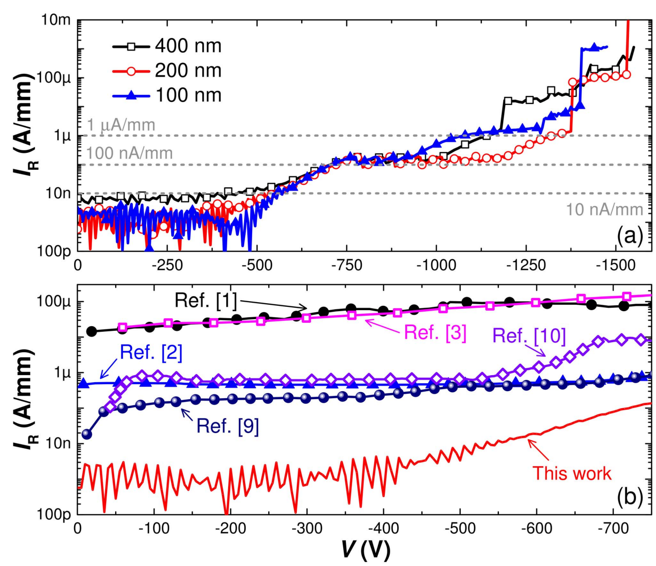

Fig. 3. (a) Reverse-bias characteristics of the tri-anode SBDs versus anode bias for different w and (b) comparison of I_R of the tri-anode SBD (w = 200 nm) and state-of-the-art high-voltage GaN lateral SBDs on silicon. The I_R for SBDs with w of 200 and 100 nm was likely around or below the measurement limit of our setup.

With w below 400 nm, the I_R of all tri-anode SBDs was below 10 nA/mm at a bias of -10 V, and a w of 400 nm yielded a good balance between I_R and R_{ON}. The I_R and I_F of the tri-anode SBDs with w of 400, 200 and 100 nm are plotted in Fig. 2(b) and (c) versus anode voltage (V), respectively, with their detailed characteristics listed in Tab. I. The tri-anode SBDs with w of 100 nm exhibited I_R of 0.15 ± 0.13 nA/mm, which is, to the best of our knowledge, the smallest leakage current for GaN lateral SBDs up to date.

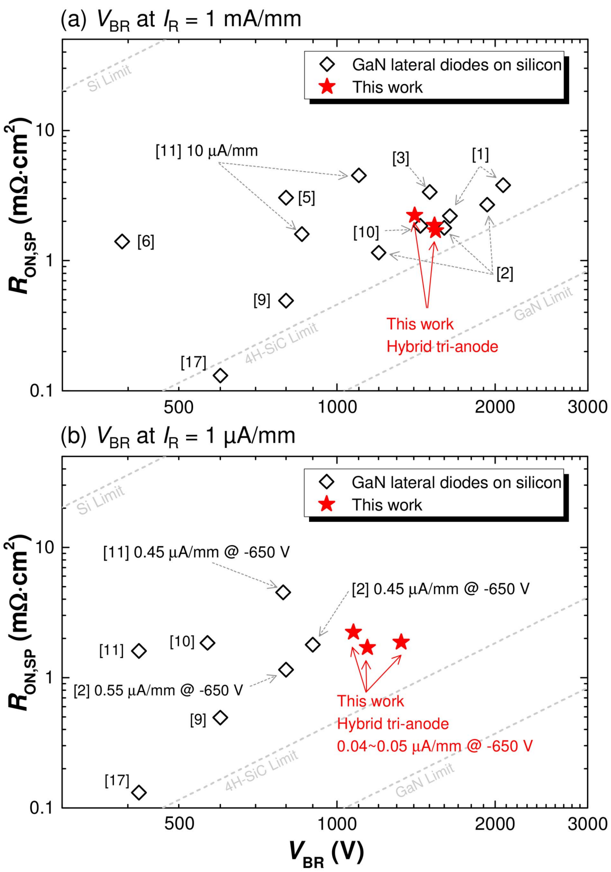

Fig. 4. Specific R_{ON} ($R_{ON,SP}$) versus V_{BR} benchmarks of the tri-anode SBDs with state-of-the-art GaN lateral power diodes by defining V_{BR} at I_R = 1 mA/mm (a) and 1 μA/mm (b). For fair comparison, lieterature results with unspecified $R_{ON,SP}$ or I_R were not included.

Figure 3(a) presents the I_R of the tri-anode SBDs versus V. All devices exhibited very small I_R below 10 and 100 nA/mm with V up to about 500 and 700 V, respectively. For V below 400 V, the I_R of the tri-anode SBDs with w of 200 and 100 nm was close or below the measurement limit of our setup, hence large oscillations in current were observed. The best V_{BR} measured at $I_R = 1$ μA/mm was 1140, 1325 and 1075 V for the tri-anode SBDs with w of 400, 200 and 100 nm. We have not observed a clear dependence of the V_{BR} on w in this work, and the difference in V_{BR} was likely impacted by local variations in oxide quality or possible fabrication misalignments. Nevertheless, the I_R profile was quite consistent up to 900 V among all devices with w from 100 to 400 nm, as well as their hard breakdown voltage at around 1400 - 1550 V.

The reverse leakage current of the tri-anode SBDs (w = 200 nm) was much lower than that from state-of-the-art high-voltage GaN-on-silicon lateral SBDs (with hard breakdown voltage beyond 1000 V) in the literature, as plotted in Fig. 3(b). For reverse voltages below 500 V, the I_R of the tri-anode SBD was about 2 orders of magnitude lower with respect to the smallest I_R [9] among these references and over 4 orders of magnitude as compared to the reference SBD with the highest reported hard V_{BR} [1]. Most of the references presented I_R beyond 100 nA/mm and 1 μA/mm at V of -100 and -650 V, respectively. In contrast, the I_R of the tri-anode SBD did not reach 100 nA/mm until -725 V and was as small as 41 nA/mm at -650 V. Such significant reduction in I_R can potentially improve the reliability of the device, and more importantly, reduce the OFF-state power dissipation and increase the efficiency of power converters. The OFF-state power dissipation, calculated using $Power = I_R \times V$, varied from 0.31 - 78 mW/mm at -650 V for the reference SBDs, while that of the tri-anode SBD was several orders of magnitude smaller, below 0.03 mW/mm.

The tri-anode SBDs presented in Fig. 3 were benchmarked against state-of-the-art GaN lateral diodes on silicon substrate, as shown in Fig. 4. Two commonly used definitions of V_{BR} for GaN power devices were adopted, taken at $I_R = 1$ mA/mm and 1 μA/mm. In the benchmark considering V_{BR} at $I_R = 1$ mA/mm (Fig. 4(a)), the tri-anode SBDs with w of 400, 200 and 100 nm exhibited high-power FOMs of 1355, 1255 and 865 MW/cm^2, respectively, which are comparable to the best results for GaN lateral diodes on silicon and even other substrates [4], [18], [19]. Since 1 mA/mm is a large leakage current level to define the V_{BR} for power devices, 1 μA/mm level is becoming more commonly used to compare more fairly the blocking performance of power devices. Figure 4(b) shows the benchmark with V_{BR} at $I_R = 1$ μA/mm. The V_{BR} for all reference devices was re-calculated based on the reported data, following the definition of V_{BR} at $I_R = 1$ μA/mm. The tri-anode SBDs with w of 400, 200 and 100 nm presented FOM values of 747, 939 and 518 MW/cm^2. These are high FOM values with record V_{BR} among up-to-date GaN lateral power diodes on silicon, which in addition to the low turn-ON voltage, low I_R and small ON-resistance, reveal the extraordinary potential of nanowire-based approaches for GaN power electronics.

IV. Conclusion

In this letter we demonstrated high voltage and low leakage AlGaN/GaN tri-anode SBDs with integrated tri-gate transistors. The SBDs exhibited a small V_{ON} of 0.76 $\pm$ 0.05 V due to the tri-anode structure. The embedded tri-gate transistor enabled electrostatic control over the leakage current in addition to the Schottky barrier, leading to ultra-low I_R below 100 nA/mm at reverse bias of 700 V, and high V_{BR} up to 1325 V (1 μA/mm). These results confirm the superb potential of the hybrid tri-anode SBDs for future high-efficiency power conversion systems, and offer a technology platform to improve the reverse blocking in lateral SBDs even in other materials.

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