Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance

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***Abstract*—This paper presents a comprehensive study on the influences of parasitic elements on the MOSFET switching performance. A circuit-level analytical model that takes MOSFET parasitic capacitances and inductances, circuit stray inductances, and reverse current of the freewheeling diode into consideration is given to evaluate the MOSFET switching characteristics. The equations derived for emulating MOSFET switching transients are assessed graphically, which, compared to results obtained merely from simulation or parametric study, can offer better insight into where the changes in switching performance lie when the parasitic elements are varied. The analysis has been successfully substantiated by the experimental results of a 400 V, 6 A test bench. A discussion on the physical meanings behind these parasitic effect phenomena is included. Knowledge about the effects of parasitic elements on the switching behavior serves as an important basis for the design guidelines of fast switching power converters.**

***Index Terms*—MOSFET, parasitic elements, switching characteristics.**

I. Introduction

An increase in switching frequency has always been in great request to push up the power density and facilitate the miniaturization of switching converters. Power MOSFETs have found the most extensive application in high-frequency power converters [1]. However, increasing switching frequency is also increasingly inflicted with higher switching loss that can considerably compromise the power efficiency. In addition, with a dramatic increase in switching speed, parasitic inductances that mainly result from current sensing transformer, PCB traces, and device packages may severely oscillate with parasitic capacitances of the MOSFET, and will induce excessive voltage and current stresses on the switch. The effect of these parasitic elements can be detrimental in that it can precipitate the failures of the switching devices and degrade the EMI and reliability performance of the converters. These problems come as the penalties high-frequency power converters will be subject to, and turn out to be the major hurdles ahead of the real application of high-frequency technology. With ever faster switching speed, parasitic elements of the MOSFET can exert more and more profound impact on their switching performance. Negligence of these parasitic elements can no longer stand up to scrutiny.

Investigation into the effect of parasitic elements on the switching performance can be classified into two categories. One is to study directly through experimental switching waveforms under the influence of parasitic elements [2]–[4]. This method is very intuitional, however, it only demonstrates what are observed, whose validity largely depend on the accuracy of the measurement system, and do not provide detailed explanations on the mechanism behind those observations. The other is to make use of the MOSFET model to evaluate the impact of parasitic elements [4]–[11]. As discussed in [12], there are three typical models: physics-based model, behavioral model, and analytical model. Subsequently, the simulation methods of exploring the effect of parasitic elements can be further divided into three subcategories. Technology computer aided design (TCAD) mixed-mode simulation utilizes physics-based model of the MOSFET under boundary conditions in combination with behavioral model of external circuit components to model the MOSFET switching transients and calculate the switching losses [5], [6]. This method excels in the accurate prediction of the effect of diode reverse recovery characteristics and package interactions because it is directly based on the actual physical models. However, for the same reason, it is often very time consuming and intractable. As a result, they are more likely to be used by process engineers for device development and optimization. Others are devoted to the extraction and characterization of parasitic parameters of transformer and PCB traces in an existent circuit by using ANSOFT or Maxwell Q3D. Based on the values obtained from parameter extraction, the effect of parasitic elements is analyzed by PSpice or Saber simulation in which behavioral model of the MOSFET is used [4], [7]. However, as the experimental method, it still cannot suffice to explain the physical meaning behind those observations. Additionally, in [7], the source inductance is lumped into the stray inductance in the power circuit, while actually they play different roles in the circuit, as the source inductance also forms part of the gate drive circuit. Switching characteristics

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of the MOSFET is modeled analytically to assess the effect of parasitic elements in [8]–[11]. Emphasis has, nonetheless, only been placed on the stray and source inductances; besides, current stress induced by the reverse current of the freewheeling diode is not taken into account. Extensive research has been conducted to develop an analytical model of the MOSFET in [12]–[17]. They may either be too complicated to directly exhibit the effect of the parasitic elements in the expressions [12]–[14], or neglect certain important parasitic elements such as source inductance and drain inductance of the MOSFET [15]–[17].

The objective of this paper is to carry out a comprehensive investigation into the effect of parasitic elements on the MOSFET switching performance. A detailed model of the MOSFET-diode configuration switching an inductive load current considering all important parasitic elements as well as the interaction between gate drive stage and power stage will be derived. The turn-on and turn-off transients of the MOSFET are divided into five stages respectively, when different operating conditions and constraints apply. A sequence of closed-form equations will be derived which contains information pertinent to the effect of the parasitic element on the MOSFET. Accordingly, the analytical switching waveforms under the influence of the parasitic elements will be illustrated to visualize their effects. The analytical study will further be verified by comparison with parametric study of a 400 V, 6 A test bench in terms of switching loss and device stresses. Underlying reasons for these parasitic effects will be explained to enhance the conclusions acquired from analytical and parametric studies. Based on the conclusions obtained, brief guidelines on switching device selection and circuit design will be given.

II. Analysis of the Switching Characteristics of the MOSFET

In this section, the switching process of the MOSFET will be studied stage by stage. A typical testing circuit switching a clamped inductive load is adopted for the modeling of MOSFET switching characteristics. The equivalent circuit model considering all the crucial parasitic elements is shown in Fig. 1. The input is a constant voltage source $V_{\rm DD}$, and the output is modeled as a constant current source $I_{\rm DD}$. The gate signal is assumed to flip between 0 and $V_{\rm GG}$ with zero rise time and fall time in the analysis. It is known that the predicted waveforms will have a shorter switching time than in reality due to this assumption; however, it will not affect drawing conclusion on the effect of the parasitic elements. As a result, the effect of the gate drive characteristics is neglected in this study. Parasitic elements of the MOSFET that are considered are gate–source capacitance $C_{\rm gs}$, gate–drain capacitance $C_{\rm gd}$, drain–source capacitance $C_{\rm ds}$, source inductance L_{s1}, and drain inductance L_{d1}. The internal gate drive resistance $R_{g\_{\rm int}}$ (which is usually around 1 Ω for high-frequency power MOSFETs) is merged into the external gate drive resistance $R_{g\_{\rm ext}}$ to form the gate drive resistance $R_g = R_{g\_{\rm int}} + R_{g\_{\rm ext}}$ as they are connected in series and play the same role in the circuit. All stray inductances in the power loop and external to the MOSFET are lumped and represented by L_{s2} and L_{d2}, which are at the source and drain terminals of the MOSFET, respectively. $L_s = L_{s1} + L_{s2}$ and $L_d = L_{d1} + L_{d2}$ are denoted as the total inductances at the source and drain terminals of the MOSFET, respectively. The gate inductance L_g is neglected in the analysis. Although it can introduce delay, it is the effect of L_s that dominates when the voltage and current of the MOSFET change, for L_s has the much faster drain current flowing through it. In addition, the value of L_g is usually not specified in a datasheet as L_{s1} and L_{d1}, and many circuit design guidelines suggest that the gate drive circuit should be placed as close to the switch as possible to minimize the potential oscillation introduced by L_g [18]. The effect of L_g will later be examined by experiment. $C_{\rm iss} = C_{\rm gs} + C_{\rm gd}$ and $C_{\rm oss} = C_{\rm ds} + C_{\rm gd}$ are denoted as the input and output capacitances of the MOSFET, respectively. It should be noted that the capacitances are functions of transistor parameters and sizing, especially $C_{\rm gd}$ and $C_{\rm ds}$, whose variation with the applied voltage can be modeled by $C(v) = C_0/(1 + v/K)^{\gamma}$ [12], where K and γ can be extracted from the capacitance versus voltage curve and C_0 is the capacitance value when $v = 0$. However, for simplicity, a common practice of expressing them as two discrete values [15] is adopted. In this way, the nonlinear characteristics of these parasitic capacitances are linearized and the channel conditions of the MOSFET are listed in Table I. The freewheeling diode is modeled by a diode considering only the reverse recovery characteristics in parallel with its parasitic capacitance C_f and then in series with its parasitic resistance R_f. The parasitic inductance of the diode can also be lumped into the stray inductance L_d. Fig. 2(a) and (b) illustrates the qualitative turn-on and turn-off switching waveforms, which will be thoroughly examined in the following.

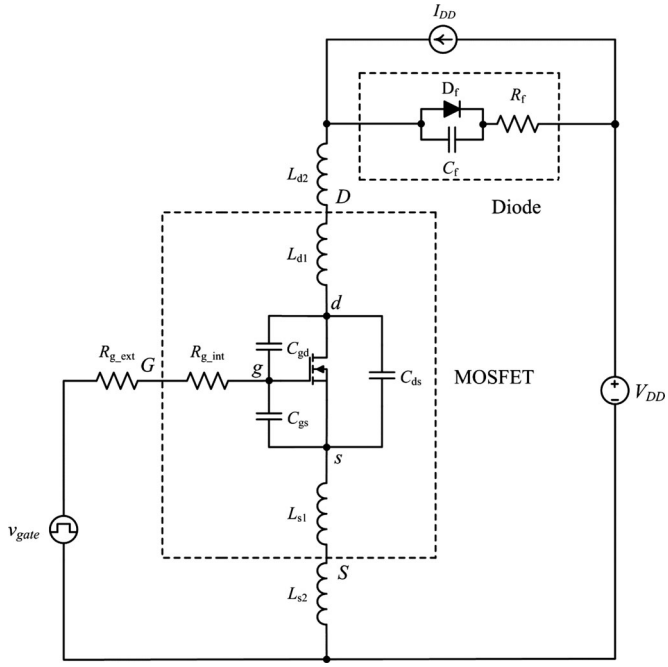

Fig. 1. Equivalent model of the testing circuit.

TABLE I
SPECIFICATION ON THE OPERATING MODE OF THE MOSFET

	$v_{gs} > V_{th}$ and $v_{ds} \le v_{gs} - V_{th}$	$v_{gs} > V_{th}$ and $v_{ds} > v_{gs} - V_{th}$	$v_{gs} < V_{th}$
Operating region	ohmic	saturation	cutoff
C_{gs}	C_{gs}	C_{gs}	C_{gs}
C_{gd}	C_{gd2}	C_{gd1}	C_{gd1}
C_{ds}	C_{ds2}	C_{ds1}	C_{ds1}
Channel condition	constant resistance $R_{ds(on)}$	voltage-controlled current source with constant g_{fs}	open circuit

Remark: $C_{gd1} << C_{gd2}$ and $C_{ds1} << C_{ds2}$.

A. Turn-on Switching Transients (Stage 1–Stage 5)

Stage 1 [$t_0 - t_1$] turn-on delay time: When the gate signal $V_{\rm GG}$ is applied through R_g, $C_{\rm iss}$ is charged up. The MOSFET will not leave the cutoff region until the gate–source voltage $v_{\rm gs}$ reaches the threshold voltage $V_{\rm th}$; thus, the load current still circulates through the diode. Since this stage does not affect the drain current, the effect of L_s can be neglected. $v_{\rm gs}$ is given by

$$v_{\rm gs}(t) = V_{\rm GG}[1 - e^{-(t-t_0)/\tau_{\rm iss}}] \tag{1}$$

where $\tau_{\rm iss} = R_g(C_{\rm gs} + C_{\rm gd})$ and $C_{\rm gd} = C_{\rm gd1}$.

Stage 2 [$t_1 - t_2$] current rise time: In this stage, $v_{\rm gs}$ goes beyond $V_{\rm th}$ and the drain current i_d starts to increase from zero to its peak value $I_{d\_\rm peak}$, which is larger than the load current $I_{\rm DD}$ and is contributed by the reverse current of the freewheeling diode. The drain–source voltage $v_{\rm ds}$ simultaneously decreases by $v_{Ls\_\rm on} + v_{Ld\_\rm on}$, which is the voltage drop induced by the rising drain current across the inductances L_s ($v_{Ls\_\rm on}$) and L_d ($v_{Ld\_\rm on}$). This voltage drop $v_{Ls\_\rm on} + v_{Ld\_\rm on}$ deserves special attention, as it determines whether $v_{\rm ds}$ will drop to $v_{\rm gs} - V_{\rm th}$ before or after i_d rises to its full value $I_{\rm DD}$. As $v_{\rm ds} = v_{\rm gs} - V_{\rm th}$ is the boundary condition for the MOSFET to switch into the ohmic region, it can further determine the operating mode of the MOSFET in this and the following stages. If the stray inductances and the slew rate of i_d are both small, or the load is light, the increase in i_d may precede the decrease in $v_{\rm ds}$, otherwise $v_{\rm ds}$ may decrease to $v_{\rm gs} - V_{\rm th}$ before there is any significant increase in i_d. Both of them are described as follows.

Case I: The MOSFET works in the saturation region. i_d is governed by

$$i_d(t) = g_{fs}[v_{\rm gs}(t) - V_{\rm th}] \tag{2}$$

where g_{fs} is transconductance of the MOSFET.

It is acknowledged that this equation is originally given to describe the relationship between the channel current and gate–source voltage. However, the almost constant voltage drop in v_{ds} during this stage allows the assumption that the current through the parasitic output capacitances $C_{\rm ds}$ and $C_{\rm gd}$ is negligible com-

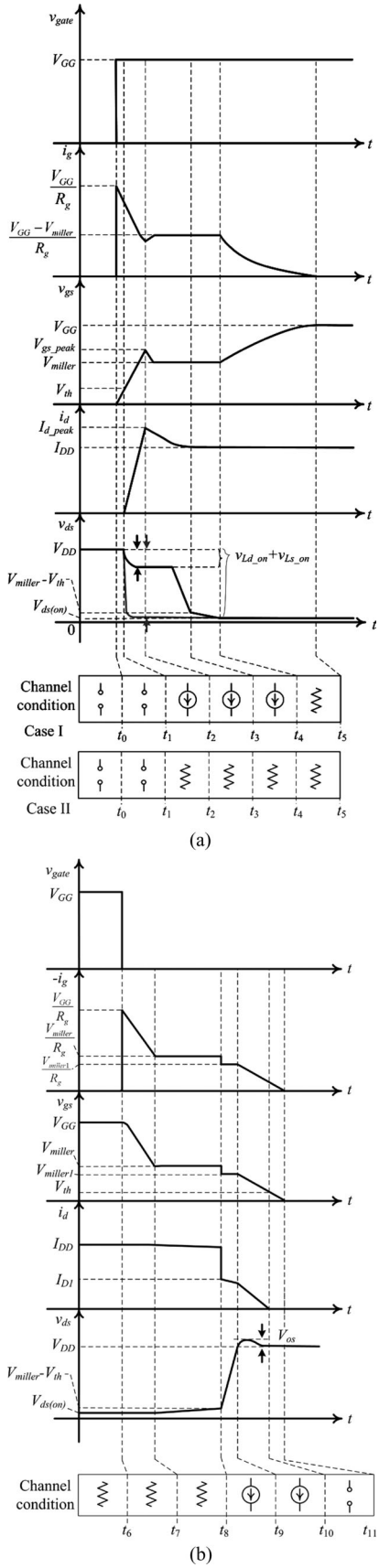

Fig. 2. Qualitative switching waveforms with ten stages. (a) Turn-on. (b) Turn-off.

pared to the drain current. As a result, (2) can be used in this stage to represent the drain current.

During this period, the circuit equations can be expressed as

$$R_g i_g(t) = V_{\rm GG} - v_{\rm gs}(t) - L_s \frac{di_d}{dt} \tag{3}$$

$$i_g(t) = C_{\rm gs}\frac{dv_{\rm gs}(t)}{dt} + C_{\rm gd}\frac{dv_{\rm gd}(t)}{dt} \tag{4}$$

$$v_{\rm gs}(t) = v_{\rm gd}(t) + v_{\rm ds}(t) \tag{5}$$

$$v_{\rm ds}(t) = V_{\rm DD} - (L_s + L_d)\frac{di_d}{dt}. \tag{6}$$

By performing the Laplace transformation of (2)–(6), $v_{\rm gs}(s)$ is given by

$$v_{\rm gs}(s) = \frac{V_{\rm GG}(s)}{\tau_m^2 s^2 + \tau_n s + 1} \tag{7}$$

where $\tau_m^2 = R_g C_{\rm gd} g_{fs}(L_s + L_d)$, $\tau_n = R_g(C_{\rm gd} + C_{\rm gs}) + g_{fs}L_s$, and $C_{\rm gd} = C_{\rm gd1}$.

By inverse transforming (7), there are two possible cases as described in the following:

Case I.A (overdamped condition): When $\tau_n^2 > 4\tau_m^2$

$$v_{\rm gs}(t) = V_{\rm GG} - \frac{V_{\rm GG} - V_{\rm th}}{\tau_a - \tau_b}\left[\tau_a e^{-(t-t_1)/\tau_a} - \tau_b e^{-(t-t_1)/\tau_b}\right] \tag{8}$$

$$i_d(t) = g_{fs}(V_{\rm GG} - V_{\rm th}) \left\{1 - \frac{1}{\tau_a - \tau_b}\left[\tau_a e^{-(t-t_1)/\tau_a} - \tau_b e^{-(t-t_1)/\tau_b}\right]\right\} \tag{9}$$

$$\frac{di_d}{dt} = \frac{g_{fs}(V_{\rm GG} - V_{\rm th})}{\tau_a - \tau_b}\left[e^{-(t-t_1)/\tau_a} - e^{-(t-t_1)/\tau_b}\right] \tag{10}$$

where $\tau_a = (\tau_n + \sqrt{\tau_n^2 - 4\tau_m^2})/2$, $\tau_b = (\tau_n - \sqrt{\tau_n^2 - 4\tau_m^2})/2$.

Case I.B (underdamped condition): When $\tau_n^2 < 4\tau_m^2$

$$v_{\rm gs}(t) = V_{\rm GG} - (V_{\rm GG} - V_{\rm th})e^{-(t-t_1)/\tau_c} \times \left(\frac{\tau_d}{\tau_c}\sin\frac{t-t_1}{\tau_d} + \cos\frac{t-t_1}{\tau_d}\right) \tag{11}$$

$$i_d(t) = g_{fs}(V_{\rm GG} - V_{\rm th}) \times \left[1 - e^{-(t-t_1)/\tau_c}\left(\frac{\tau_d}{\tau_c}\sin\frac{t-t_1}{\tau_d} + \cos\frac{t-t_1}{\tau_d}\right)\right] \tag{12}$$

$$\frac{di_d}{dt} = g_{fs}(V_{\rm GG} - V_{\rm th})e^{-(t-t_1)/\tau_c}\left(\frac{\tau_d}{\tau_c^2} + \frac{1}{\tau_d}\right)\sin\frac{t-t_1}{\tau_d} \tag{13}$$

where $\tau_c = 2\tau_m^2/\tau_n$, $\tau_d = 2\tau_m^2/\sqrt{4\tau_m^2 - \tau_n^2}$.

$v_{\rm ds}$ is given by

$$v_{\rm ds}(t) = V_{\rm DD} - (v_{Ls\_{\rm on}} + v_{Ld\_{\rm on}}) = V_{\rm DD} - (L_s + L_d)\frac{di_d}{dt} \tag{14}$$

where di_d/dt is given by (10) for Case I.A, or (13) for Case I.B.

Case II: The MOSFET works in ohmic region. The drain current will increase at a rate that is dependent on the stray inductances instead of the gate–source voltage. Assume that $v_{\rm ds}$ is much smaller than $V_{\rm DD}$ and can be neglected. With $V_{\rm DD}$ entirely dropping on L_s and L_d, the drain current will rise at a constant rate

$$\frac{di_d}{dt} = \frac{V_{\rm DD}}{L_s + L_d}. \tag{15}$$

Hence, L_s can be deemed as a constant voltage source $V_{Ls} = L_s V_{\rm DD}/(L_s + L_d)$, which is independent of the gate–source voltage.

As long as $V_{Ls} < V_{\rm GG}$ and $i_g > 0$, i.e., $L_s/(L_s + L_d) < V_{\rm GG}/V_{\rm DD}$, i_d can be approximated by

$$i_d(t) = \frac{V_{\rm DD}}{L_s + L_d}(t - t_1). \tag{16}$$

In real application, the three cases are usually defined by the value of L_d. Case I.A features the smallest L_d with Case I.B and Case II followed in sequence. For example, it will take $L_d = 500$ nH for the testing conditions shown later in this paper to enter Case I.B. The drain current in both Cases I.A and I.B has exponential profile. Case I.A shows faster current slew rate than Case I.B and is more likely to appear in a well-designed high-frequency converters. Since Case II only occurs when the stray inductance is extremely large and is most unlikely to appear in a well-designed high-frequency converter, it will not be discussed in the following.

Once i_d reaches $I_{\rm DD}$, the diode current will reverse its polarity and start the reverse recovery process. Even if silicon carbide (SiC) diode features nonreverse recovery charge, its junction capacitance will also introduce reverse current. The reverse recovery time $t_{\rm rr}$ is divided into two parts $t_{\rm rr\_1}$ and $t_{\rm rr\_2}$, when i_f rises from 0 to $I_{\rm rr\_max}$ and then returns to 0, respectively. Recalling the analysis of reverse recovery phenomenon of the diode, which will be given in the Appendix, $t_{\rm rr}$ and the maximum reverse current $I_{\rm rr\_max}$ are

$$t_{\rm rr} = \sqrt{\frac{2Q_{\rm rr}(S+1)}{di_d/dt|_{i_d = I_{\rm DD}}}} \tag{17}$$

$$I_{\rm rr\_max} = \sqrt{\frac{2Q_{\rm rr}di_d/dt|_{i_d = I_{\rm DD}}}{S+1}} \tag{18}$$

where $Q_{\rm rr}$ is the reverse recovery charge, S is the snappiness factor and $di_d/dt|_{i_d = I_{\rm DD}}$ is the current slew rate of i_d at $i_d = I_{\rm DD}$, which can be obtained from (10) and (13), depending on which case the MOSFET works in.

Accordingly, the current slew rate of the diode during $t_{\rm rr\_2}$, di_{f_2}/dt, which is to be used in the next stage can be determined

$$\frac{di_{f\_2}}{dt} = \frac{1}{S}\frac{di_d}{dt}|_{i_d = I_{\rm DD}}. \tag{19}$$

The peak value of the drain current $I_{d\_\rm peak}$ is given by

$$I_{d\_\rm peak} = I_{\rm DD} + I_{\rm rr\_max}. \tag{20}$$

At t_2, i_f reaches its reverse peak $I_{\rm rr\_max}$, and i_d reaches its maximum value correspondingly. If the MOSFET works in the saturation region, $v_{\rm gs}$ will go higher than $V_{\rm miller}$, as the increase in i_d is reflected to the gate drive stage. $V_{\rm gs\_peak}$ that is

corresponding to I_{d_peak} can be given by

$$V_{\mathrm{gs\_peak}} = \frac{I_{d\_\mathrm{peak}}}{g_{fs}} + V_{\mathrm{th}}. \tag{21}$$

Stage 3 [$t_2 - t_3$] voltage falling time I: In this stage, the diode current i_f returns to zero from $I_{\mathrm{rr\_max}}$ and begins to block voltage, therefore v_{ds} will resume decrease in the saturation region until it reaches the boundary voltage V_{miller}.

Since v_{ds} decreases rapidly in this stage, the current flowing through C_{oss} of the MOSFET and C_f can no longer be disregarded. The slew rate of the diode current di_{f_2}/dt has been deducted in the previous stage, based on its relationship with the slew rate of the drain current

$$\frac{di_d}{dt} = -\frac{di_{f\_2}}{dt} = -\frac{1}{s}\frac{di_d}{dt}|_{i_d = I_{\mathrm{DD}}} \tag{22}$$

$$i_d = i_{\mathrm{ch}} + i_c \tag{23}$$

$$i_c = (C_{\mathrm{oss}} + C_f)\frac{dv_{\mathrm{ds}}}{dt} \tag{24}$$

$$v_{\mathrm{gs}}(t) = \frac{i_{\mathrm{ch}}}{g_{fs}} + V_{\mathrm{th}} = V_{\mathrm{gs\_peak}} + \frac{1}{g_{fs}}\left[\frac{di_d}{dt}(t - t_2) - (C_{\mathrm{oss}} + C_f)\frac{dv_{\mathrm{ds}}}{dt}\right]. \tag{25}$$

By putting (22)–(25) into (2)–(5), the voltage slew rate can be found out, as shown in (26) at the bottom of the page.

Notably, the time that v_{ds} falls to V_{miller} does not necessarily coincide with the time i_d returns to I_{DD}. The sequence depends on the specific switching speed. If the decrease in i_d finishes first, it will stay constant at I_{DD}, and v_{ds} will continue to fall to V_{miller} according to

$$\frac{dv_{\mathrm{ds}}}{dt} = -\frac{V_{\mathrm{GG}} - V_{\mathrm{miller}}}{R_g C_{\mathrm{gd}}} \tag{27}$$

where $V_{\mathrm{miller}} = I_{\mathrm{DD}}/g_{fs} + V_{\mathrm{th}}$ and $C_{\mathrm{gd}} = C_{\mathrm{gd1}}$.

If the decrease in v_{ds} finishes first, the MOSFET will switch to the next stage. Normally, the former is the situation in reality. Thus, this case will be considered for the following analysis.

Stage 4 [$t_3 - t_4$] voltage falling time II: Once v_{ds} reaches the boundary V_{miller}, the MOSFET will go into the ohmic region. L_d stays constant at $v_{\mathrm{gs}} = V_{\mathrm{miller}}$. dv_{ds}/dt can be given by (27) with $C_{\mathrm{gd}} = C_{\mathrm{gd2}}$. At the end of this stage, v_{ds} will arrive at its on-state value $V_{\mathrm{ds(on)}}$.

Stage 5 [$t_4 - t_5$] on-state operation: Once v_{ds} reaches $V_{\mathrm{ds(on)}}$, it remains at $V_{\mathrm{ds(on)}}$ and i_d keeps constant at I_{DD}, no longer controlled by v_{gs}. v_{gs} continues to charge up and will reach V_{GG} at t_5.

B. Turn-off Switching Transients (Stage 6–Stage 10)

Stage 6 [$t_6 - t_7$] turn-off delay time: The gate signal is set to zero and the MOSFET operates in the ohmic region. v_{ds} will not increase until v_{gs} reduces to V_{miller}. C_{iss} is being discharged through R_g and L_s. Since i_d remains unchanged, the effect of L_s can be neglected. v_{gs} is given by

$$v_{\mathrm{gs}}(t) = V_{\mathrm{GG}}\, e^{-(t - t_6)/\tau_{\mathrm{iss}}} \tag{28}$$

where $\tau_{\mathrm{iss}} = R_g(C_{\mathrm{gs}} + C_{\mathrm{gd}})$ and $C_{\mathrm{gd}} = C_{\mathrm{gd2}}$.

Stage 7 [$t_7 - t_8$] voltage rise time I: Stages 7 and 8 are the rise time of v_{ds}. In this stage, the MOSFET still works in ohmic region and $C_{\mathrm{gd}} = C_{\mathrm{gd2}}$, hence v_{ds} increases with the smaller slope. Ideally i_d stays constant at I_{DD} and v_{gs} remains at its Miller voltage. This allows both L_s and the small current required to charge up C_{gd} and C_{ds} to be neglected. As the gate voltage steps down to zero during the turn-off transients, the following relationships can be given

$$i_g = \frac{v_{\mathrm{gs}}}{R_g} \tag{29}$$

$$\frac{dv_{\mathrm{ds}}}{dt} = \frac{i_g}{C_{\mathrm{gd}}} = \frac{v_{\mathrm{gs}}}{R_g C_{\mathrm{gd}}} \tag{30}$$

where $C_{\mathrm{gd}} = C_{\mathrm{gd2}}$ and $v_{\mathrm{gs}} = V_{\mathrm{miller}}$.

At t_8, v_{ds} rises to V_{miller} and the MOSFET begins operating in the saturation region.

Stage 8 [$t_8 - t_9$] voltage rise time II : The MOSFET works in the saturation region in this stage, when v_{ds} continues to rise until it reaches V_{DD}. The drain current remains constant, so there is a plateau region in v_{gs} which is also constant. As C_{gd} changes to the smaller value C_{gd1}, the voltage slew rate is much larger than in the previous stage. Similar to its turn-on counterpart (stage 3), as the voltages across C_{oss} and C_f change simultaneously, the current flowing through them should also be taken into consideration. The channel current in this plateau region I_{CH} is thereby given as

$$I_{\mathrm{CH}} = I_{\mathrm{DD}} - (C_f + C_{\mathrm{oss}})\frac{V_{\mathrm{th}} + I_{\mathrm{CH}}/g_{fs}}{R_g C_{\mathrm{gd1}}}. \tag{31}$$

Rearranging it, I_{CH} under this condition can be derived as

$$I_{\mathrm{CH}} = I_{\mathrm{DD}} - \frac{(C_f + C_{\mathrm{oss}})(I_{\mathrm{DD}} + V_{\mathrm{th}} g_{fs})}{g_{fs} R_g C_{\mathrm{gd1}} + (C_f + C_{\mathrm{oss}})}. \tag{32}$$

The drain current in the plateau region I_{D1} should include the current flowing through the output capacitance as

$$I_{D1} = I_{\mathrm{DD}} - \frac{C_f(I_{\mathrm{DD}} + V_{\mathrm{th}} g_{fs})}{g_{fs} R_g C_{\mathrm{gd1}} + (C_f + C_{\mathrm{oss}})}. \tag{33}$$

Equation (30) can still be applied here to calculate the voltage slew rate with $C_{\mathrm{gd}} = C_{\mathrm{gd1}}$ and

$$v_{\mathrm{gs}} = V_{\mathrm{miller1}} = \frac{I_{\mathrm{CH}}}{g_{fs}} + V_{\mathrm{th}}. \tag{34}$$

Likewise, the drain current can be given by (23) and (24).

Stage 9 [$t_9 - t_{10}$] current falling time: After the diode ceases blocking the voltage at t_9, the current begins to divert from the

$$\frac{dv_{\mathrm{ds}}}{dt} = -\frac{V_{\mathrm{GG}} - V_{\mathrm{gs\_peak}} + \{L_s + [R_g(C_{\mathrm{gs}} + C_{\mathrm{gd1}}) + (t - t_2)]/g_{fs}\}(1/S)(di_d/dt)|_{i_d = I_{\mathrm{DD}}}}{R_g C_{\mathrm{gd1}} + (C_{\mathrm{oss}} + C_f)/g_{fs}}. \tag{26}$$

MOSFET to the diode. This stage will extend until the drain current becomes zero and $v_{\rm gs}$ reaches $V_{\rm th}$. The same analytical method and parameters defined in stage 3 at the turn-on transients can be used here, the results can be found in the Appendix. Since the diode stops blocking voltage, $v_{\rm ds}$ can be calculated by (14). As the decreasing drain current will induce a voltage drop across the parasitic inductances, which will incur an extra stress on the MOSFET, a voltage overshoot $V_{\rm os}$ is expected to appear in $v_{\rm ds}$. Its value can be predicted by finding out the maximum value of $v_{\rm ds}$ according to (14).

Stage 10 [$t_{10}-t_{11}$] off-state operation: After the load current flows entirely through the diode, $v_{\rm gs}$ reduces from $V_{\rm th}$ to zero and the MOSFET operates in the cutoff region. Eventually, the voltage overshoot in the power stage is damped by the stray resistance $R_{\rm stray}$ of the circuit. No current flows through the MOSFET channel; however, as $v_{\rm ds}$ still changes, there will be a consequential current in $C_{\rm oss}$, which affects the drain current. $v_{\rm ds}$ and i_d can be deducted as

$$v_{\rm ds}(t) = V_{\rm DD} + V_{\rm os}e^{-\alpha(t-t_{10})}\cos[\omega(t-t_{10})] \tag{35}$$

$$i_d(t) = C_{\rm oss}\frac{dv_{\rm ds}}{dt} = -C_{\rm oss}V_{\rm os}e^{-\alpha(t-t_{10})} \times\{\omega\sin[\omega(t-t_{10})+\alpha\cos[\omega(t-t_{10})]\} \tag{36}$$

where $\alpha = R_{\rm stray}/2(L_s+L_d)$ and $\omega = \sqrt{1/[C_{\rm oss}(L_s+L_d)]-\alpha^2}$.

It can be seen from the aforementioned analysis that the turn-off switching transients are a reversely symmetrical process of the turn-on switching transients. Now that the equations for $v_{\rm ds}$ and i_d have been determined stage by stage, the switching loss can be calculated by integrating them in a complete switching transient as

$$P_{\rm sw} = f\int v_{\rm ds}i_d dt. \tag{37}$$

The switching trajectories of the MOSFET without and with consideration of the effect of the parasitic elements are compared in Fig. 3. It reveals that parasitic elements can significantly influence the device stresses and switching loss, which is the area enclosed by the curves.

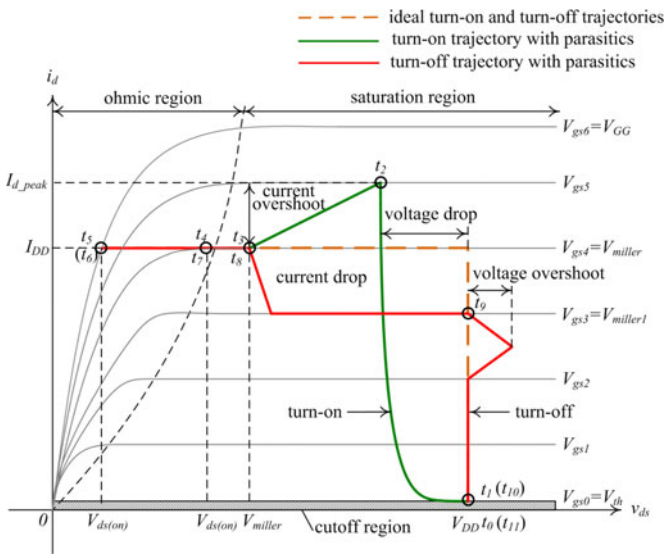

Fig. 3. Analytical switching trajectories of a MOSFET in both ideal and nonideal case.

TABLE II
KEY SWITCHING CHARACTERISTICS

Turn-on transients			Turn-off transients		
Stage	Feature	Symbol	Stage	Feature	Symbol
2	current slew rate	di_d/dt	8	voltage slew rate	dv_{ds}/dt
2	voltage drop	$v_{Ls\_on}+v_{Ld\_on}$	8	current drop	$I_{DD}-I_{D1}$
2	current stress	I_{d_peak}	9	voltage stress	$V_{os}+V_{DD}$
3	voltage slew rate	dv_{ds}/dt	9	current slew rate	di_d/dt
on	turn-on loss	P_{sw_on}	off	turn-off loss	P_{sw_off}

III. EFFECT OF PARASITIC ELEMENTS ON SWITCHING CHARACTERISTICS

The switching process of the MOSFET is modeled in detail thereupon the effect of parasitic elements can undergo full scrutiny according to the switching model. Apart from that, R_g is also considered as it can affect the switching behavior by changing the gate drive current. It should be noted that although the nonlinear characteristics of $C_{\rm gd}$ and $C_{\rm ds}$ are linearized into two discrete values in the previous section, the analysis on the switching transients clarifies that the smaller $C_{\rm gd1}$ and $C_{\rm ds1}$ at higher voltage level have more important and discernable effects than the far larger $C_{\rm gd2}$ and $C_{\rm ds2}$ at lower voltage level. Thus, as far as $C_{\rm gd}$ and $C_{\rm ds}$ are regarded in the following, only $C_{\rm gd1}$ and $C_{\rm ds1}$ will be considered.

In order to interpret the switching model in a way that such effects can be directly perceived through senses, the circuit equations will be used to plot the analytical switching waveforms with varied parasitic elements. The timeline-based switching waveforms are composed of the gate–source voltage $v_{\rm gs}$, the drain current i_d, and the drain–source voltage $v_{\rm ds}$. It must be pointed out that for the sake of emulating the switching waveforms taken in experiment, the voltage drop across the package inductances L_{s1} and L_{d1} and the internal gate drive resistance $R_{g\_\rm int}$ have to be included in the analytical waveforms for $v_{\rm gs}$ and $v_{\rm ds}$, as they are intrinsic and inside the MOSFET package. The key characteristics at both turn-on and turn-off transients that will be examined are listed in Table II. Oscillation conditions that might happen after the drain current reaches a steady-state value will not be considered in this paper, as it requires separate and precise development of the small-signal model of the configuration. The original parameter setup of the waveform calculation is given in Table III. The variations in the parameters under examination are designed within reasonable ranges of actual conditions.

TABLE III
PARAMETER SETUP

Model	Parameter	Value	Parameter	Value
Power circuit	V_{DD}	400 V	I_{DD}	6 A
	L_d	120 nH	R_{stray}	3 Ω
Gate drive circuit	R_g	20 Ω	V_{GG}	14 V
	L_{s2}	4.5 nH	f_s	120 kHz
	t_r	30 ns	t_f	20 ns
Si diode (LQA08TC600)	Q_{rr}	36 nC	V_F	2.85 V
	S	1.6	C_f	33 pF
SiC Diode* (SCS108AG)	Q_c	15 nC	V_F	1.5 V
	S	-	C_f	38 pF
MOSFET (STP20NM60FD)	$R_{ds(on)}$	0.26 Ω	L_{s1}	7.5 nH
	L_{d1}	4.5 nH	C_{gs}	1.5 nF
	C_{gd1}	30 pF	C_{gd2}	1 nF
	C_{ds1}	160 pF	C_{ds2}	1 nF
	V_{th}	4 V	g_{fs}	5 S

*SiC diode is only used in the experiment of varied C_f.

A. Gate–Source Capacitance $C_{\rm gs}$

The analytical switching waveforms with varied $C_{\rm gs}$ are illustrated in Fig. 4. The increase in $C_{\rm gs}$ prolongs the delay times and abates the current slew rate, while it does not exhibit great influence on the voltage slew rate. It indicates that the current stress, voltage stress, and voltage drop are all positively correlated to the current slew rate, while the current drop is positively correlated to the voltage slew rate. Therefore, knowledge of the current and voltage slew rates can elicit the variation trend in all of them, which can also be applied to the following analysis.

B. Gate–Drain Capacitance $C_{\rm gd}$

Fig. 5 presents the analytical switching waveforms with varied $C_{\rm gd}$. It exemplifies that the increase in L_d hardly affects the time constant of $v_{\rm gs}$, nor will it affect the current slew rate. The voltage slew rate, on the contrary, is apparently reduced with $C_{\rm gd}$.

C. Drain–Source Capacitance $C_{\rm ds}$

The analytical switching waveforms with varied $C_{\rm ds}$ are shown in Fig. 6. As $C_{\rm ds}$ does not appear in the gate drive circuit, it will affect neither $v_{\rm gs}$ nor i_d. The only difference lies in the slightly reduced voltage slew rate, which is due to the longer discharging time resulted from $C_{\rm ds}$.

D. Source Inductance L_s

Source inductance L_s provides a negative feedback from the power stage to the gate drive stage. When the MOSFET works in the saturation region, any change in the drain current will generate a voltage drop across this inductance which opposes the trend of changing in the drain current; hence, it will slow down the current slew rate. Fig. 7 displays the analytical switching waveforms with varied L_s. It shows that i_d is obviously decelerated by L_s, while no recognizable difference is made in the voltage slew rate.

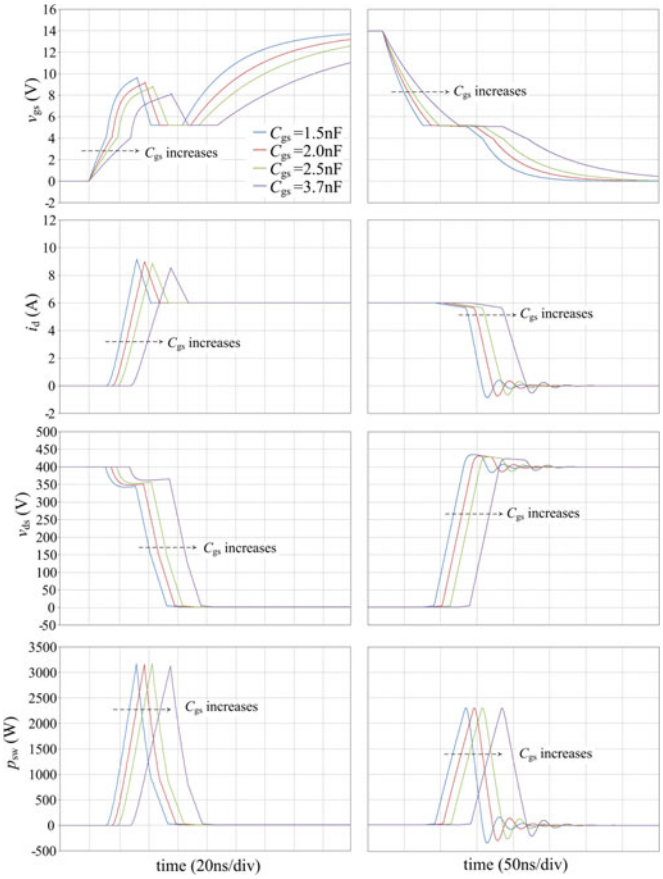

Fig. 4. Analytical switching waveform showing the effect of $C_{\rm gs}$. Left: turn-on, right: turn-off.

E. Drain Inductance L_d

L_d lumps all the stray inductances along the power loop and the parasitic drain inductance of the MOSFET alike, and is the cause of voltage stress. The analytical switching waveforms with varied L_d are shown in Fig. 8. Similar to the effect of L_s, L_d slows down i_d, while the difference in the voltage slew rate is barely noticeable. Although the drain current slew rate decreases, the voltage drop in stage 2 and the voltage stress still exhibit distinctive increase with the greater increase in L_d.

F. Junction Capacitance C_f

The change in the diode voltage requires an extra current to charge its junction capacitor C_f, which can also affect the switching performance. Fig. 9 illustrates the analytical switching waveforms with varied C_f. The major difference lies in the current stress, which is increased by the charging current of the junction capacitance. That is why even SiC diode with nonreverse recovery characteristics still has reverse current.

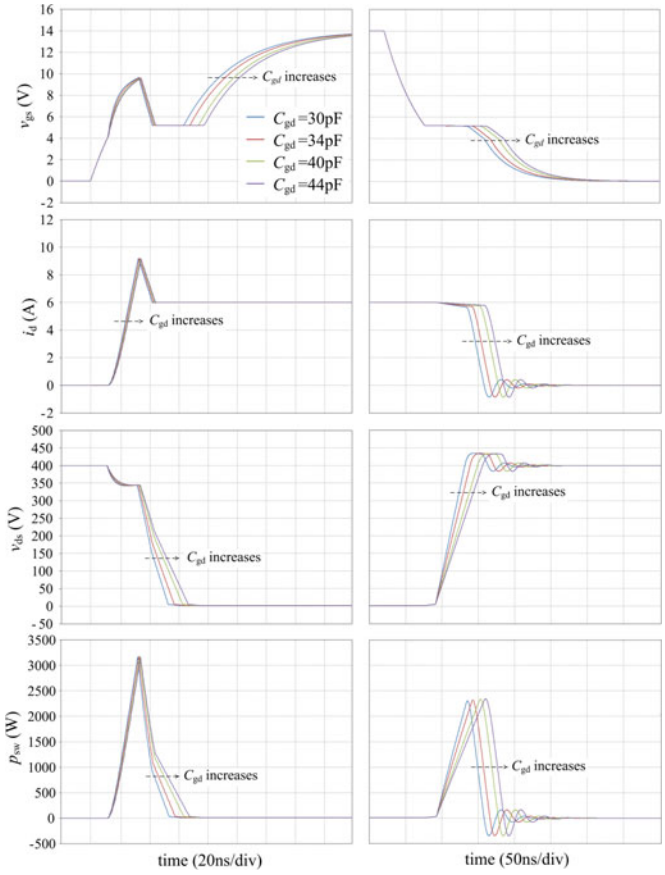

Fig. 5. Analytical switching waveform showing the effect of $C_{\rm gd}$. Left: turn-on, right: turn-off.

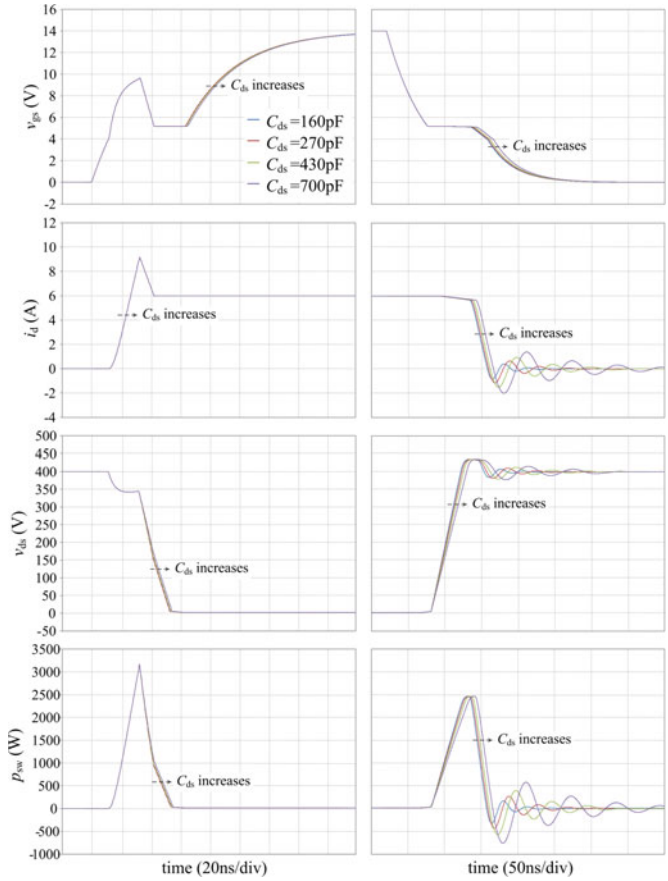

Fig. 6. Analytical switching waveform showing the effect of $C_{\rm ds}$. Left: turn-on, right: turn-off.

In the turn-off transients, the larger current drop is due to the larger current required by the simultaneous change in the diode voltage. With this increased drop in the drain current, the Miller voltage will decrease, which leads to a slight reduction in the voltage slew rate.

G. Gate Drive Resistance R_g

The analytical switching waveforms with varied R_g are shown in Fig. 10. It can be seen that its effect on the switching performance is in all aspects. Broadly speaking, large R_g will slow down the switching speed (both current and voltage slew rates), as a result, the device stresses and the current and voltage drops that are negatively correlated to the switching speed will all decrease.

IV. Experimental Evaluation on the Effect of Parasitic Elements

In this section, comparisons between the experimental and calculated results will be made to validate the characterization of the effect of parasitic elements.

A. Parameters

The original experimental setup of a 6 A, 400 V tester employs the components and parameters in Table III. Of all the parameters, most are either directly obtained from the datasheet or designed. However, the total stray inductance $L_s + L_d$ remains unknown, for it is determined by the specific layout and PCB traces of the circuit. Methods to find out its value can be classified into two categories: computational electromagnetics and experiment. The most frequently adopted computational methods are the finite element analysis (FEA) and partial element equivalent circuit (PEEC); nevertheless, they can be quite demanding in terms of computation time and the accuracy of the component and PCB layout information. The experimental methods make use of the existing information in the switching waveforms, which is not only very simple, but also convincing to present the actual conditions.

There are three feasible methods to find out the stray inductance.

1) The voltage drop in stage 2 is $v_{Ls\_\rm on} + v_{Ld\_\rm on} = (L_s + L_d)di_d/dt$, $v_{Ls\_\rm on} + v_{Ld\_\rm on}$ and di_d/dt can be measured in the turn-on switching waveforms, therefore $L_s + L_d$ can be determined.
2) The voltage overshoot in stage 9 is $V_{\rm os} = (L_s + L_d)di_d/dt$, $V_{\rm os}$ and di_d/dt can be measured in the turn-off switching waveforms, therefore $L_s + L_d$ can be determined.
3) The undamped frequency ω_d and attenuation α of the ringing can be measured in the turn-off switching wave-

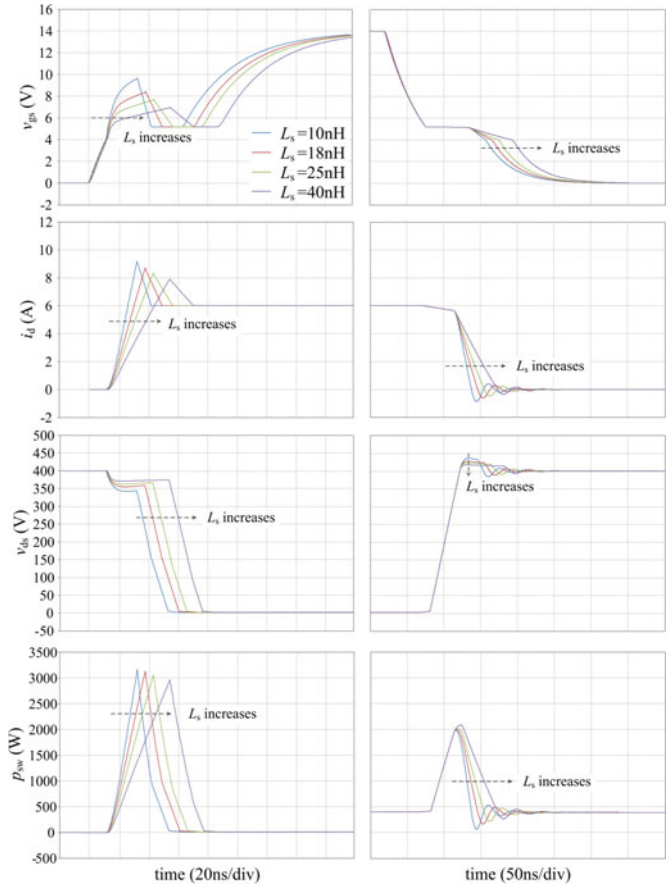

Fig. 7. Analytical switching waveform showing the effect of L_s. Left: turn-on, right: turn-off.

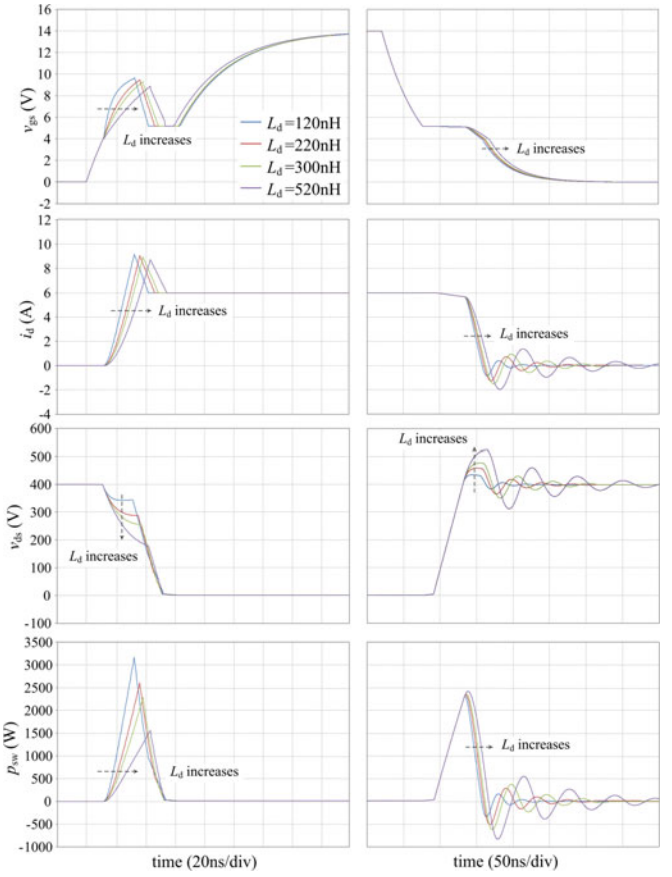

Fig. 8. Analytical switching waveform showing the effect of L_d. Left: turn-on, right: turn-off.

forms, referring to RLC circuit, the resonant frequency is $\omega_0 = \sqrt{\omega_d^2 + \alpha^2}$, the stray inductance can be obtained by $\omega_0^2 = 1/(L_s + L_d)/C_{\rm oss}$ and $\alpha = R_{\rm stray}/2(L_s + L_d)$.

Compared to the first two methods, method 3 is more prone to inaccuracy due to the prerequisite knowledge of $C_{\rm oss}$ and the evaluation of the undamped frequency ω_d and attenuation α. Therefore, the first two methods will be used here to determine the values of the stray inductance. The experimental turn-on and turn-off switching waveforms are shown in Fig. 11(a) and (b), respectively, and the calculation results are given in Table IV. The average value of the two results $L_s + L_d = 132$ nH is set as the inductance value for model calculation.

As mentioned earlier, the source inductance consists of the package inductance of the MOSFET L_{s1} and the inductance from the PCB trace L_{s2}. L_{s1} can be acquired from package specification, while L_{s2} remains unknown. As the gate driver is put as close as possible to the gate and source terminals of the MOSFET, L_{s2} will be small. The most direct estimation can only be implemented by means of computational electromagnetics, which is beyond this discussion. Here, L_{s1} is assigned the value from datasheet, and L_{s2} is given a rule-of-thumb value [10]. It should be noted that even though the value of L_s can impair the accuracy of loss calculation and the estimation on switching speed, it will not affect the conclusions on the effect of parasitic elements.

The gate drive signal is provided by PWM controller AS3843 and MOSFET driver MC34152, whose rise time t_r and fall time t_f are shown in Table III. The gate drive resistance is chosen as $R_g = 20\ \Omega$ for four reasons.

1) Relatively long switching transients enables clear demonstration of the ten stages.
2) The effect of the internal gate drive resistance on the measurement of $v_{\rm gs}$ can be disregarded.
3) With limited measurement bandwidth, large R_g helps ensure credibility of measurement results, for smaller R_g with faster switching speed will push up requirement of measurement bandwidth.
4) Large R_g help justify the assumption of zero rise time and fall time of gate drive signal $v_{\rm gate}$, for it prolongs the turn-on delay time and current rise time but does not change the gate signal. Fig. 12(a) illustrates that at t_2 when $v_{\rm gs}$ exceeds $V_{\rm th}$ and the drain current starts to flow, $v_{\rm gate}$ has already been twice $v_{\rm gs}$ and can reach $V_{\rm GG}$ before $v_{\rm ds}$ begins to fall. In this case, the assumption makes the predicted turn-on delay time and current rise time shorter than in real case, but will not affect the evaluation of the voltage falling time and the conclusion on the effect of the parasitic elements. Likewise, Fig. 12(b) shows that before the turn-off delay time ends at t_7, $v_{\rm gate}$ has already fallen near to zero which is much smaller than $V_{\rm GG}$. In this case,

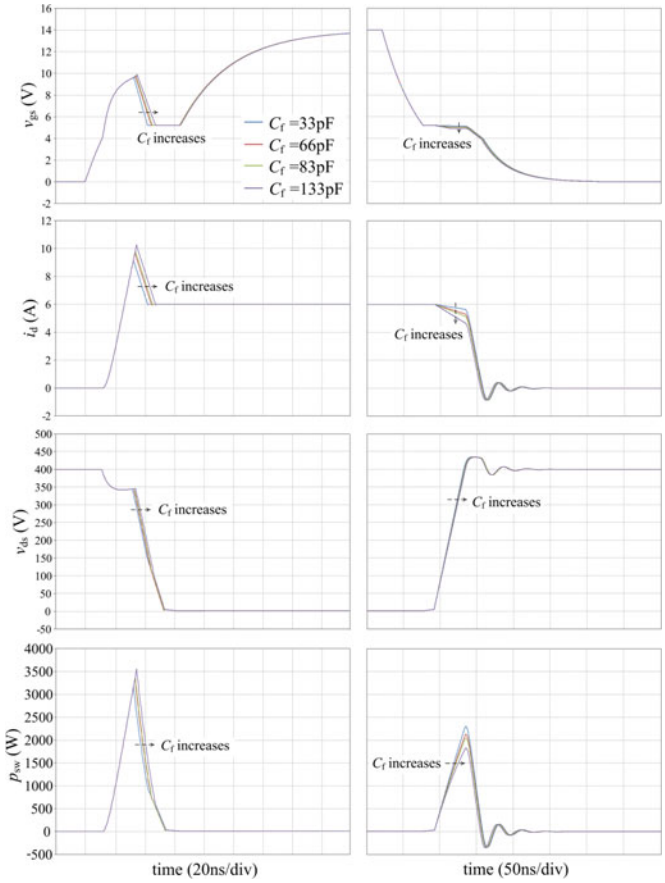

Fig. 9. Analytical switching waveform showing the effect of C_f. Left: turn-on, right: turn-off.

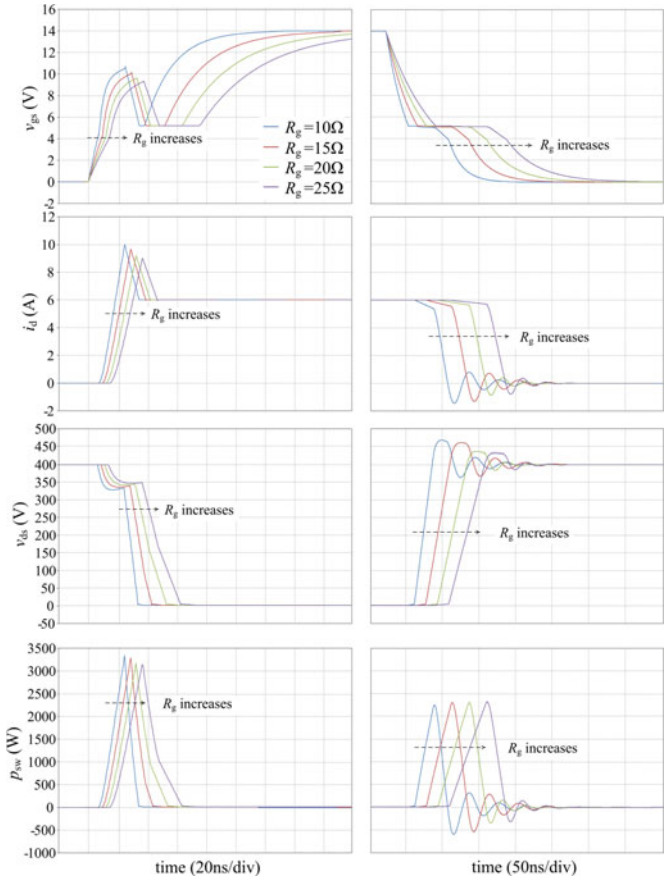

Fig. 10. Analytical switching waveform showing the effect of R_g. Left: turn-on, right: turn-off.

the assumption only makes the predicted turn-off delay time and voltage falling time a little shorter than in the real case.

To vary the value of parasitic elements, external capacitances, inductances, and resistances are added across the device terminals to emulate the bigger values. Two things should be noted: first, paralleled capacitances are used to reduce the equivalent series resistance (ESR) and equivalent series inductance (ESL); second, as the capacitances can only be connected between the external terminals (*G*, *D*, and *S* in Fig. 1), internal parasitic inductances L_{s1} and/or L_{d1} will be included. Such influence can be the most obvious in the increase of $C_{\rm ds}$, which forms an *LC* resonance with both L_{s1} and L_{d1}. However, the trend of increase in the parasitic capacitances can still be correctly inferred by the analysis, which will be shown later.

B. Description on Measurement System

The measurement system should have enough bandwidth to acquire trustworthy experimental results. It has been explained earlier that a relatively large R_g is chosen to avoid unreliable measurement. Simulation results with $R_g = 20\ \Omega$ indicate a rising edge of at least 30 ns which is supposed to be captured. The measurement equipment is selected as in Table V.

The tips of the voltage probes are clipped to the corresponding pins of the MOSFET to obtain the waveforms of $v_{\rm gs}$ and $v_{\rm ds}$. Even so, the voltage across the internal inductances L_{s1} and L_{d1} as well as the internal gate drive resistance $R_{g\_\rm int}$ will still be imposed on the measurement; therefore, it is $v_{\rm GS}$ and $v_{\rm DS}$ in Fig. 1 that are measured. That is why the voltage drop across $R_{g\_\rm int}$, L_{s1}, and L_{d1} have to be included in the analytical waveforms for $v_{\rm gs}$ and $v_{\rm ds}$ as stated before. However, the inductances will take effect only when the current is changing and they are much smaller compared to the external inductances L_{d2}. Besides, as $R_{g\_\rm int}$ is much smaller than $R_{g\_\rm ext}$, the voltage drop across $R_{g\_\rm int}$ can be neglected. Hence, such influences can be negligible and $v_{\rm GS}$ and $v_{\rm DS}$ can be approximately seen as the internal $v_{\rm gs}$ and $v_{\rm ds}$.

C. Experimental Results

The experimental switching trajectories of the MOSFET under the operating condition of Table III are shown in Fig. 13, which are in good agreement with the analytical shape in Fig. 3. The experimental waveforms under the influence of $C_{\rm gs}$ are shown in Fig. 14, which are consistent with the calculation results in Fig. 4. Switching losses from the experiment match well with those from the modeling work as compared in Fig. 15. Both turn-on and turn-off switching losses increase with $C_{\rm gs}$, which is due to the decrease in the current slew rate and the lengthening switching time duration.

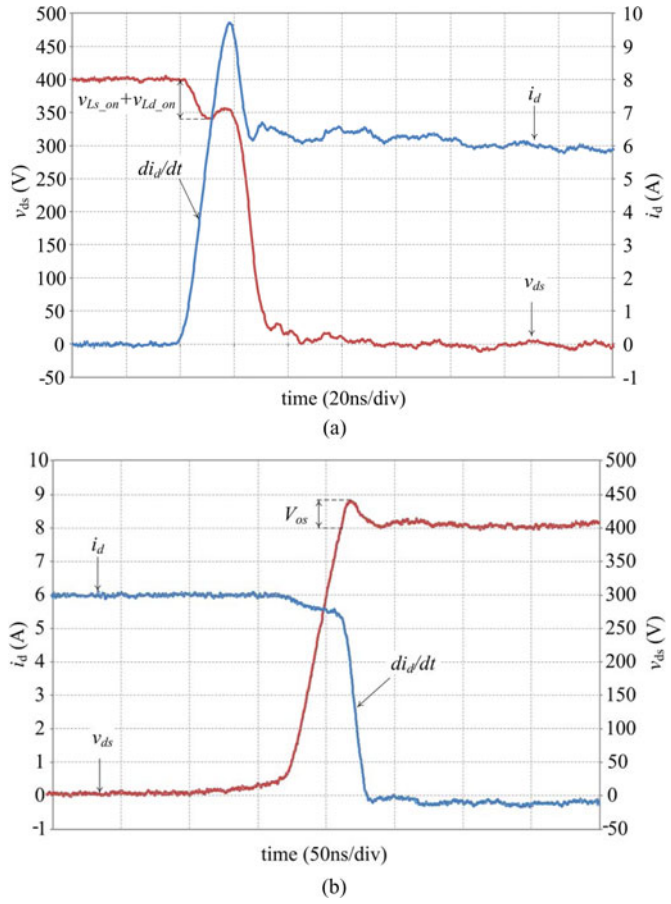

Fig. 11. Experimental switching waveform for stray inductance calculation. (a) Turn-on. (b) Turn-off.

TABLE IV
RESULTS OF STRAY INDUCTANCE CALCULATION

Method	1	2
Calculation	$v_{Ls\_on}+v_{Ld\_on}=60V$ $di_d/dt=457\mu s$	$V_{os}=40V$ $di_d/dt=300A/\mu s$
Results	$L_s+L_d=131nH$	$L_s+L_d=133nH$

Fig. 16 displays the experimental waveforms under the influence of $C_{\rm gd}$, which shows the same characteristics as Fig. 5 predicts. Comparison of switching losses obtained from experiment and calculation in Fig. 17 proves that both turn-on and turn-off switching losses increase with $C_{\rm gd}$, which results from slowdown of the voltage slew rate and the lengthening switching time duration.

The experimental waveforms under the influence of $C_{\rm ds}$ are illustrated in Fig. 18. Compared to the analytical results, with other aspects predicted correctly, the impact that $C_{\rm ds}$ has on the voltage slew rate is more obvious than estimated. The resultant oscillation during turn-off transients is also underestimated though the trend is right, for the resonance of external $C_{\rm ds}$ and

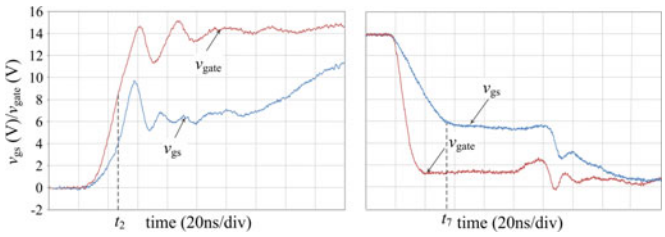

Fig. 12. Experimental switching waveform showing $v_{\rm gate}$ and $v_{\rm gs}$. Left: turn-on; right: turn-off.

TABLE V
MEASUREMENT EQUIPMENT

Part No.	Description	Bandwidth	Propagation delay	Measured signal
DP7104	Digital oscilloscope	1GHz		
HP10071A	Passive 10X voltage probe	150MHz	7 ns	v_{gs}
P5205	Differential probe	100MHz	17 ns	v_{ds}
TCP202	Current probe	50MHz	17 ns	i_d

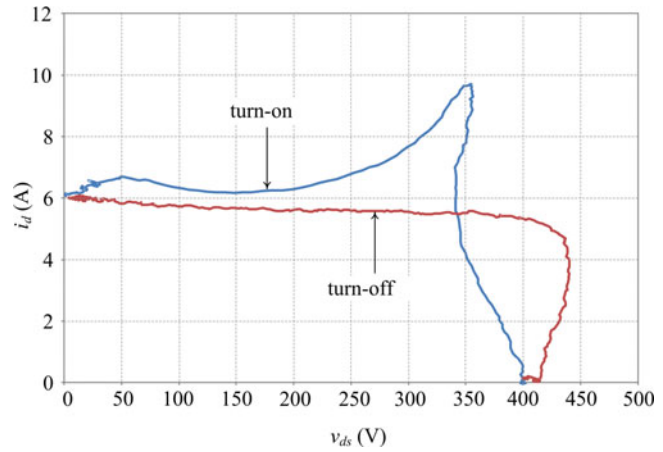

Fig. 13. Experimental switching trajectories.

internal parasitic inductances has not been considered by the model. Both of them account for the discrepancy between the calculated and experimental switching losses shown in Fig. 19.

Fig. 20 shows the experimental waveforms under the influence of L_s, which agrees with the analytical switching waveforms shown in Fig. 7. The change in the switching losses can be properly estimated by the analytical calculation as shown in Fig. 21. It can be seen that L_s can add to both turn-on and turn-off switching loss by reducing the current slew rate.

The experimental switching waveforms under the influence of L_d are depicted in Fig. 22. Discrepancy between the experimental and calculated waveforms lies in the current overshoot that is predicted by the model to decrease with L_d. It is well known that with other conditions unchanged, the reverse current of the diode is inversely proportional to the current slew rate, and di_d/dt in the experimental is indeed reduced. However, the reverse recovery charge $Q_{\rm rr}$ is actually heavily dependent on the stray inductance in the circuit [5]. This characteristics cannot be explored by circuit-level analysis, where a constant value is

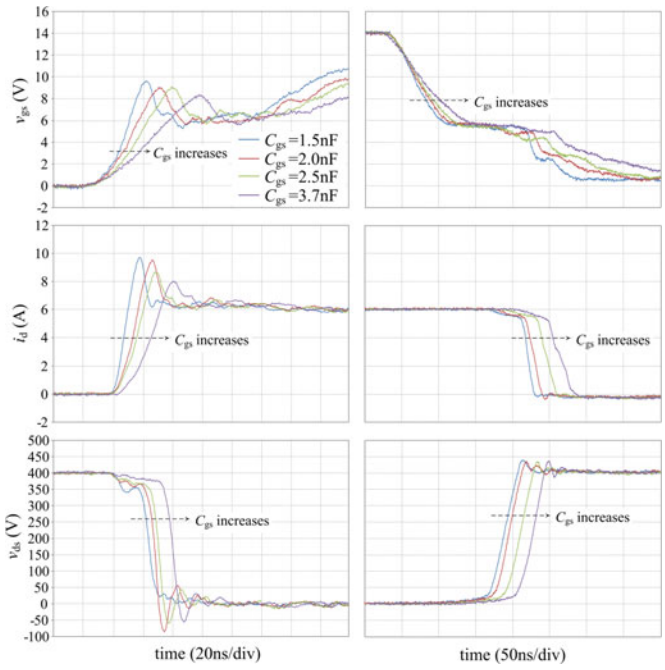

Fig. 14. Experimental switching waveform showing the effect of $C_{\rm gs}$. Left: turn-on, right: turn-off.

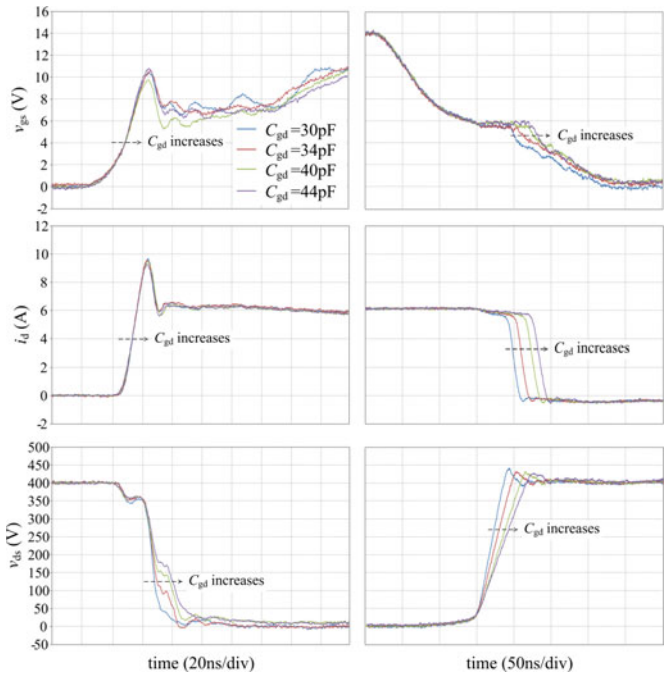

Fig. 16. Experimental switching waveform showing the effect of $C_{\rm gd}$. Left: turn-on, right: turn-off.

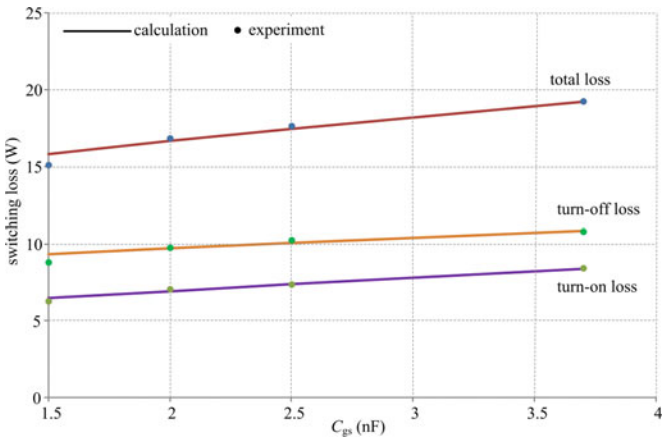

Fig. 15. Experimental and calculated switching losses under the influence of $C_{\rm gs}$.

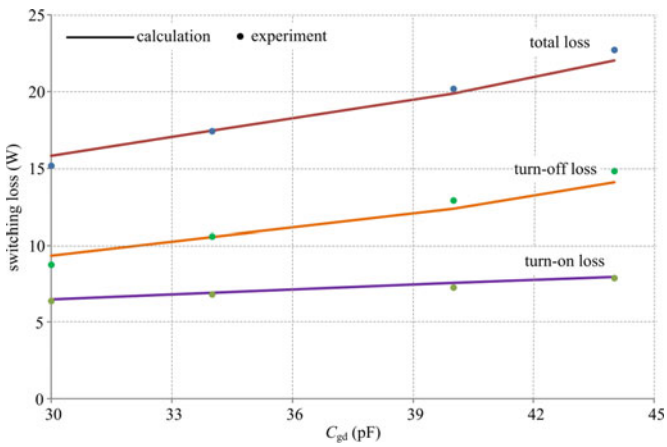

Fig. 17. Experimental and calculated switching losses under the influence of $C_{\rm gd}$.

used for $Q_{\rm rr}$. It can only be learnt from physical level analysis that $Q_{\rm rr}$ will increase with stray inductance. If the $Q_{\rm rr}$ – L_d relationship can be modeled first, the analytical model can give the right prediction. Comparison between calculated and experimental switching losses under the influence of L_d is made in Fig. 23. It reveals that the turn-on loss will decrease with L_d, which is due to the increase in the voltage drop during current rise time, and that the turn-off loss will increase with L_d, which is caused by the reduced current slew rate and the increased voltage overshoot.

The experimental switching waveforms under the influence of L_g are also captured as in Fig. 24. It proves that L_g influences the delay time more than the switching speed, which makes the disregard of it reasonable in the analysis. The switching losses are given in Fig. 25, which shows little difference with different L_g.

Fig. 26 shows the experimental switching waveforms under the influence of C_f, which are consistent with the analytical switching waveforms shown in Fig. 9. The experimental switching losses are in good accordance with the calculation results as given in Fig. 27. It is discovered that the turn-on loss will increase with C_f because of the increase in the current overshoot, and that the turn-off loss will decrease with C_f because of the increased current drop during voltage falling time.

For comparison, this set of experiment is repeated with a SiC diode (SCS108AG) which has the same voltage and current rating as the Si diode. The experimental switching waveforms under the influence of C_f are shown in Fig. 28. It demonstrates

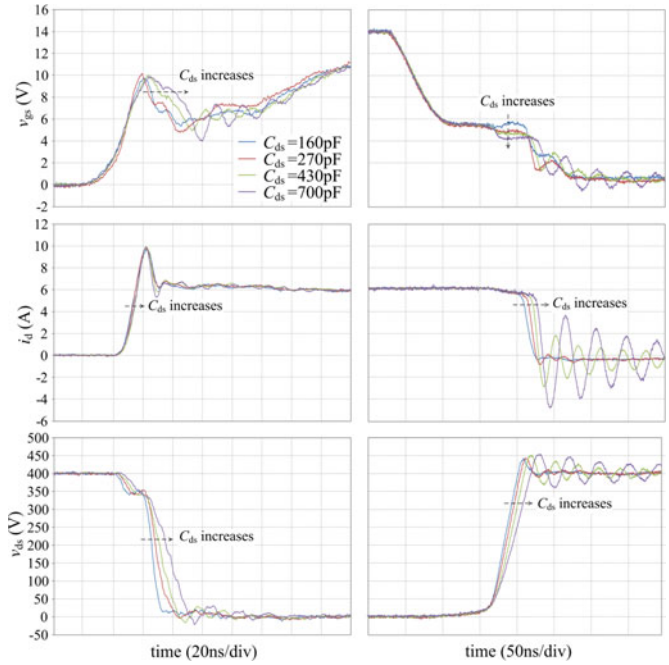

Fig. 18. Experimental switching waveform showing the effect of $C_{\rm ds}$. Left: turn-on, right: turn-off.

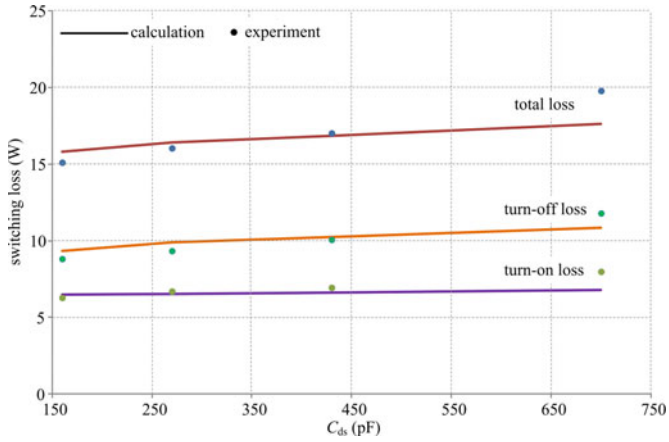

Fig. 19. Experimental and calculated switching losses under the influence of $C_{\rm ds}$.

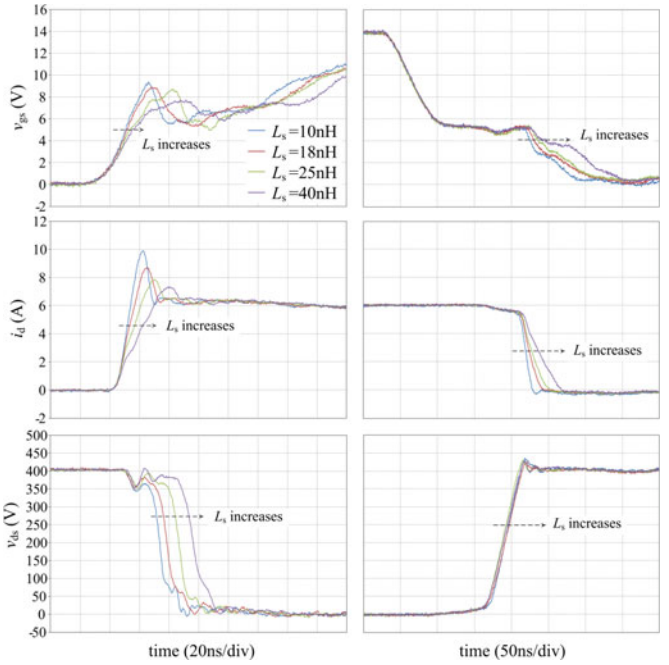

Fig. 20. Experimental switching waveform showing the effect of L_s. Left: turn-on, right: turn-off.

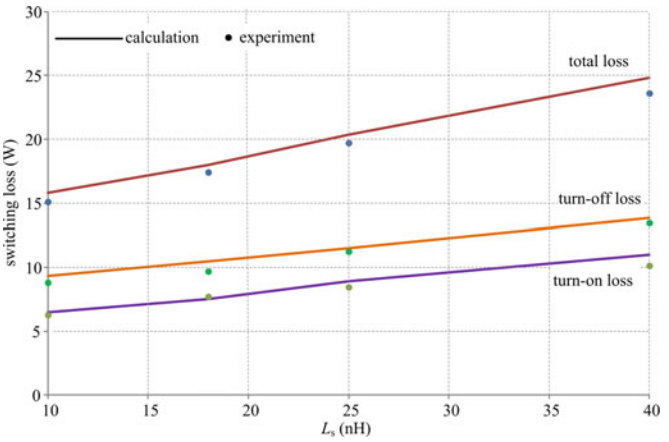

Fig. 21. Experimental and calculated switching losses under the influence of L_s.

that although smaller, there is still a current overshoot resulted from the reverse current of the diode. This arises from the total capacitive charge specified in its datasheet [19]. Making use of this parameter, the switching losses can still be well predicted by the model as given in Fig. 29.

The switching waveforms under the influence of R_g are displayed in Fig. 30. Observations from the experiment are consistent with those from the calculation in Fig. 10. Switching losses from the experiment matches with those from the calculation as compared in Fig. 31. Both turn-on and turn-off switching losses increase with R_g, which is due to the reduction in both current and voltage slew rate and the lengthening switching time duration. Also compared in Fig. 31 are the current and voltage stresses. The discrepancy in the current stress can be explained by the fact that the reverse recovery charge $Q_{\rm rr}$ will decrease with the switching speed [5], which can only be learnt from physical level analysis, while a fixed value from the datasheet is used for $Q_{\rm rr}$in the calculation. Both the current and voltage stresses are positively correlated to the current slew rate, which will be reduced by the increase in R_g. As stated earlier, R_g is the only changeable component in the gate drive circuit, it can be chosen to mitigate the conflict between switching losses that increase with it, and the device stresses that decrease with it.

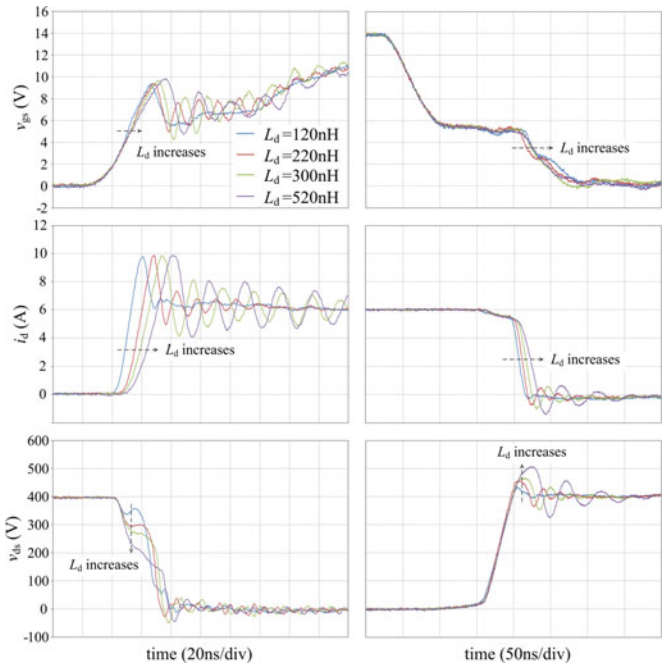

Fig. 22. Experimental switching waveform showing the effect of L_d. Left: turn-on, right: turn-off.

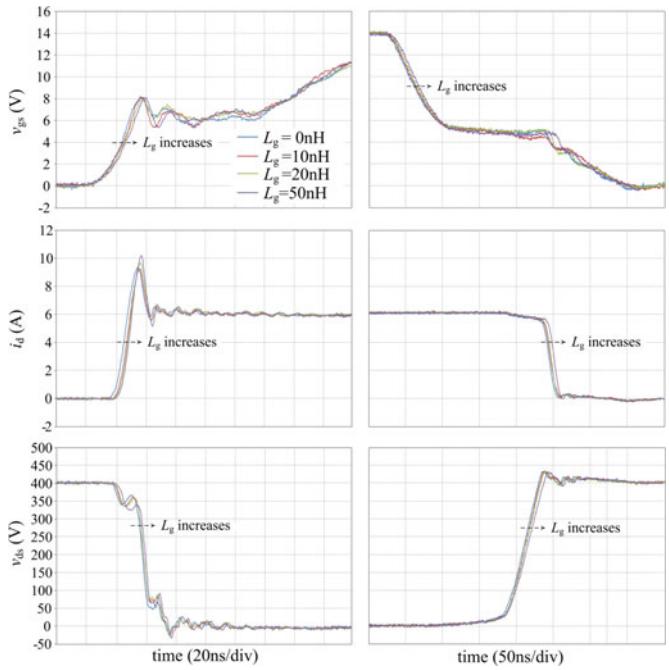

Fig. 24. Experimental switching waveform showing the effect of L_g. Left: turn-on, right: turn-off.

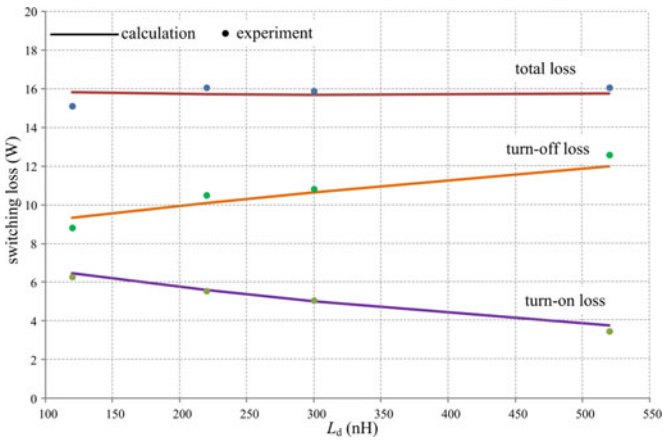

Fig. 23. Experimental and calculated switching losses under the influence of L_d.

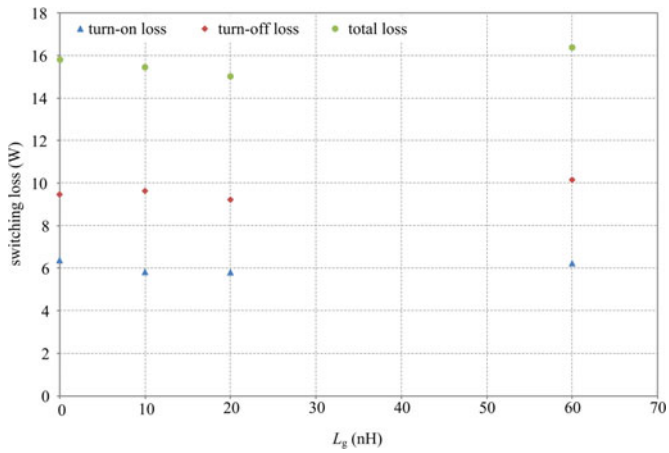

Fig. 25. Experimental switching losses under the influence of external L_g.

V. Results and Discussion

The effect of the parasitic elements can be summarized with reference to the intrinsic characteristics of the MOSFET as follows.

A. Switching Speed

The switching transients of the MOSFET are essentially the charging process of its parasitic capacitances. Since the channel current is gate-source voltage dependent in the saturation region, it is out of question that $C_{\rm gs}$ can affect the current slew rate. As for the voltage slew rate, it is clarified that the charging of $C_{\rm gd}$ leads to the change in the drain–source voltage. That is why the influence of $C_{\rm gs}$ on the drain current is much more significant, while $C_{\rm gd}$ dominates the drain–source voltage. In addition, the charging time of $C_{\rm ds}$ can also affect the voltage slew rate, for simultaneous action is demanded in $C_{\rm ds}$ if there is any change in $C_{\rm gd}$.

The effect of the parasitic inductances L_s and L_d can be attributed to the innate characteristics of inductors that they can resist the changing in the current flowing through them, and that there is no such effect in the voltage across them. That is why an increase in either parasitic inductance can slow down the current slew rate, while neither can affect the voltage slew rate.

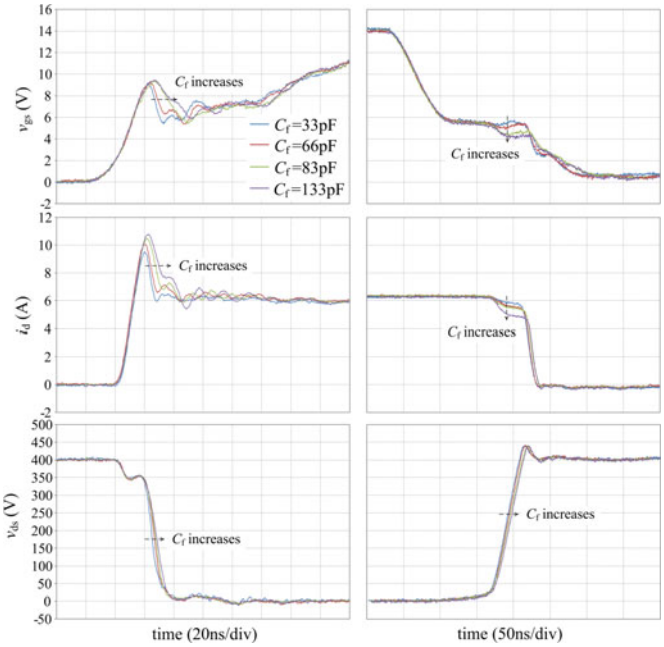

Fig. 26. Experimental switching waveform showing the effect of C_f. Left: turn-on, right: turn-off.

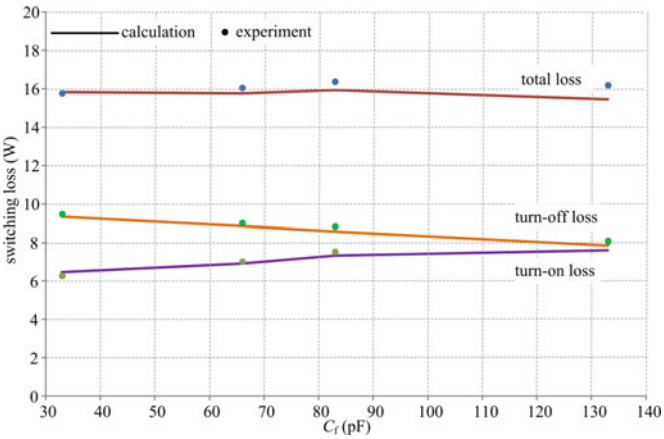

Fig. 27. Experimental and calculated switching losses under the influence of C_f.

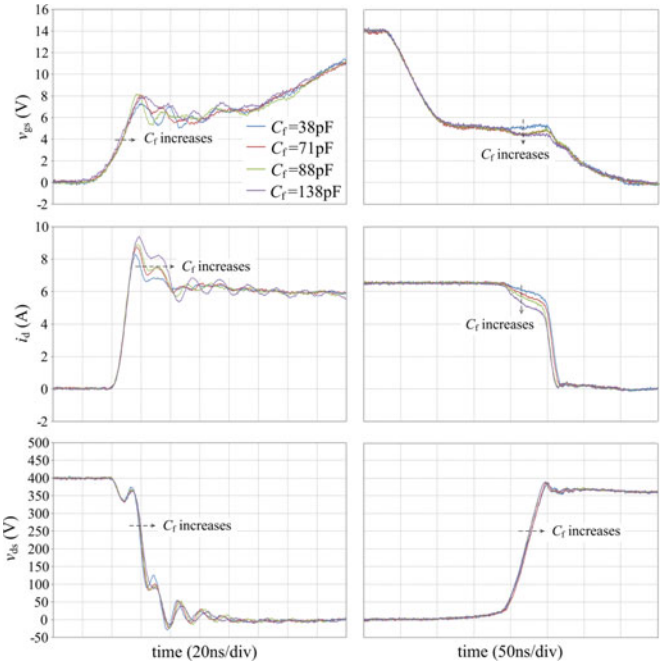

Fig. 28. Experimental switching waveform showing the effect of C_f of a SiC diode. Left: turn-on, right: turn-off.

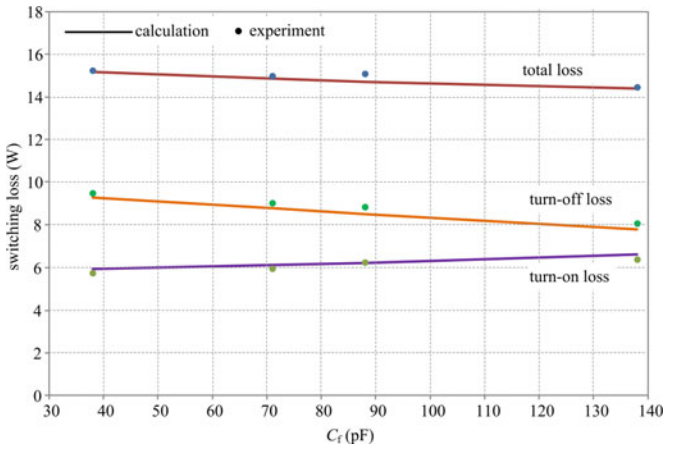

Fig. 29. Experimental and calculated switching losses under the influence of C_f of a SiC diode.

B. Voltage and Current Stresses

Going back to their origin, voltage stress stems from the extra voltage induced upon the parasitic inductances by the falling drain current during turn-off process, while the current stress mainly derives from the displacement current of the diode as well as the reverse recovery current of the diode. Both stresses are positively correlated to the current slew rate of the MOSFET, whose relationship with parasitic elements has been given. Moreover, although L_d can reduce the current slew rate, the increase in L_d outweighs the decrease in the current slew rate, therefore, the overall effect of L_d on the voltage stress is increased, which can also be applied to the voltage drop in stage 2. With respect to the current stress, another point is that C_f can add to the reverse current of the diode during turn-on transients of the MOSFET, which is also true for the current drop in stage 8.

C. Switching Loss

According to (37), with a constant switching frequency, three factors account for the switching loss: the time duration of the switching transients, which is determined by the switching speed, and the magnitude of $v_{\rm ds}$ and i_d, both of which can be affected by the current and voltage stresses and drops. $C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$, L_s, and R_g increases switching loss by slowing down the switching speed and prolonging the switching process.

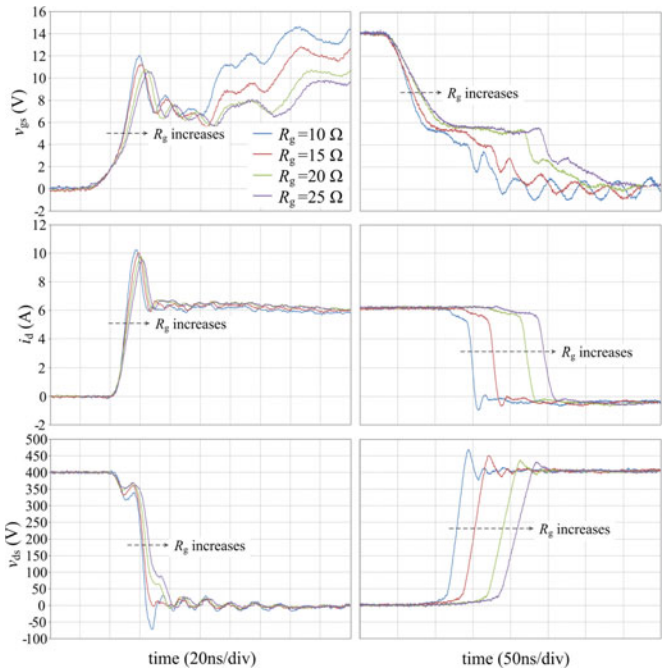

Fig. 30. Experimental switching waveform showing the effect of R_g. Left: turn-on, right: turn-off.

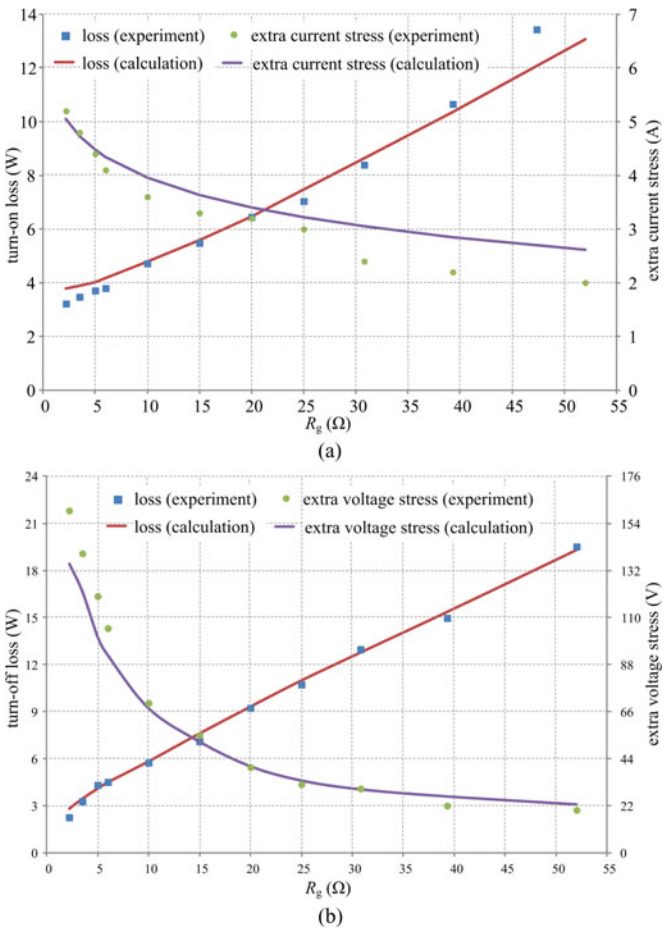

Fig. 31. Experimental and calculated switching losses and device stresses under the influence of R_g. (a) Turn-on loss and extra current stress. (b) Turn-off loss and extra voltage stress.

However, for C_f, it is the change in the magnitude of i_d rather than in the time duration that affects the switching loss. The current stress at turn-on is increased by C_f, with other conditions unchanged, the turn-on loss is thereby increased. Likewise, the current drop at turn-off is also increased by C_f, therefore the turn-off loss is reduced. In this situation, the effect of C_f on the total switching loss remains uncertain. Similar for L_d, it is the change in the magnitude of $v_{\rm ds}$ that greatly affects the switching loss. The voltage drop at turn-on is increased by L_d; other conditions unchanged, the turn-on loss is thereby reduced; the voltage overshoot at turn-off is also increased by L_d; therefore, the turn-off loss is increased. In this situation, the effect of L_d on total switching loss also remains uncertain.

D. Design Guidelines

It can be concluded that parasitic elements of the MOSFET have a profound influence on the switching performance; hence, it calls for special attention to the selection of components and circuit design. The voltage slew rate is most sensitive to $C_{\rm gd}$, $C_{\rm ds}$, and R_g; for high-speed high-voltage applications, these values should not be large. The current slew rate is most sensitive to $C_{\rm gs}$, L_s, L_d, and R_g.

If power dissipation is the only concern, larger L_d and C_f may be beneficial to the overall switching loss; however, oscillation and device stresses may pose another problem for the switching performance; therefore, the PCB traces should be carefully routed to reduce the stray inductance in the circuit. The other parasitic elements should be minimized to achieve fast switching and low loss; however, deteriorated oscillation and device stresses always comes as the penalty of small switching loss, which deserves a second thought. The only element that can be minimized to reduce both switching loss and oscillation is L_s. That is why source inductance contributed by PCB trace L_{s2} should be minimized.

All parasitic elements are determined once the MOSFET and the diode are selected and the PCB design is finished. The only component that can be chosen and change the switching performance is R_g. A common practice is to use a rule-of-thumb value of several to tens of ohms for this resistance, which offers less freedom to mediate the conflicts between switching loss and device stresses. It is known from Fig. 31 that this contradiction can actually be divided into two sets: first, turn-on loss and current stress; second, turn-off loss and voltage stress. In light of this, separate values for turn-on and turn-off gate drive resistance can be used to fulfill a better compromise. This idea has been issued by some application notes on gate driver design such as [20], but it contains only the concept and does not constitute complete design rules. Since the turn-on loss and the current stress as well as the turn-off loss and the voltage stress under the influence of R_g can be predicted by the analytical model as in Fig. 31, once the design criteria are known, it is possible to properly design R_g to achieve a better compromise. It is especially meaningful if either the current or the voltage stress is quite small, or if the turn-on or turn-off loss is dominant in the total switching loss.

VI. Conclusion

A detailed investigation into the effect of parasitic elements on the switching characteristics of the MOSFET is achieved in this paper. A circuit-level model that takes MOSFET parasitic capacitances and inductances, circuit stray inductances, and reverse current of the freewheeling diode into account has been established to emulate the switching process of the MOSFET. The influence of parasitic elements on the switching performance is assessed graphically according to the analytical model, and successfully verified by experimental results of a 400 V, 6 A test bench. Compared to results obtained merely from simulation or parametric study, it can offer better insight into where the changes in switching performance lie when the parasitic elements are varied.

Appendix

A. Analysis of Reverse Recovery Charge Phenomenon of the Diode

$$t_{\rm rr} = t_{\rm rr\_1} + t_{\rm rr\_2} \tag{A1}$$

$$I_{\rm rr,max} = \frac{di_d}{dt}|_{i_d = I_{\rm DD}} t_{\rm rr\_1} \tag{A2}$$

$$Q_{\rm rr} = \frac{1}{2} I_{\rm rr\_max} t_{\rm rr} \tag{A3}$$

$$S = \frac{t_{\rm rr\_2}}{t_{\rm rr\_1}}. \tag{A4}$$

B. Stage 9

Case I: When $\tau_n^2 > 4\tau_m^2$

$$v_{\rm gs}(t) = \frac{V_{\rm miller}}{\tau_a - \tau_b}[\tau_a e^{-(t-t_9)/\tau_a} - \tau_b e^{-(t-t_9)/\tau_b}] \tag{B1}$$

$$i_d(t) = g_{fs}\left\{\frac{V_{\rm miller}}{\tau_a - \tau_b}[\tau_a e^{-(t-t_9)/\tau_a} - \tau_b e^{-(t-t_9)/\tau_b}] - V_{\rm th}\right\} \tag{B2}$$

$$\frac{di_d}{dt} = -\frac{g_{fs} V_{\rm miller1}}{\tau_a - \tau_b}[e^{-(t-t_9)/\tau_a} - e^{-(t-t_9)/\tau_b}]. \tag{B3}$$

Case II: When $\tau_n^2 < 4\tau_m^2$

$$v_{gs}(t) = V_{\rm miller1} e^{-(t-t_9)/\tau_d}\left(\frac{\tau_d}{\tau_c}\sin\frac{t-t_9}{\tau_d} + \cos\frac{t-t_9}{\tau_d}\right) \tag{B4}$$

$$i_d(t) = g_{fs}\left[V_{\rm miller1} e^{-t-t_9/\tau_d} \times \left(\frac{\tau_d}{\tau_c}\sin\frac{t-t_9}{\tau_d} + \cos\frac{t-t_9}{\tau_d}\right) - V_{\rm th}\right] \tag{B5}$$

$$\frac{di_d}{dt} = -g_{fs} V_{\rm miller1} e^{-(t-t_9)/\tau_d}\left(\frac{\tau_d}{\tau_c^2} + \frac{1}{\tau_d}\right)\sin\frac{t-t_9}{\tau_d}. \tag{B6}$$

Similar to its turn-on counterpart stage 3, the drain current has exponential profile under both conditions. Case I features faster current slew rate than case II and is more likely to happen.

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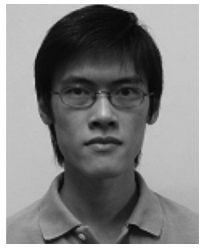

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