An Accurate Matlab/Simulink Based SiC MOSFET Model for Power Converter Applications

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***Abstract*—In this paper, an analytical model of a silicon carbide power DMOSFET is developed in Matlab/Simulink environment, intended for high performance converter simulations. The proposed Simulink-based model is a highly useful tool that allows users to study system response to transient phenomena and calculate energy losses in a variety of topologies, control strategies and operating conditions. The static characteristics of the model and its performance during hard switching are validated through experimental testing and comparison with similar models in other commercially available simulation platforms. A 1 kW single phase, high frequency inverter is developed using SiC MOSFETs to investigate the accuracy of the proposed model when simulating a complete power converter.**

Keywords—modeling; parameter extraction; power MOSFET; silicon carbide (SiC); simulation; Matlab/Simulink

I. INTRODUCTION

Silicon Carbide (SiC) power transistors are constantly gaining ground over the conventional silicon (Si) devices in next generation converters due to their advanced operational characteristics [1], [2]. This raises the need for simulation models capable of capturing the behavior of complete converters, implemented with such devices. According to recent bibliography, there are three main model development strategies:

- Interconnecting multiple active components in SPICE-like simulators [3]–[5]. This approach is deprived of a physical interpretation and exhibits increased complexity.
- Physical-based models [6]. In this case, an accurate semiconductor device profile is required, which is rarely available, while a multidimensional simulation environment is necessary. This renders the strategy ineffective for simulating real world power converters.
- Stand-alone models based on electrical circuit equations [7]–[9]. By applying a suitable parameter extraction technique, the device performance is captured in the most intuitive and efficient way.

The latter technique is the one selected for modeling a 1.2 kV SiC power MOSFET (*C2M0080120D*) [10], [11], in Matalab/Simulink. The cross section of the SiC semiconductor along with its dimensions is depicted in Fig. 1, [9]. The development of the model is chosen to be made on this popular software platform, widely used for simulating industrial systems and devices but still lacking in accurate models of commercially available semiconductors. Hence, the main contribution of this work is the introduction of a new simulation model for a SiC power MOSFET, hereafter denoted as the *Analytical* model, which is accurate enough to permit reliable calculation of losses and capture the dynamic response of the system.

The proposed model is described in Section II followed by its validation in transient phenomena in Section III. The performance of the *Analytical* model is confirmed in Section IV, were a fully functional, 1 kW single-phase inverter is developed and simulated using the proposed model. Section V summarizes the main conclusions of this work.

II. MODEL ANALYSIS

The development of a stand-alone model for a power semiconductor requires precise representation of both static and dynamic characteristics of the power switch, as will be shown in this section.

A. Forward DC Characteristics

In order to capture the DC performance of the SiC power MOSFET, the *Level 1* SPICE NMOS block from the SimElectronics library is initially used. The *Level* 1 model is the simplest way to represent the physical characteristics of a MOSFET. The model is based on a small signal Lateral

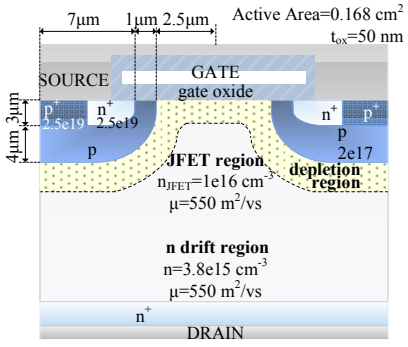

Fig. 1. Cross section of the *C2M0080120D* SiC MOSFET along with its physical characteristics.

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MOSFET which, as it will be shown later on, is a limiting factor for accurately modeling a Power MOSFET.

The parameters of this model are extracted using the manufacturer's output characteristics, through explicit nonlinear curve fitting techniques over the normal operating range:

- $0 \le i_D \le 32$ A
- $0 \le v_{DS} \le 7$ and
- $v_{GS} \in \{10\text{ V}, 12\text{ V}, 14\text{ V}, 16\text{ V}, 18\text{ V}, 20\text{ V}\}$

The selection of this particular $v_{DS} - i_D$ region is justified, since the steady state current of a modern power converter does not exceed the nominal current rating of the power device, while the gate voltage is no less than 15 V during the conduction state. The corresponding parameters are given in TABLE I and the resulting forward characteristics of the model and the actual device behavior are compared in Fig. 2(a). Note that initial parameter estimation can be performed using the physical parameters of Fig. 1. The standard deviation (σ), defined in (1), where N is the total samples number, is used as an indicator of the reliability of the model. For a single *Level* 1 model, σ is calculated 2.52 A. Hence, the simplicity of the *Level* 1 model results in a small number of parameters and low computational cost, but its accuracy is limited.

$$\sigma = \sqrt{\sum_{1}^{N} \frac{\left(I_{d-Model} - I_{d-actual}\right)^2}{N}} \qquad (1)$$

Another modeling technique for SiC MOSFET is based on the use of the inbuilt *Level* 3 SPICE NMOS. It is an empirical model in the sense that its equations derive from modifying the PSPICE *Level* 2 equations rather than solving the Maxwell and Boltzmann equations for a Lateral MOSFET. Despite its lack of physical representation, this model exhibits improved accuracy, while incorporating several phenomena such as the carrier velocity saturation, surface mobility degradation and moderate - weak inversion. The parameters extracted for this model are summarized in TABLE I and the forward DC characteristics are illustrated in Fig. 2(b). The standard deviation of a *Level* 3 model is calculated equal to 0.66 A. However, there are restrictions using the *Level* 3 NMOS for modeling power SiC MOSFETs because of the high leakage currents recorded at the presence of high v_{DS} potential during the off-state.

Alternatively, the SiC MOSFET can be precisely modeled by connecting two *Level 1* NMOSs in parallel as shown in the block diagram of Fig. 3. More specifically, the operation of a MOSFET during conduction can be divided into two distinct modes:

a. under low drain currents, the MOSFET conduction is attributed to diffusion phenomena near the channel edges

b. under high drain currents, the entire device is conducting

This discretization can be simulated by connecting in parallel two channels with different threshold voltages and transconductances, the first called the Low NMOS and the second the High NMOS. The parameter values chosen for both the Low and High NMOSs are included in TABLE I, while the effectiveness of the model in capturing the DC characteristics of the SiC MOSFET is illustrated in Fig. 2(c). The standard deviation in this case is 1.10 A, significantly improved compared to that of a single *Level* 1 model. The proposed model combines reduced complexity and low computational cost with high accuracy, while overcoming the limitations arising from the use of a *Level* 3 model in power MOSFETs.

TABLE I. *ANALYTICAL* MODEL PARAMETERS

PARAMETERS	**Single *Level* 1**	**Single *Level* 3**	**Two *Level* 1 in parallel** Low voltage NMOS	High Voltage NMOS
LENGTH	$1{\cdot}10^{-6}$ m	$1{\cdot}10^{-6}$ m	$1{\cdot}10^{-6}$ m	
WIDTH	$100{\cdot}10^{-6}$ m	$100{\cdot}10^{-6}$ m	$100{\cdot}10^{-6}$ m	
RD	$5{\cdot}10^{-3}$ Ω	$5{\cdot}10^{-3}$ Ω	$5{\cdot}10^{-3}$ Ω	
RS	$5{\cdot}10^{-3}$ Ω	$5{\cdot}10^{-3}$ Ω	$5{\cdot}10^{-3}$ Ω	
VTO	3.050 V	4.7866 V	1.71563 V	6.4882 V
KP	0.0112 A/V^2	0.0203 A/V^2	$5.43{\cdot}10^{-3}$ A/V^2	$6.00\ 10^{-3}$ A/V^2
GAMMA	0	10.69083 V$^{0.5}$	5 V$^{0.5}$	
PHI	0	2.8	5 V	
LAMDA	0	–	0	
ETA	–	2.47765	–	
THETA	–	0.0451 V^{-1}	–	
TOX	0	$50{\cdot}10^{-9}$ m	$50{\cdot}10^{-9}$ m	
NSUB	–	$1{\cdot}10^{16}$	–	
U0	0	550	0	

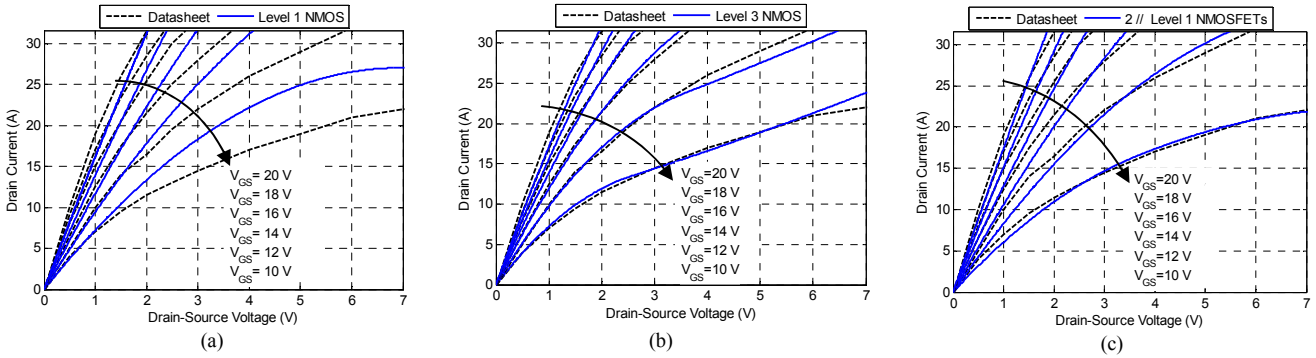


Fig. 2. Forward DC characteristics of both the *C2M0080120D* and the *Analytical* model implemented as (a) a single Level 1 NMOS, (b) a single Level 3 NMOS and (c) two Level 1 NMOSFETS connected in parallel.

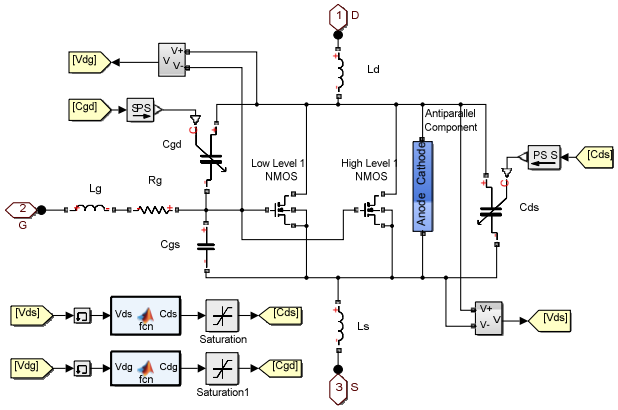


Fig. 3. Schematic diagram of the *Analytical* model implemented in Matlab/Simulink.

B. Reverse DC Characteristics

Since the inbuilt Simulink SPICE NMOS represents a small signal Lateral Si MOS, attention should be paid when negative drain-source bias is applied. In particular, the limited reliability of the standard Simulink model derives from two factors:

a. Due to the lateral structure, large reverse current may flow through the body-drain diode when reverse bias is imposed. This problem is easily surpassed by setting the saturation current parameter *IS* to zero.

b. The third quadrant v_{DS} – i_D characteristics of the inbuilt Simulink block are inappropriate when modeling a vertical power SiC MOSFET as can be seen in Fig. 4(a).

This issue is addressed by connecting in parallel to both *Level* 1 MOSFETs yet another electrical component, exhibiting the desired third quadrant characteristics, as illustrated in Fig. 3. By subtracting the reverse characteristics of the inbuilt antiparallel NMOS diodes from the real ones retrieved from the datasheet (see Fig. 4(a)), the v_{DS} – i_D characteristics of the additional component are obtained and presented in Fig. 4(b). It is worth noting that this electrical component should be v_{GS} voltage-dependent and the v_{DS} – i_D curve may be located in the second quadrant if high gate bias is applied (e.g., $v_{GS} \geq 15$ V). A nonlinear variable resistance is selected in order to realize the additional component.

The parameters of this nonlinear resistor are extracted for each v_{DS} – i_D characteristic, through implicit nonlinear curve fitting. Consequently, five different parameter sets are obtained for the five v_{GS} values given in TABLE II. The dependence of each parameter on the gate voltage is approximated by the fourth-degree polynomial functions shown in (2). The reverse properties of the *Analytical* model, incorporating the antiparallel component, are illustrated in Fig. 4(c). Although a significant improvement of the reverse performance is achieved, it is important to emphasize that the additional component is a passive element and thus, unable to simulate the second quadrant characteristics.

$$\left.\begin{aligned} Is &= 1.07\cdot10^{-9}v_{gs}^4 - 6.65\cdot10^{-8}v_{gs}^3 + 1.53\cdot10^{-6}v_{gs}^2 - 1.52\cdot10^{-5}v_{gs} \\ &\quad + 5.56\cdot10^{-5} \\ N &= 3.07\cdot10^{-4}v_{gs}^4 + 1.53\cdot10^{-2}v_{gs}^3 + 0.268v_{gs}^2 + 1.915v_{gs} + 11.021 \\ R_0 &= 1\cdot10^{-5} \\ R &= 9.25\cdot10^{-6}v_{gs}^4 + 4.62\cdot10^{-4}v_{gs}^3 + 8.09\cdot10^{-3}v_{gs}^2 + 5.78\cdot10^{-2}v_{gs} \\ &\quad + 2.98\cdot10^{-2} \end{aligned}\right\} \quad (2)$$

C. Dynamic Characteristics

The dynamic behavior of the SiC MOSFET is mainly attributed to three capacitances, the constant C_{GS} = 945 pF and the nonlinear C_{DS} and C_{DG}. An exponential equation is used for the latter two voltage dependent capacitances as indicated in (3) and (4) where C_{DS0}=800 μF, C_{DG0}=600μF, m_{DS}=0.45 and m_{DG} =1.03. These capacitances exhibit a linear relation to v_{DS} and v_{DG} during reverse bias (α = 5 in (3),(4)), [12]. C_{DS} and C_{DG} are implemented as code-based Matlab *S-functions*, as shown in Fig. 3. The variation of the proposed model capacitances with v_{DS} is illustrated in Fig. 5 against the datasheet curves.

Regarding the parasitic elements at the device terminals, the typical packaging (TO-247) stray inductances are incorporated in the *Analytical* model (i.e., L_G = 7.52 nH, L_D = 5.93 nH and L_S= 9.23 nH).

TABLE II. PARAMETERS OF THE ANTIPARALLEL COMPONENT FOR EACH V_{GS}

v_{GS}	*IS*	*N*	*R0*	*R*
0 V	$5.62\cdot10^{-5}$	11.132	$1.00\cdot10^{-5}$	0.030
5 V	$1.00\cdot10^{-5}$	6.488	$1.00\cdot10^{-5}$	0.170
10 V	0	6.488	$1.00\cdot10^{-5}$	0.170
15 V	0	6.488	$1.00\cdot10^{-5}$	0.170
20 V	0	6.488	$1.00\cdot10^{-5}$	0.170

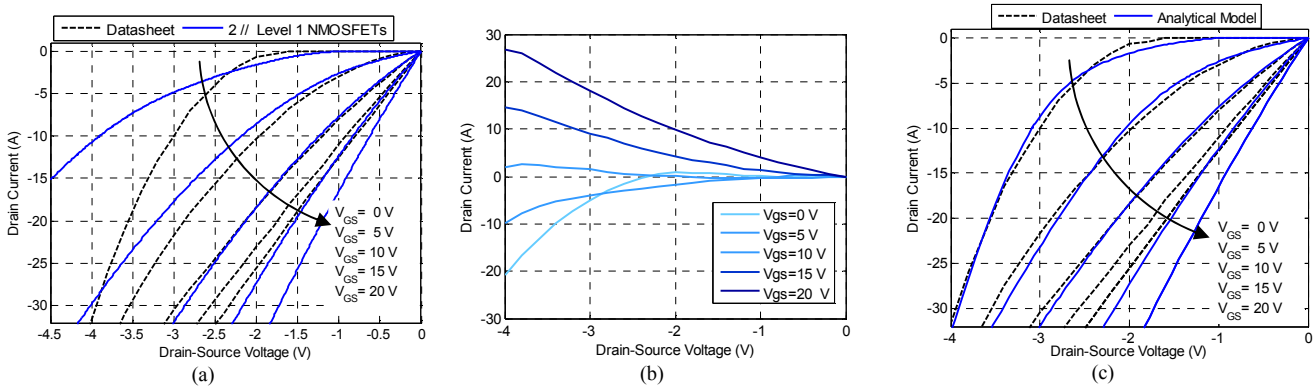


Fig. 4. (a) Reverse operation of both the *C2M0080120D* and the two inbuilt antiparallel diodes of the 2 // *Level* 1 NMOSFETs (b) ideal reverse properties of the additional electrical component and (c) *Analytical* model third quadrant characteristics.

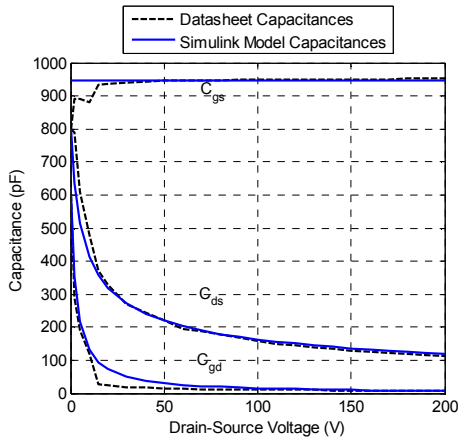


Fig. 5. *Analytical* model capacitance variation with voltage against the datasheet capacitances.

$$C_{DS} = \begin{cases} \dfrac{C_{DS0}}{\left(1+{v_{DS}}/{V_{th}}\right)^{m_{ds}}}, & v_{DS} > 0 \\ C_{DS0}\cdot\left(-{v_{DS}}/{\alpha}\right), & v_{DS} \le 0 \end{cases} \quad (3)$$

$$C_{DG} = \begin{cases} \dfrac{C_{DG0}}{\left(1-{v_{DG}}/{V_{th}}\right)^{m_{dg}}}, & v_{DG} > 0 \\ C_{DG0}\cdot\left(-{v_{DG}}/{\alpha}\right), & v_{DG} \le 0 \end{cases} \quad (4)$$

III. SWITCHING PERFORMANCE

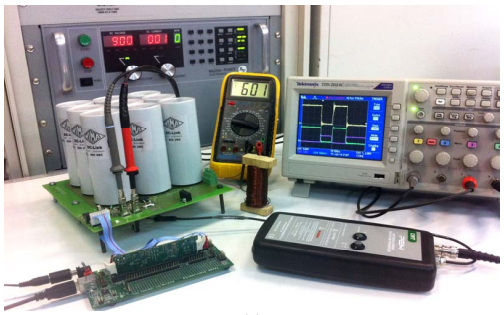
The credibility of the developed model in transients is confirmed through both experimental testing and comparison with similar models in commercially available simulation platforms.

A. *Double Pulse Tester Setup*

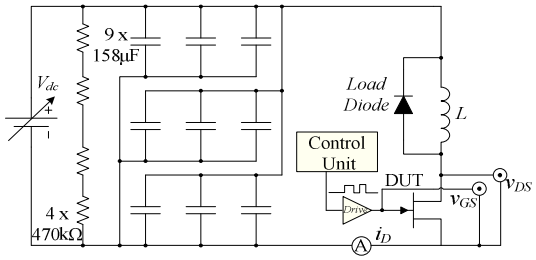
The experimental setup for validating the performance of the developed model is a typical Double Pulse Tester (DPT), illustrated in Fig. 6. In order to minimize drain path parasitic inductances, the parallel-plates design technique has been adopted for the two-layer printed circuit board (PCB). The voltage source is formed by nine polypropylene film capacitors (*DCP5N06158D200KS00*) exhibiting extremely low internal series resistance (ESR). The load consists of a 710 μH inductor and an antiparallel SiC Schottky diode (*C2D10120A*) placed as close as possible to the device under test (DUT). Two BNC connectors mounted on top of the PCB are used to measure the high frequency v_{GS} and v_{DS} voltages avoiding the use of a probe grounding clip. A 30 MHz bandwidth Rogowski coil is utilized for the i_D measurement, avoiding any interjection at the main power loop. All measurements are performed with a 10 Ω gate resistor (R_g) and in ambient temperature. The components used for this experiment are listed in TABLE III.

B. *Synopsys SaberRD*

To ensure the validity of the *Analytical* model, it is considered appropriate to compare it against similar models in commercially available simulation platforms. For this purpose, the Synopsys SaberRD is chosen, being one of the most advanced and reliable programs for power semiconductor device modeling.



(a)



(b)

Fig. 6. (a) Experimental setup for the switching characteristics of the *C2M0080120D* SiC power MOSFET. (b) DPT schematic.

The DPT setup of Fig. 6(b) is simulated in SaberRD utilizing the embedded SiC MOSFET model [7], [12] with the parameter values summarized in TABLE IV. Note that the default values are kept for all other parameters not included in TABLE IV. The inbuilt *APT2X61D60J* is selected as the antiparallel diode of the inductor [13]. This choice is justified, since the particular Si diode exhibits ultra fast recovery times, similar to those of the SiC Schottky Diode of the experimental setup [14].

TABLE III. COMPONENT LIST FOR DPT EXPERIMENTAL SETUP

DC Power Supply	Magna Power TSA1000-20
Oscilloscope	*Tektronix* TDS2024C
10:1 voltage probe	*Agilent Technologies N2862A*
100:1 voltage probe	*B&K Precision* PR2000B
Current Probe	*PEM* Rogowski Coil CWT6 Ultra-mini
Control Unit	*Texas Instruments* TMS320F28335

TABLE IV. PARAMETER VALUES OF SYNOPSYS SABERRD SIC MOSFET

wb	$20\cdot10^{-4}$	*kp*	1.3662
nb	$3.8\cdot10^{15}$	*cgs*	$945\cdot10^{-12}$
a	0.1222	*coxd*	$600\cdot10^{-12}$
agd	0.0281	*tnom*	27
vt	3	*vbigd*	2.8
rs	0.02	*kfl*	0.5
theta	0.02689	*pvf*	0.51988
kf	5	*dvtl*	1.4

C. Switching Performance Validation

The performance of the developed *Analytical* model during transient phenomena is depicted in Fig. 7 against both SaberRD and experimental results (DPT of paragraph A). Remarkable accuracy is observed in all v_{GS}, v_{DS} and i_D waveforms.

Simulation and experimental results regarding the turn-on and turn-off switching losses are depicted in Fig. 8. The response of the developed Simulink model is in agreement with the switching performance of the SiC MOSFET, while exhibiting similar accuracy as SaberRD. Some discrepancies observed at the v_{DS} voltage during turn-off are attributed to an incomplete model of the antiparallel load diode [15], [16]. Such modeling is beyond the scope of this paper. The oscillatory behavior observed during turn-on is attributed to small variations of the parasitic component values.

I. Single Phase Inverter Application

A fully functional, single phase inverter, illustrated in Fig. 9, has been developed in the lab to validate the dependability of the *Analytical* model. The nominal output power of the system is 1 kW and the input voltage is 250 V. Four 30 μF

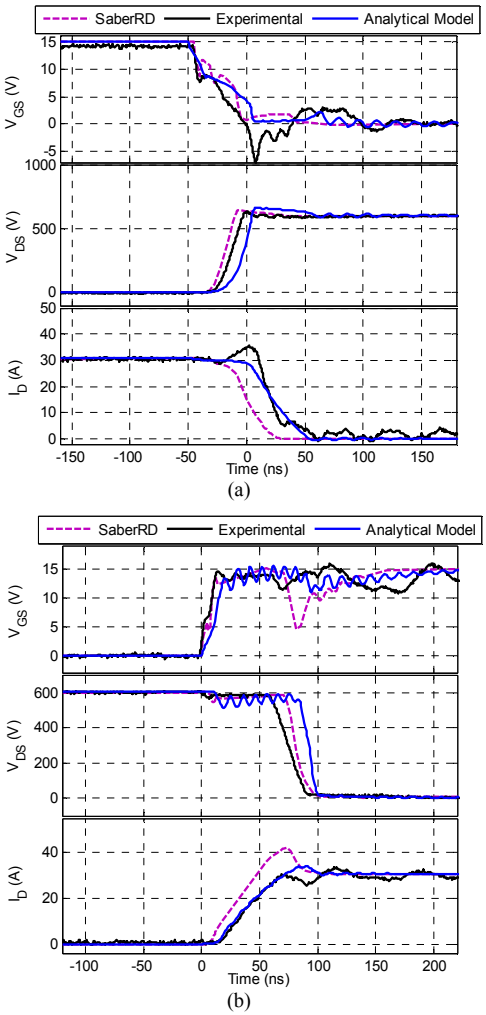


Fig. 7. Simulation and experimental results for (a) turn-off and (b) turn-on transients of the SiC DMOSFET.

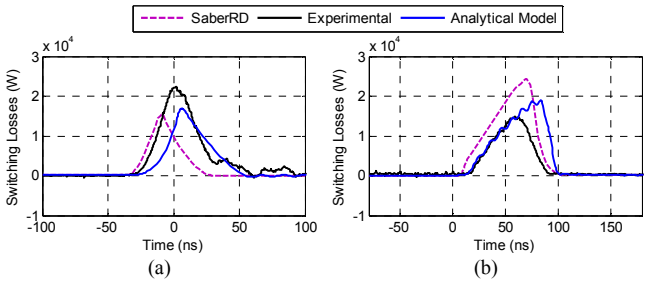


Fig. 8. Simulation and experimental results of switching losses during (a) turn-off and (b) turn-on of the SiC DMOSFET.

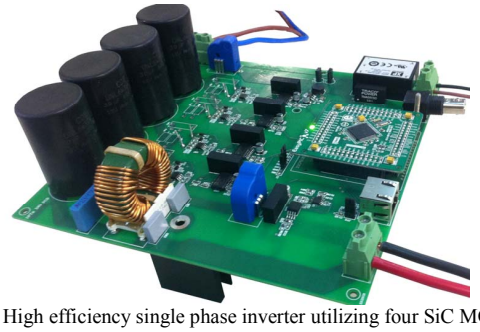


Fig. 9. High efficiency single phase inverter utilizing four SiC MOSFETs.

polypropylene film capacitors (*UNL6W30KF*), ideal for high switching frequency operation, constitute the DC link capacitor bank. The load consists of a series connection of a 17 Ω resistor and a 5.7 mH inductor. The power supply of all driving circuits is set to 20 V. All SiC MOSFETs are located at the bottom of the PCB, mounted on a heat sink, the temperature of which is constantly monitored. A simple sinusoidal pulse width modulation (SPWM) technique is adopted having a carrier frequency of f_{sw} = 50 kHz and a reference frequency of f_{ref} = 50 Hz. The modulation index m_a is kept constant at 0.8. The input current, DC voltage and output current are monitored and transferred to the microcontroller's (*PIC33EP512MU810*) analog pins.

A. Power Loss Calculation

An infrared (IR) camera (*FLIR* E60) is utilized to measure the temperature increase of the heat sink (ΔT) and thus, the power losses (P_L) of the inverter prototype. In order to obtain an accurate formula for the $P_L - \Delta T$ relation, thermal calibration needs to be performed [17]. All four power switches are connected in parallel and the duty cycle of their driving signal is set to 100% [18]. Simultaneously, the gate voltage is significantly reduced so that the power device operates at the moderate inversion region. From the experimental results illustrated in Fig. 10, a linear relation between the dissipated power and the temperature increase is observed with almost unity gradient (λ = 0.9629). Two thermal images of the inverter during power-off mode and operation under nominal conditions are presented in Fig. 11. An increase of 19.6 K from the initial room temperature (i.e. 304.75 K) is recorded at 1 kVA output power, corresponding to 18.9 W power losses according to the thermal calibration (98.11 % efficiency).

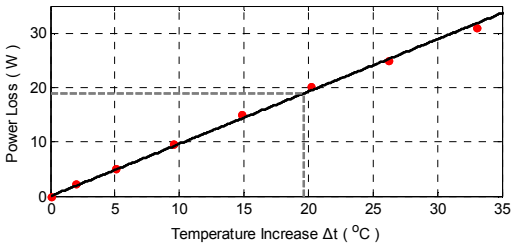
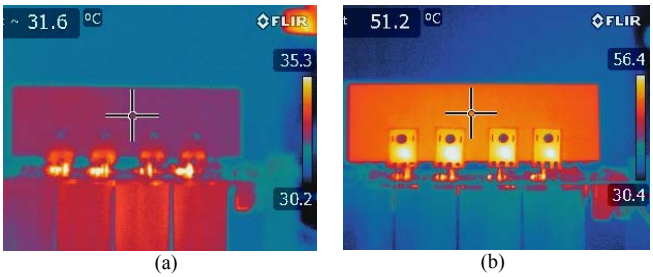


Fig. 10 Characteristic curve of inverter power losses versus heat sink temperature increase.



(a) (b)

Fig. 11. Thermal image of the inverter heat sink in (a) standby mode and (b) during operation at 1 kVA.

B. Simulation Results

The single phase inverter setup described above is subsequently simulated in Matlab under exactly the same operating conditions and utilizing the *Analytical* model. The corresponding block diagram is presented in Fig. 12. By selecting the variable-step solver *ode23t* and setting the maximum step size to 5 ns, the total power loss on the semiconductor devices is 18.3 W (98.17 % efficiency). The difference between experimental and simulated inverter efficiency is negligible (0.06 %) and hence, the notable performance of the developed model is confirmed.

II. Conclusions

A stand-alone SiC DMOSFET model has been proposed for simulating high efficiency converters for industry applications, in Matlab/Simulink software. The parameters of the two inbuilt *Level* 1 NMOSs, constituting the SiC DMOSFET model, have been extracted through explicit nonlinear curve fitting. A nonlinear resistor has been combined with the two *Level* 1 NMOSs to capture the reverse properties of the SiC DMOSFET. The *Analytical* model is ideal for simulations of real life converters in a variety of topologies, control strategies and operating conditions. This enables the user to accurately calculate power losses and transient phenomena. The exceptional static and dynamic performance of the proposed model is verified through comparison with a commercially available simulation platform and experimental results. The *Analytical* model was eventually validated on an experimental high frequency inverter, whose losses were calculated with remarkable accuracy.

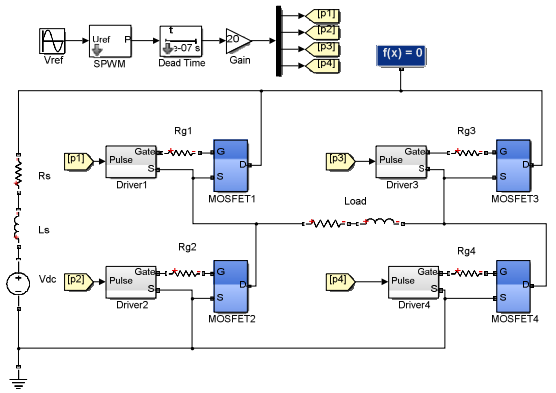


Fig. 12. Block diagram of the simulated single phase inverter in Matlab/Simulink.

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