Advanced Power Electronic Devices Based on Gallium Nitride (GaN)

Daniel Piedra*, Bin Lu+, Min Sun*, Yuhao Zhang*, Elison Matioli*, Feng Gao*, Jinwook (Will) Chung*, Omair Saadat+, Ling Xia+, Mohamed Azize+, and Tomás Palacios*+

*Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139, USA
+Cambridge Electronics, Inc. (CEI), 14th floor, One Broadway, Cambridge, MA 02142, USA
†Phone: +1 617-710-7013, †E-mail: tpalacios@gantechnology.com

Abstract

It is the most exciting time for power electronics in decades. The combination of new applications, such as microinverters, electric vehicles and solid state lighting, with the new opportunities brought by wide bandgap semiconductors is expected to significantly increase the reach and impact of power electronics. This paper describes some of the recent advances on developing power devices based on Gallium Nitride (GaN), the key design constrains, and the process to take a new device material and structure from the research laboratory of universities to full commercialization.

Introduction

The intrinsic material properties of Gallium Nitride (GaN) make it an ideal material for the future of power electronics. The combination of high electron mobility and critical electric field enables the fabrication of devices with specific on resistances up to 1000-fold better than in Si-based devices. This allows efficient high voltage (>100 V) switching at MHz frequencies (0.1-20 MHz), which significantly increases the power density of power converters.

In spite of the great promise offered by GaN-based power electronics, the availability of commercial GaN devices is still very limited. This is due to the many challenges related to material quality, process compatibility with Silicon fabs, the fabrication of true-normally-off (or enhancement-mode, E-mode) devices, gate dielectric quality and traps, and circuit integration, among others. This paper will describe some of the key technologies we have been working on over the last 9 years at MIT and, since 2012, at Cambridge Electronics, Inc. (CEI), to take GaN from the university fab to full commercialization. We will also discuss new directions of research to improve the performance of GaN power devices even further, including new vertical device structures.

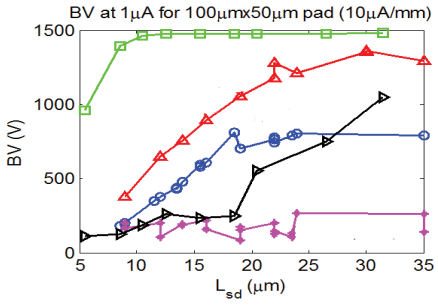

Fig. 1. Buffer breakdown voltage for wafers with different carbon doping concentration in the buffer. The higher the carbon, the higher the breakdown.

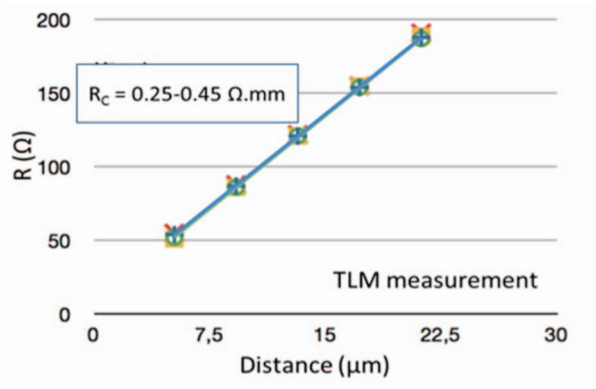

Fig. 2. TLM characterization of Au-free contact technology for GaN-based power transistors.

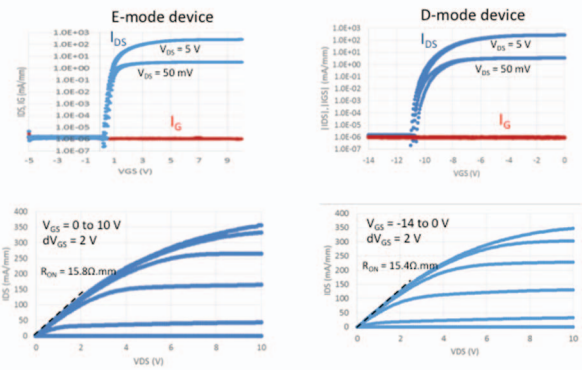

Fig. 3. Current-voltage characteristics for E-mode and D-mode GaN power transistors fabricated side-by-side on the same chip.

GaN Lateral Power Transistors

To make GaN power electronics a commercial success, it has to be cost competitive with Si-based power electronics. For this, GaN grown on 6" and 8" Si wafers is a must, as these wafer diameters allow the use of conventional Si fabrication infrastructure. The growth of high quality GaN on Si is however very challenging,

especially when trying to optimize the trade-off between breakdown voltage, GaN thickness, and current collapse. Fig. 1 shows the buffer breakdown of GaN buffer layers with different carbon concentration. As the carbon concentration increases, the breakdown also increases at the expense of current collapse (not show).

It is also important that the fabrication technology is optimized to allow Au- and lift-off-free processing. A Ti/Al-based metallization with optimized annealing and recess has been used to achieve state-of-the-art contact resistances and devices on 6" GaN-on-Si wafers processed in a Si fab (Fig. 2). Both enhancement-mode (E-mode) and depletion-mode (D-mode) transistors are integrated side-by-side (Fig. 3). This close integration is critical for the development of monolithic power management chips. The threshold voltage in the E-mode devices needs to be larger than 1 V for noise and ringing immunity (Fig. 4). In addition, an optimized gate dielectric allows hysteresis-free transfer curves up to V_{GS} of 10 V, which increases the compatibility with Si drivers. 150 V and 650 V-class transistors have been fabricated. In these devices, the field-termination is very important to ensure minimum leakage current all the way to the hard-breakdown event (Fig. 5).

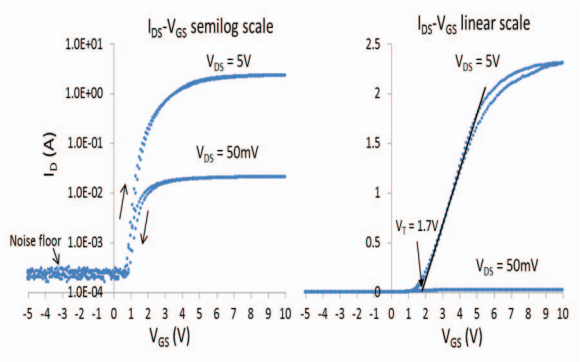

Fig. 4. Transfer characteristics of GaN E-mode power transistors. An optimized gate dielectric allows gate voltage swings up to 10 V with minimum hysteresis.

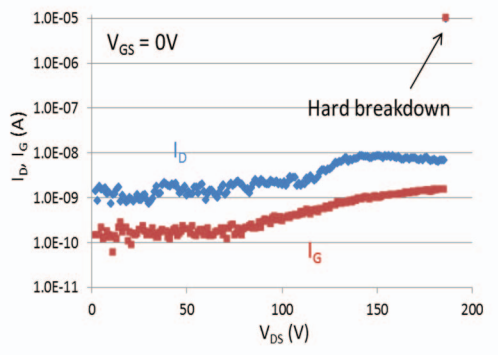

Fig. 5. Drain and gate leakage characteristics of 150-V-class GaN E-mode power transistor.

Long-term device reliability is critical for successful commercialization. A number of degradation mechanisms, such as inverse piezoelectric effect, peak electric field and hot electron damage, have been shown in the past to impact reliability. Among them, electrochemical oxidation plays a key role in inducing macroscopic defects and pits next to the gate electrode after long-term stress in the off-state (Fig. 6). With proper passivation and field management, very stable devices have been achieved (Fig. 7).

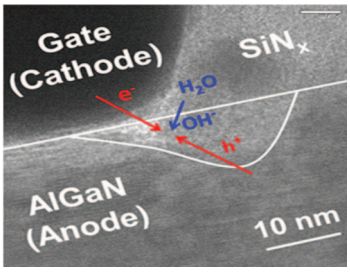

Fig. 6. Scanning electron micrograph (SEM) image of the AlGaN/Gate/SiN junction. At this junction, an electrochemical cell forms under reverse bias conditions and oxidizes the AlGaN surface, creating pits on the surface of the device [1].

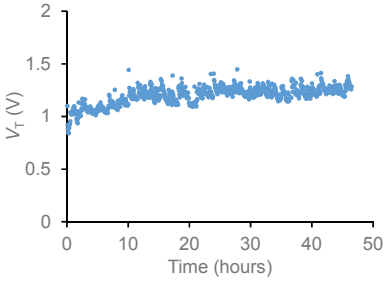

Fig. 7. Variation of the threshold voltage as a function of time for a typical E-mode GaN power transistor.

DC and, even, pulsed IV performance data are not enough to ensure the proper operation of GaN power switches. It is necessary to also evaluate their behavior under switched conditions to understand the impact of dynamic on-resistance. Fig. 8 shows a GaN-based 8 MHz power converter with efficiencies close to 96% over a broad range of power levels. Proper design of the field-plate structures was key to achieve this efficiency.

In addition to excellent performance, one of the main advantages of lateral devices is that they allow for complex circuit integration, not only with other GaN transistors, but also with Silicon-based CMOS electronics, as shown in Fig. 9. The new opportunities brought by this heterogeneous integration will enable a new generation of power processing circuits and systems over the next few years.

GaN Vertical Power Transistors

In spite of the excellent performance of lateral GaN devices, theoretical considerations indicate that vertical GaN transistors offer the ultimate power density management capability, as shown in Fig. 10. This is due to a much more uniform heat generation, thanks to the vertical current path in these devices. Unfortunately, the bulk GaN substrates traditionally used for GaN vertical devices are expensive and their small diameter precludes the use of state-of-the-art Si fabs for device fabrication,

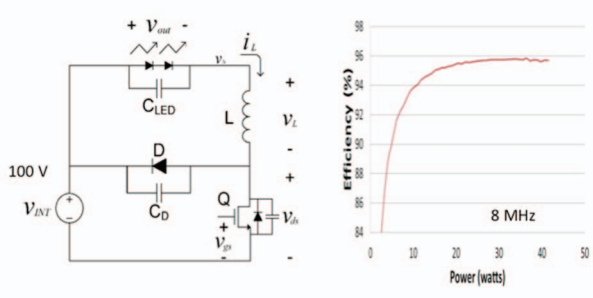

Fig. 8. Circuit diagram and efficiency *vs* output power curve of a GaN-based power converter to drive solid state lighting applications [2].

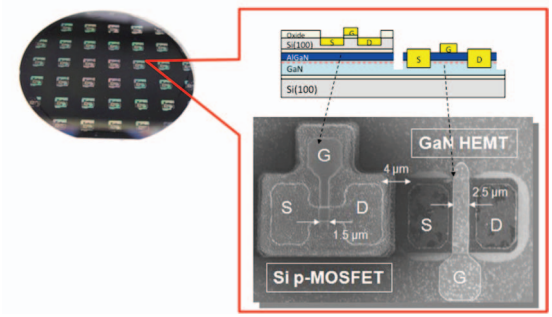

Fig. 9. Optical image and SEM detail of a hybrid wafer where Silicon (100) transistors are seamlessly integrated with GaN devices [3].

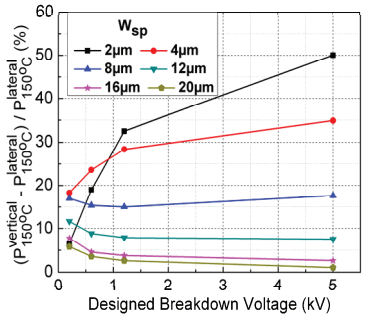

Fig. 10. Maximum power handling capability of GaN vertical transistors with respect to lateral devices, as a function of their breakdown voltage and minimum feature size. The maximum power is defined as the power at which the device channel temperature reaches 150 C [4].

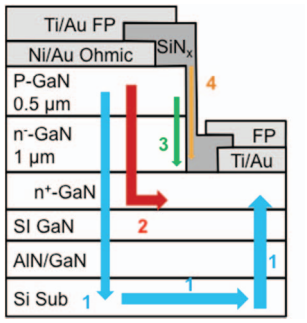

Fig. 11. Main leakage paths in a GaN vertical diode grown on a silicon wafer.

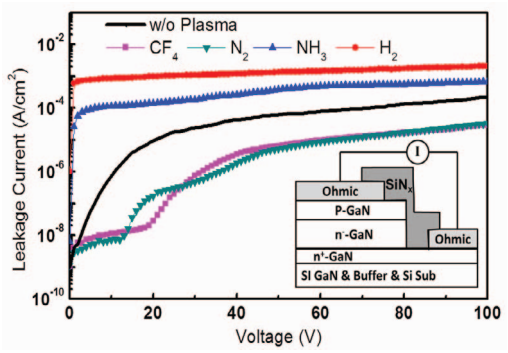

Fig. 12. Leakage current of the structure with different sidewall plasma treatments (CF_4, N_2, NH_3 and H_2) after GaN dry-etching. (inset) Structure for leakage current measurements.

which further increases the device cost.

At MIT, we are developing a new generation of vertical GaN devices on Si substrates to take advantage of the high power density of vertical devices, at the cost-point of silicon. One of the main challenges for these devices is the high off-state leakage current. Fig. 11 shows the different paths that this off-state leakage current can take. Out of these, the leakage through the GaN sidewall was found to dominate our first generation of GaN vertical diodes. Once that this sidewall was passivated with a novel plasma-based surface treatment, vertical GaN power diodes on Silicon were fabricated with better off-state leakage current levels than lateral devices (Table 1). This opens a path towards the use of these new vertical devices in commercial applications.

Conclusion

GaN technology has evolved tremendously over the last few years. GaN-only normally-off transistors are now commercially available from CEI with gate voltage swings (+/- 10 V) that make them compatible with standard Silicon gate drivers. In addition, the integration of both E-mode and D-mode GaN devices, as well as Silicon devices, on the same chip brings unprecedented flexibility to circuit designers. In parallel, novel technologies are

quickly improving the performance and lowering the cost of vertical GaN devices. Although this vertical technology is still not ready for insertion into commercial systems, it may play an important role in the future.

Acknowledgement

The work presented here has been partially supported by the ARPA-E ADEPT and SWITCHES programs, the DOE GIGA project, as well as the ONR PECASE project. CEI's effort was partially funded by an ONR SBIR grant. The design and fabrication of the power converter for solid state lighting applications was done by Prof. Perreault's group at MIT.

Reference

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Diode Structure	Leakage Current (Density) at -200 V	I_{on}/I_{off} ratio	Available Substrate	Substrate Cost per CM^2
GaN-on-Si Vertical Diodes (This work)	< 1 μA (10^{-4} -10^{-3} A/cm^2)	~ 10^6	200 mm Si	~ $0.08
GaN-on-Sapphire Vertical Diodes [5]	10^{-3} A/cm^2	~ 10^5	100 mm Sapphire	~ $2.2
GaN-on-GaN Vertical Diodes [6]	10^{-5} – 10^{-6} A/cm^2	~ 10^9	50 mm GaN	~ $100
AlGaN/GaN Lateral Diodes [7]	10^{-2} A/cm^2 [4]	~ 10^5	200 mm Si	~ $0.08
Si Diode (NTE 588)	5 μA	~ 10^6	200 mm Si	~ $0.08
SiC Diode (APT6SC60K)	< 1 μA	~ 10^6	75 mm SiC	~ $6

Table 1. Leakage current and on/off current ration for different lateral and vertical power technologies.