APEC 2016 LONG BEACH California March 20-24, 2016
LONG BEACH CONVENTION & ENTERTAINMENT CENTER

iDrive

Navitas

Breaking Speed Limits with GaN Power ICs

March 21st 2016

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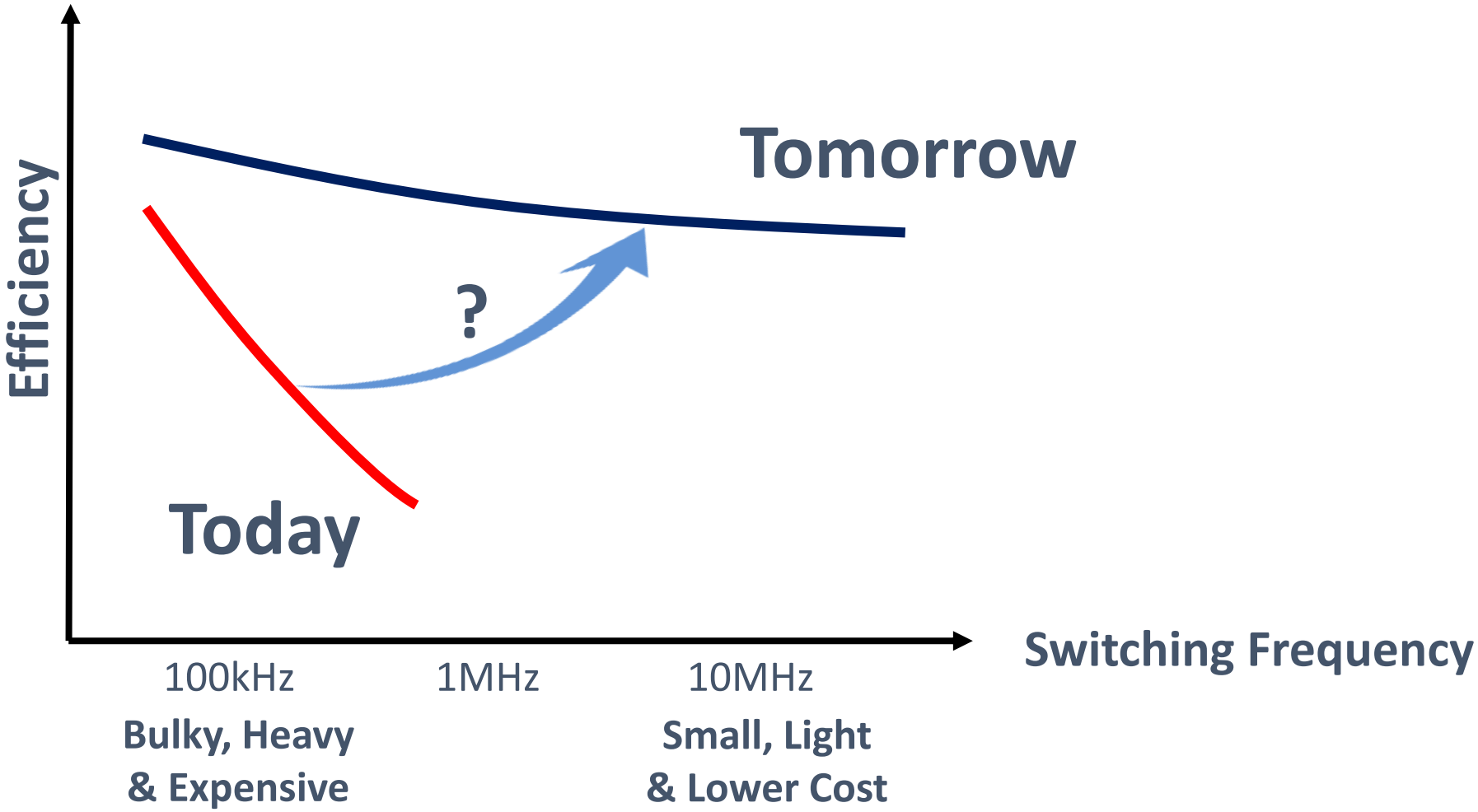
The Need for Speed

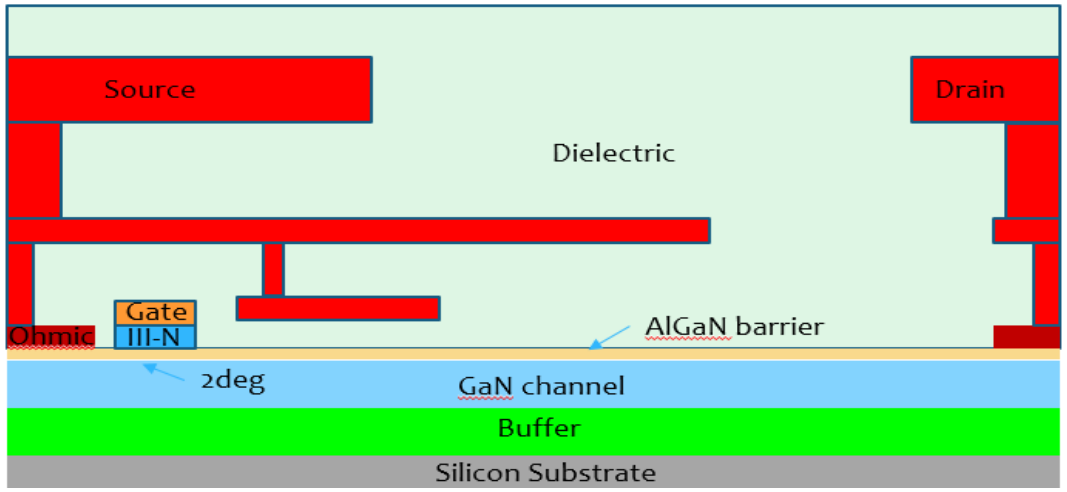


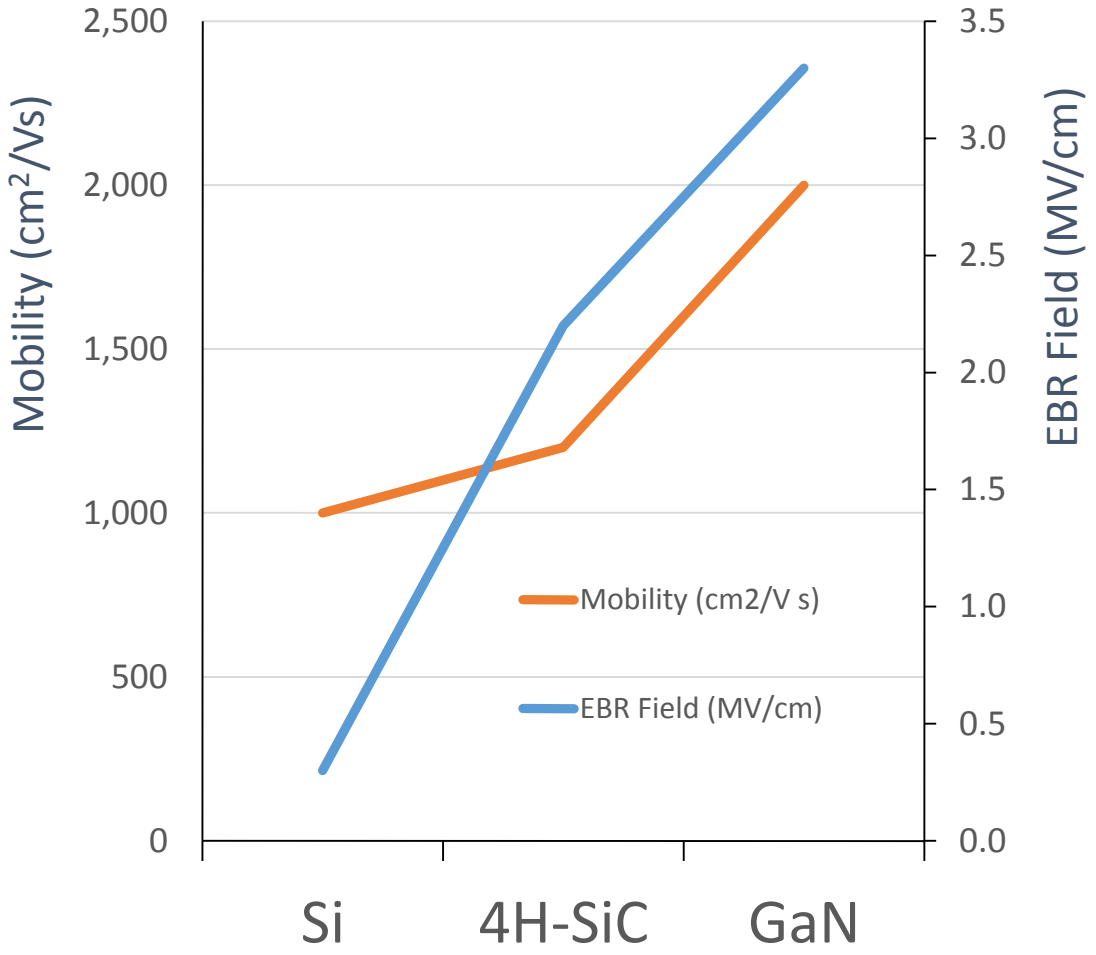
What is Slowing Us Down?

Wide Bandgap (WBG) Devices:

Physics Drives Switch Performance

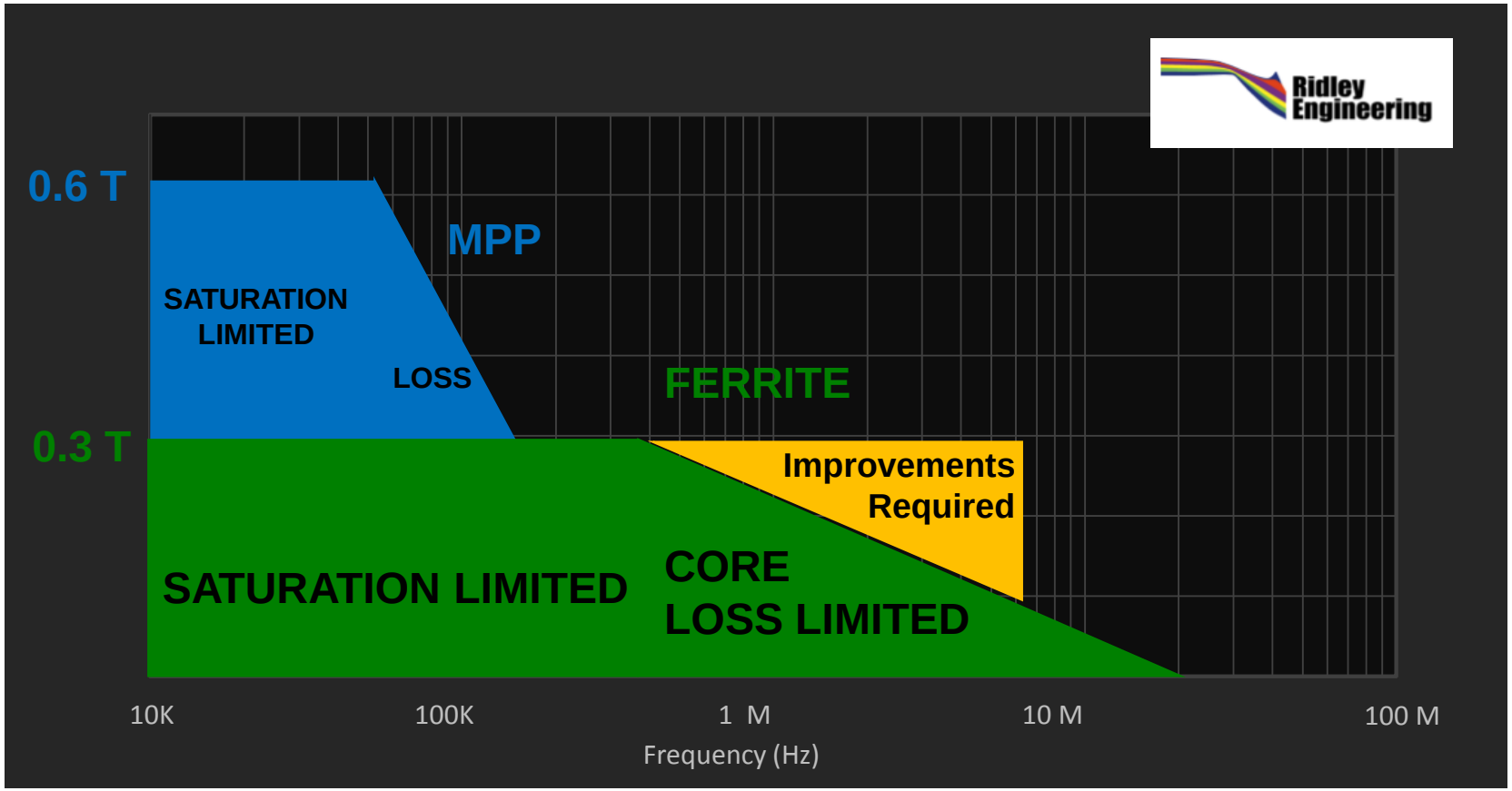
- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low Q_g and Q_{OSS} and allows integration





Can Magnetics Rise to the Speed Challenge?

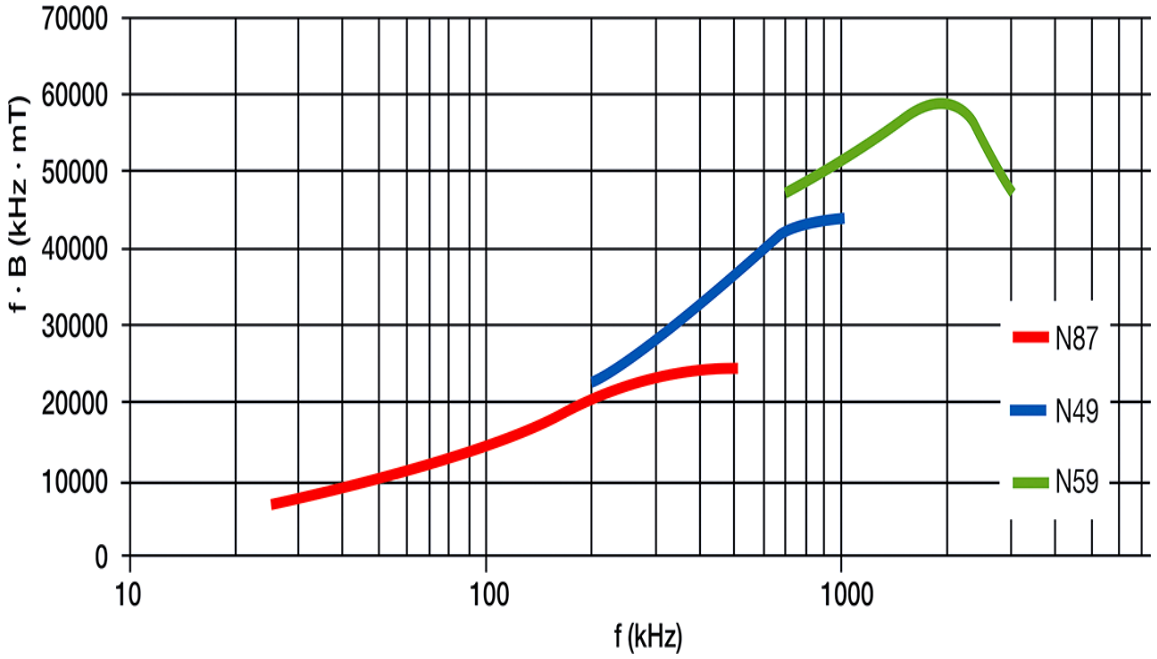
- Boundaries vary with material, DC/AC current mix, power, etc.
- Majority of mass production applications run 65kHz – 150kHz
- 5x frequency increase is within today's capability



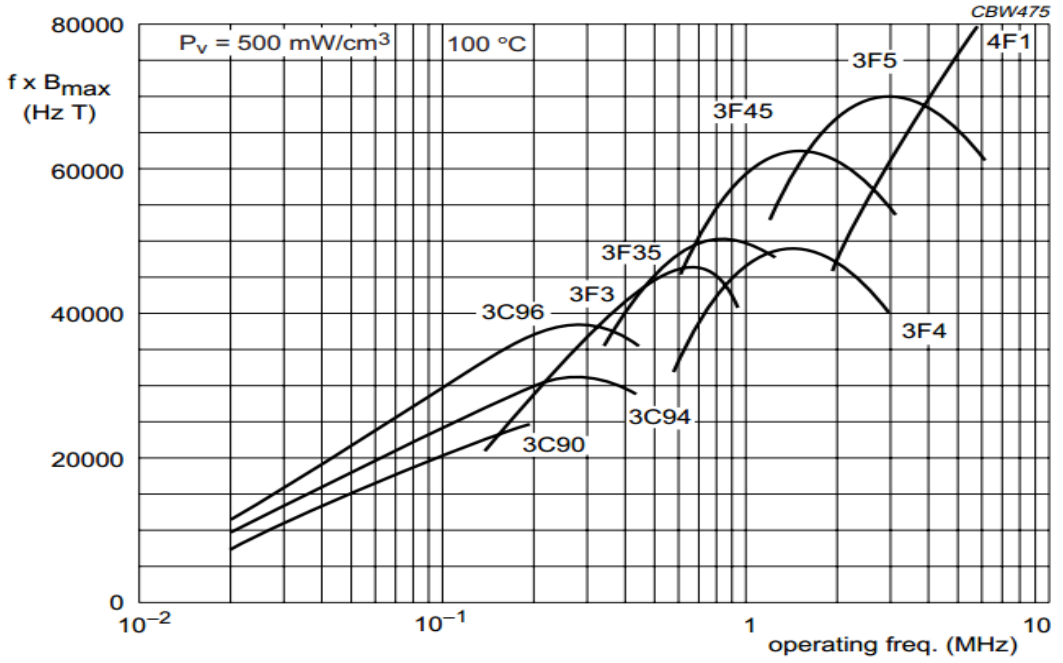
Removing speed limits:

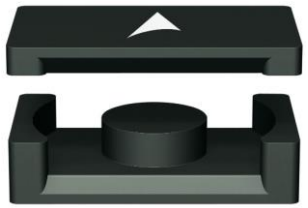
High Frequency Magnetics “GaN Optimized”

N59 optimized for 2MHz

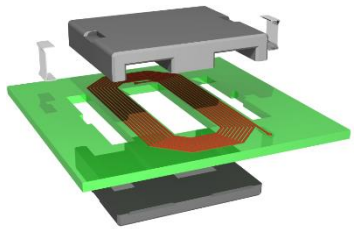


3F & 4F up to 10MHz





TDK



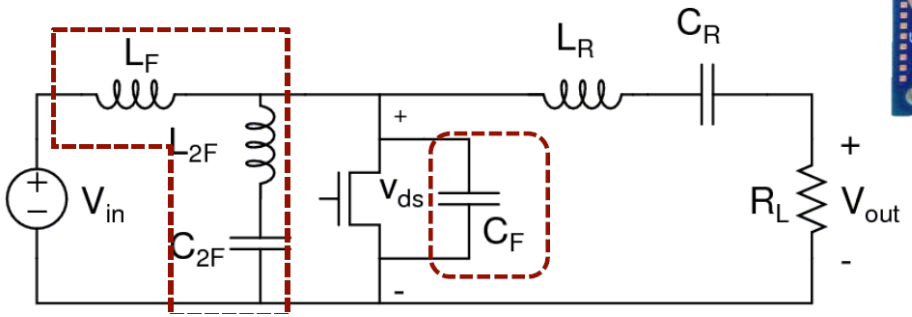
PRECISION INCORPORATED

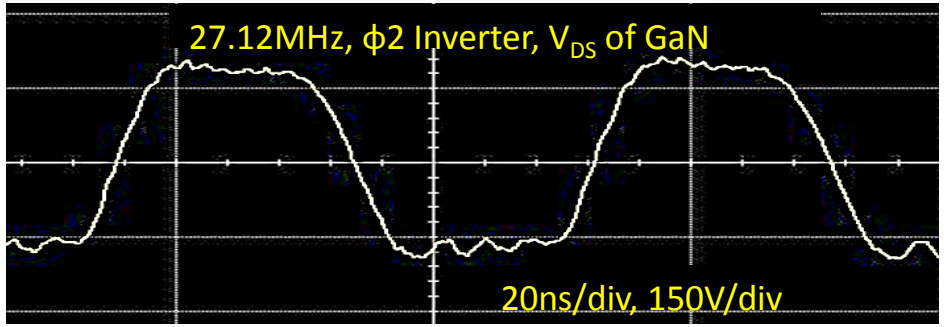
Breaking Speed Limits:

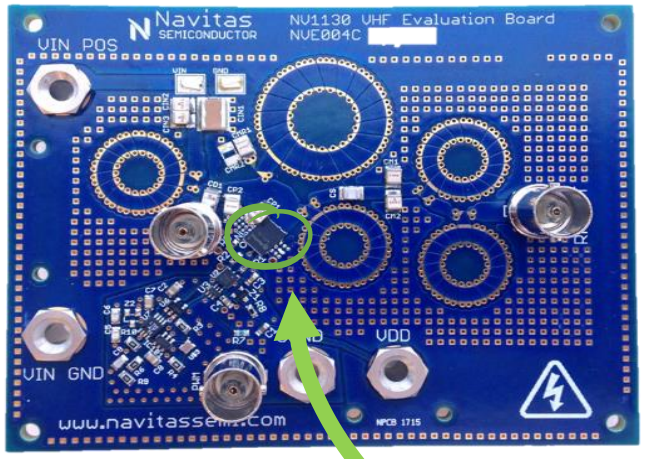
650V Navitas eMode GaN at 27MHz & 40MHz

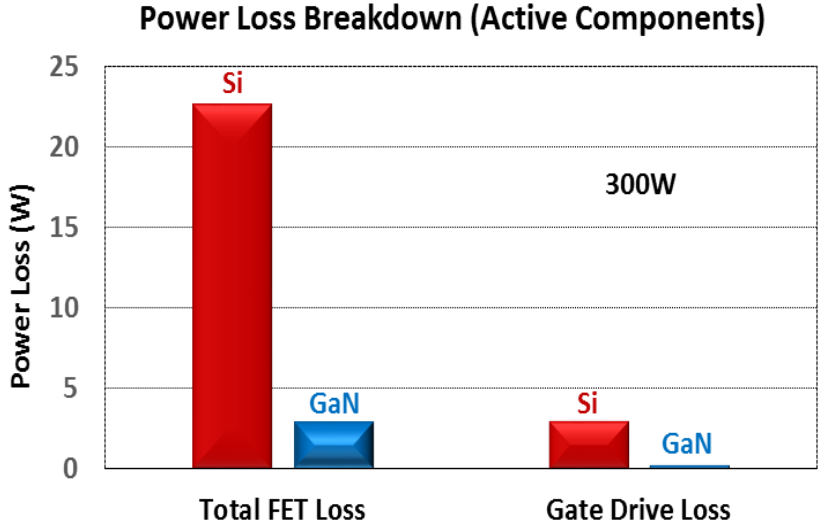
Class Phi-2 DC/AC converter: Stanford / Navitas demo

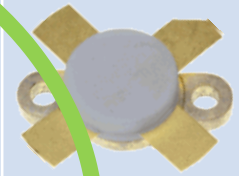
- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss



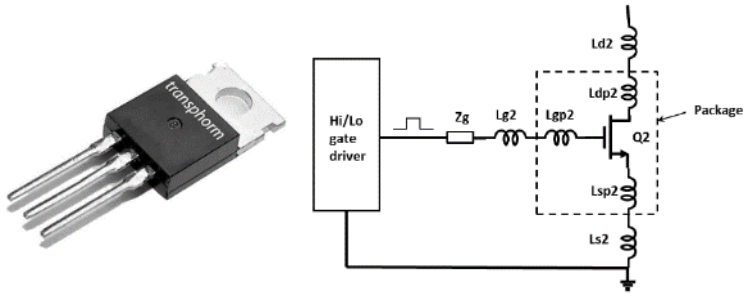




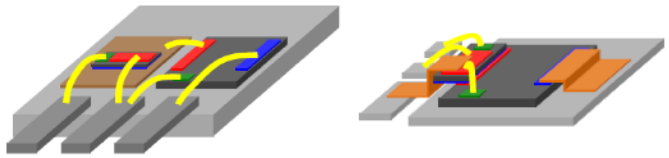


Technology	V	Pack (mm)		F_{SW} (MHz)	Eff. (%)	Power (W)
RF Si (ARF521) Microsemi POWER PRODUCTS GROUP	500	M174 22x22		27.12	91%	150
eMode GaN Navitas	650	QFN 5x6		27.12	96%	150
				40.00	93%	115

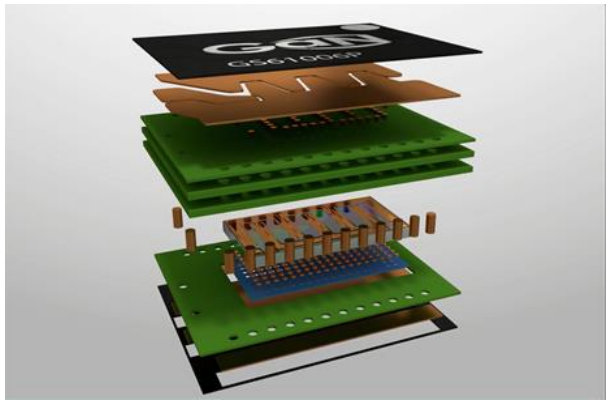
Slow, Expensive, Non-Standard



- **Through-hole**
  - High inductance, limits switching frequency



- **Cascode** (co-pack and/or stacking)
  - Multi-die, additional components
  - Higher cost for dice and assembly

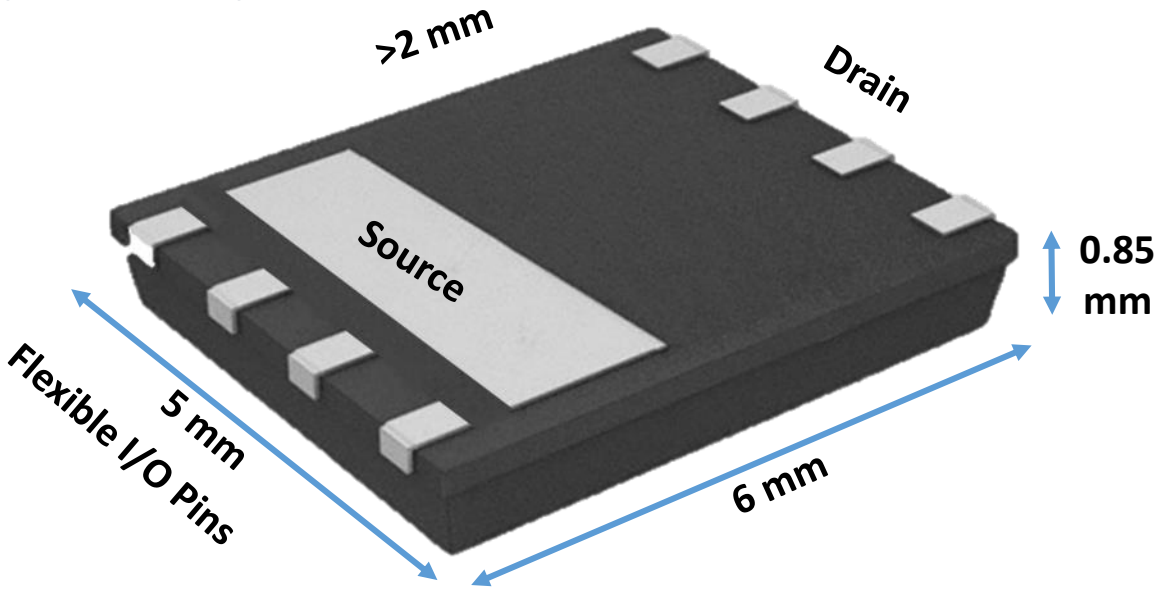


- **PCB-embedded**
  - Non-standard, high cost

Removing Speed Limits:

Fast, Low Cost, Industry-Standard QFN

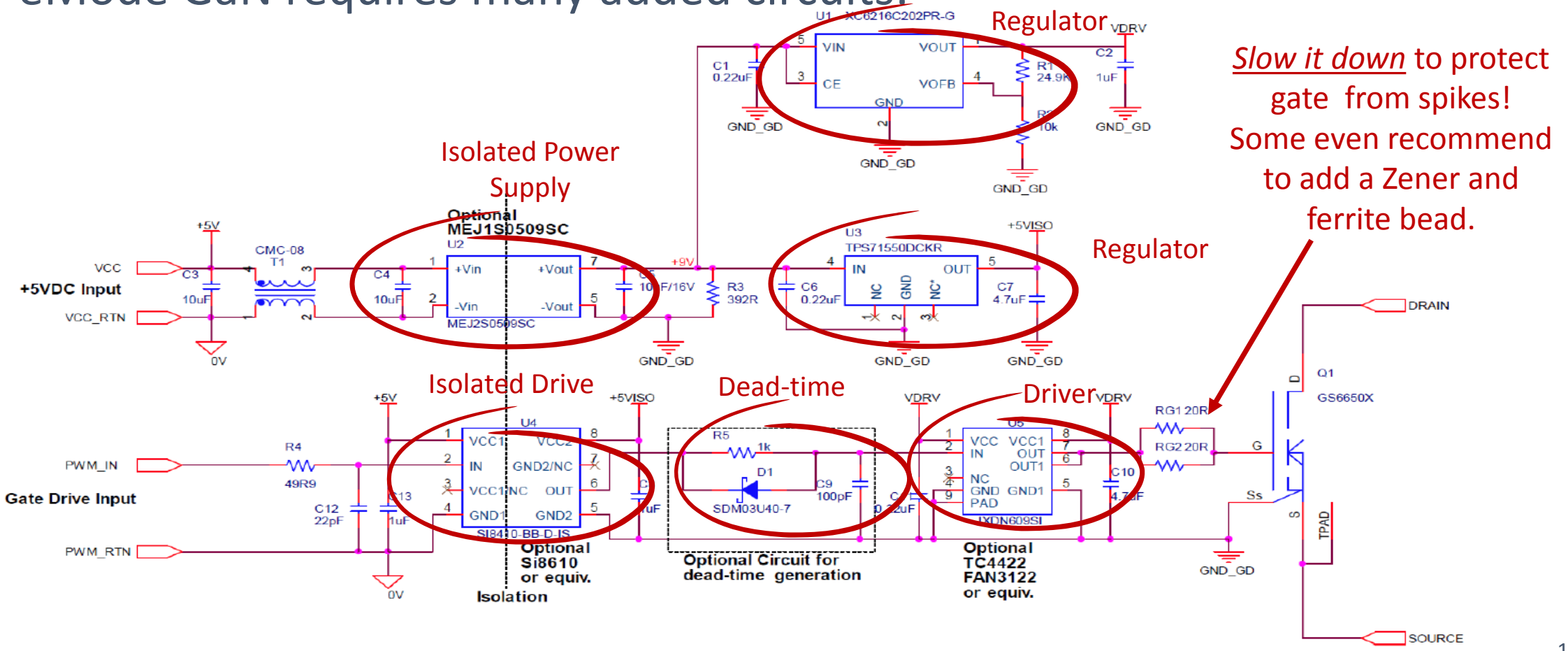
- Leadframe-based 5X6mm power package outline
- Low profile, small footprint with HV clearance
- Kelvin source connection for gate drive return
- Low inductance power connections (~0.2nH)
- Low thermal resistance (<2°C/W)
- I/O pins enough for drive functions
- High volume
- Reliable
- Low cost



Speed Limit:

Complex Drive

- dMode GaN needs extra FET, extra passives, isolation, complex packaging
- Early eMode GaN requires many added circuits:



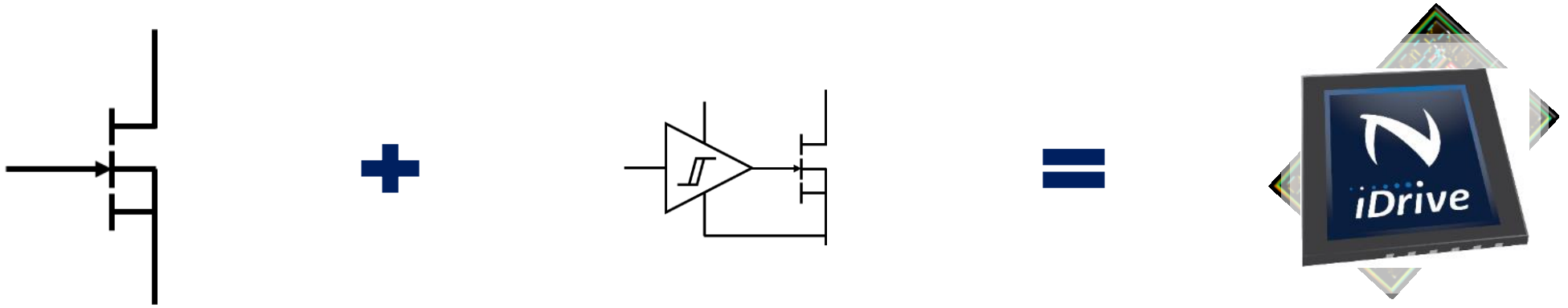
Ref: GaN Systems Application note GN001 Rev 2014-10-21

Creating the World's First allGaN™ Power ICs

Fastest, most efficient
GaN Power FETs

iDrive First & Fastest
Integrated GaN Gate Driver

World's First
allGaN™ Power IC

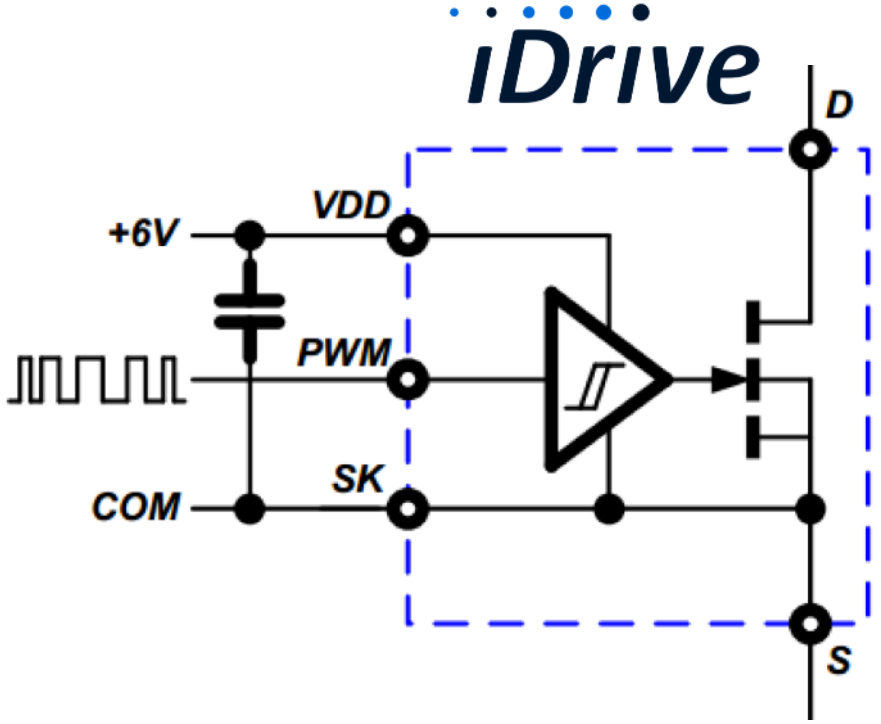


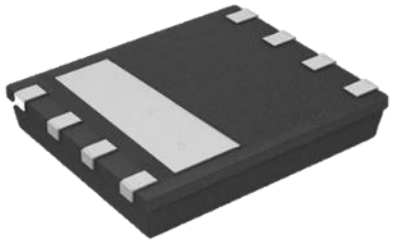
Up to 40MHz switching, 4x higher density & 20% lower system cost

Removing Speed Limits:

Navitas iDrive™ GaN Power IC

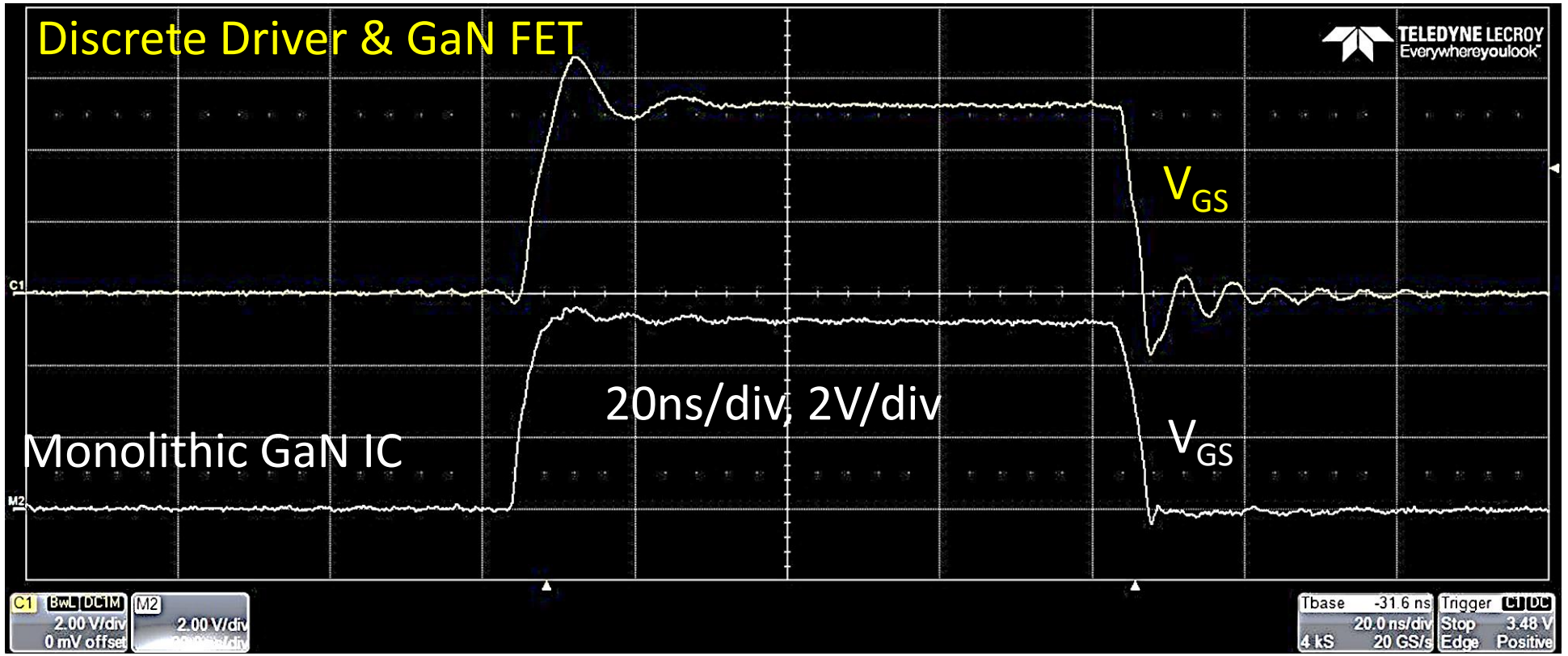
- **Monolithic** integration
- 20X lower drive loss than silicon
- Driver impedance matched to power device
- Shorter prop delay than silicon (10ns)
- Zero inductance turn-off loop
- Digital input (hysteretic)
- Rail-rail drive output
- Layout insensitive





iDrive Crisp & Efficient Gate Control

- Eliminates gate overshoot and undershoot
- Zero inductance on chip insures no turn-off loss



Hard-Switched

Primary Switch Power Loss:

$$P_{FET} = P_{COND} + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

Hard-Switched → Soft-Switched

Primary Switch Power Loss:

$$P_{FET} = P_{COND} * k + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓2-3X (silicon devices can have high Coss charging/discharging losses)

Hard-Switched → Soft-Switched with eMode GaN

Primary Switch Power Loss:

Minimized Reduced

$$P_{FET} = P_{COND} * k + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10X ~~2-3X~~ (GaN Coss charging/discharging loss negligible up to 2Mhz)
- P_{DRIVER} ↓10X (GaN P_{DR} negligible up to 2Mhz)
- P_{QRR} = 0
- P_{DIODE} ↓2X (reverse conduction loss reduced by synchronous rectification)
- $P_{T\text{-}OFF}$ = Reduced (limited by I-V crossover loss due to drive loop impedance)

Hard-Switched → Soft-Switched with GaN Power IC

Primary Switch Power Loss:

Minimized Minimized

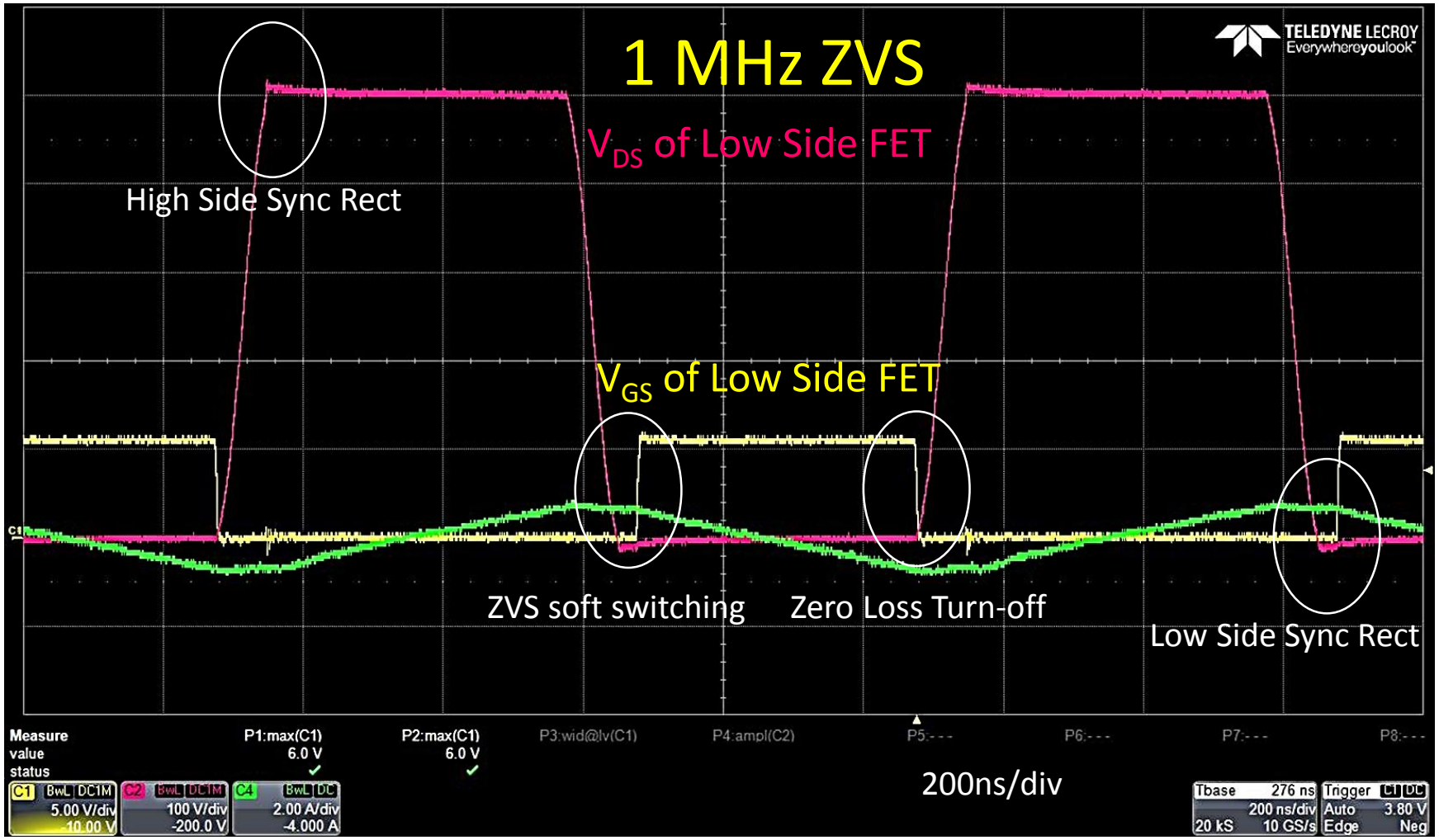
$$P_{FET} = P_{COND} * k + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10X ~~2-3X~~ (GaN Coss charging/discharging loss negligible up to 2Mhz)
- P_{DRIVER} ↓10X (GaN P_{DR} negligible up to 2Mhz)
- P_{QRR} = 0
- P_{DIODE} ↓3X ~~2X~~ (synchronous rectification with improved deadtime control)
- $P_{T\text{-}OFF}$ = 0 ~~Reduced~~ (near-zero drive loop impedance with integration)

>10x frequency increase possible with higher efficiencies

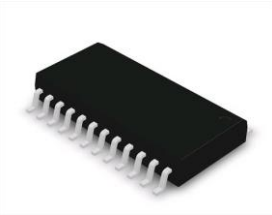
EMI: Smooth, clean, controlled waveforms

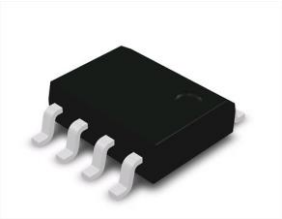
- 500V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- ZVS Turn-on
- Zero Loss Turn-off
- Sync Rectification
- High frequency
- Small, low cost filter

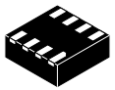


Removing speed limits:

MHz Controllers … with more, faster to come







PFC (BCM):
- L6562 (1MHz)
- NCP1608 (1MHz)
- UCC28061 (500kHz)

DC-DC (LLC):
- NCP1395 (1.2MHz)
- FAN7688 (500kHz) (+SR)
- ICE2HS01G (1MHz)

DC-DC (Sync Rectifier):
- NCP4305 (1MHz)
- UCC24610 (600kHz)

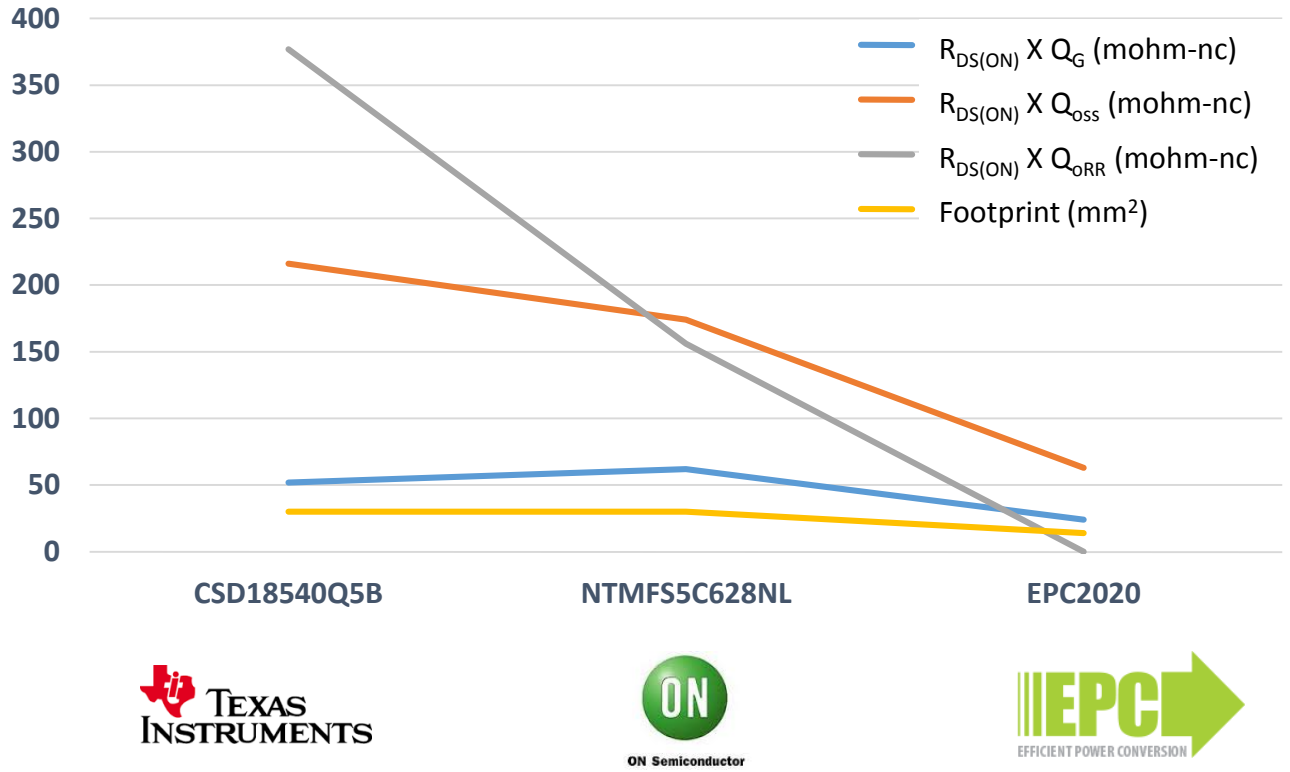
PWM:
- NCP1252 (500kHz)
- NCP1565 (1.5MHz)
- UCC28C44 (1MHz)
- UCC25705 (4MHz)

DSP
- UCD3138 (2MHz)
- dsPIC33xx (5MHz)
- ADP1055 (1MHz)

ANALOG DEVICES · FAIRCHILD · Infineon · MICROCHIP · ON Semiconductor · TEXAS INSTRUMENTS

Secondary Side SR FETs Get Better with GaN

- All relevant performance FOMs favor GaN at 60V
- $R_{DS(ON)}$ X Q_G reflects drive losses
- $R_{DS(ON)}$ X Q_{OSS} reflects turn-off losses with non-resonant rectification
- $R_{DS(ON)}$ X Q_{RR} reflects stored minority carrier turn-off losses
  - Minimized with deadtime control
- Silicon FETs are in QFN5X6 packages, GaN is WLCSP



Note: Taken from datasheet typicals at 4.5/5V gate drive and capacitance curves

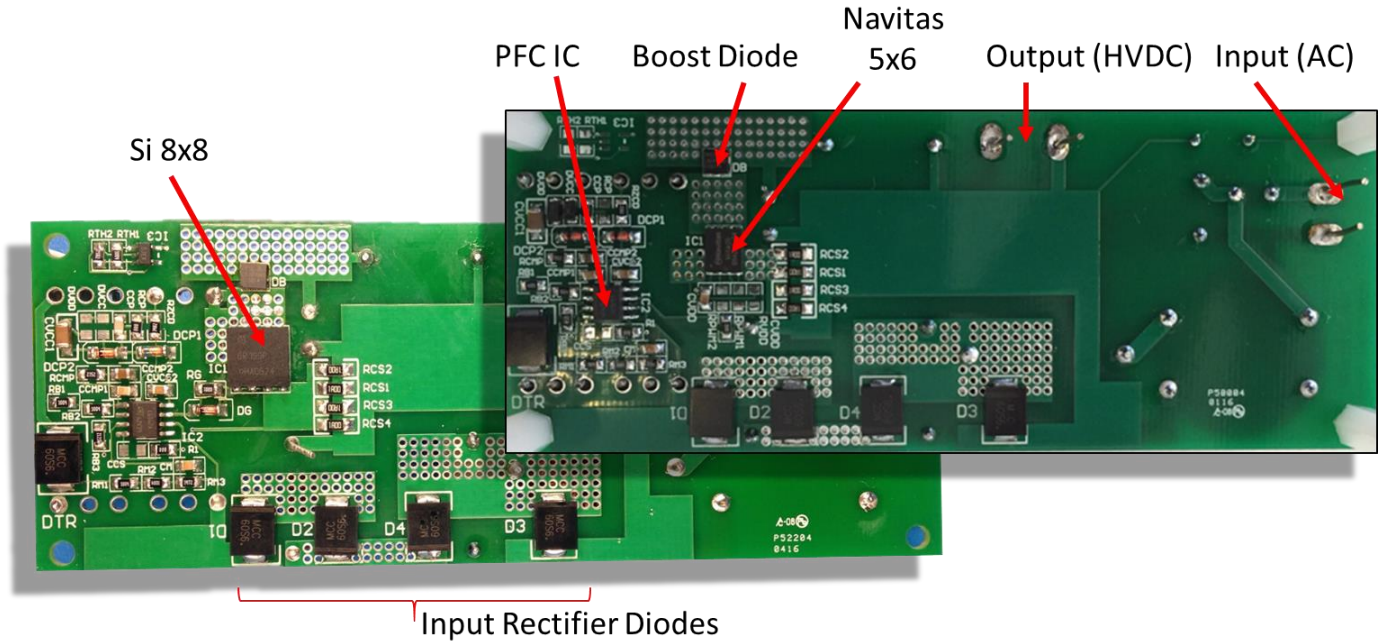
Speed test:
150W Boundary Conduction Mode (BCM) Boost PFC

- $120V_{AC}$ = 167-230kHz
- $220V_{AC}$ = 230-500kHz
- 265V peaks at 1MHz (L6562 F_{SW} max)

	Pack	$R_{DS(ON)}$ mΩ	Q_G nC	$C_{OSS}(er)$ pF	$C_{OSS}(tr)$ pF	$R*Q_G$ mΩ.nC	$R*C_{OSS}(tr)$ mΩ.pF	$R*C_{OSS}(er)$ mΩ.pF
Navitas with iDrive™	5x6	160	2.5	30	50	400	8,000	4,800
Si CP Series	8x8	180	32	69	180	5,760	32,400	12,400
Si C7 Series	8x8	115	35	53	579	4,025	66,600	6,100
GaN Benefits	>50%	n/a	>10x	>2x	>10x	>10x	>7x	>2.5x

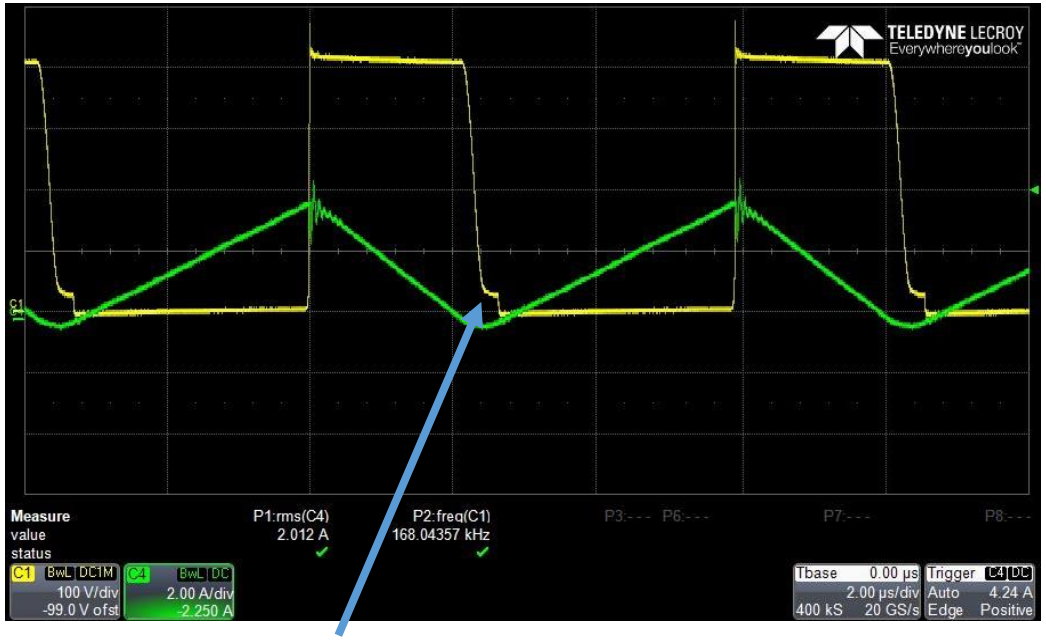
100 x 50 x 10mm with 2-layer, 2 oz Cu

No heatsinks, no forced air,
no glue, potting or heat spreaders

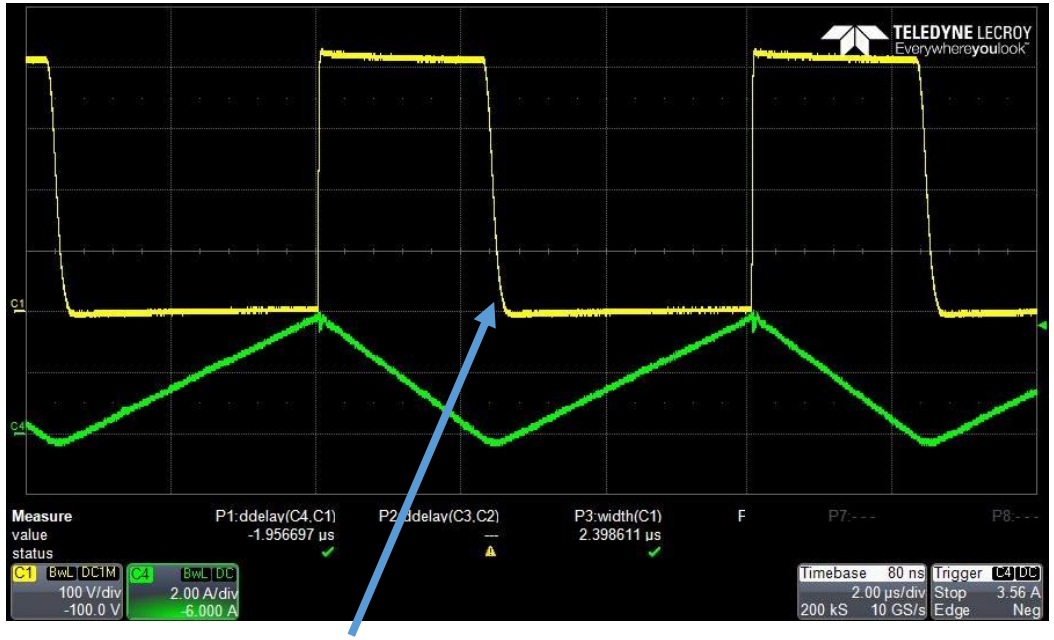


Speed Test:

Silicon Hits the Soft-Switching Speed Limit



120V_{AC}, Si CP partial hard-switching (~200kHz)



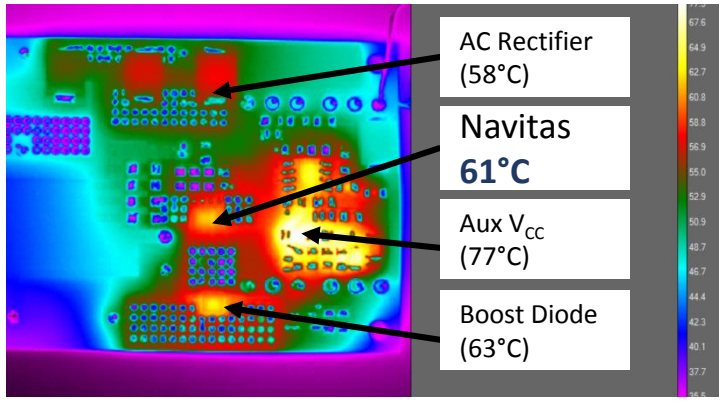
120V_{AC}, GaN clean ZVS waveforms (~200kHz)

- Si C_{OSS} is 50x-100x worse than GaN at V_{DS} < 30V
- High loss due to large stored charge while hard-switching

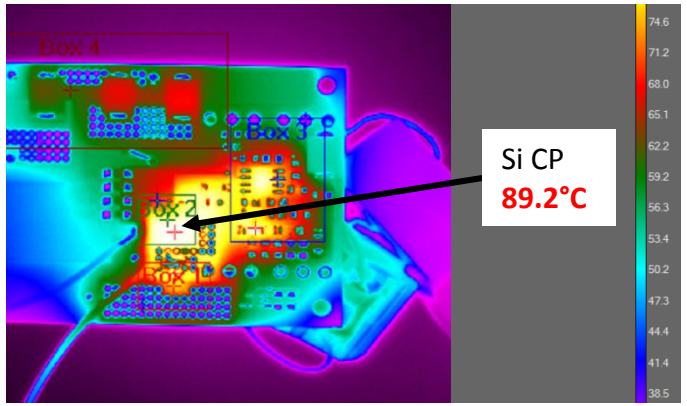
- Turn-off losses are low due to powerful and parasitic-free drive integration with no overshoot
- Near loss-less ZVS turn-on transition
- Minimize deadtime for low reverse conduction loss

Speed Test:

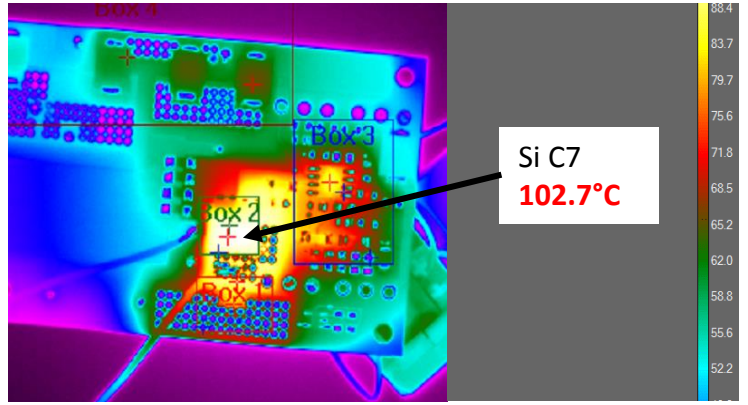
Silicon Hits a Speed Bump … and GaN Drives On



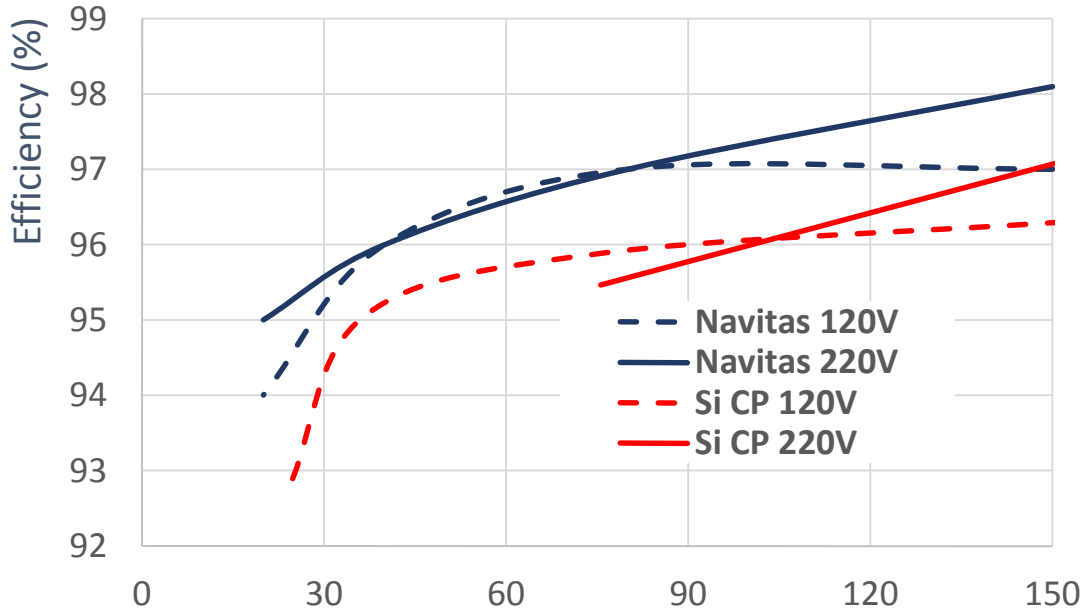
220V_{AC}, 150W



220V_{AC}, 150W



180V_{AC}, 150W



- 'No heatsink' design
- GaN runs cool
- Superjunction silicon FETs
  - Run 30-50°C hotter
  - Cannot deliver the power
  - Exhibit highly lossy resonant behavior

The Road Ahead…

Questions?