Optimization of the Drive Circuit for Enhancement Mode Power GaN FETs in DC-DC Converters

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***Abstract*—This paper discusses the practical concerns and optimization of the drive circuit for enhancement mode Gallium-Nitride (GaN) power transistors in dc-dc converters. The GaN FET's 6.0V absolute maximum gate voltage rating and ultra low threshold voltage impose strict constrains on the drive circuit. It is critical to achieve precise gate voltage limit, realize a low impedance gate signal path, and meet the stringent noise immunity requirements by optimizing the gate drive circuit. Prototype converters were built and experimental results are presented as proof of concept.**

I. INTRODUCTION

In recent years, enhancement mode Gallium-Nitride power transistors (GaN FET) have emerged as promising devices for high power density switch mode power supplies [1-6]. Given the same die size, the GaN FET presents lower conduction resistance, smaller gate charge, and faster switching capability than the comparable MOSFET devices. The enhancement mode allows the GaN FET to operate similarly as power MOSFET, minimizing the learning curve for power supply designers. However, driving a GaN FET needs particular care, because the low gate-to-source maximum voltage (Vgs) rating and ultra low gate threshold voltage (Vth) raise some strict constrains and challenges. This paper examines these challenges and discusses practical implementation and optimization of the drive circuit. Prototype converters were built, and experimental results are presented as the proof of concept.

II. CHALLENGES OF DRIVING GAN FET

Fig. 1 shows a typical GaN FET ON-resistance Rds(ON) as a function of gate-to-source voltage Vgs; Fig. 2 shows typical GaN FET drain current as a function of Vgs; and Table I compares the Vgs requirements of the GaN FET and silicon based power MOSFET. It can be seen that GaN FET's 6V absolute Vgs maximum rating [4, 5] is much lower than the typical power MOSFET's 20V rating. This imposes a challenge to drive GaN FET.

On one hand Vgs must be limited below 5.5V, leaving about 0.5V safe margin. On the other hand, as shown in Fig.1, a Vgs voltage between 4.5V and 5.5V is desirable to realize full enhancement of the GaN FET in order to minimize its Rds(ON) and consequently the associated conduction losses. Observing both Vgs absolute maximum rating and the desirable full enhancement Vgs voltage, the gate drive bias supply should be tightly regulated at about 5.0V. The conventional bias supply produced by a loosely cross-regulated transformer winding that is suitable for MOSFET drivers cannot be directly used.

The second challenge comes from the fact that GaN FET does not have the body diode. When in reverse conduction with the GaN FET gate held low, as shown in Fig. 3, the reverse drain-to-source voltage Vsd increases with increasing current. This causes a major problem in driving a high side GaN FET in a totem pole configuration such as synchronous Buck or half-bridge converters. Fig. 4 shows the conventional bootstrap technique to drive the high side FET in a buck converter [7, 8]. When the low side FET is turned on, the bootstrap capacitor is charged by VCC via the bootstrap diode. Then, the charged bootstrap capacitor serves as the bias supply for the high side driver. When this technique is applied to a GaN FET, the bootstrap capacitor will be charged to a voltage V_{boot} which is mainly determined by

$$V_{boot} = V_{CC} - V_F + V_{sd\_Q2} \tag{1}$$

where V_{CC} is the low side bias supply voltage, V_F the forward voltage drop of the bootstrap diode, and V_{sd_Q2} is the low side FET reverse drain-to-source voltage.

TABLE I. COMPARISON OF GAN FET AND MOSFET GATE VOLTAGE REQUIREMENTS

	GaN FET	**MOSFET**
Vgs Max Rating	6V Abs Max	20V Max
Vgs Threshold (Vth)	1.5V Typ	2 to 4V Typ
Vgs for Full Enhancement	4.5 to 5.5V	8 to 10V
Vgs Safe Margin	<0.5V	10V

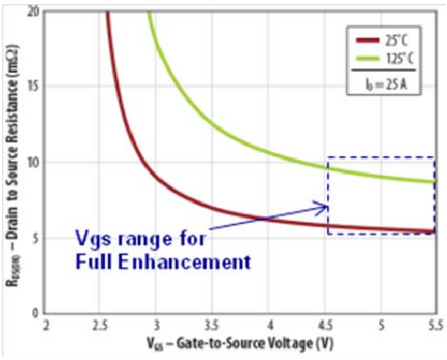


Figure 1. GaN FET Rds(ON) vs. Vgs (Courtesy of EPC).

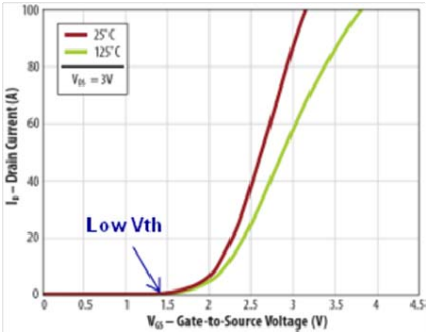


Figure 2. GaN FET drain current vs. Vgs (Courtesy of EPC).

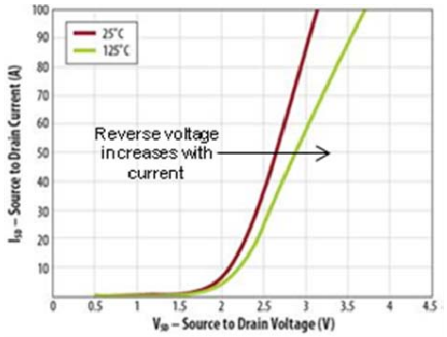


Figure 3. GaN FET reverse drain-to-source voltage vs reverse drain current (Courtesy of EPC)

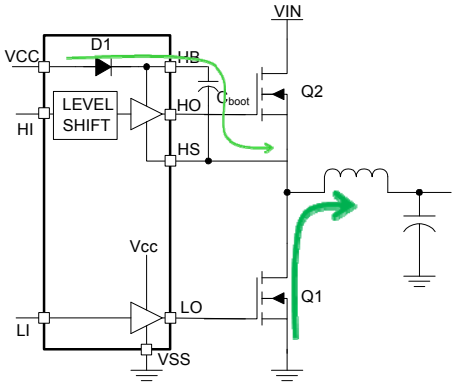


Figure 4. Bootstrap technique to drive the high side FET in a buck converter.

Figure 5. Bootstrap voltage vs. load current

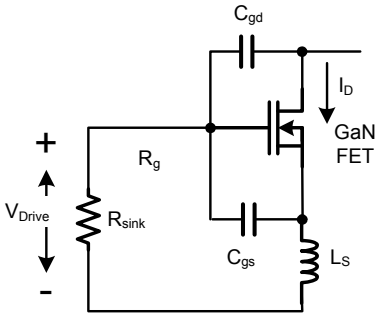


Figure 6. Stray inductance that may resonate with GaN FET inherent gate capacitance.

Since V_{CC} is apparently 5V, and since V_{sd_Q2} will increase quickly with the load current, V_{boot} will rise quickly to exceed the 6V maximum rating to damage the high side GaN FET. This problem can be seen in Fig. 5, which shows the test results of a conventional bootstrap technique applied to a synchronous GaN FET Buck converter.

It should be pointed out that adding an external diode to the low side GaN FET is not an effective solution to prevent the problem shown in Fig. 5, because charging the bootstrap capacitor completes in less than a few tens of nanoseconds. The lead inductance of the diode will greatly reduce its effectiveness of clamping the reverse drain-to-source voltage during this short period.

The third challenge of driving GaN FET comes from the low gate threshold voltage Vth, which is less than 1.5V as shown in Fig. 2. The minimum Vth can be as low as 0.7V [4, 5]. In contrast, the threshold voltage of power MOSFET is usually greater than 2V. The ultra low Vth of GaN FET imposes stringent requirements on the gate drive. Fig. 6 shows some stray inductance along the gate drive path in a practical circuit board as well as the gate capacitance of the GaN FET. These parasitic elements cause a resonance during switching transient, and some low magnitude voltage ringing can usually be observed at the gate. Though unwanted, such ringing is normally harmless for power MOSFET, but it can easily result in unintended turn-on of GaN FET during turn-off, increasing losses and even causing shoot-through.

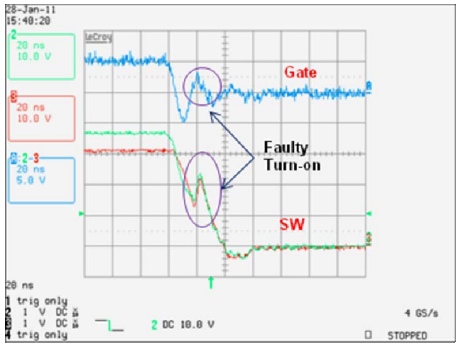


Figure 7. Small gate resonant ringing may cause faulty turn-on of the GaN FET. Top Trace (Blue) =Vgs, 5V/div. Middle Trace (Green) =High side gate voltage, 10V/div. Bottom Trace (Red)=High side source voltage, 10V/div.

Fig. 7 shows key waveforms of a typical unintended turn-on caused by gate ringing. To improve the gate drive noise immunity, it is critical to minimize stray inductance by layout optimization techniques.

The GaN FET's ultra low Vth causes another problem. The most commonly used gate drive structure is the totem pole structure formed by two small MOSFETs with the P-channel FET on the high side and the N-channel FET on the low side [9-11]. When driving a power MOSFET, as shown in Fig. 8, designers often use a diode in parallel with a gate resistor to control the turn-on speed without affecting the turn-off speed. Unfortunately, this simple approach cannot be used with GaN FET, because the diode forward drop may exceed the ultra low gate threshold, preventing the GaN FET from being turned off.

III. PRACTICAL OPTIMIZATION OF THE DRIVER CIRCUIT

A. Gate Drive Bias Supply

A voltage regulator of 5V is recommended as the supply to power the GaN FET gate drive, such that the GaN FET can be fully enhanced to realize the minimum Rds(ON) and lowest condition losses. A simple low drop-out (LDO) regulator can be selected to regulate the gate drive supply voltage from an available higher voltage rail, a transformer winding, or directly from the unregulated input voltage. Assuming the GaN FET has a total gate charge of Q_g, the average current required to turn on the GaN FET is determined by

$$I_g = Q_g \cdot f_s \tag{2}$$

where I_g is the averaged gate current, and f_s is the switching frequency.

The selection of the LDO module should also consider the package's thermal capability such that it can handle the regulator power dissipation, which is determined by

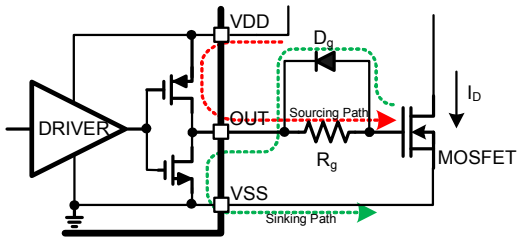


Figure 8. Conventional MOSFET gate drive employing to adjust turn-on and turn-off time.

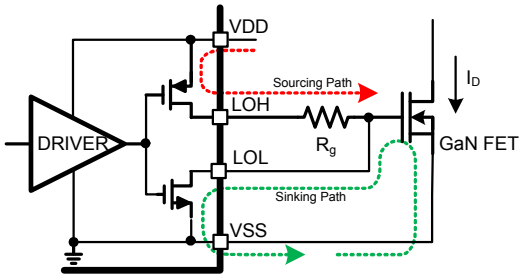


Figure 9. Separate current sourcing and sinking paths to drive GaN FET.

$$P_g = (V_{i\_max} - 5V) \cdot I_g \tag{3}$$

where V_{i_max} is the maximum voltage feeding into the LDO. If equation (3) produces excessive losses, a more efficient switch mode regulator like a buck converter module should be used.

B. Separate Sourcing and Sinking Path

When driving a GaN FET, particular attention needs to be paid to the driver's pull-down path to present a low impedance, because of the ultra low Vth of the GaN FET. This leads to the approach given in [12] that separates the gate current sourcing and sinking paths as shown in Fig. 9. However, the effectiveness of this approach heavily depends on the layout design.

C. High-side Bootstrap Voltage Clamp

In a half bridge type application, conventional bootstrap technique cannot be directly used without risking the damage of the high side GaN FET. This requires limiting the high side bootstrap voltage from exceeding the 6V maximum rating. An example of such a voltage clamp technique, as shown in Fig. 10, is given in [12]. A clamp in series with the boot-strap diode limits the boot-strap capacitor voltage to 5.2V. Fig. 11 shows the performance of the clamp circuit over a large load current range.

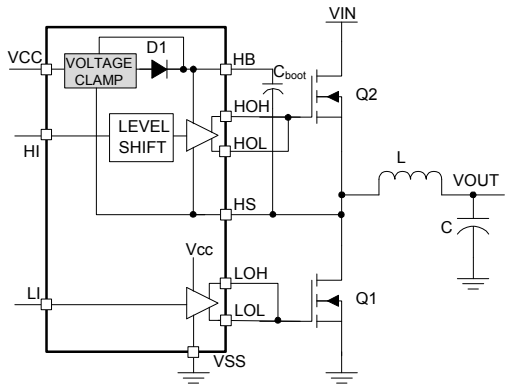


Figure 10. Bootstrap voltage clamp.

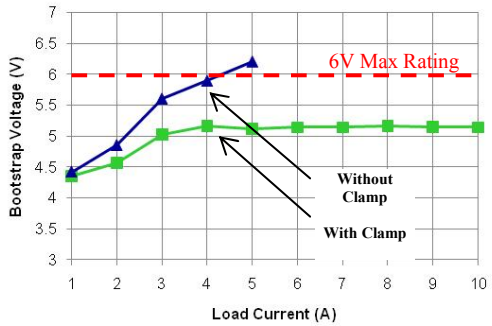


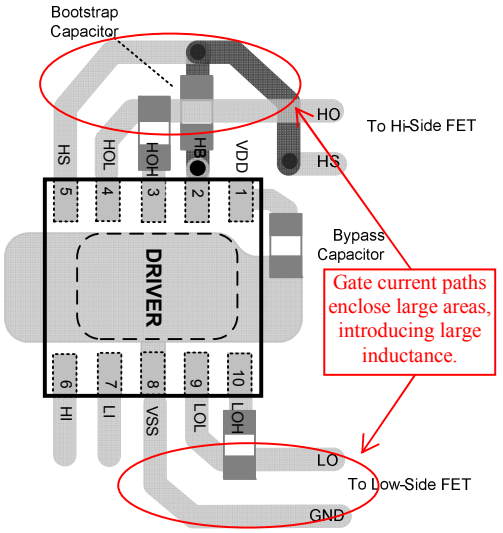
Figure 11. Bootstrap voltage vs. load current

D. *Layout Optimization*

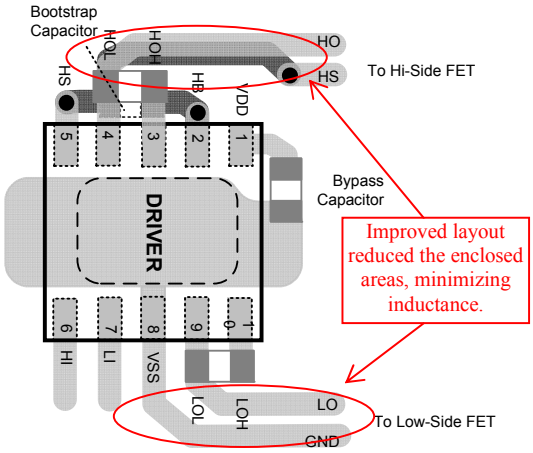
Layout optimization is critical to improve the GaN FET performance. The most important issue is to minimize stray inductance. Printed Circuit Board (PCB) via holes, spatial area looped by the gate signal and its return path, both contribute to total stray inductance. Minimize the trace length, limiting (or eliminating) the number of via holes, and placing the gate signal trace and the return trace closely side by side, are strongly recommended. Fig. 12 shows an example of non-optimized and optimized gate trace artwork using the LM5113 half-bridge driver in a LLP package. Fig. 13 shows another example of optimized layout artwork using LM5113 driver in a µSMD package. In both examples, the closely placed gate drive traces result in the minimum inductance, preventing the gate resonance and faulty turn-on during switching transients.

Placing the Vcc decoupling capacitor as well as the bootstrap capacitor closely beside the corresponding pins of the driver device is also important. These recommendations are demonstrated in both Fig. 12(b) and Fig. 13.

Regarding the power circuit, minimize the loop length and size of high frequency ac current paths. Fig. 14 shows a layout example of a synchronous buck converter power stage, where the high side and low side GaN FET switches are placed side by side, with the input capacitor (dashed-line box) placed directly underneath on the back side. In this way the ac current is limited within the smallest area.



(a) Non-optimized gate drive layout



(b) Optimized gate drive layout

Figure 12. Layout optimization Example 1. Darker traces on back side.

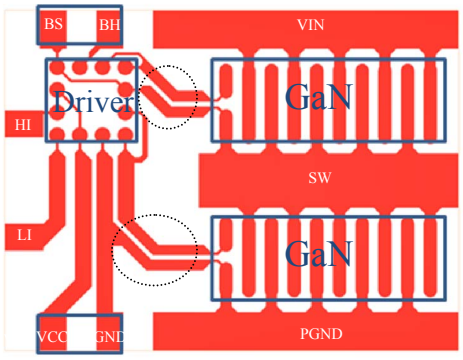


Figure 13. Layout optimization Example 2.

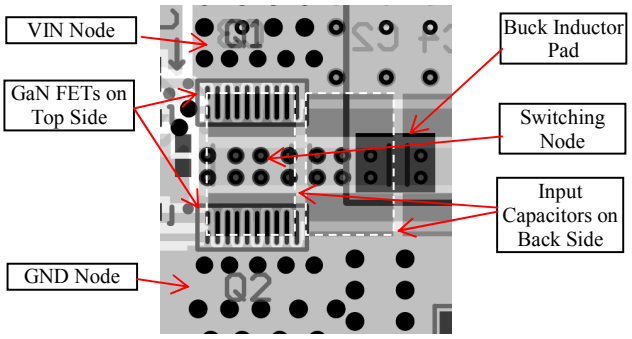


Figure 14. Layout optimization Example 3. "colored" trace on the back side.

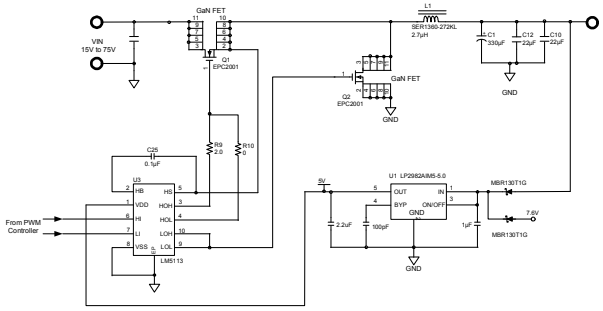


Figure 15. Schematic of Prototype Converter Power Stage.

IV. Experiment Results

Two prototype synchronous buck converters utilizing 100V GaN FETs have been developed. Fig. 15 shows the schematic of the power stage. The two circuit boards employ the same components, and the switching frequency is at 800 kHz. The 5V Vcc bias supply is implemented with an LP2982 5.0V LDO, and the LM5113 is used as the gate driver. The PWM controller (not shown) employs the LM5025. The main differences between the two boards are in the gate drive and input ac current path layout. One converter followed generic layout guidelines dealing with conventional power MOSFET converters, the other implemented the recommendations and layout optimization discussed previously for GaN FET. Fig. 16 shows the gate drive signal of the optimized circuit, in contrast with Fig. 7 which is the result of the non-optimized circuit. It is seen that the gate drive signal is much cleaner in the optimized circuit. Fig. 17 shows the comparison of overall efficiencies of the two prototype converters. It is seen that the optimized circuit achieves better efficiency.

V. Conclusions

Practical concerns and optimization of GaN FET gate drive circuit are discussed. It is critical to tightly regulate the supply voltage for the gate drive such that GaN FET can be safely operated to realize the minimum Rds(ON). In the case of bootstrap circuit for high side gate drive, a voltage clamping mechanism should be used to prevent excessive gate voltage. Also critical is optimization of the circuit board layout. Minimizing use of via holes, and placing the gate signal and return traces closely side by side, are strongly recommended. These proposed concepts are verified by the experimental results obtained on prototype converters.

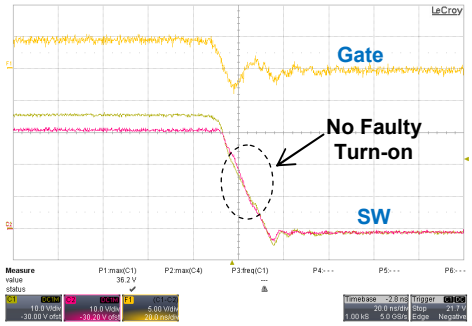


Figure 16. Gate drive waveform of the optimized circuit board. Top Trace (Yellow) =Vgs, 5V/div. Middle Trace (Green) =High side gate voltage, 10V/div. Bottom Trace (Red)=High side source voltage, 10V/div.

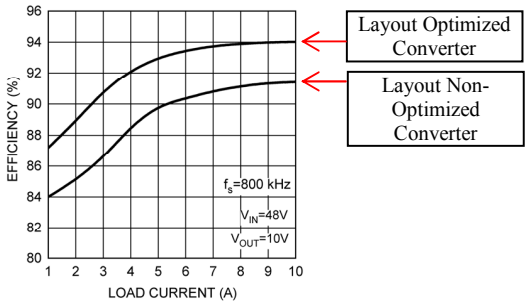


Figure 17. Comparison of Overall Efficiency between the Two Converters

Acknowledgment

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References

[1] N. Ikeda, J. Li, and S. Yoshida, "Normally-off operation power AlGaN/GaN HFET", in *Proc. of the 16th ISPSD* 2004, pp. 369-372.

[2] T. Palacios, C.S. Suh, A. Chakraborty, S. Keller, S. S.P. DenBaars, and U.K. Mishra, "High-performance E-mode AlGaN/GaN HEMTs", *IEEE Electron Device Letters*, vol. 27, Issue 6, pp. 428-430, 2006,.

[3] H. Otake, S. Egami, O. Ohta, Y. Nanishi1, and H. Takasu, "GaN-Based Trench Gate Metal Oxide Semiconductor Field Effect Transistors with Over 100 cm2/(V s) Channel Mobility", *Japanese J. of Appl. Phys*, Vol. 46 (2007) pp. pp.599-601.

[4] "EPC2001 Enhancement Mode Power Transistor", EPC Datasheet.

[5] "EPC2015 Enhancement Mode Power Transistor", EPC Datasheet.

[6] D. Costinett, H. Nguyen; R. Zane, and D. Maksimovic, "GaN-FET based dual active bridge DC-DC converter", in *IEEE APEC 2010*, pp1425-1432.

[7] M. Pomper, L. Leipold, J. Tihanyi, and H.E. Longo, "High-voltage DIMOS driver circuit", *IEEE J.of Solid-State Circuits*, vol. 15, Issue 3, pp. 328-330, 1980.

[8] LM5100/LM5101 High Voltage High Side and Low Side Gate Driver, National Semiconductor Datasheet.

[9] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics, Converters, Applications and Design*, John Willey & Sons, 1989, pp. 559-560.

[10] A. Pressman, *Switching Power Supply Design*, McGraw-Hill, 1991, pp. 350-351.

[11] *Unitrode High Speed Power Driver UC1705*, Unitrode Product Data Handbook 1997.

[12] *LM5113 5A, 100V Half-Bridge Gate Driver for Enhancement Mode GaN FETs*, National Semiconductor Datashee