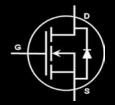
EPC1007 – Enhancement Mode Power Transistor

 $\overline{V_{DSS}}$, $\overline{100}$ \overline{V} $R_{DS(0N)}$, $30 \text{ m}\Omega$ I_D , 6 A





Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{\rm DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_{\rm G}$ and zero $Q_{\rm RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings				
V_{DS}	Drain-to-Source Voltage	100	V	
I _D	Continuous ($T_A = 25^{\circ}C$, $\theta_{JA} = 90$)	6	Δ.	
	Pulsed (25°C, Tpulse = 300 μs)	25	A	
V _{GS}	Gate-to-Source Voltage	6	· V	
	Gate-to-Source Voltage	-5		
T,	Operating Temperature	-40 to 125	°C	
T _{STG}	Storage Temperature	-40 to 150		



EPC Power Transistors are supplied only in passivated die form with solder bumps

Applications

- High Speed DC-DC conversion
- Class D Audio
- Hard Switched and High Frequency Circuits

Benefits

- Ultra High Efficiency
- Ultra Low R_{DS(on)}
- Ultra low Q_G
- Ultra small footprint

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characte	eristics (T _J = 25°C unless otherwise state	ed)					
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V, } I_D = 75 \mu\text{A}$	100			V	
I _{DSS}	Drain Source Leakage	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$		20	60	μΑ	
1	Gate-Source Forward Leakage	$V_{GS} = 5 V$.25	2	- mA	
I _{GSS}	Gate-Source Reverse Leakage	$V_{GS} = -5 \text{ V}$		0.1	0.5		
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_{D} = 1.2 \text{ mA}$	0.7	1.4	2.5	V	
R _{DS(ON)}	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}, I_{D} = 6 \text{ A}$		24	30	mΩ	
Dynamic Chara	acteristics (T _J = 25°C unless otherwise s	tated)					
C_{ISS}	Input Capacitance			200			
C _{oss}	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$		110		pF	
C_{RSS}	Reverse Transfer Capacitance			10			
Q_{G}	Total Gate Charge ($V_{GS} = 5 \text{ V}$)			2.7			
Q_{GD}	Gate-to-drain Charge	V 50VI 6A		1			
Q_GS	Gate-to Source Charge	$V_{DS} = 50 \text{ V}, I_{D} = 6 \text{ A}$		0.75		nC	
Qoss	Output Charge			8			
Q_{RR}	Source-Drain Recovery Charge			0		1	
ource-Drain (Characteristics (T _J = 25°C unless otherw	vise stated)					
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A, } V_{GS} = 0 \text{ V, } T = 25^{\circ}\text{C}$		1.8			
		$I_S = 0.5 \text{ A}, V_{GS} = 0 \text{ V}, T = 125 ^{\circ}\text{C}$		1.75		V	

DATASHEET EPC1007

Figure 1: Typical Output Characteristics

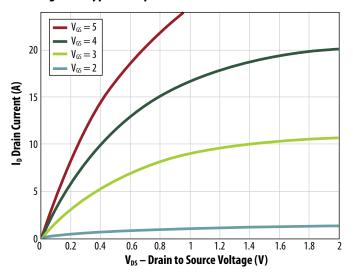


Figure 2: Transfer Characteristics

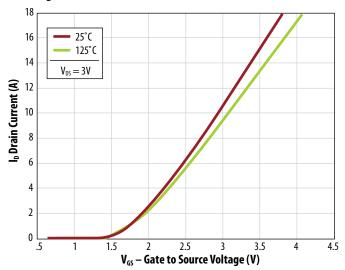


Figure 3: R_{DS(ON)} vs V_G for Various Current

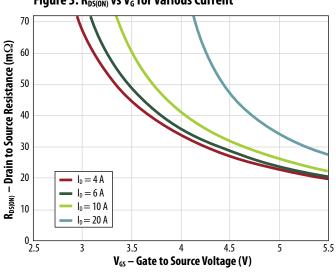


Figure 4: R_{DS(ON)} vs V_G for Various Temperature

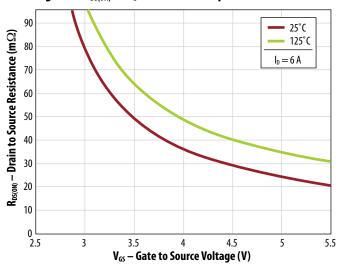


Figure 5: Capacitance

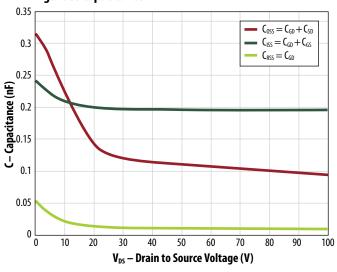


Figure 6: Gate Charge

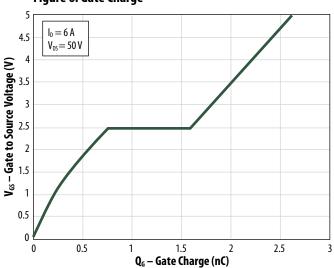


Figure 7: Reverse Drain-Source Characteristics

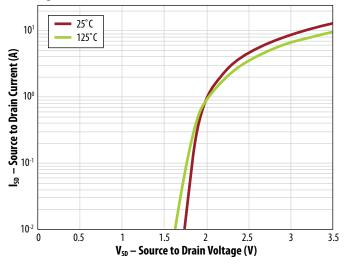


Figure 8: Normalized On Resistance Vs Temperature

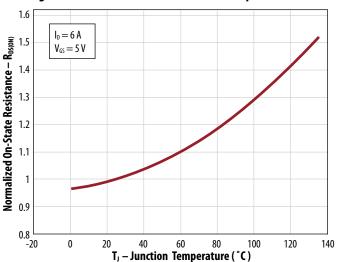


Figure 9: Normalized Threshold Voltage

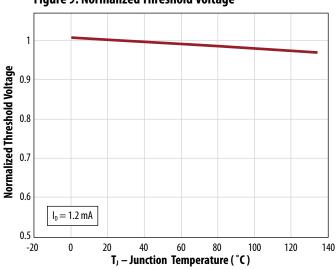
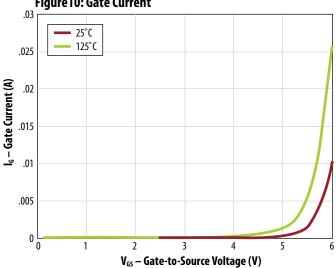
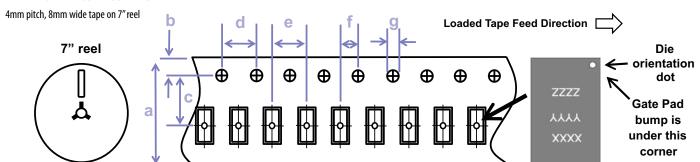


Figure 10: Gate Current



TAPE AND REEL CONFIGURATION



	EPC1007		
Dimension (mm)	target	min	max
а	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
е	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Die is placed into pocket bump side down (face side down)

Note: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole **DATASHEET EPC1007**

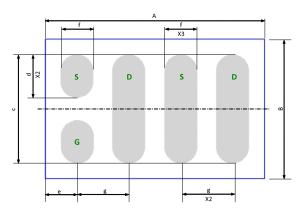


Gate Pad bump is under this corner

Part	Laser Markings			
Number	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3	
EPC1007	1007	YYYY	ZZZZ	

DIE OUTLINE

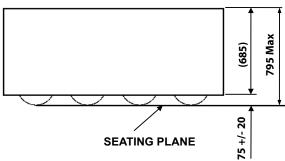
Bottom View



ZZZZ

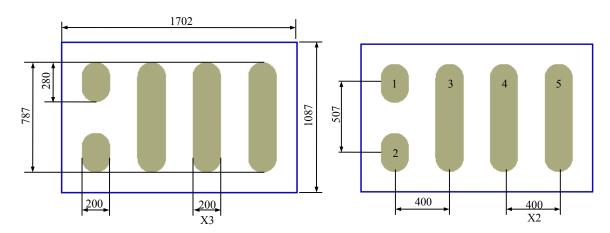
DIM	MICROMETERS		
	MIN	Nominal	MAX
А	1672	1702	1732
В	1057	1087	1117
С	834	837	840
d	327	330	333
е	235	250	265
f	248	250	252
g	400	400	400

Side View



RECOMMENDED LAND PATTERN

(measurements in μ m)



Pad no. 1 is Gate;

Pads no. 3 and 5 are Drain;

Pads no. 2 and 4 are Source.

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

Information subject to change without notice. Revised April, 2010