EE314 DIGITAL ELECTRONICS LABORATORY

SPRING 2016-2017 TERM PROJECT: COIN COUNTER

Introduction:

This document contains the project definition of the EE313 laboratory. Here are the important points about the project:

• Note that this is not a weekend project. Start working on it now. If you would like to test your designs you can use the equipment in the EE314 lab in working hours unless there is a laboratory session proceeding. During weekends, laboratory will be closed. However after practical finals FPGA development boards will be lent to groups (probably 1 board for 3 groups).

• The aim of this project work is to make you more familiar with some subjects you were introduced in digital electronics and logic design class. However, you may need to do some research and study extra material to accomplish the task. This will be a good step for 4th year graduation projects.

• The project groups will contain at most 2 students. Although it is not recommended, you may do your project alone. So, determine your project partner as soon as possible. It is not necessary that your lab partner and project partner is the same person.

• You are free and encouraged to use your own ideas. Although your design approach is not limited, the systems are supposed to be economical.

• All assistants are responsible for the project. Primary contact mechanism with the assistants is via email.

•No early demonstration will be allowed (apart from the crucial reasons, such as Erasmus, foreign student, etc.).

Important Dates:

-26th May: Proposal Report

-10-11th June: Project Demonstrations

-12th June 17:00: Final Report Submissions

Report Format

Proposal Report: The aim of the proposal report is for you to start your research early on so that you can have a solid idea about the project. This report will contain preliminary work on your project. A good report should include your proposed way to solve the problem, the equipment required for the solution, some block diagrams of the overall system and any additional info (circuit schematics, mathematical calculations etc.) you see fit. Maximum page limit for the preliminary report is 4 pages (Times New Roman, 10 point font). Longer reports will be rejected. It is crucial that you determine your project partner, and do some brain storming to come out with solutions well before the preliminary report deadline. Your report is supposed to include filter design and circle detection algorithms. You should add give at least 2 references about filter design from the literature. Moreover you should propose a filter design in your report. It is not necessary to continue with this filter design but you should show that you have worked on the project. You can simulate your filters and circle detection algorithms using MATLAB.

You have to upload your proposal report in pdf format to ODTUCLASS until 26th May, 23:59. Late submissions will not be accepted.

Final Report: The final report should be in the IEEE double column paper format (please check the IEEE paper format) and it should not exceed 10 pages in total, any more pages will decrease your grade. The formatting is one of the most important parts of the project. If the final report is not in the IEEE paper format, the project will not be graded and you will get zero from the whole project. Any formatting mistake (such as no figure captions, not referral to the figure in your main text, etc.) will result in grade deduction. You have to upload your proposal report in pdf format to ODTUCLASS until 12th of January, 17:00. Late submissions will not be accepted. Your report should include the following items:

- Theoretical background and literature research
- Design methodology and mathematical analysis of the subsystems
- Simulation results verifying that your subsystems and overall system is working properly.
- Experimental results
- Comparison of the experimental results with the simulation results and mathematical calculations and explanation of any discrepancies.

Grading:

-Proposal Report: 10 pts

-Project Demonstrations: 50 pts

-Final Report: 40 pts

Project Definition

In this term project, you need to design a coin counter. Implementation will be done by using Verilog, and FPGA development boards available at laboratory.

The input will be a grey-scaled image of coins. Designed system should give the amount of money as the output. A simple block schematic of the system is given in the Figure 1.

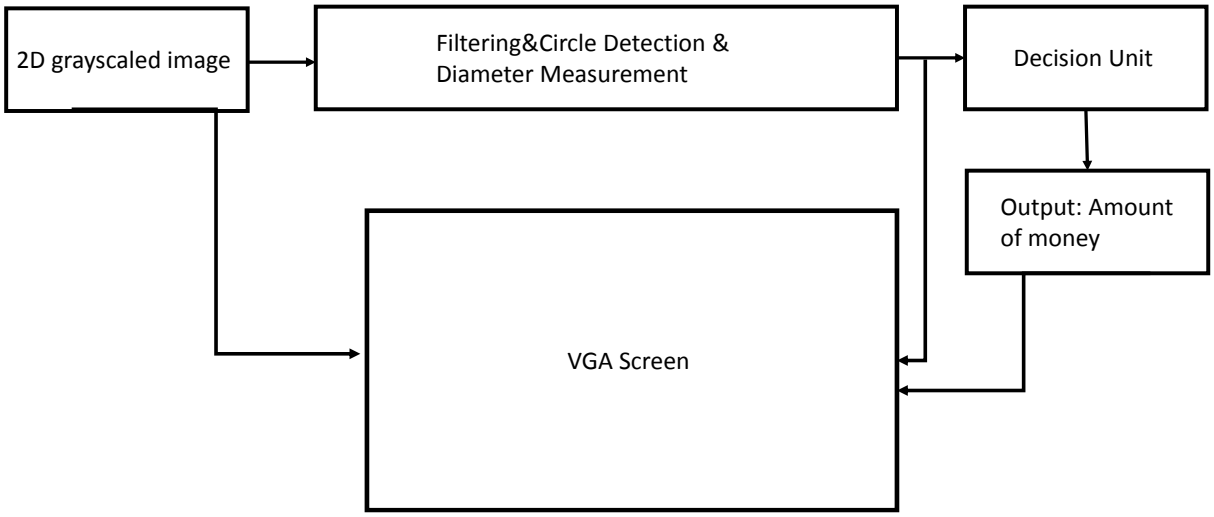

Figure 1: The schematic view of the project

2D grayscaled image: Coins should be placed on an A4 paper. You can use black filled 1 cm x 1 cm squares at the corners for the scaling purpose. The photo should be vertical as it is shown in Figure 2. You are supposed to map the color values of image and then upload it to the FPGA. You should study on bitmapping and uploading an image to FPGA.

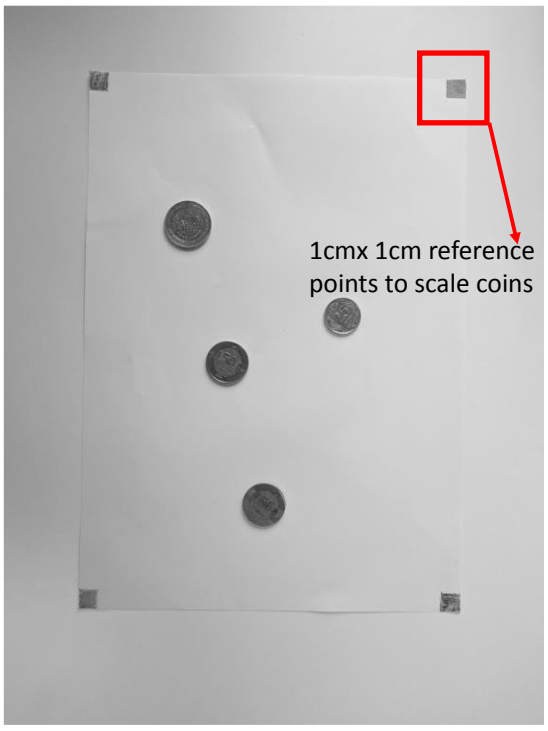

Figure 2: An example image

Filtering & Circle Detection and Diameter Measurement Unit: You need to design a filter to extract the boundaries of coins better (ie:high pass filter). This will help to detect the edges of coins. Further research on edge detection algorithms and their implementation in FPGA is recommended. After edge detection, you need to detect circles and their diameters for the classification of coins.

Decision Unit: According to diameter information, you need to design a system which decides the total amount of the money. For example the required output of Figure 2 is shown in below:

Coin Type	Amount
1 TL	1
50 Kr	2
25 Kr	1
Total	**2 TL and 25 Kr**

VGA Screen: The output of the designed system should be displayed on a VGA screen. Moreover, uploaded image and image after circle detection process should be displayed. You are encouraged to add visual aids (highlights, circles, lines, etc.) Detailed information about VGA drive unit will be supplied as appendix.

Project Specifications:

-You need to detect 3 kind of coins; 1 TL, 50 Kr, 25 Kr.

-Your system should ignore fake coins. (Circle shaped objects with different diameters or square shaped objects should be ignored)

-Your system should work with different images of 320x240 resolution. During demonstration your assistant will test your system using different images. Example images will be provided. You can also use your images to test your system.

-The images should be in vertical orientation.

-The distance between the target and the camera can vary. Therefore, you need to use reference points to normalize dimensions.

-You are not allowed to use any extra component or development board other than the FPGA development board used in our laboratory. After practical finals, FPGA boards will be given to groups (probably 1 FPGA board for 3 groups).

-You are not allowed to use VHDL or schematic designs. You are only able to use Verilog for this project.

-You are not allowed to do any post-process to images. You can only make a conversion of RGB images to grayscale and re-arrange the resolution. Filtering operations should be implemented using FPGA.

Bonuses

- Detection with a photograph which is taken with perspective (not right angle) (10 points)
- Detection of fake coin whose diameter is equal to diameter of any coin (for example distinguishing 2 € and 1 TL) (10 points)
- Detection of 10 Kr and 5 Kr (5 points)

Appendix : VGA Interface

VGA is a widely used standard in video industry for the transmission of video signals from a computer or microprocessor into a monitor or TV. Each 640x480 image is called a 'frame' and each frame contains 480 lines which are made up of 640 pixels.

The monitor starts displaying each frame by beginning from the first line and then the first pixel of this line. In each line, the display order is from left to right; and each frame is written in an order from top to bottom. So, your first pixel is always at the top left corner, while the last pixel at the bottom right. You will need to generate an image buffer with at least 640x480 = 307200 bits to store each line and frame in order to form a coherent image; however you will also need to adjust two synchronization signals called HSync (Horizontal Synchronization) and VSync (Vertical Synchronization) in order to see a video. These signals tell the monitor when a line or frame is finished, and the monitor should start from the next line or frame.

As shown in Figure 3, VGA interface is actually very simple, and you will only need to make 3 connections, namely R-G-B. For example, for a white pixel all three inputs should be high, and for a black pixel the inputs should be low. The FPGA cards in the laboratory already have a VGA output port with color outputs, so you will only need to supply the R-G-B data digitally to the VGA port. Necessary pins for these assignments can be found in the user manual. (http://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=English&No=836&FID=eac30a7aaacf5187a4ace0d613cd4676)

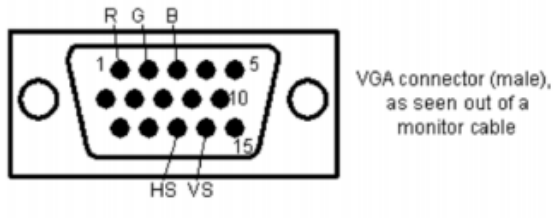

Figure 1: VGA interface.

HSync and VSync: HSync and VSync are necessary in order to tell the monitor to 'start' or 'stop' writing a line or frame. You will need to build the necessary digital blocks in order to correctly form these two signals. These blocks are basically counters with some modifications and are very easy to implement in Verilog. You can see the horizontal and vertical synchronization signals in Figure 2 with the corresponding timing in Table 1.

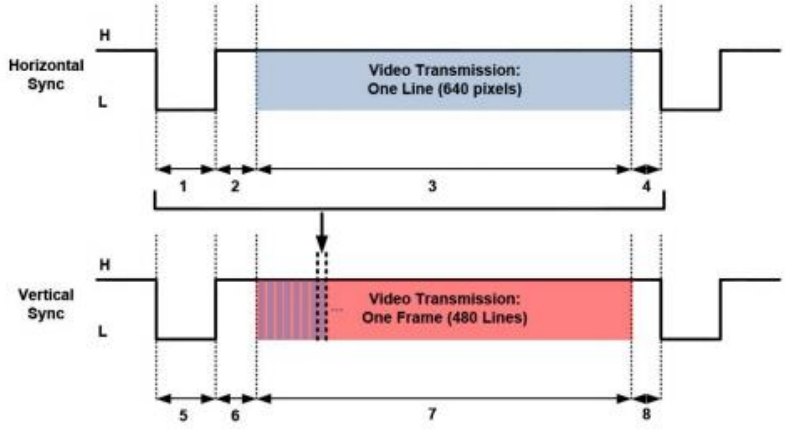

Figure 2: HS and VS.

Timeline # on Fig. 1	Name	Duration	Clock Count
1	H. Sync	3.84 µs	96
2	Back Porch (H)	1.92 µs	48
3	Video Signal (One Line)	25.6 µs	640
4	Front Porch (H)	0.64 µs	16
5	V. Sync	0.064 ms	2
6	Back Porch (V)	1.056 ms	33
7	Video Signal (One Frame)	15.36 ms	480
8	Front Porch (V)	0.32 ms	10

Table 1: Timing.

By observing Figure 2 and Table 1, we can understand that the HSync signal is used to synchronize one line in a frame, while VSync is used to synchronize each frame. Basically, when HSync or VSync is low, the monitor understands that it needs to switch from one line or frame to the next. Back and front porch are idle stages where the monitor is getting ready to write the next pixel or line. They also include 8 pixel and line over scan or 'border' pixel/lines outside our standard view of the monitor.

IMPORTANT NOTE: The video input signals (R, G, B) of a VGA monitor should be off (or black) during H. or V. Sync stages, and front/back porch stages. The video input signals should only be active during an active video transmission stage, which are highlighted in Figure 2.
In order to construct these HSync and VSync signals and to achieve transmission of each line/pixel, you will need a 25 MHz clock signal. This will also mean that each pixel will be transmitted at 25 MHz to the monitor during active video stages.
Internal clock information about ALTERA can be found under the Clock Circuitry part of the user manual.

http://www.epanorama.net/documents/pc/vga_timing.html
http://martin.hinner.info/vga/640x480_60.html