Chapter 1. Introduction

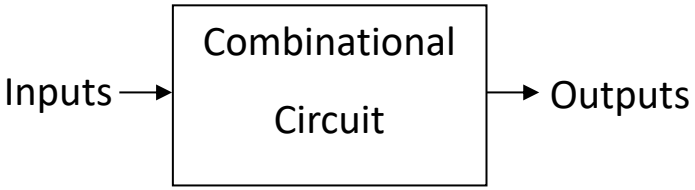
Latches and Flip-Flops

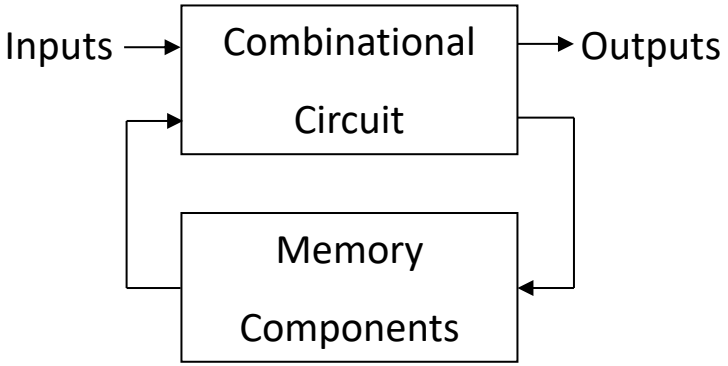
Flip-Flop Types

- SR-type
- D-type
- T-type
- JK-type

Introduction

Logic circuits are classified into two categories: combinational circuits and sequential circuits. Sequential circuits are further divided into synchronous and asynchronous types. The outputs of combinational circuits depend solely on the current input values, while the outputs of sequential circuits depend on both the current and previous input values. In sequential circuits, latches, flip-flops, and registers are used as memory components.

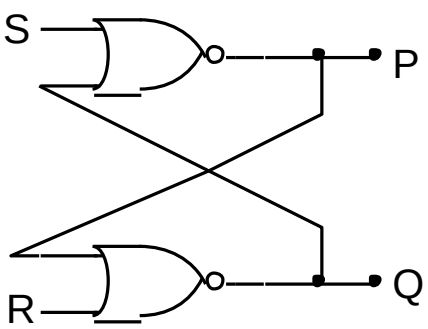




Latches and Flip-Flops

Latches are memory components that store binary data, created by connecting two logic gates in a feedback loop.

SR-Type Latch:



P = (S+Q)'
Q = (R+P)'

- Store State: This is the state where both inputs are zero.

When S = R = 0, the outputs are complements of each other: P = Q' and Q = P'.

- Loading Data: A latch stores either a 1 or a 0.

⇒ To store 1, set the inputs as S = 1 and R = 0. In this case Q = 1 and P = 0.

⇒ To store 0, set the inputs as S = 0 and R = 1. In this case Q = 0 and P = 1.

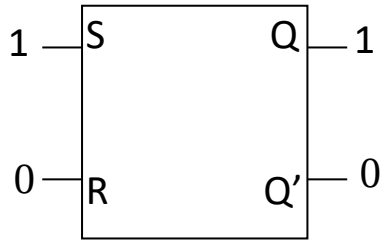
The output P can also be referred to as Q'.

The inputs S and R stand for Set and Reset, respectively.

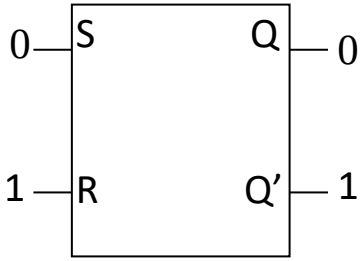
SR-Type Latch

In summary, as shown in the diagram:

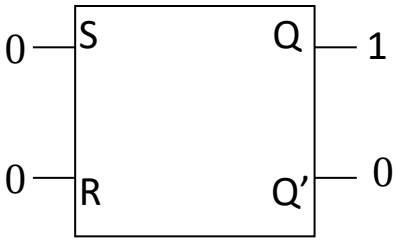
Set State

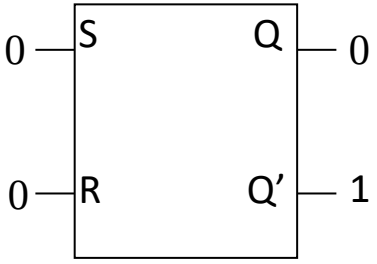


Reset State



If SR is set to 00 after being set or reset, the latch enters the store state.





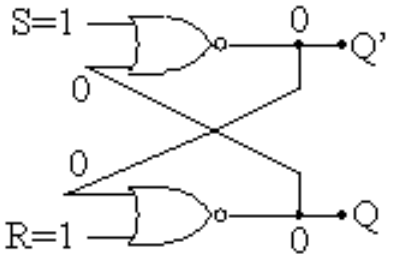
SR-Type Latch

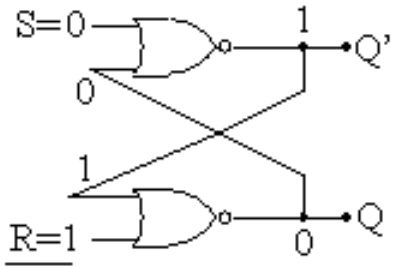
If both inputs are set to 1:

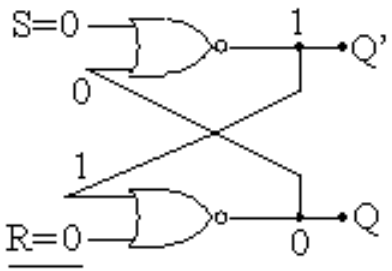
We substitute SR = 11 into the defining equations P= (S+Q)' and Q = (R+P)'

P = (1+Q)' = 0 and Q = (1+P)' = 0

Both outputs become 0, which are not complements of each other. This is invalid. Therefore, the SR latch does not permit both inputs to be 1 simultaneously.







Flip-Flops (F/F)

Flip-flops were developed to store data more reliably compared to latches.

Flip-flops are storage elements with a clock input.

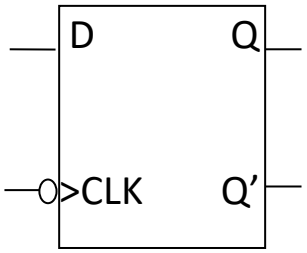
The output value of a flip-flop changes only with a clock transition. Those triggered by the transition from 1 to 0 are negative edge-triggered, and those triggered by the transition from 0 to 1 are positive edge-triggered (trailing-edge triggered) flip-flops.

What is loaded into the flip-flop with the clock transition depends on the data inputs and what was loaded during the previous transition.

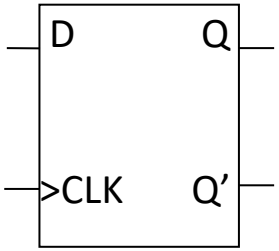
There are four basic types of flip-flops: D, JK, SR, and T.

D Type Flip-Flop

The "D" in D-type flip-flop stands for either "Data" or "Delay." The input is delayed until the next clock pulse. The output of the D flip-flop depends on the value of the D input just before the clock pulse.



Negative-edge triggered



Positive-edge triggered

Truth table for a D-type F/F

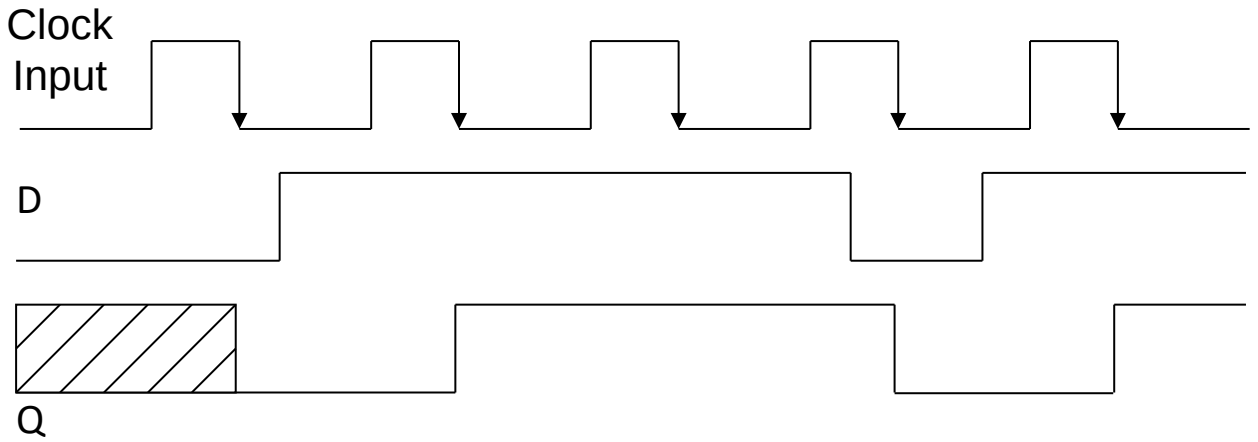
D q	Q
0 0	0
0 1	0
1 0	1
1 1	1

D	Q
0	0
1	1

Q = D

D-Type Flip-Flop

Let's analyze the behavior of a negative-edge triggered D-type flip-flop using a timing diagram.



The signal D in the diagram represents a sample input.

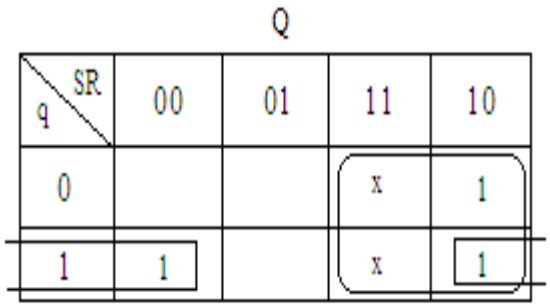
SR-Type Flip-Flop

The SR-type flip-flop has two inputs, called Set and Reset, like the SR-latch.

Truth table for an SR-type F/F

S	R	q	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

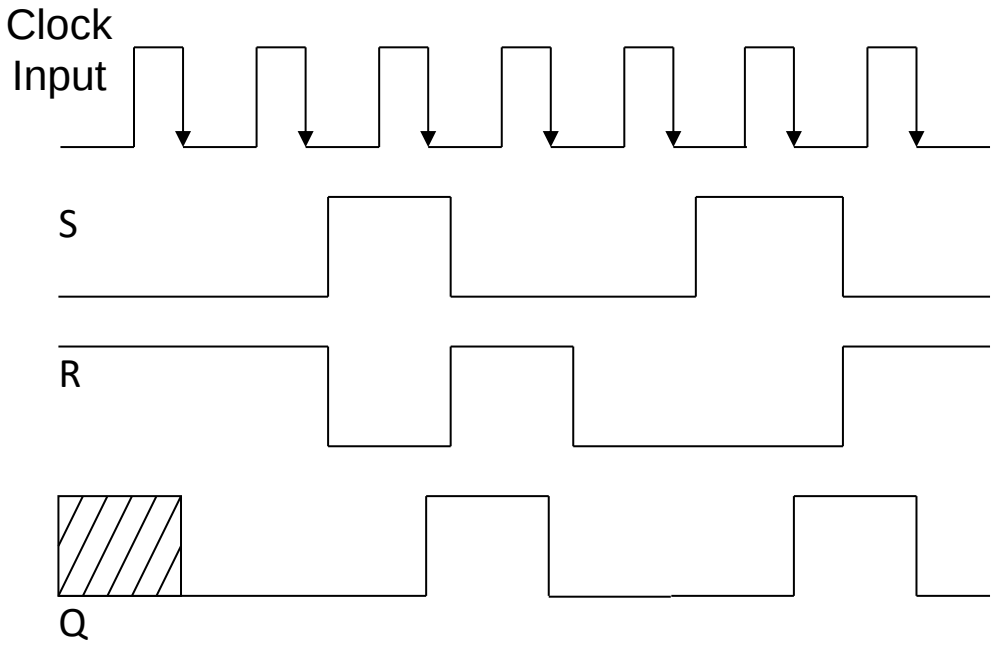
S	R	Q
0	0	q
0	1	0
1	0	1
1	1	-



$Q = S + R'.q$

SR-Type Flip-Flop

Let's analyze the behavior of a negative-edge triggered SR-type F/F using a timing diagram.



The signals S and R in the diagram represent sample inputs.

T-Type Flip-Flop

The T-type flip-flop has an input called T (Toggle). When T = 1, the flip-flop complements its output, and when T = 0, it retains the current output value.

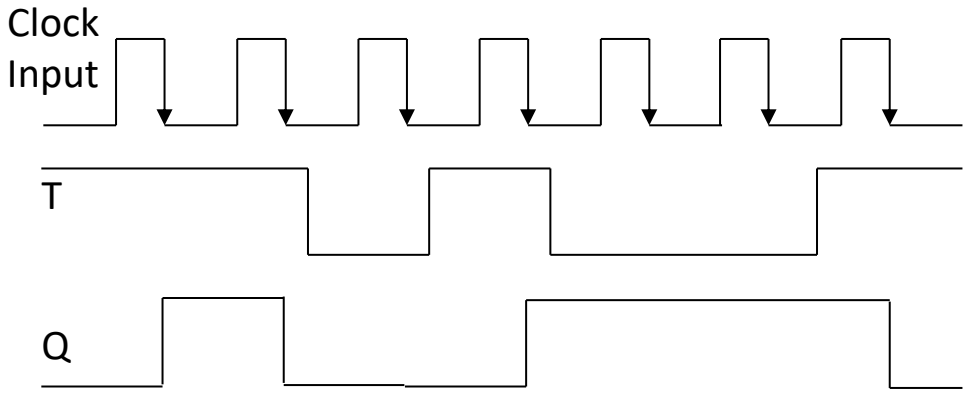
Truth table for a T-type F/F

T q	Q
0 0	0
0 1	1
1 0	1
1 1	0

T	Q
0	q
1	q’

$Q = T \oplus q$

Let’s analyze the behavior of a negative-edge triggered T-type F/F using a timing diagram, assuming the initial value of Q=0.



The signal T in the diagram represents a sample input.

JK-Type Flip-Flop

The JK-type flip-flop has two inputs, called J and K. It can be considered a combination of the SR-type and T-type flip-flops. It behaves like an SR-type flip-flop except when J = K = 1. In this case, it behaves like a T-type flip-flop.

Truth table for a JK-type F/F

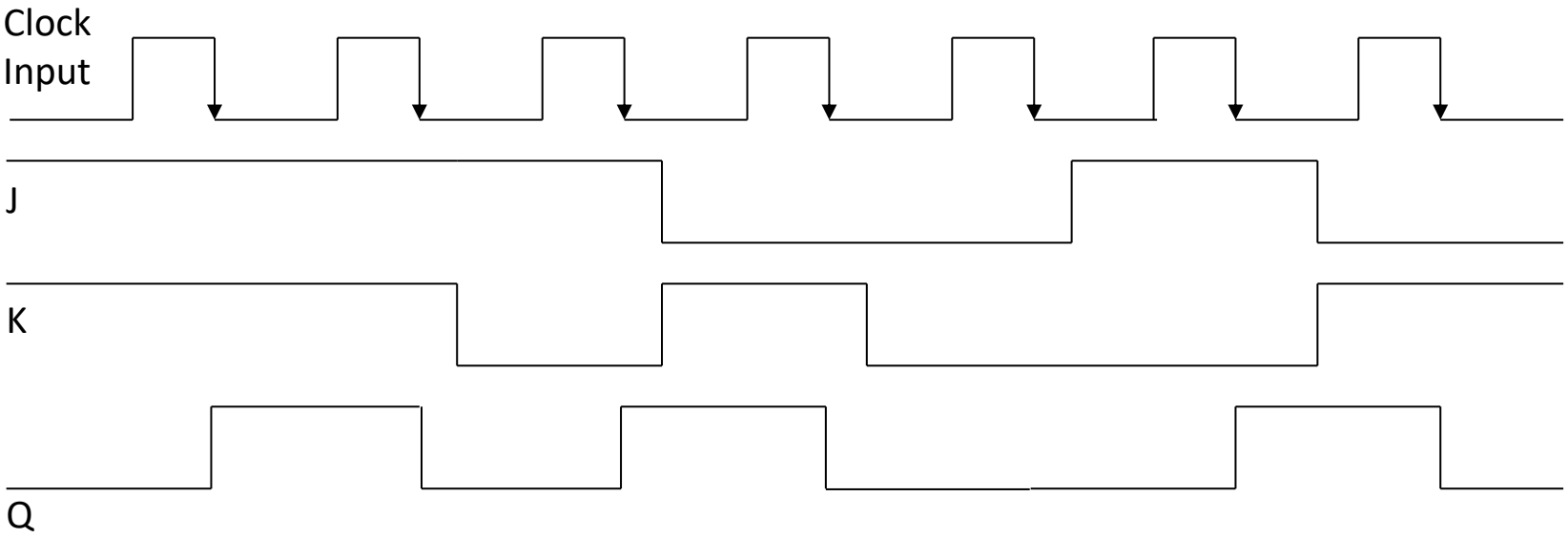
J	K	q	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J	K	Q
0	0	q
0	1	0
1	0	1
1	1	q’

Q = J’K’q + JK’ + JKq’
= J’K’q + JK’(q+q’) + JKq’
= J’K’q + JK’q + JK’q’ + JKq’
= J.q’+K’.q (Characteristic equation)

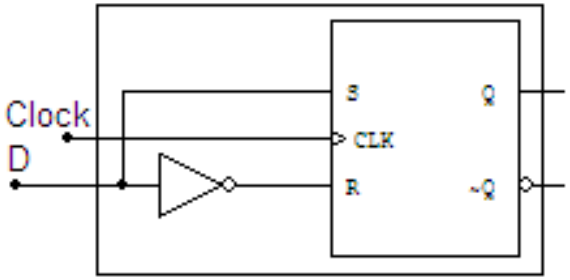
JK-Type Flip-Flop

Let's analyze the behavior of a negative-edge triggered JK-type flip-flop using a timing diagram, assuming the initial value of Q = 0.



Conversion of Flip-Flops

We can convert SR and JK flip-flops into a D flip flop.

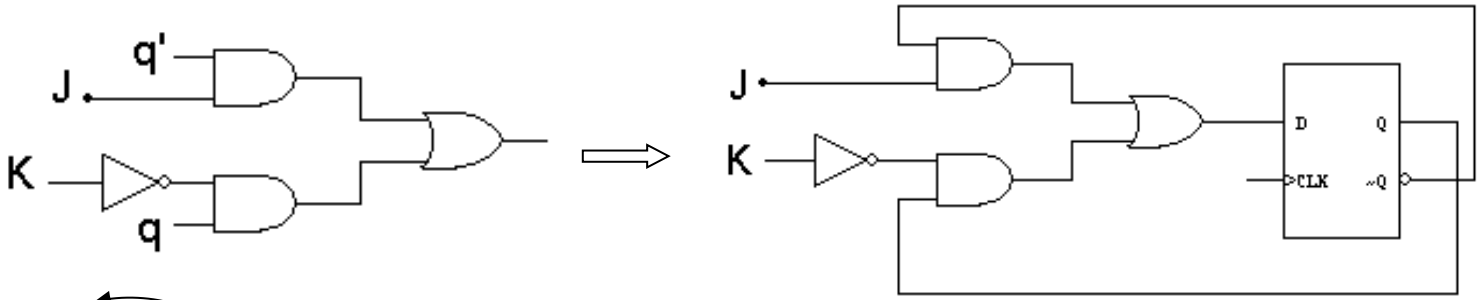


$Q = S+R'.q$

$Q = D(q+1)=D+Dq$

Characteristic equation of a JK flip-flop is: $Q = J.q'+K'.q$

If we input this logic equation into a D flip-flop, we obtain a JK flip-flop.



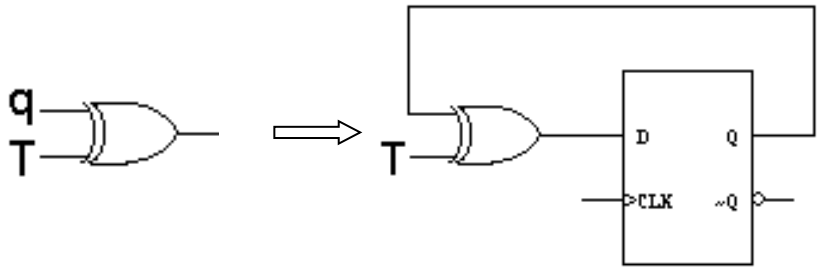
$Q = D$

$Q = J.q'+K'.q$

Conversion of Flip-Flops

Characteristic equation of a T flip-flop is: $Q = T \oplus q$

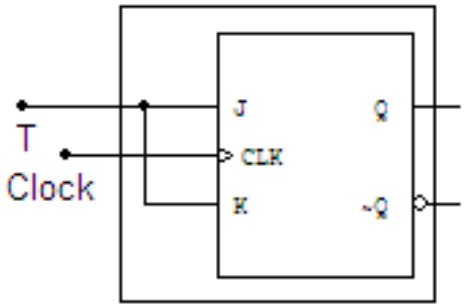
If we input this logic equation into a D flip-flop, we obtain a T flip-flop.



$Q = D$

$Q = T \oplus q$

By connecting the two inputs of a JK flip-flop, we obtain a T flip-flop.



$Q = T \oplus q = T.q' + T'.q$

$Q = J.q' + K'.q$