Chapter 1. Sequential Circuits

Last Week
Excitation tables of flip-flops

Analysis of sequential circuits
　　　　Implementation of sequential circuits from given state tables

This Week
Steps of sequential circuit design

Steps of Synchronous Sequential Circuit Design

1. Define the states or memory element values based on the problem's description.

2. Develop a state table and diagram to represent system behavior.

3. Choose flip-flops (if unspecified) and prepare excitation tables.

4. Generate logical expressions and design the circuit using output and excitation tables.

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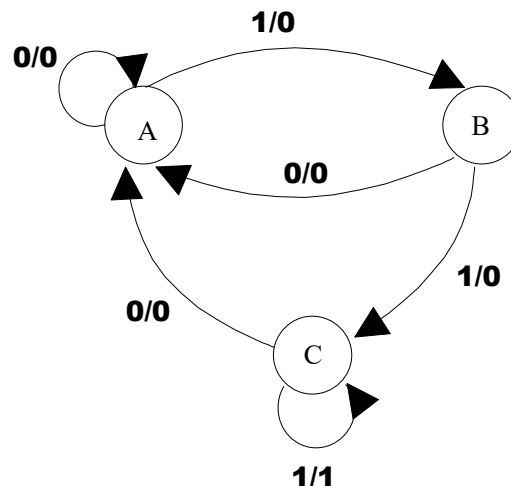# Steps of Synchronous Sequential Circuit Design

Example: Consider a Mealy-type circuit with one input and one output. The circuit outputs 1 if and only if the last three inputs are all 1.

This system requires 3 states, which are stored in memory components:
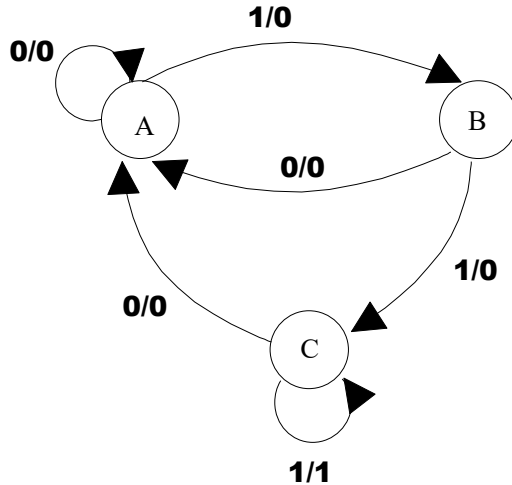
State A: Represents the condition where the most recent input is 0.

State B: Represents the condition where the last two inputs are "01".

State C: Represents the condition where the last two inputs are "11".

Example (2nd Page)

State Diagram

Present State (q)	Next State (Q)		Output (z)	
	x=0	x=1	x=0	x=1
A	A	B	0	0
B	A	C	0	0
C	A	C	0	1

State table of the circuit

Since the state table has 3 states, we need to use 2 flip-flops.

Let's assign letters as follows:
A = 00
B = 01
C = 10

Present State q_1q_2	Next State (Q_1Q_2)		Output (z)	
	x=0	x=1	x=0	x=1
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1

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Example (3rd Page)

Let's implement the circuit with JK flip-flops.

Next step is to derive the inputs of the flip-flops.

Present State $q_1 q_2$	Next State $(Q_1 Q_2)$ $x=0$	$x=1$	Flip-Flop Inputs $x=0$ $J_1 K_1$ $J_2 K_2$	$x=1$ $J_1 K_1$ $J_2 K_2$	Output (z) $x=0$	$x=1$
0 0	0 0	0 1	0 x 0 x	0 x 1 x	0	0
0 1	0 0	1 0	0 x x 1	1 x x 1	0	0
1 0	0 0	1 0	x 1 0 x	x 0 0 x	0	1

q Q	J K
0 0	0 x
0 1	1 x
1 0	x 1
1 1	x 0

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Example (4th Page)

Let's draw a Karnaugh map for each flip-flop input (J_1, K_1, J_2, K_2) and the output (z) to determine the equations.

Present State q_1q_2	Next State (Q_1Q_2)		Flip-Flop Inputs				Output (z)	
	x=0	x=1	x=0		x=1		x=0	x=1
			J_1K_1 J_2K_2		J_1K_1 J_2K_2			
0 0	0 0	0 1	0 x 0 x		0 x 1 x		0	0
0 1	0 0	1 0	0 x x 1		1 x x 1		0	0
1 0	0 0	1 0	x 1 0 x		x 0 0 x		0	1

$$J_1 = x.q_2$$

$$J_2 = x.q_1'$$

$$K_1 = x'$$

$$K_2 = 1$$

$$z = x.q_1$$

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Steps of Synchronous Sequential Circuit Design

Example: Consider a Moore-type circuit with one input and one output. The circuit outputs 1 if and only if the last three inputs are all 1.
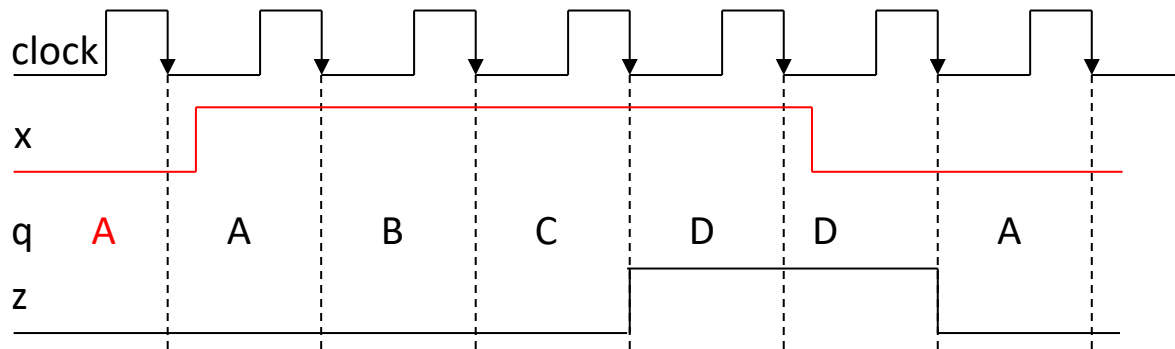

Assuming the system starts in state A, let's analyze the state transitions and the output based on a sample input sequence.

A   A B C D D D D D A B C A B C D A B

x   0 1 1 1 1 1 1 1 0 1 1 0 1 1 1 0 1

z   0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 1 0 0 0

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Example (2nd Page)
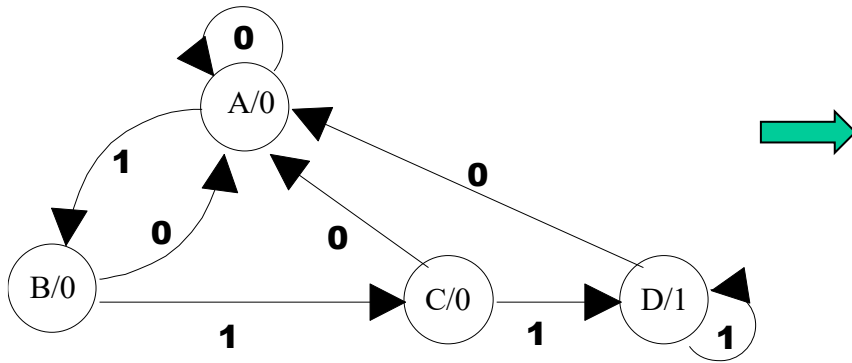
Let's analyze the behavior of the circuit using a timing diagram.

Let's assign the flip-flop outputs to represent the states as follows:
A=00, B=01, C=10, D=11.

Present State	Next State	Flip-Flop Inputs		Output
$x\ q_1\ q_2$	$Q_1\ Q_2$	$J_1\ K_1$	$J_2\ K_2$	z
0 0 0	0 0	0 x	0 x	0
0 0 1	0 0	0 x	x 1	0
0 1 0	0 0	x 1	0 x	0
0 1 1	0 0	x 1	x 1	1
1 0 0	0 1	0 x	1 x	0
1 0 1	1 0	1 x	x 1	0
1 1 0	1 1	x 0	1 x	0
1 1 1	1 1	x 0	x 0	1

Example (4th Page)

After constructing the Karnaugh maps for J_1, K_1, J_2, K_2, and z, the equations for each are derived as follows:

Present State x q_1 q_2	Next State Q_1 Q_2	Flip-Flop Inputs J_1 K_1	J_2 K_2	Output z
0 0 0	0 0	0 x	0 x	0
0 0 1	0 0	0 x	x 1	0
0 1 0	0 0	x 1	0 x	0
0 1 1	0 0	x 1	x 1	1
1 0 0	0 1	0 x	1 x	0
1 0 1	1 0	1 x	x 1	0
1 1 0	1 1	x 0	1 x	0
1 1 1	1 1	x 0	x 0	1

Karnaugh ⟹

$J_1 = q_2.x$
$K_1 = x'$
$J_2 = x$
$K_2 = x'+q_1'$
$z = q_1.q_2$

Since it's a Moore-type circuit, the output depends only on the current state. Given that the output is 1 only in State D (where $q_1 q_0 = 11$), the output equation can be simplified as: $z = q_1 \cdot q_0$
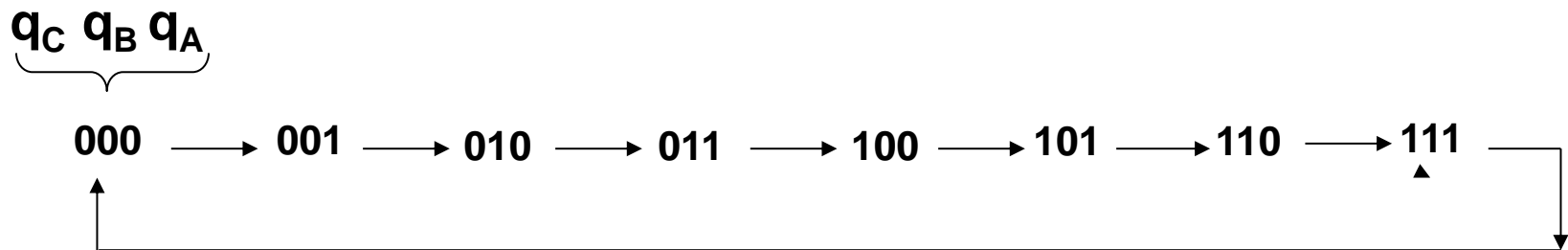
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Steps of Synchronous Sequential Circuit Design

Example: Synchronous Counter Design

Counter circuits typically do not have inputs. The state transitions occur with each clock pulse. The outputs are simply the states of the flip-flops, meaning the flip-flops' outputs serve as the circuit's outputs. If control over counting direction (up or down) is needed, an input can be added for this purpose.

Design steps for a 3-bit binary counter:

Since the counter will count from 0 to 7, it requires 8 distinct states, which means 3 flip-flops. Let's name these flip-flops as q_C (MSB), q_B, and q_A (LSB).

$$q_C \ q_B \ q_A$$

$$000 \longrightarrow 001 \longrightarrow 010 \longrightarrow 011 \longrightarrow 100 \longrightarrow 101 \longrightarrow 110 \longrightarrow 111$$

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Example (2nd Page)

Present State $q_C q_B q_A$	Next State $Q_C Q_B Q_A$
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0

Present State $q_C q_B q_A$	Next State $Q_C Q_B Q_A$	J_C K_C	J_B K_B	J_A K_A
		Flip-Flop Inputs		
0 0 0	0 0 1	0 x	0 x	1 x
0 0 1	0 1 0	0 x	1 x	x 1
0 1 0	0 1 1	0 x	x 0	1 x
0 1 1	1 0 0	1 x	x 1	x 1
1 0 0	1 0 1	x 0	0 x	1 x
1 0 1	1 1 0	x 0	1 x	x 1
1 1 0	1 1 1	x 0	x 0	1 x
1 1 1	0 0 0	x 1	x 1	x 1

Using Karnaugh maps, we determine that:

$J_C = K_C = q_B \cdot q_A$
$J_B = K_B = q_A$
$J_A = K_A = 1$

It can be inferred that if we were to design a 4-bit counter, the equation for J_D and K_D would be as follows:
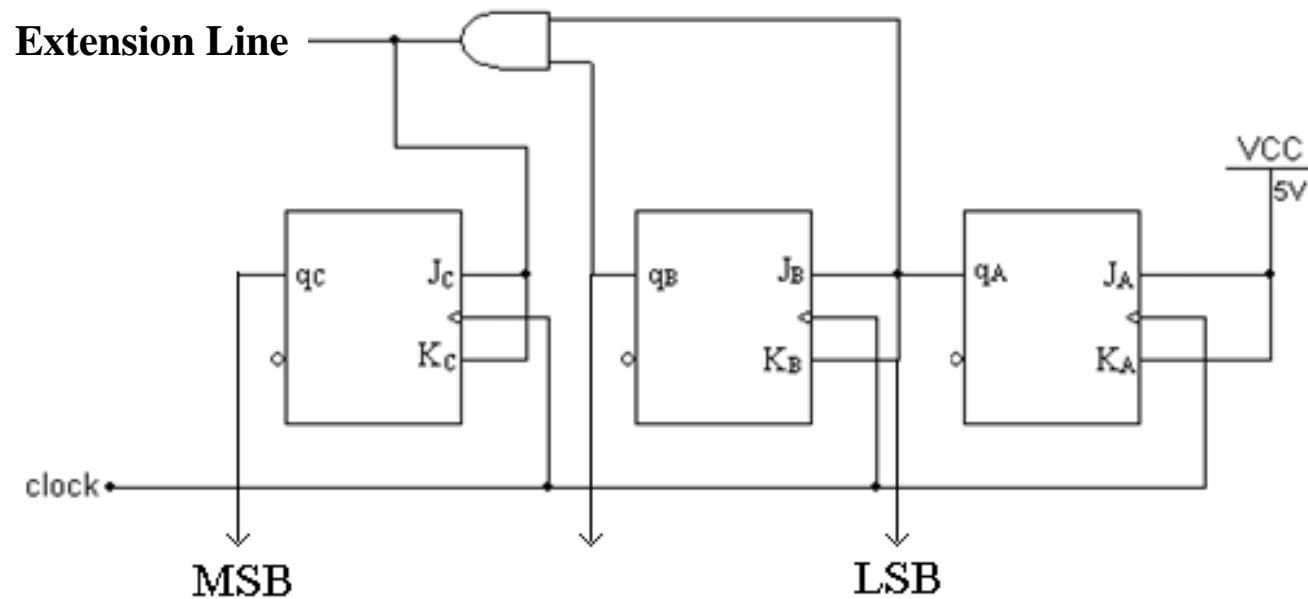
$J_D = K_D = q_C \cdot q_B \cdot q_A$

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Example (3rd Page)

$$J_C = K_C = q_B \cdot q_A$$
$$J_B = K_B = q_A$$
$$J_A = K_A = 1$$

Logic Diagram for a 3-bit Counter

More About Counters

1. If we use q' instead of q as the circuit's output in an up counter, the circuit will function as a down counter, and vice versa.

2. If the counter application is not sequential, the design steps remain the same. However, if there are unused states, the next state is treated as a don't-care condition. In such cases, if the circuit starts from one of these states, it becomes impossible to predict the next state (to prevent this, flip-flops have clear and preset inputs in addition to D/T/SR/JK inputs). Preset and Clear inputs override the clock signal to set or reset the output of flip-flops, and they are used to initialize the state of the flip-flops.

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