# تکلیف سری چهارم درس زبان های توصیف سخت افزار و مدارات

## گزارشات سوال اول:

```
================================================================================
                                *Design Summary*
================================================================================
Top Level Output File Name         : Top_module.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                      : 499
#      GND                  : 1
#      INV                  : 1
#      LUT1                 : 60
#      LUT2                 : 45
#      LUT3                 : 2
#      LUT4                 : 85
#      LUT5                 : 3
#      LUT6                 : 101
#      MUXCY                : 130
#      VCC                  : 1
#      XORCY                : 70
# FlipFlops/Latches         : 76
#      FDC                  : 70
#      FDCE                 : 6
# Clock Buffers             : 1
#      BUFGP                : 1
# IO Buffers                : 99
#      IBUF                 : 97
#      OBUF                 : 2

Device utilization summary:
---------------------------
Selected Device : 6slx16csg324-3
Slice Logic Utilization:
 Number of Slice Registers:          76  out of  18224     0%
 Number of Slice LUTs:              297  out of   9112     3%
   Number used as Logic:            297  out of   9112     3%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   299
   Number with an unused Flip Flop:    223  out of    299    74%
   Number with an unused LUT:          2  out of    299     0%
   Number of fully used LUT-FF pairs:  74  out of    299    24%
   Number of unique control sets:      3

IO Utilization:
 Number of IOs:                100
 Number of bonded IOBs:            100  out of    232    43%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:           1  out of     16     6%
```



ملوین مختاری (۹۸۳۱۱۴۳)

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Partition Resource Summary:
---
No Partitions were found in this design.
---

==========
Timing Report
==========
Timing Summary:
---
Speed Grade: -3

Minimum period: ۳.۹۲۱ns (Maximum Frequency: ۳۳٤.۷۲۱MHz)
Minimum input arrival time before clock: ۱٤.۱۳۸ns
Maximum output required time after clock: ۲.۲۹۱ns
Maximum combinational path delay: No path found

Timing Details:
---
All values displayed in nanoseconds (ns)

==========
Timing constraint: Default period analysis for Clock 'Clock'
Clock period: 3.۹۲۱ns (frequency: ۳۳٤.۷۲۱MHz)
Total number of paths / destination ports: 1890 / 82
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گزارشات ماژول سوال دوم-بخش اول:

```
================================================================================
                        *                Design Summary                *
================================================================================
Top Level Output File Name         : Correlation_32.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                      : 1235
#      LUT2                : 289
#      LUT3                : 51
#      LUT4                : 131
#      LUT5                : 133
#      LUT6                : 630
#      MUXF7               : 1
# FlipFlops/Latches         : 4
#      FDC                 : 4
# Clock Buffers             : 1
#      BUFGP               : 1
# IO Buffers                : 549
#      IBUF                : 545
#      OBUF                : 4

Device utilization summary:
---------------------------
Selected Device : 6slx16csg324-3

Slice Logic Utilization:
 Number of Slice LUTs:              1234  out of   9112    13%
   Number used as Logic:            1234  out of   9112    13%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   1234
   Number with an unused Flip Flop:    1234  out of   1234   100%
   Number with an unused LUT:             0  out of   1234     0%
   Number of fully used LUT-FF pairs:     0  out of   1234     0%
   Number of unique control sets:         1

IO Utilization:
 Number of IOs:                  550
 Number of bonded IOBs:              550  out of    232   237% (*)
   IOB Flip Flops/Latches:           4

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:             1  out of     16     6%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
```

```
==========================================================================================
                                    Timing Report
==========================================================================================
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: ۷۹.۲٦٤ns
   Maximum output required time after clock:٤ .۱٥۲ns
   Maximum combinational path delay: No path found

Timing Details:
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All values displayed in nanoseconds (ns)

==========================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clock'
  Total number of paths / destination ports: ۷۸1132318591404 / 8
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```

گزارشات ماژول سوال دوم-بخش دوم:

```
================================================================================
                                        *Design Summary*
================================================================================
Top Level Output File Name         : RFCorrelator.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                      : 76
#      GND                 : 1
#      INV                 : 1
#      LUT2                : 4
#      LUT3                : 10
#      LUT4                : 7
#      LUT5                : 19
#      LUT6                : 30
#      MUXF7               : 4
# FlipFlops/Latches         : 38
#      FDC                 : 38
# Clock Buffers             : 1
#      BUFGP               : 1
# IO Buffers                : 6
#      IBUF                : 2
#      OBUF                : 4

Device utilization summary:
---------------------------
Selected Device : 6slx16csg324-3

Slice Logic Utilization:
 Number of Slice Registers:           38  out of  18224     0%
 Number of Slice LUTs:                71  out of   9112     0%
    Number used as Logic:             71  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   102
   Number with an unused Flip Flop:    64  out of    102    62%
   Number with an unused LUT:          31  out of    102    30%
   Number of fully used LUT-FF pairs:   7  out of    102     6%
   Number of unique control sets:       1

IO Utilization:
 Number of IOs:                   7
 Number of bonded IOBs:           7  out of    232     3%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:        1  out of     16     6%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
```

==========
Timing Report
==========

Timing Summary:
---
Speed Grade: -3

Minimum period: ۷.۱۵۳ns (Maximum Frequency: ۱۵۷.۹۲۱MHz)
Minimum input arrival time before clock: ۷.۲۶۳ns
Maximum output required time after clock: 3.۷۳۴ns
Maximum combinational path delay: No path found

Timing Details:
---
All values displayed in nanoseconds (ns)

==========
Timing constraint: Default period analysis for Clock 'Clock'
Clock period: ۷.۱۵۳ns (frequency: ۱۵۷.۹۲۱MHz)
Total number of paths / destination ports: 888 / 37
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