تکلیف سری سوم درس زبان های توصیف سخت افزار و مدارات

گزارشات ماژول RegisterBank (سوال اول تکلیف دوم که کدش به درستی قابل سنتز بود):

```
==========================================================================
                                *Design Summary*
==========================================================================
Top Level Output File Name         : RegisterBank.ngc

Primitive and Black Box Usage:
------------------------------
 #BELS                     : 4217
      #INV                 : 1
      #LUT2                : 1
      #LUT3                : 80
      #LUT5                : 2299
      #LUT6                : 1835
      #MUXF7               : 1
 #FlipFlops/Latches        : 2176
      #FDR                 : 128
      #FDRE                : 2048
 #Clock Buffers            : 1
      #BUFGP               : 1
 #IO Buffers               : 78
      #IBUF                : 45
      #OBUFT               : 33

Device utilization summary:
---------------------------
Selected Device : 6slx16csg324-3

Slice Logic Utilization :
 Number of Slice Registers:         2176  out of  18224    11%
 Number of Slice LUTs:              4216  out of   9112    46%
    Number used as Logic:           4216  out of   9112    46%

Slice Logic Distribution :
 Number of LUT Flip Flop pairs used:   4216
   Number with an unused Flip Flop:    2040  out of   4216    48%
   Number with an unused LUT:             0  out of   4216     0%
   Number of fully used LUT-FF pairs:  2176  out of   4216    51%
   Number of unique control sets:      128

IO Utilization :
 Number of IOs:                 79
 Number of bonded IOBs:             79  out of    232    34%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:          1  out of     16     6%
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Partition Resource Summary:
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  No Partitions were found in this design.
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```


ملوین مختاری (۹۸۳۱۱۴۳)

```
==========================================================================
                                Timing Report
==========================================================================
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 1.321ns (Maximum Frequency: 637.814MHz)
   Minimum input arrival time before clock: 8.835ns
   Maximum output required time after clock: 7.259ns
   Maximum combinational path delay: 12.763ns

Timing Details:
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All values displayed in nanoseconds (ns)

==========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 1.321ns (frequency: 637.814MHz)
  Total number of paths / destination ports: 4288 / 2176
```

تکلیف سری سوم درس زبان های توصیف سخت افزار و مدارات

گزارشات ماژول m_counter (سوال دوم تکلیف دوم که کدش به درستی قابل سنتز بود):

```
================================================================================
*                      Design Summary                      *
================================================================================
Top Level Output File Name         : m_counter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                      : 140
#      GND                  : 1
#      INV                  : 4
#      LUT2                 : 13
#      LUT3                 : 15
#      LUT4                 : 28
#      LUT5                 : 16
#      LUT6                 : 6
#      MUXCY                : 32
#      VCC                  : 1
#      XORCY                : 24
# FlipFlops/Latches         : 29
#      FDC                  : 3
#      FDCE                 : 26
# Clock Buffers             : 1
#      BUFGP                : 1
# IO Buffers                : 48
#      IBUF                 : 23
#      OBUF                 : 25
# DSPs                      : 2
#      DSP48A1              : 2

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:
 Number of Slice Registers:          29  out of  18224     0%
 Number of Slice LUTs:               82  out of   9112     0%
    Number used as Logic:            82  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    84
   Number with an unused Flip Flop:     55  out of    84    65%
   Number with an unused LUT:           2  out of    84     2%
   Number of fully used LUT-FF pairs:   27  out of    84    32%
   Number of unique control sets:       7

IO Utilization:
 Number of IOs:                49
 Number of bonded IOBs:             49  out of    232    21%
```


ملوین مختاری (۹۸۳۱۱۴۳)

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs: 1 out of 16 6%
 Number of DSP48A1s: 2 out of 32 6%

Partition Resource Summary:

 No Partitions were found in this design.

==========
Timing Report
==========
Timing Summary:

Speed Grade: -3

 Minimum period: 2.393ns (Maximum Frequency: 346.514MHz)
 Minimum input arrival time before clock: 3.921ns
 Maximum output required time after clock: 16.114ns
 Maximum combinational path delay: 7.213ns

Timing Details:

All values displayed in nanoseconds (ns)

==========
Timing constraint: Default period analysis for Clock 'Clock'
 Clock period: 2.393ns (frequency: 346.514MHz)
 Total number of paths / destination ports: 140 / 52

گزارشات ماژول sequence_detector (سوال سوم تکلیف دوم که کدش قابل سنتز بود):

```
================================================================================
                                        *Design Summary*
================================================================================
Top Level Output File Name         : sequence_detector.ngc
Primitive and Black Box Usage:
------------------------------
 #BELS                     : 77
      #GND                 : 1
      #INV                 : 3
      #LUT1                : 15
      #LUT2                : 2
      #LUT3                : 18
      #LUT4                : 2
      #LUT5                : 1
      #LUT6                : 2
      #MUXCY               : 15
      #MUXF7               : 1
      #VCC                 : 1
      #XORCY               : 16
 #FlipFlops/Latches        : 27
      #FD_1                : 7
      #FDRE                : 4
      #FDRE_1              : 16
 #Clock Buffers            : 1
      #BUFGP               : 1
 #IO Buffers               : 21
      #IBUF                : 4
      #OBUF                : 17

Device utilization summary:
---------------------------
Selected Device : 6slx16csg324-3
Slice Logic Utilization :
 Number of Slice Registers:          27  out of  18224     0%
 Number of Slice LUTs:               43  out of   9112     0%
    Number used as Logic:            43  out of   9112     0%

Slice Logic Distribution :
 Number of LUT Flip Flop pairs used:    46
   Number with an unused Flip Flop:     19  out of    46    41%
   Number with an unused LUT:           3  out of    46     6%
   Number of fully used LUT-FF pairs:   24  out of    46    52%
   Number of unique control sets:       3

IO Utilization :
 Number of IOs:                 22
 Number of bonded IOBs:             22  out of    232     9%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:           1  out of    16     6%
```

```
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Partition Resource Summary:
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  No Partitions were found in this design.

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=====================================================================
                        Timing Report
=====================================================================

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.580ns (Maximum Frequency: 322.125MHz)
   Minimum input arrival time before clock: 3.291ns
   Maximum output required time after clock: 4.021ns
   Maximum combinational path delay: No path found

Timing Details:
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All values displayed in nanoseconds (ns)

=====================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 3.580ns (frequency: 322.125MHz)
  Total number of paths / destination ports: 358 / 60
```

گزارشات ماژول Binary_Divisibility_By_7 (سوال چهارم تکلیف دوم که کدش به درستی قابل سنتز بود):

```
================================================================================
                                    *Design Summary*
================================================================================
Top Level Output File Name         : Binary_Divisibility_By_7.ngc

Primitive and Black Box Usage:
------------------------------
 #BELS                     : 4
      #LUT3                : 1
      #LUT4                : 3
 #FlipFlops/Latches        : 3
      #FDR                 : 3
 #Clock Buffers            : 1
      #BUFGP               : 1
 #IO Buffers               : 6
      #IBUF                : 2
      #OBUF                : 4

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization :
 Number of Slice Registers:           3  out of  18224     0%
 Number of Slice LUTs:                4  out of   9112     0%
    Number used as Logic:             4  out of   9112     0%

Slice Logic Distribution :
 Number of LUT Flip Flop pairs used:     7
   Number with an unused Flip Flop:      4  out of     7    57%
   Number with an unused LUT:            3  out of     7    42%
   Number of fully used LUT-FF pairs:    0  out of     7     0%
   Number of unique control sets:        1

IO Utilization :
 Number of IOs:                   7
 Number of bonded IOBs:           7  out of    232     3%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:        1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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```

```
==========================================================================
                                Timing Report
==========================================================================

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 1.752ns (Maximum Frequency: 591.425MHz)
   Minimum input arrival time before clock: 2.425ns
   Maximum output required time after clock: 4.745ns
   Maximum combinational path delay: No path found

Timing Details:
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All values displayed in nanoseconds (ns)

==========================================================================
Timing constraint: Default period analysis for Clock 'Clock'
  Clock period: 1.752ns (frequency: 591.425MHz)
  Total number of paths / destination ports: 9 / 3
```

- لازم به ذکر است که تمامی قطعه کد های طراحی شده در تکلیف سری دوم، برای این تکلیف به درستی قابل سنتز بودند.