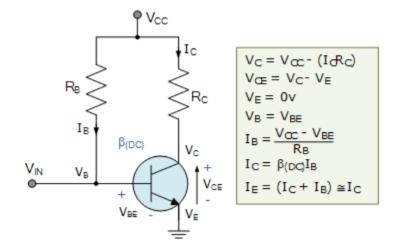
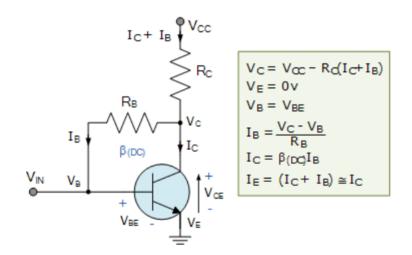
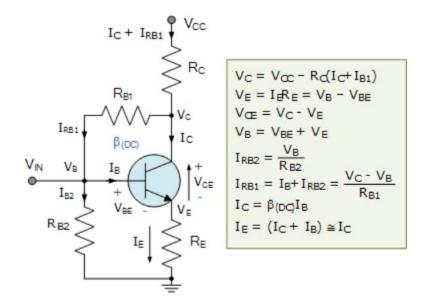
# Fixed Base Biasing a Transistor



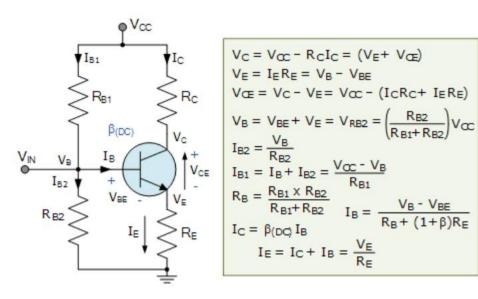
# **Collector Feedback Biasing**



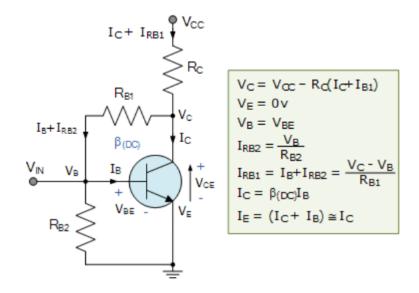
## **Emitter Feedback Configuration**



#### **Voltage Divider Transistor Biasing**



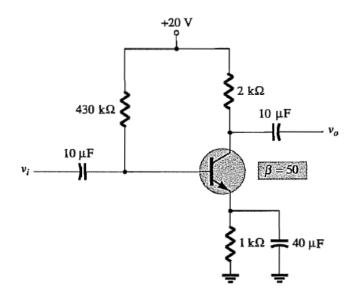
### **Dual Feedback Transistor Biasing**



For the emitter bias network of Fig. 1 determine:

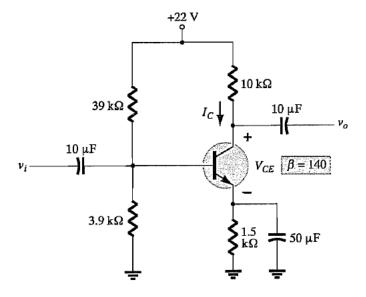
- a.  $I_B$ .
- b.  $I_C$ .
- c.  $V_{CE}$ .
- d.  $V_C$ . e.  $V_E$ . f.  $V_B$ .

- g.  $V_{BC}$ .

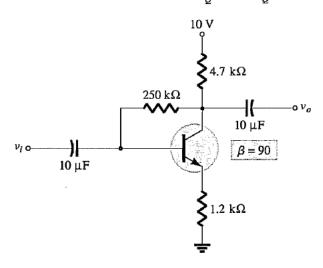


1.

Determine the dc bias voltage  $V_{CE}$  and the current  $I_C$  for the voltage-divider configuration of Fig. 2

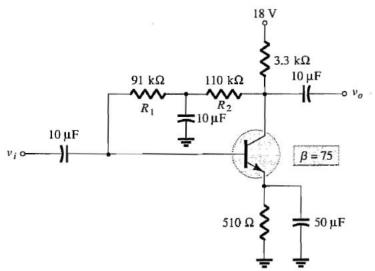


Determine the quiescent levels of  $I_{C_Q}$  and  $V_{CE_Q}$  for the network of Fig.

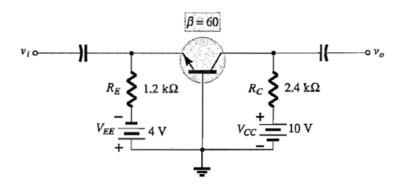


3.

Determine the dc level of  $I_B$  and  $V_C$  for the network of Fig.



4. Determine the voltage  $V_{CB}$  and the current  $I_B$  for the common-base configuration of Fig. 4.



5.