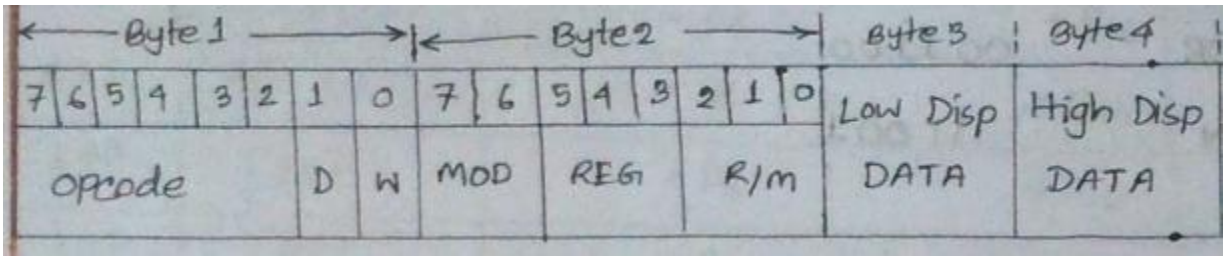
Converting assembly language to machine language

The general instruction for converting assembly language into machine code is given below:



Opcode: Operation code

Operation	**Opcode**
MOV	100010
ADD	000000
SUB	010010
XOR	001100
IN	111001

D: Direction to register or from register

=1 if destination is considered

=0 if source is considered

W: Word or byte

=0 for 8 bit register

=1 for 16 bit register

MOD: Register mode or memory mode with displacement

MOD	**Indication**
00	Memory mode, no displacement
01	Memory mode, with 8 bit displacement. For example: [BX]+12H
10	Memory mode, with 16 bit displacement. For example: [BX]+1234H
11	Register mode, no displacement

REG: Identifies a register which is one of the instruction operands.

REG	**W=0**	**W=1**
000	AL	AX
001	CL	CX
010	DL	DX
011	BL	BX, DS
100	AH	SP
101	CH	BP
110	DH	SI
111	BH	DI

R/M: Register/Memory coding

– Depends on the MOD field

• If MOD = 11, then R/M field acts as a REG field (used for register to-register operations and other cases).

• If MOD ≠ 11, then R/M indicates how the effective address of the operand is calculated.

MOD / R/M	00	01	10	11	
				W=0	W=1
000	[BX]+[SI] (=P)	→ P + D_8	→ P + D_{16}	AL	AX
001	[BX]+[DI]	+ D_8	+ D_{16}	CL	CX
010	[BP]+[SI]	+ D_8	+ D_{16}	DL	DX
011	[BP] + [DI]	+ D_8	+ D_{16}	BL	BX
100	[SI]	+ D_8	+ D_{16}	AH	SP
101	[DI]	+ D_8	+ D_{16}	CH	BP
110	Direct address	[SP] + D_8	[SP] + D_{16}	DH	SI
110	[BX]	+ D_8	+ D_{16}	BH	DI

Example-1: Convert the following assembly language into machine language.

MOV BL,AL

Solution:

Here, opcode: MOV

Assume, destination register is considered (BL)

hence, **Opcode:** 100010

D=1

W=0

REG: 011

MOD: 11

R/M: 000

Byte 1								Byte 2							
1	0	0	0	1	0	1	0	1	1	0	1	1	0	0	0
Opcode						D	W	Mod		REG			R/M		

Example-2: Repeat example-1 considering register as source.

Solution:

Here, AL is source register.

Here, opcode: MOV

Assume, source register is considered (AL)

hence, **Opcode:** 100010

D=0

W=0

REG: 000

MOD: 11

R/M: 011

Byte 1								Byte 2							
1	0	0	0	1	0	0	0	1	1	0	0	0	0	1	1
Opcode						D	W	Mod		REG			R/M		

Example-3: ADD AX,[SI]

Solution:

Here, opcode: ADD

Assume, destination register is considered (AX)

Hence, **Opcode:** 000000

D=1

W=1

REG: 000

MOD: 00

R/M: 100

Byte 1								Byte 2							
0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0
Opcode						D	W	Mod		REG			R/M		

Example-4: ADD AX, [SI] + 12H

Solution:

Here, opcode: ADD

Assume, destination register is considered (AX)

Hence, **Opcode:** 000000

D=1

W=1

REG: 000

MOD: 01

R/M: 100

Byte 1								Byte 2								Byte 3							
0	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0	0	0	0	1	0	0	1	0
Opcode						D	W	Mod		REG			R/M			Displacement							

Assignment:

Example-5: ADD AX, [SI]+1234H

Example-6: XOR CL, [1234H]

Solution: Here, opcode: XOR

Destination register is CL

Hence, **Opcode:** 001100

D=1

W=0

REG: 001

MOD: 00

R/M: 110

Byte 1								Byte 2								Byte 3							
0	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0	0	0	1	1	0	1	0	0
Opcode						D	W	Mod		REG			R/M			Lower byte							

Byte 4							
0	0	0	1	0	0	1	0
Higher byte							