FIELD EFFECT TRANSISTOR (FET)

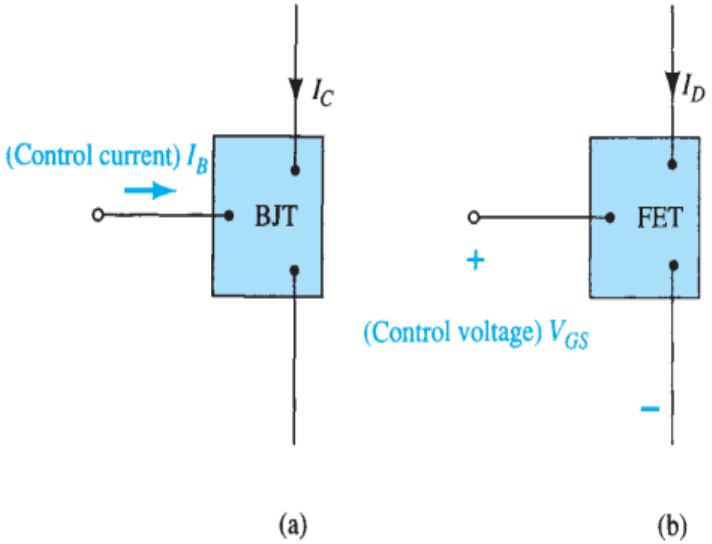
PREPARED BY-

SADIA ENAM,

LECTURER, DEPT. OF IRE, BDU

INTRODUCTION

- The field-effect transistor (FET) is a three-terminal, voltage controlled device
- The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.
- High input impedance
- More temperature stable
- Smaller in size
- Faster response



Three types:

i) JFET Junction Feild Effect Transistor

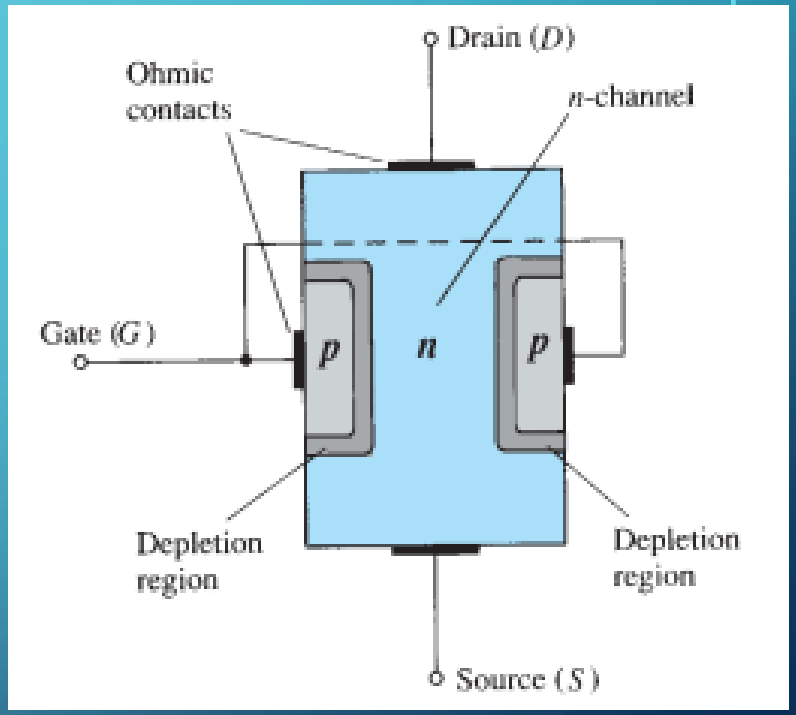
ii) MOSFET

iii)MESFET

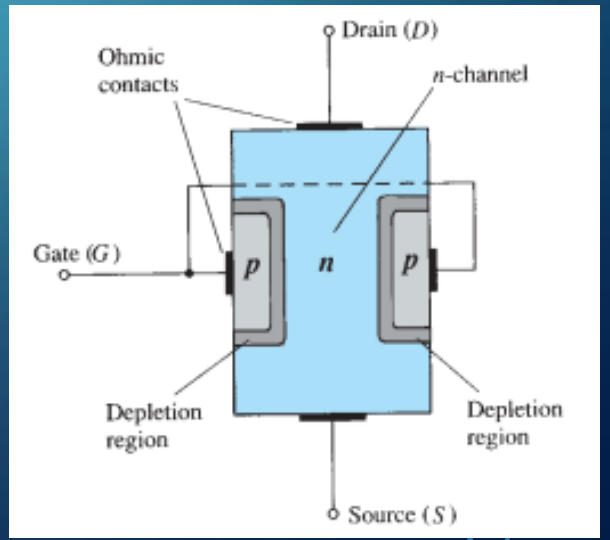
CONSTRUCTION [n-channel JFET]

- The major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material.
- The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D).*
- The lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).*
- The two *p*-type materials are connected together and to the *gate (G)* terminal.
- In the absence of any applied potentials the JFET has two *p–n* junctions under no-bias conditions

.The result is a depletion region at each junction.

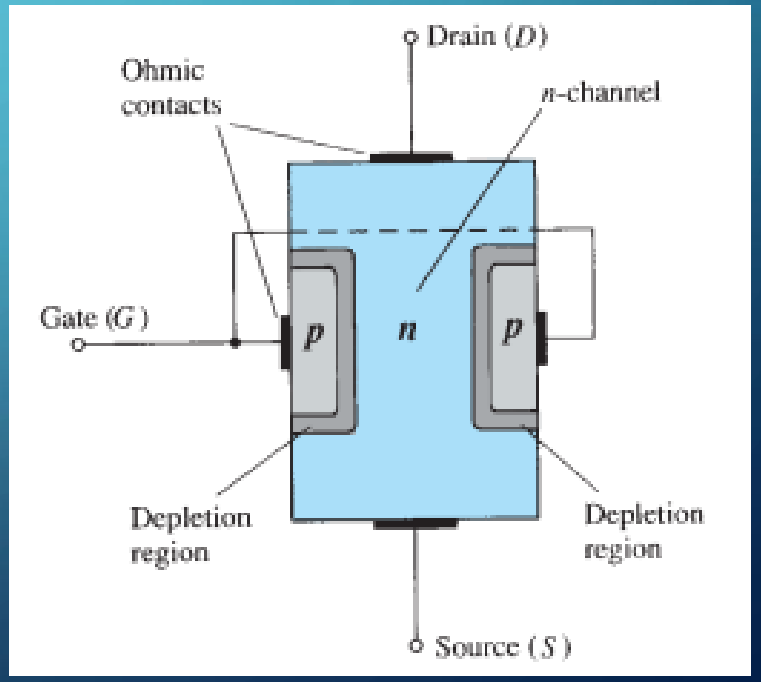


- FET uses electric field to control the flow of current through the device
- In FET current is used to flow between drain and source
- This current is controlled by applying voltage between gate and source
- So, this Vgs generates the electric field within the device by controlling the electric field/ Vgs.
- This is why it is called FET
- The path through which charge carriers flow is called channel
- The gate terminal is placed very closed to the channel so that it can control the current flow through the channel



WHY FET IS CALLED JFET?

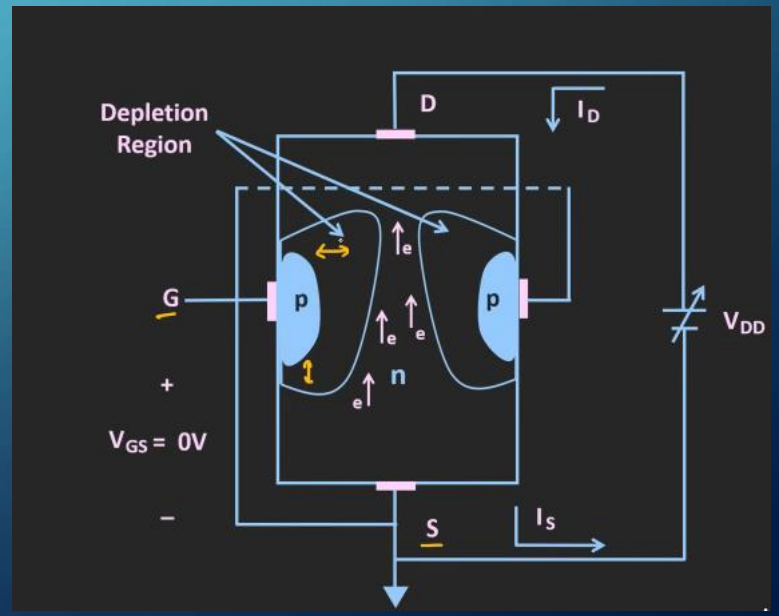
- In n-channel FET two small p-type regions are fabricated near the channel and due to that PN junction is formed near the channel and whenever the junction is reverse biased depletion layer is created which isolates the gate terminal from the channel. And only a few amount of reverse saturation current is used to flow between this two region.
- This is why this type of FET is called JFET



if Vds = 0 => no biasing

WORKING OF N-CHANNEL FET ($V_{GS}= 0, V_{DD} = V_{DS} > 0$)

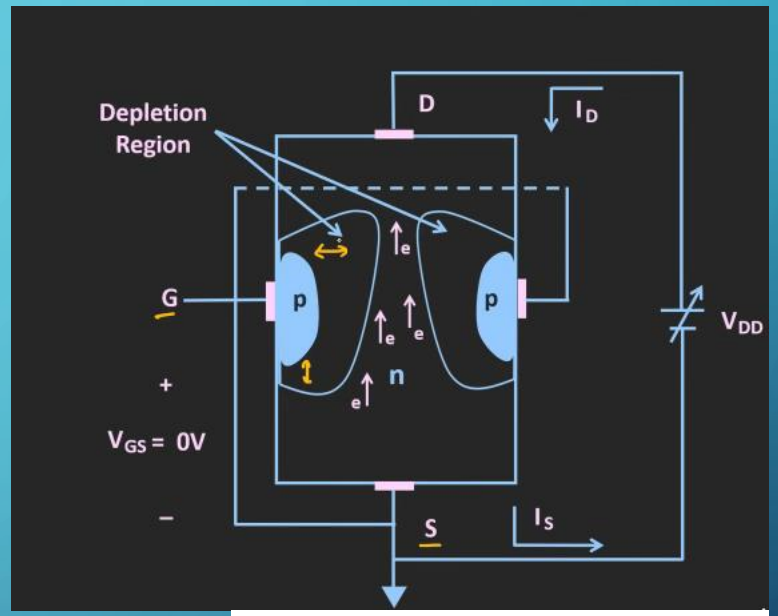
- When Vds is applied to the drain and source terminal and Vds is positive, the drain terminal should be more positive than the source terminal.
- Once voltage is applied the electrons start flowing towards the drain terminal from source as current flows from drain to source.
- Id=Is
- Whenever Vds is positive the two PN junction becomes reverse biased and the depletion region will increase.
- During this operation the n-channel acts as a resistor.

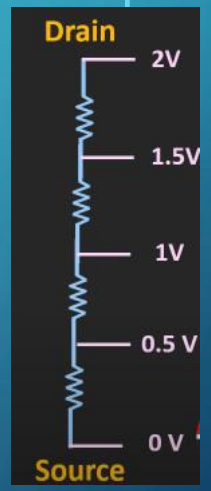


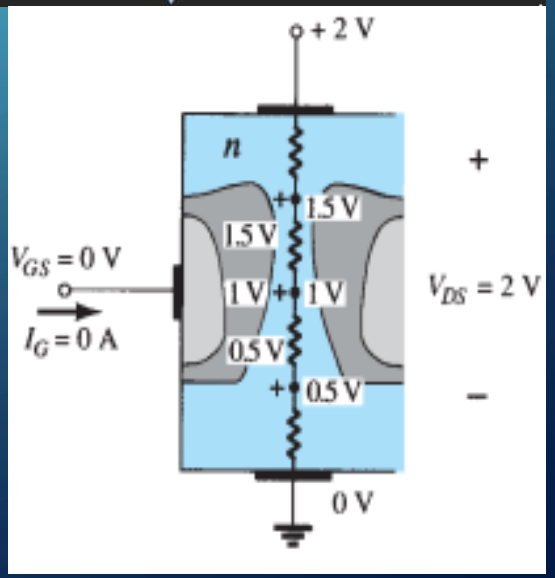
WORKING OF N-CHANNEL FET ($V_{GS}= 0, V_{DD} = V_{DS} > 0$)

- So this channel can be modeled as a series of distributed resistors between the drain and source.
- When Id flows, there will be a voltage drop in each resistor.
- The top has 2V. As we move towards the source, there will be a voltage drop across each resistor.
- Due to this, the upper region will be more reverse biased compared to the lower.
- For which depletion region is wider in the top and narrower at the bottom.

I=V/R; since Id=Is, if V gets low, R must also get lower meaning top is more resistive than bottom, thus get the butterfly/ apple shaped depletion layer.

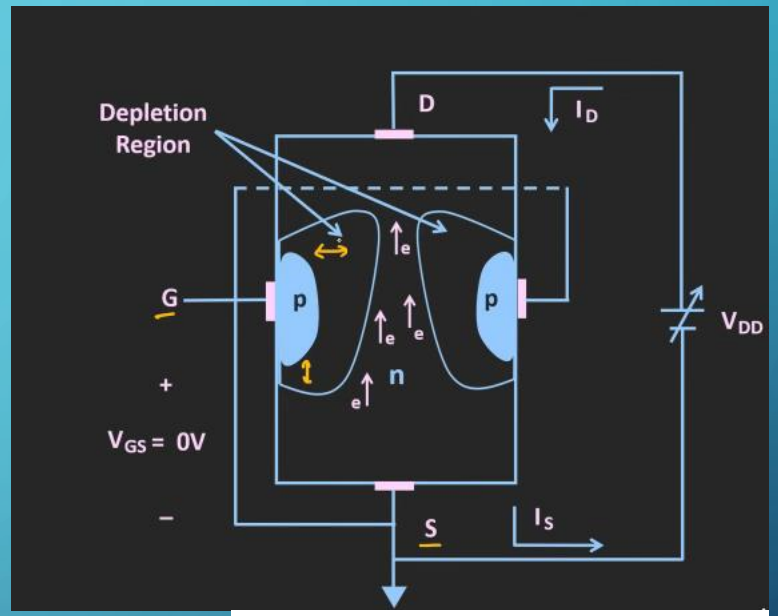


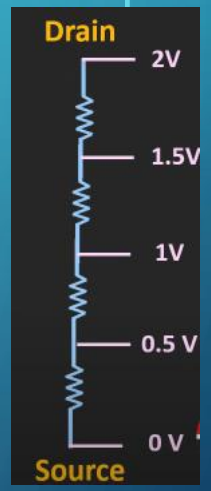


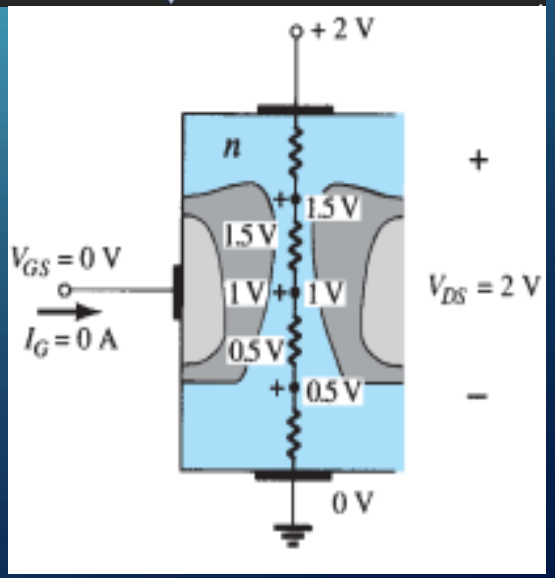


WORKING OF N-CHANNEL FET ($V_{GS}= 0, V_{DD} = V_{DS} > 0$)

- For which a small amount of reverse current will flow.
- Ig will be 0 through the gate terminal as due to wider depletion region the gate terminal is isolated from the channel.
- Due to this the input impedance is high in FET.

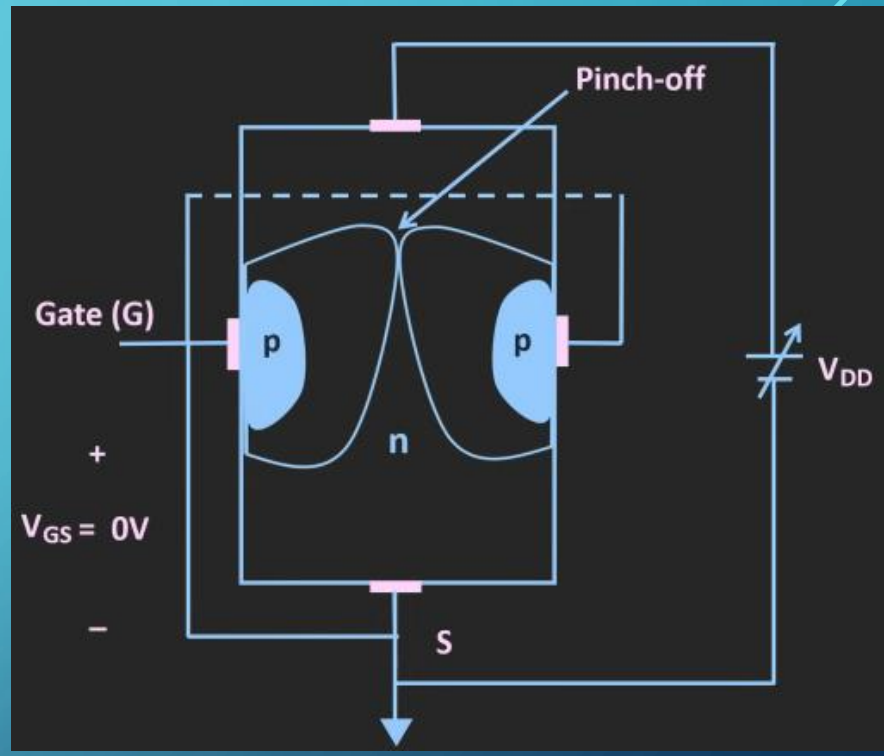






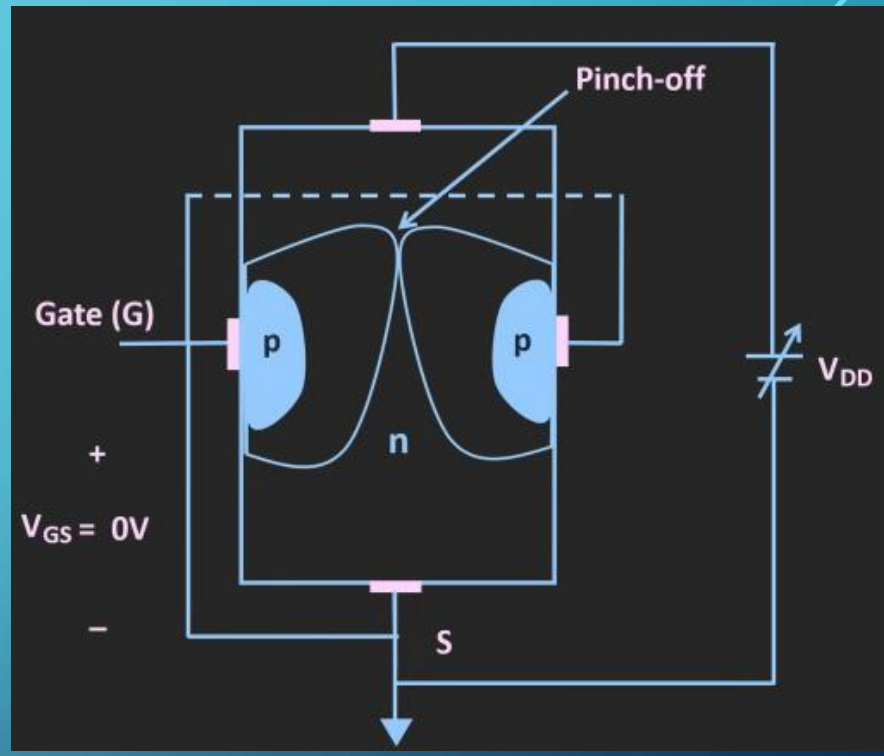
WORKING OF N-CHANNEL FET ($V_{GS}= 0, V_{DD} = V_{DS} > 0$)

- If we increase the Vds from 0 to some voltages, current flow will increase meaning that for the low voltages, the resistance of the channel remains constant.
- If we keep on increasing Vds the width of depletion region will be wider
- Due to that channel will become narrower.
- Due to the reduced channel width, the channel resistance will increase.
- If further Vds is increased at one time the two depletion region will touch each other. This is called pinch off condition



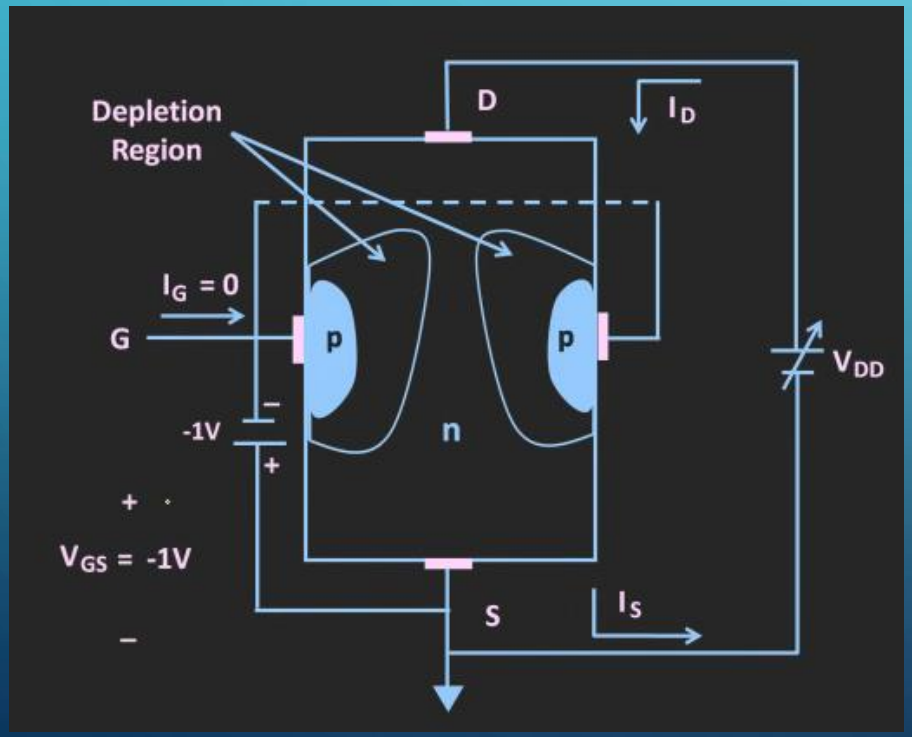
WORKING OF N-CHANNEL FET ($V_{GS}= 0, V_{DD} = V_{DS} > 0$)

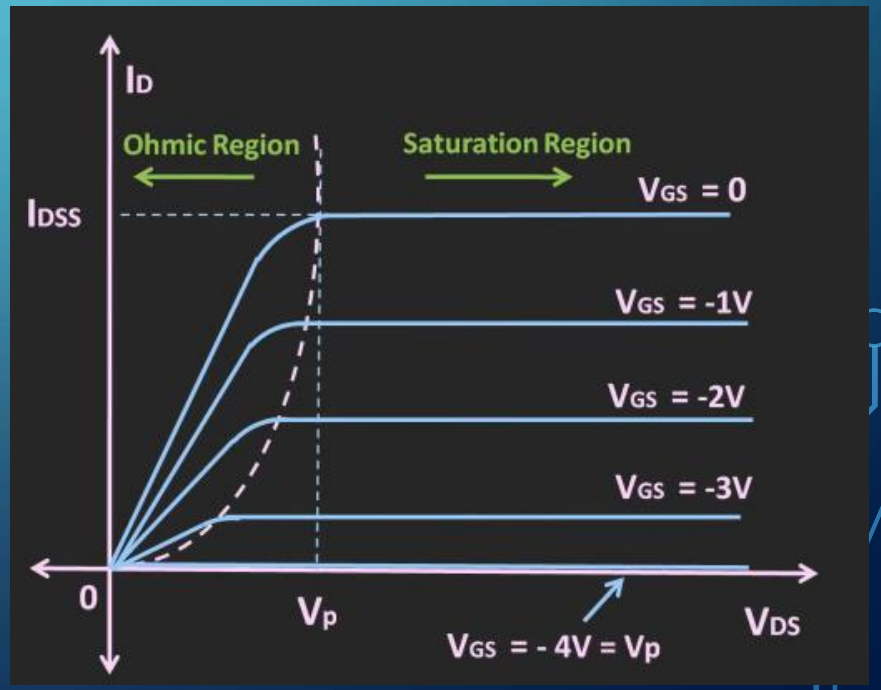
- The Vds at which pinch off occurs is called Vp and Vds≥ Vp.
- When Vp occurs Id reaches to saturation.
- Let, Id=0 at pinch off condition
- The absence of Id will remove the possibility of different voltages across the channel.
- For which the reverse bias across the junction will be removed.
- That results loss of depletion layer which caused pinch off first.
- So, Id≠0. it will be Idss



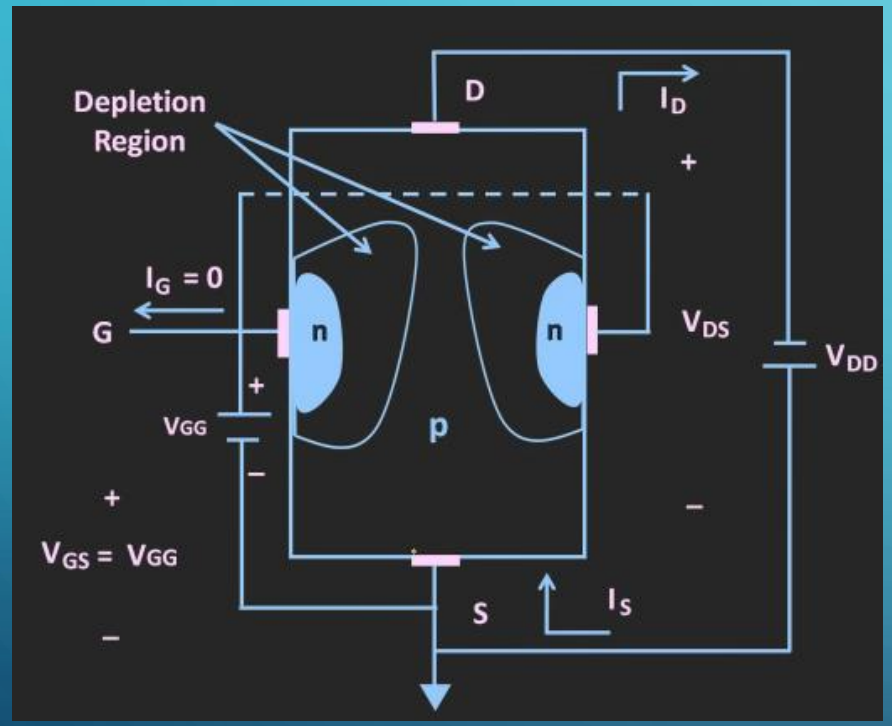
Case-2: $V_{GS} < 0, V_{DD} = V_{DS} > 0$

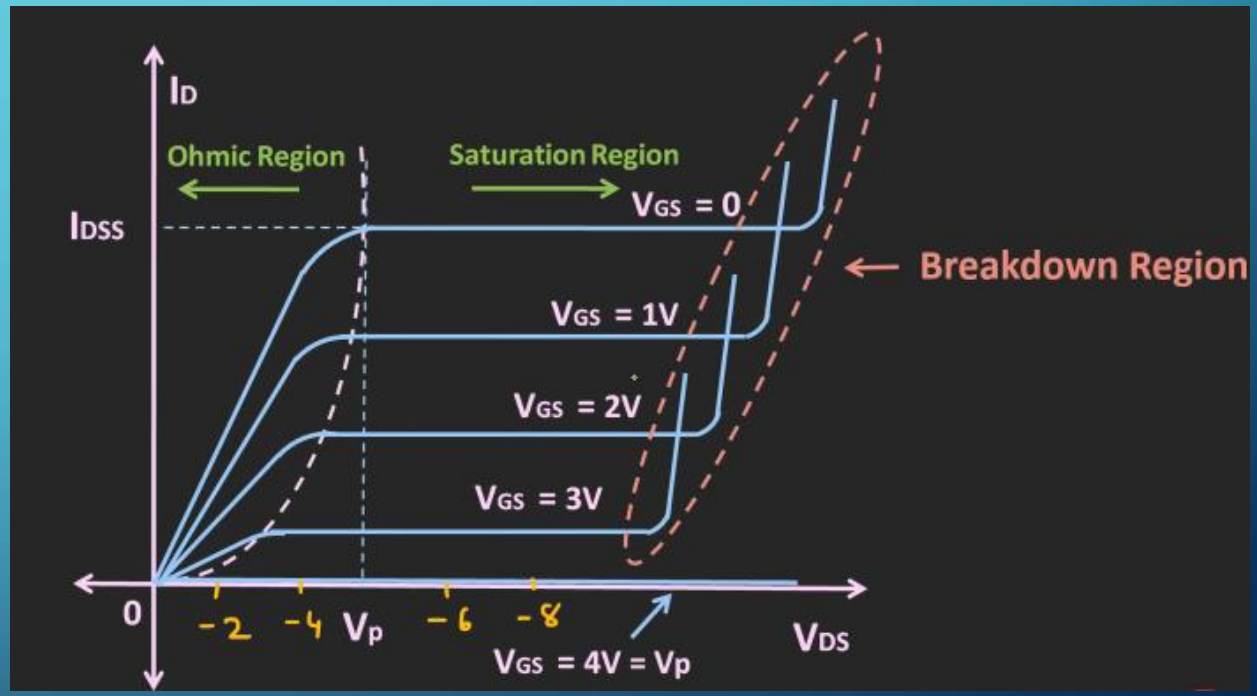
- If Vgs=-1V, the pinch off condition or saturation of Id will be reached at lower voltage of Vds.
- As the negative Vgs keeps the PN junction already reverse biased.
- When Vgs=-4V=-Vp, the Idss=0 and it is called cut off region.



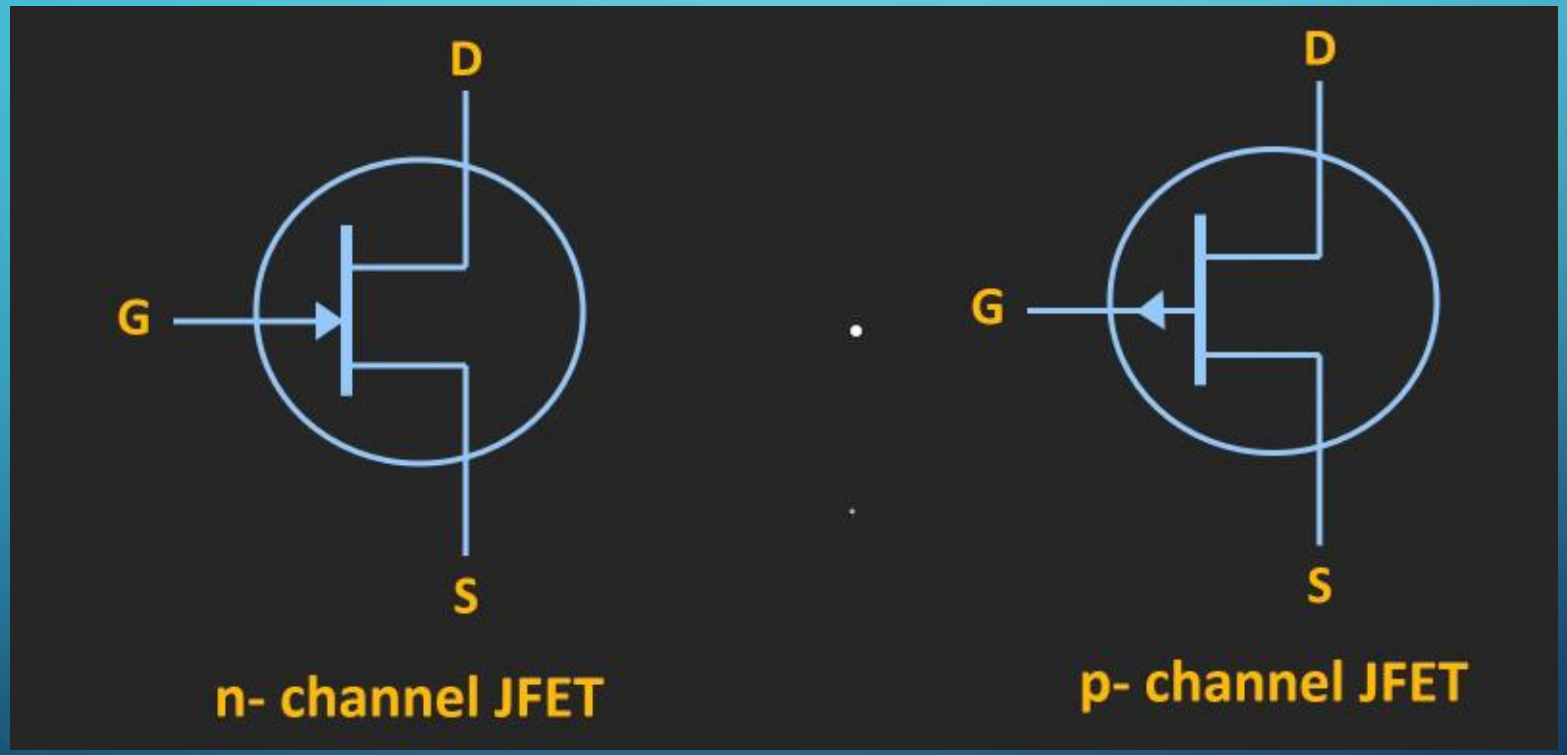


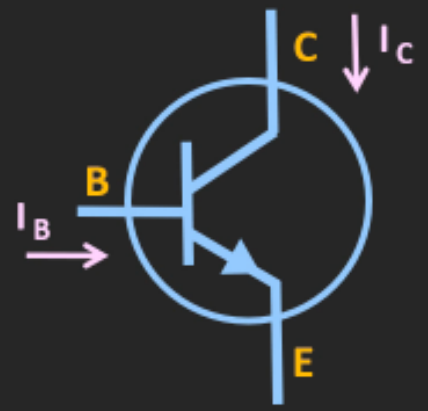
P-CHANNEL JFET





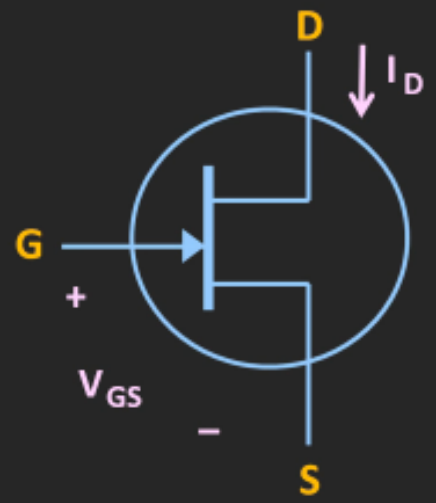
GRAPHICAL SYMBOL





BJT

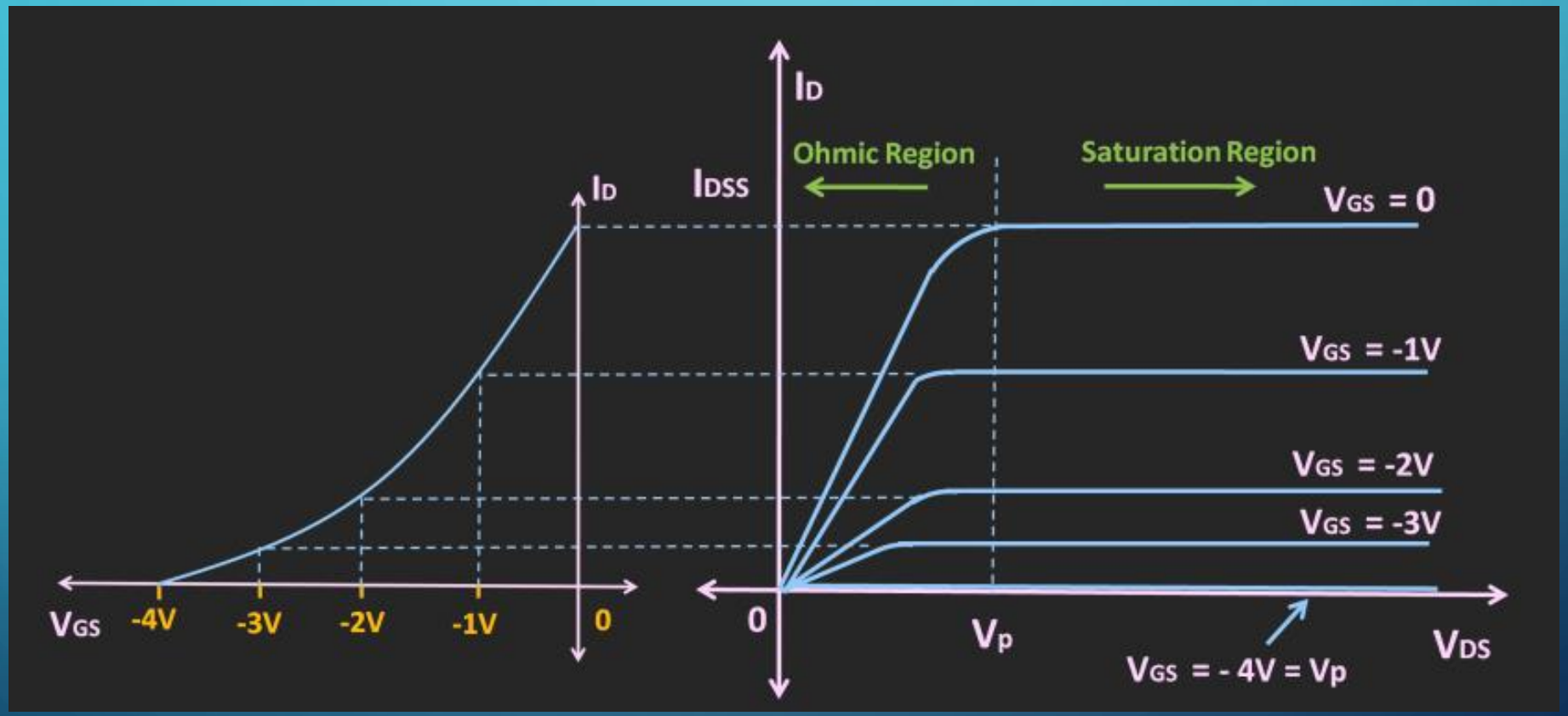
$$I_C = \beta I_B$$



FET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

TRANSFER CHARACTERISTICS OF N-CHANNEL JFET



Q1. Fig. 1 shows the transfer characteristic curve of a JFET. Write the equation for drain current.

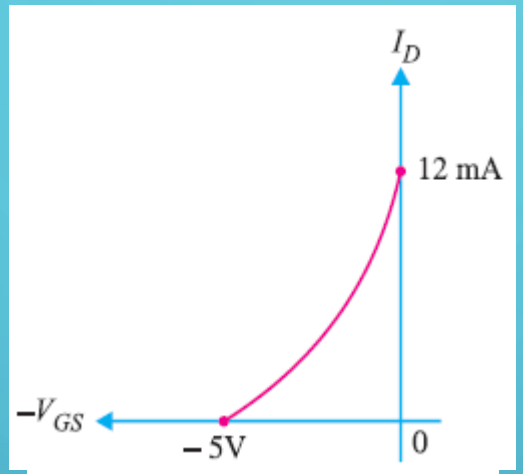


Fig.1

Solution. Referring to the transfer characteristic curve in Fig. 1, we have,

$$I_{DSS} = 12\text{ mA}$$

$$V_{GS\,(off)} = -5\text{ V}$$

$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

$$\text{or} \quad I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA}$$ **Ans.**

- **Q2. A JFET has the following parameters: IDSS = 32 mA ; VGS (off) = – 8V ; VGS = – 4.5 V. Find the value of drain current.**

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

$$= 32\left[1-\frac{(-4.5)}{-8}\right]^2 \text{ mA}$$

$$= \mathbf{6.12\ mA}$$

- **Q3. A JFET has a drain current of 5 mA. If IDSS = 10 mA and VGS (off) = – 6 V, find the value of (i) VGS and (ii) VP.**

Solution.

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

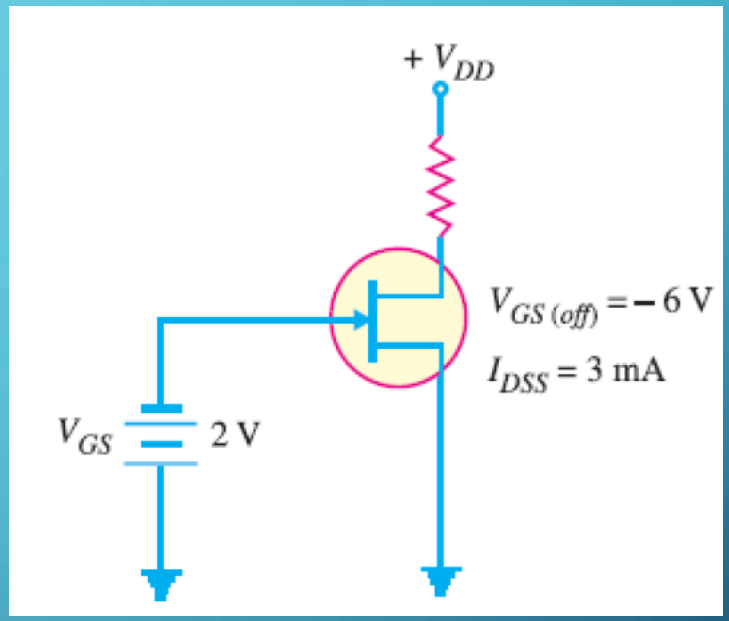
or $$5 = 10\left[1+\frac{V_{GS}}{6}\right]^2$$

or $$1+\frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

(*i*) $\therefore$ $$V_{GS} = \mathbf{-1.76\ V}$$

(*ii*) and $$V_P = -V_{GS\,(off)} = \mathbf{6\ V}$$

Q4. Determine the value of drain current for the circuit shown in Fig. 3.



Solution. It is clear from Fig. 3 that VGS = – 2V. The drain current for the circuit is given by;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 3\text{ mA}\left(1 - \frac{-2\text{V}}{-6\text{V}}\right)^2$$

$$= (3\text{ mA})\,(0.444) = \mathbf{1.33\text{ mA}}$$

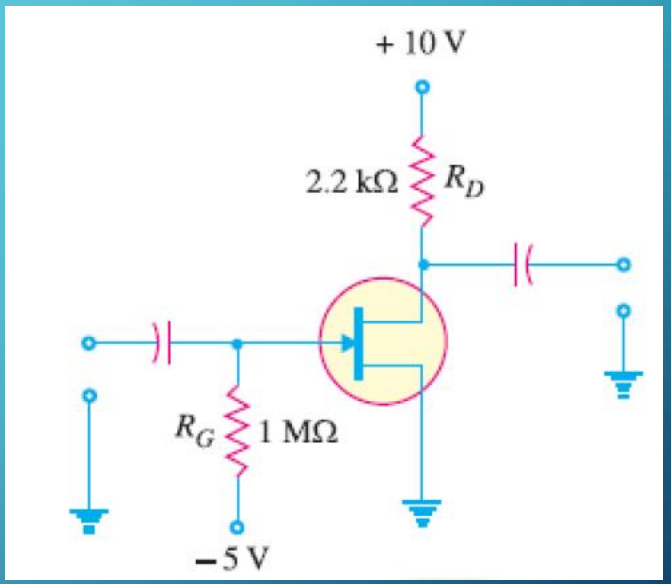
Q5. When a reverse gate voltage of 15 V is applied to a JFET, the gate current is10−3 μA. Find the resistance between gate and source.

Solution.

$$V_{GS} = 15\,\text{V};\ I_G = 10^{-3}\,\mu\text{A} = 10^{-9}\,\text{A}$$

$$\therefore \quad \text{Gate to source resistance} = \frac{V_{GS}}{I_G} = \frac{15\,\text{V}}{10^{-9}\,\text{A}} = 15 \times 10^9\,\Omega = \mathbf{15{,}000\ M\Omega}$$

Q6. A JFET in Fig. has values of VGS (off) = – 8V and IDSS = 16 mA. Determine the values of VGS, ID and VDS for the circuit.



Since there is no gate current, there will be no voltage drop across RG.

$$\therefore \quad V_{GS} = V_{GG} = -5\text{V}$$

Now
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 16\text{ mA}\left(1 - \frac{-5}{-8}\right)^2$$

$$= 16\text{ mA}\,(0.1406) = 2.25\text{ mA}$$

Also
$$V_{DS} = V_{DD} - I_D R_D$$

$$= 10\text{ V} - 2.25\text{ mA} \times 2.2\text{ k}\Omega = 5.05\text{ V}$$

Note that operating point for the circuit is 5.05V, 2.25 mA

Thank You!