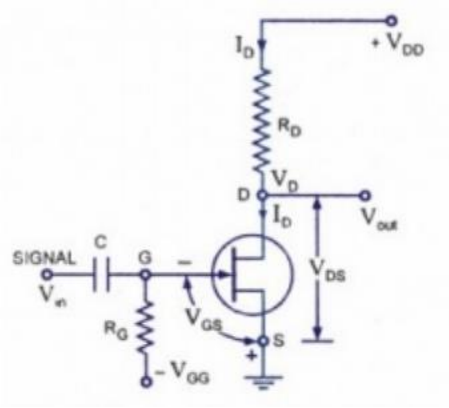
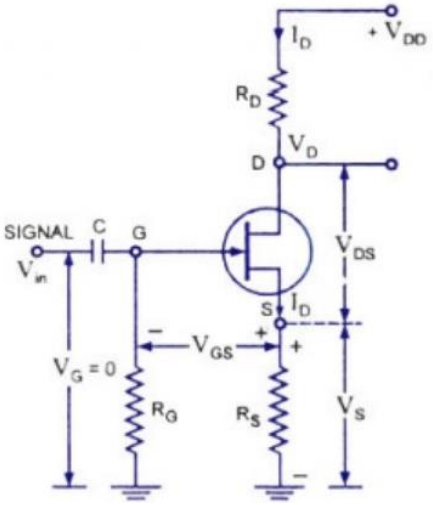
Experiment 8: N-Channel JFET Parameter Calculation and simulation in Proteus.

Theory: Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum transfer characteristics make ID levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents I_D and drain-source voltage V_{DS}, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for JFETs. Various FET Biasing Methods are discussed below :

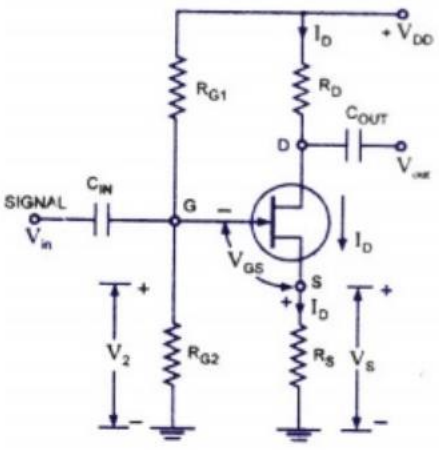
1. **Fixed Bias**



2. **Self Bias**



3. **Voltage Divider Bias**



Equipment and Software Requirements:

- Proteus simulation software
  - JFET (NJFET)
  - Resistor (8k)
  - Power (+24)
  - Cell (2.5V)
  - DC Voltmeter
  - DC Ammeter
- Computer with Proteus installed

Circuit Diagram:

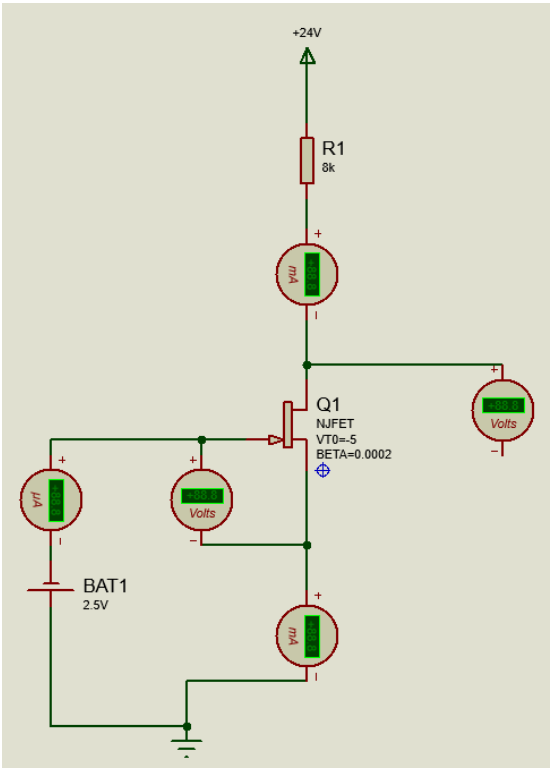


Figure-1: Self Bias Configuration

Data Collection and Analysis:

- Calculate each parameter (Ig, Id, Vgs, and Vds) by hand.
- Simulate the given circuit to determine the chosen parameters using proteus

Precautions:

- Ensure proper connections in the circuit.
- Use appropriate units and scales for measurements.
- Be cautious when using simulation software to avoid incorrect configurations.

Lab Task:

Repeat the experiment for fixed bias configuration.

Questions and Exercises:

1. are the advantages of using self-biasing (voltage divider biasing) in JFET circuits?
2. Can you explain the difference between fixed biasing and self-biasing in JFET circuits?
3. How does temperature variation affect the biasing stability of a JFET circuit?
4. What is the purpose of biasing in a JFET circuit?
5. How does the choice of biasing affect the operating point of a JFET?