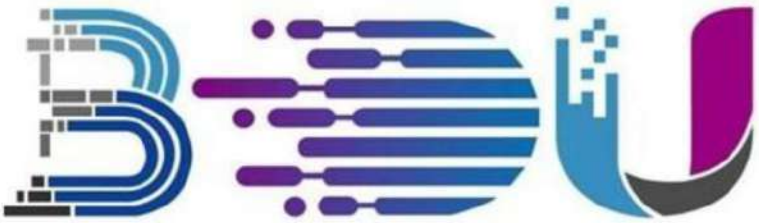

Bangabandhu Sheikh Mujibur Rahman Digital University

BANGABANDHU SHEIKH MUJIBUR RAHMAN DIGITAL UNIVERSITY, BANGLADESH

Department of Internet of Things and Robotics Engineering.
Faculty of Cyber-Physical System

Lab Report-06

Observing of BJT as a switch

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Date of Submission: 04 April, 2024

CONTENTS:

Experiment no: 06 (01)

Experiment Name: Observing of BJT as a switch.

Objective:

- To observe and understand the operation of a Bipolar Junction Transistor (BJT) as a switch.
- To differentiate between the NPN and PNP transistor configurations in switching applications.
- To study the characteristics of BJT in cutoff and saturation regions when used as a switch.
- To learn about the circuit design considerations and precautions when using a BJT as a switch.

Theory:

Transistors can serve as reliable switches, offering cost-effective alternatives to conventional relays. NPN and PNP transistors are both utilized in switching applications.

NPN Transistor:

Activation: Apply voltage (VIN > 0.7 V) between the base and emitter.

Operation: Acts as a short circuit; collector current flows.

Deactivation: Remove voltage; transistor operates in the cutoff, acting as an open circuit.

Load connected to output; current flows through the load when the transistor is ON.

PNP Transistor:

Activation: Apply low or more negative voltage to the base.

Operation: Acts as a short circuit; current flows from source to load to ground.

Deactivation: Remove base voltage; the transistor is an open circuit.

Used for negative ground setups; base always negatively biased concerning emitter.

Both configurations facilitate the opening and closing of circuits, with current flow determined by input voltage application or removal.

Required apparatus:

- Proteus simulation software
- NPN transistor
- Resistor (10k, 300)
- Power
- Logic probe (Toggle logic)
- LED

Circuit Diagram:

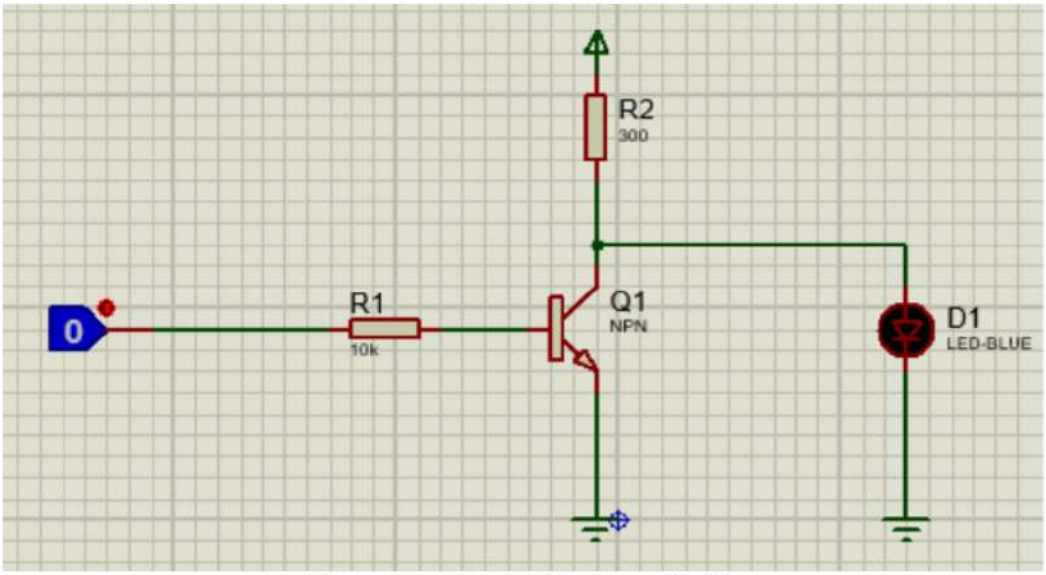

Figure 1: Circuit Diagram (**6.1**)

Output:

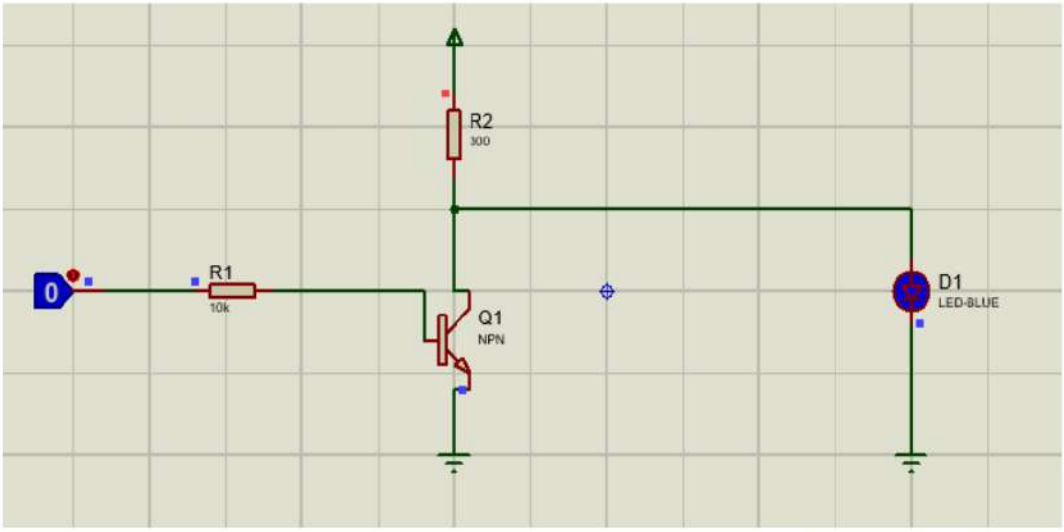

Figure 2: BJT ON when logic low (0V)

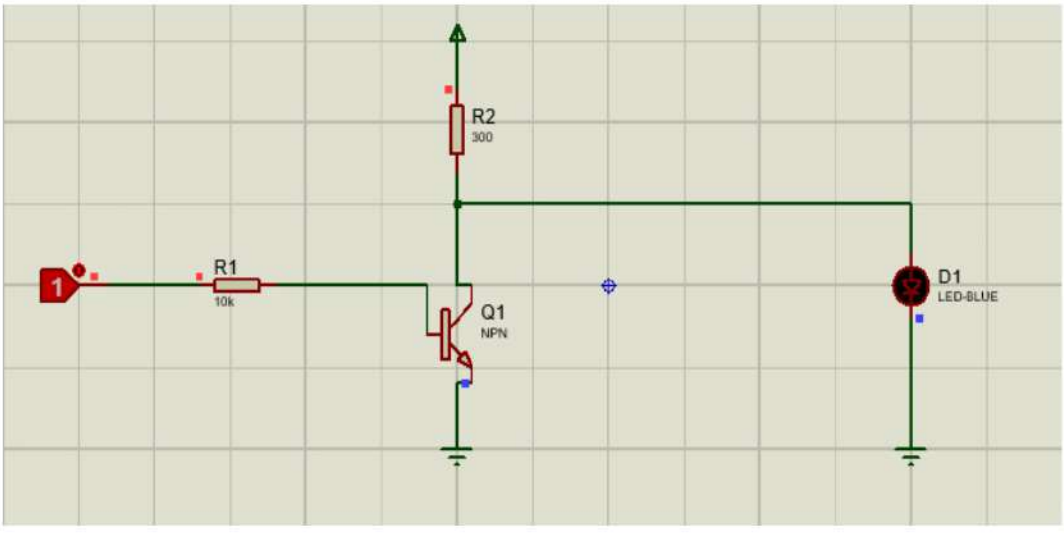

Figure 3: BJT OFF when logic high (1V)

Experiment no: 06 (02)

Experiment Name: Observing of BJT as a switch.

Objective:

- **Demonstrate Manual Control:** Showcase how manual inputs, like push switches, control electronic devices.
- **Understand BJT Switching with Manual Inputs:** Explore how BJTs respond to manual control signals.
- **Hands-on Experience:** Provide tactile learning through interaction with the push switch.
- **Explore Circuit Interactivity:** Investigate component interaction and observe the effects of input changes on circuit behavior.
- **Apply BJTs as Switches:** Apply theoretical BJT knowledge to practical switching applications.

Theory:

A transistor can be used for switching operations for the opening or closing of a circuit. This type of solid-state switching offers significant reliability and lower cost when compared to conventional relays. Both NPN and PNP transistors can be used as switches. Some of the applications use power transistors as switching devices, at that time it may be necessary to use another signal-level transistor to drive the high-power transistor.

NPN Transistor as a Switch

Based on the voltage applied at the base terminal of a transistor switching operation is performed. When a sufficient voltage (VIN > 0.7 V) is applied between the base and emitter, collector to emitter voltage is approximately equal to 0. Therefore, the transistor acts as a short circuit. The collector current VCC / RC flows through the transistor.

Similarly, when no voltage or zero voltage is applied at the input, the transistor operates in a cutoff region and acts as an open circuit. In this type of switching connection, load (here an LED is used as a load) is connected to the switching output with a reference point. Thus, when the transistor is switched ON, current will flow from source to ground through the load.

PNP Transistor as a Switch

PNP transistor works the same as NPN for a switching operation, but the current flows from the base. This type of switching is used for negative ground configurations. For the PNP transistor, the base terminal is always negatively biased concerning the emitter. In this switching, the base current flows when the base voltage is more negative. Simply, a low voltage or more negative voltage makes the transistor short circuit otherwise, it will be an open circuit.

In this connection, load is connected to the transistor switching output with a reference point. When the transistor is turned ON, current flows from the source through the transistor to the load and finally to the ground.

Required apparatus:

- Resistor (R1) 220 ohms.
- LED (D1): "LED-BIBY".
- Transistor (Q1): "2N3904" transistor.
- Power Sources:
- V1: Provides 5V.
- V2: Supplies 1V.
- Wires
- Button (Push).

Circuit Diagram:

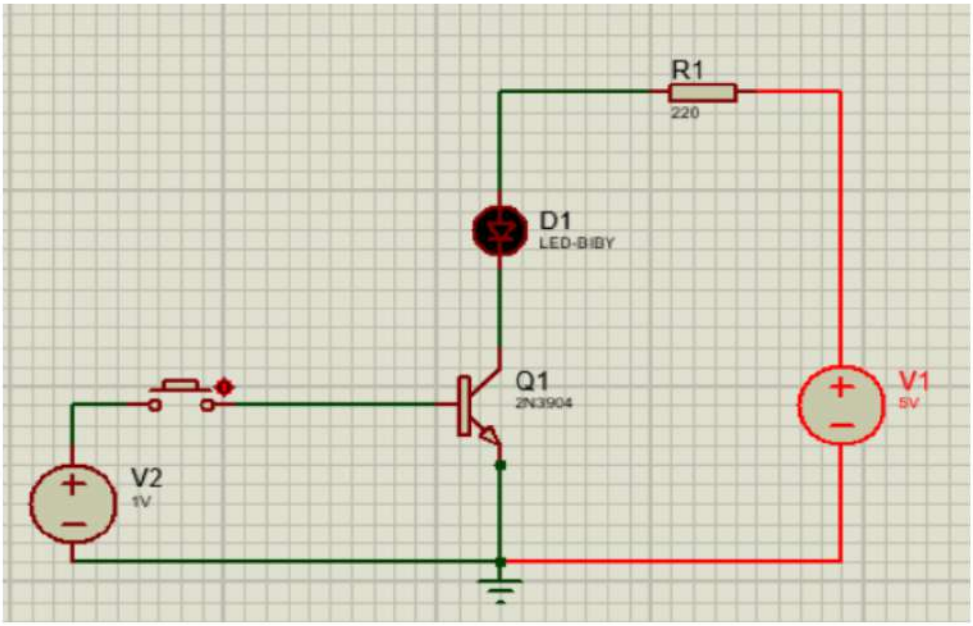

Figure 1: Circuit Diagram (**6.2**)

Output:

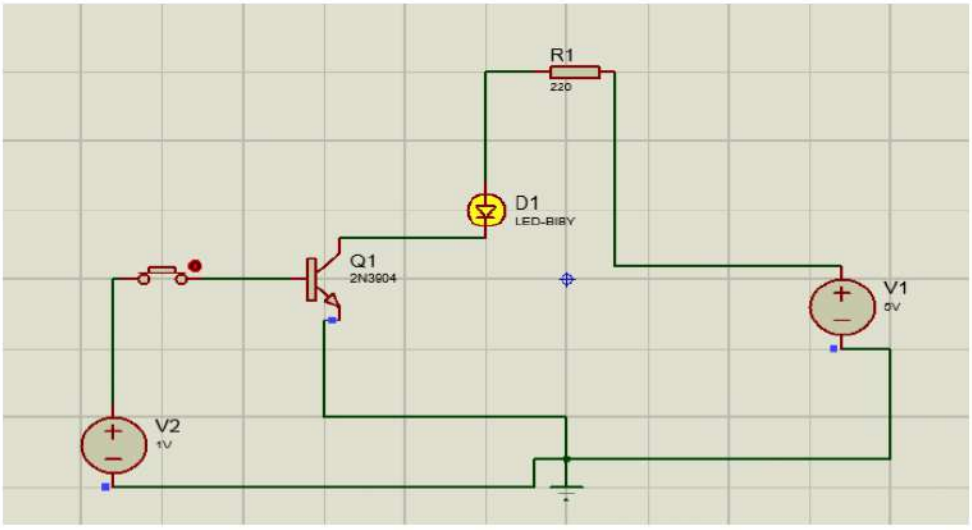

Figure 2: ON state of BJT

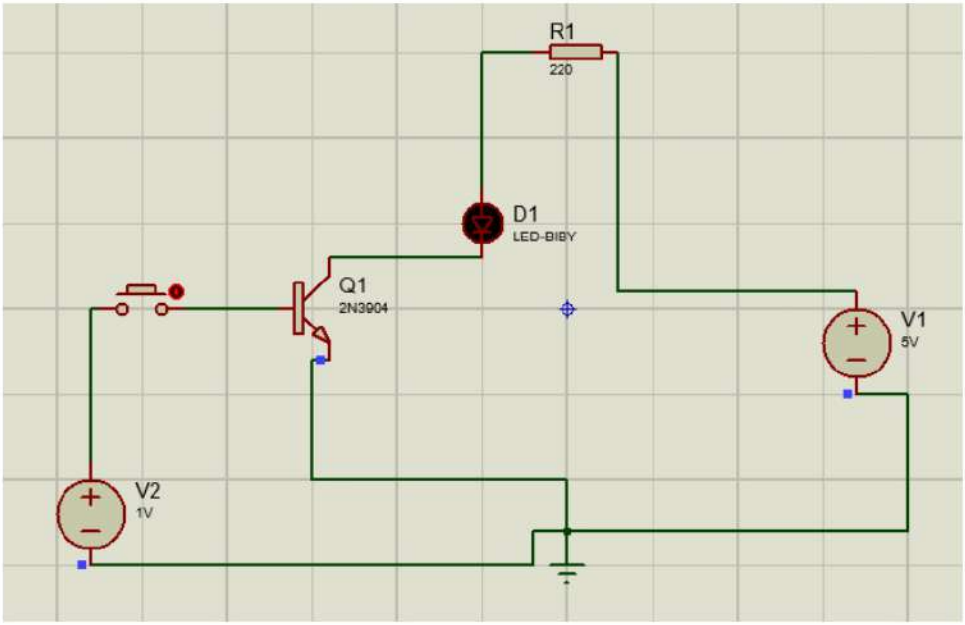

Figure 3: OFF state of BJT

Discussion:

Both circuits (6.1 and 6.2) aim to demonstrate the use of Bipolar Junction Transistors (BJTs) as switches. However, they utilize different control mechanisms to achieve this goal.

Circuit 6.1:

- Control Mechanism:
  - Utilizes a logic probe (Toggle logic) to control the BJT switch.
  - The logic probe provides a logic low (0V) or logic high (1V) signal to turn the BJT on or off, respectively.
- Purpose:
  - Demonstrates the switching action of a BJT using a logic probe, providing a digital input to control the transistor's state.

- Emphasizes the application of digital logic signals in controlling electronic devices.

Circuit 6.2:

- Control Mechanism:
  - Relies on a push switch (Button) to control the BJT switch.
  - The push switch provides a manual input to toggle the BJT between on and off states.
- Purpose:
  - Illustrates the physical interaction aspect of BJT switching, where an external manual input determines the transistor's state.
  - Highlights the versatility of BJTs as switches in responding to various control inputs, including manual switches.

Difference:

- The two circuits use different control mechanisms (logic probe vs. push switch) to demonstrate BJT switching behavior.
  - Circuit 01 emphasizes digital logic control and provides a hands-free switching mechanism.
  - Circuit 02 focuses on manual control and provides a tangible, hands-on experience of BJT switching.

Reason for Different Approaches:

- The choice of control mechanism depends on the educational objectives, target audience, and intended learning outcomes of the experiment.
- Using different control methods allows for a more comprehensive understanding of BJT switching, catering to different learning preferences and levels of expertise.
- It also showcases the versatility of BJTs as switches in responding to various control inputs, whether digital or manual.

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Faculty of Cyber Physical System

Lab Report-07

Linear Application of Operational Amplifier

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Date of Submission:28 April,2024

CONTENTS:

1 Experiment no: 01

2 Experiment Name:

Inverting Op-amp.

3 Objective:

- Understand the basic concept and operation of an inverting operational amplifier.
- Explore practical applications of the inverting amplifier configuration in signal processing and instrumentation.
- Observe the effects of negative feedback on the amplifier's performance, such as stability and distortion.
- Determine the input impedance and output impedance of the inverting amplifier.
- Analyze the gain characteristics of the inverting amplifier with varying feedback resistor values.
- Investigate the relationship between the input and output voltages of an inverting amplifier configuration.

4 Theory:

The inverting operational amplifier configuration is a fundamental circuit in analog electronics, offering simplicity and versatility. In this configuration, the input signal is applied to the inverting input terminal of the op-amp, while feedback from the output is routed back to this terminal through a feedback resistor. This setup results in an inverted output voltage relative to the input voltage, with the amplification determined by the ratio of the feedback resistor to the input resistor. Negative feedback stabilizes the amplifier's gain, reduces distortion, and improves linearity and noise performance. Widely used in signal amplification, filtering, and instrumentation circuits, understanding the characteristics and applications of the inverting op-amp is crucial for designing and analyzing analog electronic systems.

5 Required apparatus:

- Resistor
- Alternator
- IC 741
- Oscilloscope

6 Circuit Diagram:

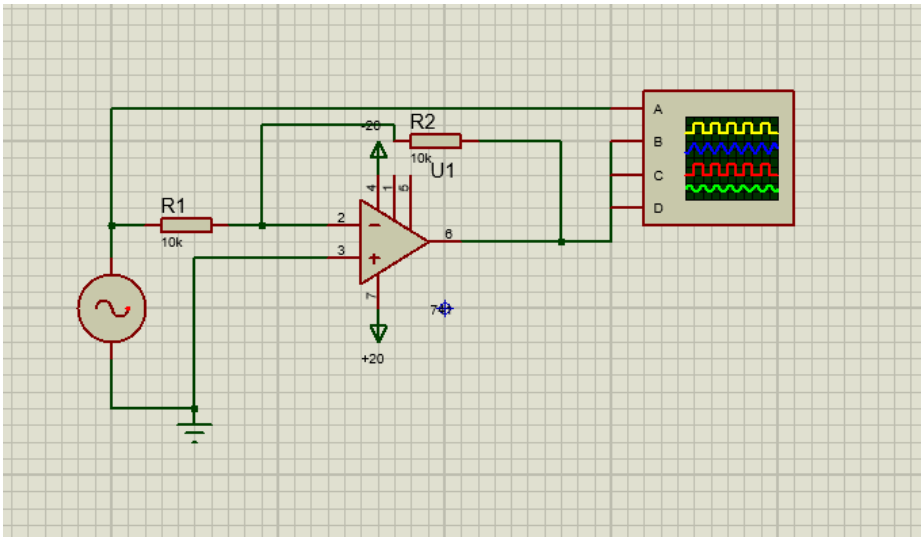


Figure 1: Circuit Diagram

7 Output:

Input Signal, Output Signal-

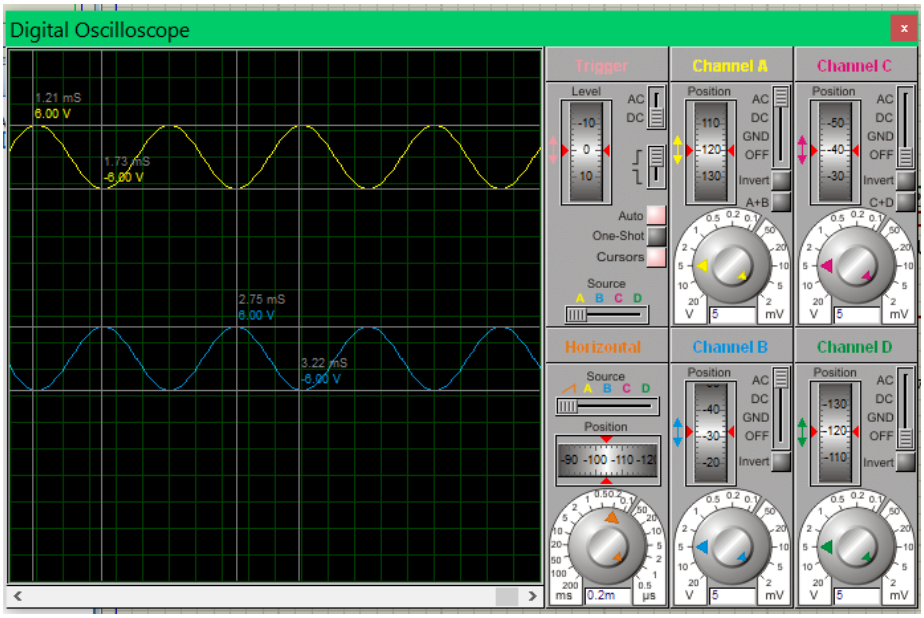


Figure 2: Input and output Signal

8 Discussion:

Here,
For channel A -
Wave top lies at 6.00 V, at this point time period = 1.21 mS
Wave feet lies at -6.00 V, at this point time period =1.73mS

Again,
For channel B (Output) -
Wave top lies at 6.00V, at this point time period = 2.75 mS
Wave feet lies at -6.00 V, at this point time period =3.22mS

9 Experiment no: 02

10 Experiment Name:

Non-inverting Op-amp.

11 Objective:

- Develop skills in troubleshooting and problem-solving by identifying and addressing common issues encountered in Non-inverting Op-amp circuits, such as offset voltage and bias current..
- Gain insight into the limitations and practical considerations associated with the Non-inverting Op-amp configuration, such as input impedance and bandwidth.
- Explore the effects of different resistor values on the voltage gain and overall performance of the Non-inverting Op-amp circuit.
- Gain practical experience in constructing and testing Non-inverting Op-amp circuits on a breadboard or electronic prototyping platform.
- Investigate the relationship between input and output voltages in the Non-inverting Op-amp circuit, focusing on voltage gain and signal amplification.
- Learn how to calculate the voltage gain of the Non-inverting Op-amp circuit theoretically using the circuit's parameters and operational amplifier characteristics.

12 Theory:

The non-inverting operational amplifier (op-amp) configuration is a fundamental circuit arrangement widely used in electronics for signal amplification and buffering. In this setup, the input signal is applied to the non-inverting terminal (+) of the op-amp, while a portion of the output voltage is fed back to the inverting terminal (-) through a resistor network. This feedback arrangement creates a closed-loop system, resulting in several key characteristics. Firstly, the input impedance of the circuit is extremely high, virtually eliminating any loading effect on the source. Secondly, the voltage gain of the circuit is determined by the feedback resistor network, typically resulting in a gain greater than unity. Moreover, due to the positive feedback configuration, the output signal is in-phase with the input, making it suitable for applications requiring signal amplification without phase inversion. Overall, the non-inverting op-amp

configuration offers simplicity, high input impedance, and predictable gain characteristics, making it a versatile and essential building block in many electronic circuits.

13 Required apparatus:

- Resistor
- Alternator
- IC 741
- Oscilloscope

14 Circuit Diagram:

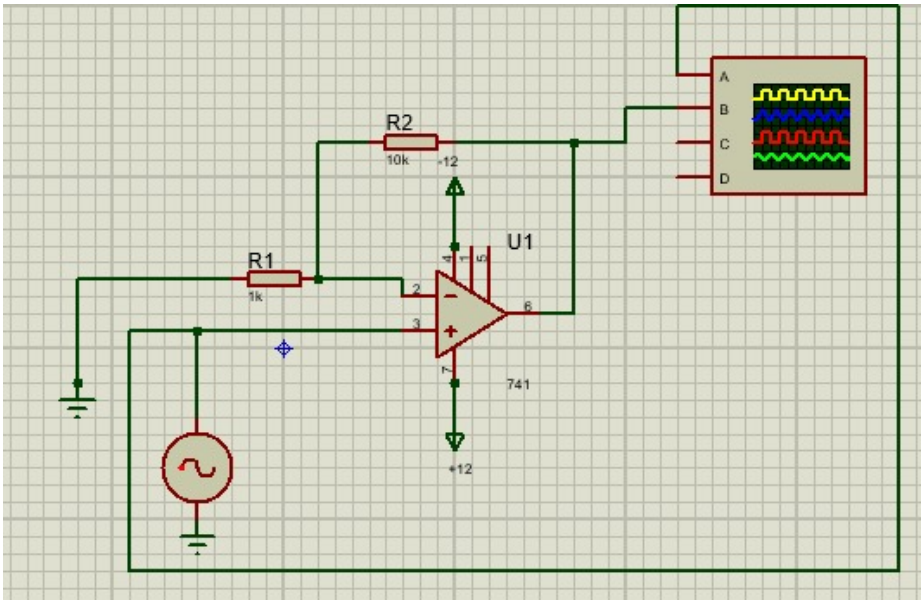


Figure 3: Circuit Diagram

15 Output:

Input Signal, Output Signal-

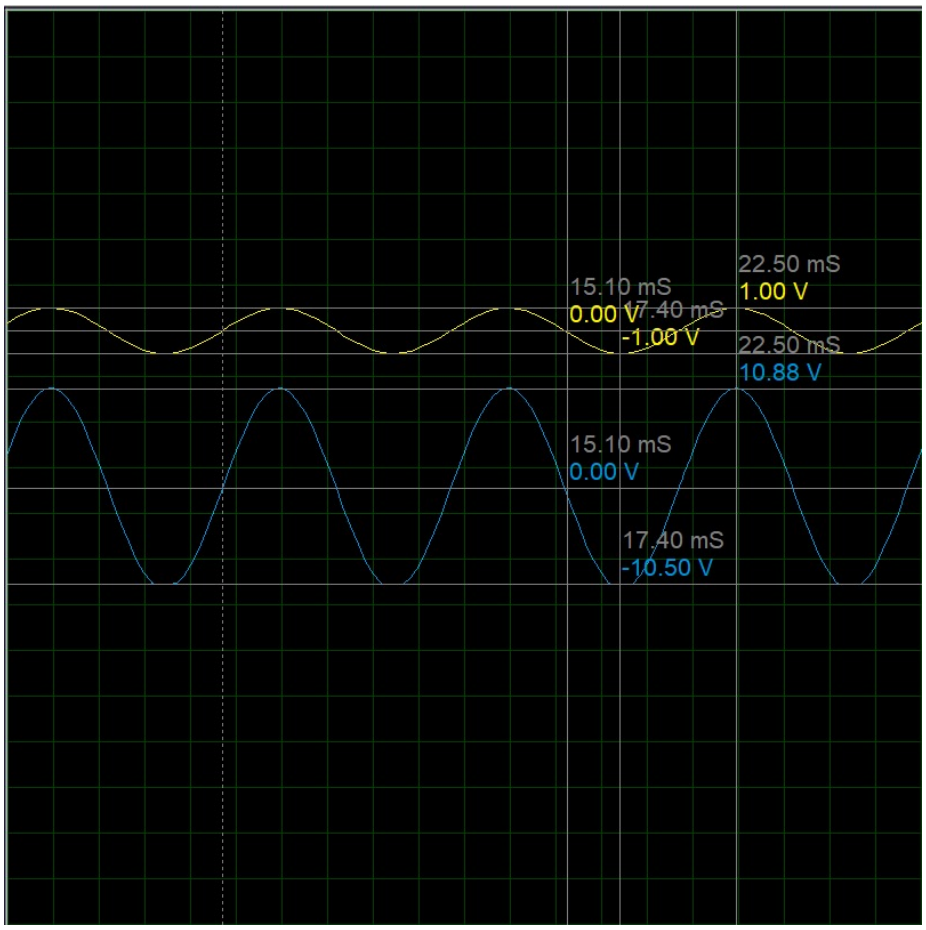


Figure 4: Input and output Signal

16 Discussion:

Here,
For channel A -
Wave top lies at 1.00 V, at this point time period = 22.50 mS
Wave feet lies at -1.00 V, at this point time period = -7.40 mS

Again,
For channel B (Output) -
Wave top lies at 10.88V, at this point time period = 22.50 mS

17 Experiment no: 03

18 Experiment Name:

Integrator Op-Amps:

19 Objective:

19.1 Understanding Integrator Op-Amp Circuit:

Gain a clear understanding of the principles behind the integrator op-amp circuit and its role in analog signal processing.

19.2 Analyzing Input-Output Relationship:

Investigate the relationship between the input and output signals of an integrator op-amp circuit, particularly focusing on how the op-amp integrates the input signal over time.

19.3 Verification of Integrator Functionality:

Verify experimentally that the op-amp circuit functions as an integrator by observing the output waveform and comparing it to the expected integrated waveform.

19.4 Exploration of Integration Time Constants:

Explore the effects of different resistor and capacitor values on the integration time constant, understanding how these parameters affect the rate of integration and the frequency response of the circuit.

19.5 Troubleshooting and Error Analysis:

Develop skills in troubleshooting op-amp circuits, identifying common errors, and understanding methods for correcting circuit deficiencies to achieve desired performance.

20 Theory:

In an integrator op-amp configuration, the operational amplifier is configured with a feedback capacitor, allowing it to perform mathematical integration of the input signal. This configuration is characterized by the capacitor connected

between the amplifier's output and the inverting input terminal, while the non-inverting input is usually grounded. The integration action occurs because the capacitor charges or discharges according to the input voltage, resulting in an output voltage that is proportional to the integral of the input voltage over time. Integrator op-amps find applications in various areas such as waveform generation, signal processing, and analog computing due to their ability to perform mathematical integration electronically. Understanding the principles and characteristics of integrator op-amps is crucial for designing and analyzing circuits in these applications.

21 Required apparatus:

- Resistor
- Capacitor
- Alternator
- IC 741
- Oscilloscope

22 Circuit Diagram:

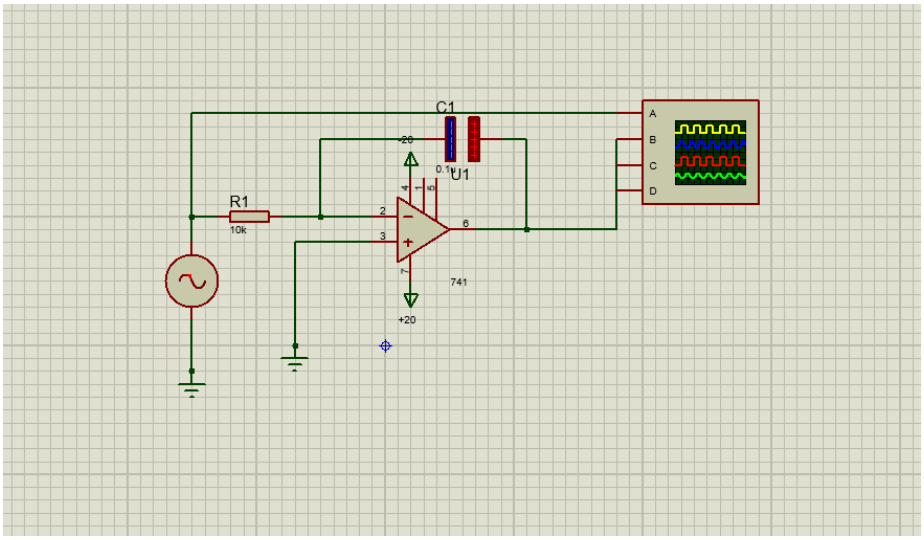


Figure 5: Circuit Diagram

23 Output:

Input Signal, Output Signal-

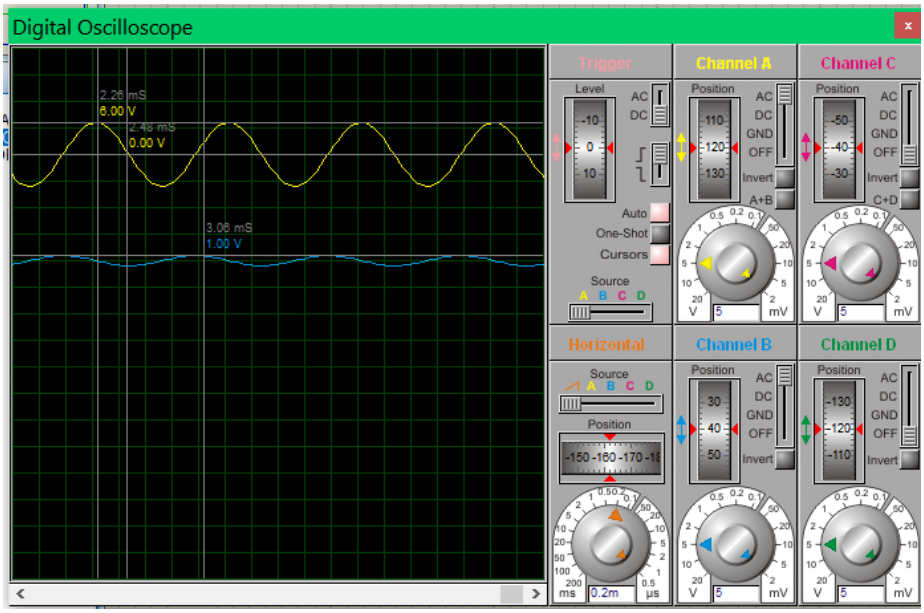


Figure 6: Input and output Signal

24 Discussion:

Here,
For channel A -
Wave top lies at 2.50 V, at this point time period = 5.21 mS
Wave feet lies at -2.50 V, at this point time period = 5.74 mS

Again,
For channel B (Output) -
Wave top lies at 2.50V, at this point time period = 6.23 mS
Wave feet lies at -2.50V, at this point time period = 6.73 mS

25 Experiment no: 04

26 Experiment Name:

Differentiator Op-Amp

27 Objective:

27.1 Understanding Differentiation in Analog Circuits:

The primary objective is to comprehend the concept of differentiation in the context of analog electronic circuits, particularly using operational amplifiers (op-amps).

27.2 Exploring Differentiator Op-Amp Configurations:

Investigate various configurations of differentiator op-amp circuits, including both passive and active configurations, to understand their behavior and characteristics.

27.3 Analyzing Frequency Response:

Evaluate the frequency response of differentiator op-amp circuits, including the roll-off characteristics, bandwidth limitations, and phase shifts, to understand their performance across different frequency ranges.

28 Theory:

Differentiator op-amps are specialized operational amplifier configurations used to perform mathematical differentiation on an input voltage signal. Unlike integrators, which output the integral of the input signal, differentiators output the derivative. This configuration typically consists of a capacitor in the feedback path and a resistor in series with the input signal. The output voltage is proportional to the rate of change of the input voltage, making differentiator op-amps useful in applications such as signal processing, waveform shaping, and frequency analysis. However, they can be sensitive to noise and high-frequency components in the input signal, requiring careful consideration of component values and circuit stability.

29 Required apparatus:

- Resistor
- Capacitor
- Signal Generator
- IC 741
- Oscilloscope

30 Circuit Diagram:

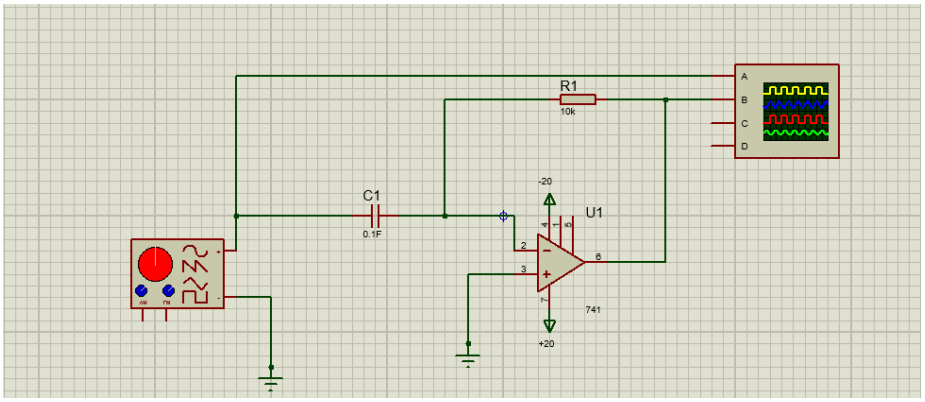


Figure 7: Circuit Diagram

31 Output:

Input Signal, Output Signal-

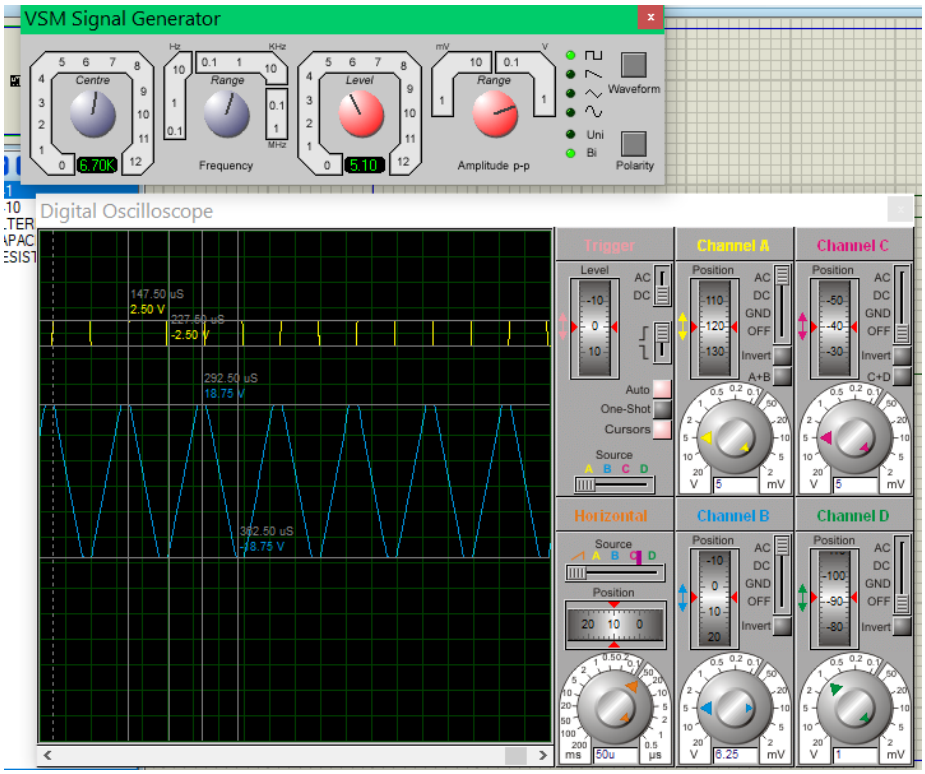


Figure 8: Input and output Signal

32 Discussion:

Here,
For channel A -
Wave top lies at 2.50 V, at this point time period = 147.50 uS
Wave feet lies at -2.50 V, at this point time period = 227.50 uS

Again,
For channel B (Output) -
Wave top lies at 18.75V, at this point time period = 292.50 uS
Wave feet lies at -18.75V, at this point time period = 382.50uS

33 Experiment no: 05

34 Experiment Name:

Instrumentation Amplifier

35 Objective:

- **High Gain:** To amplify small differential signals while rejecting common-mode signals.
- **High Input Impedance:** To minimize loading effects on the signal source.
- **High Common-Mode Rejection Ratio (CMRR):** To reject common-mode signals effectively.
- **Low Output Impedance:** To drive loads with minimal signal loss.
- **Accuracy and Precision:** To provide accurate amplification with minimal errors.

36 Theory:

An instrumentation amplifier is a specialized type of operational amplifier (op-amp) configuration designed primarily for precise and accurate amplification of small differential input signals while rejecting common-mode noise. It typically consists of three op-amps configured in a specific arrangement to achieve high gain, high input impedance, and high common-mode rejection ratio (CMRR). The two input terminals of the instrumentation amplifier are connected to the non-inverting and inverting inputs of the first stage, which amplifies the differential signal. The second stage amplifies the output of the first stage to further increase the gain. The third stage serves as a buffer, providing a low output impedance to drive external loads. By carefully designing the resistor network and feedback loops, instrumentation amplifiers can achieve excellent linearity, low noise, and high accuracy, making them ideal for precision measurement and sensor applications where signal integrity is crucial.

37 Required apparatus:

- Resistor
- Alternator
- IC 741
- Oscilloscope

38 Circuit Diagram:

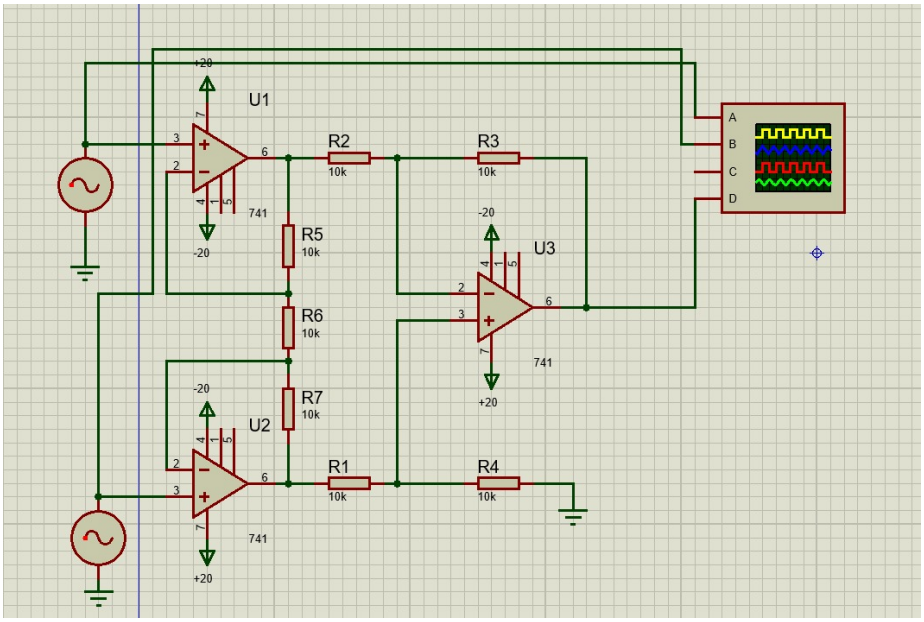


Figure 9: Circuit Diagram

39 Output:

Input Signal, Output Signal-

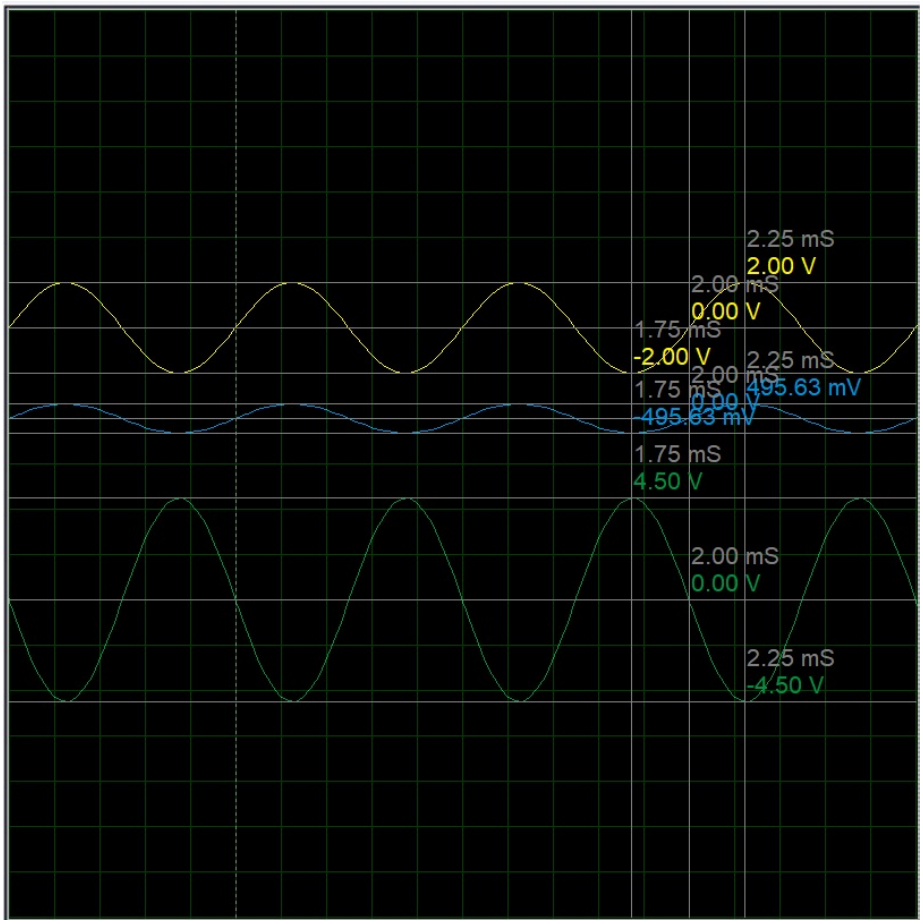


Figure 10: Input and output Signal

40 Discussion:

Here,
Input signal-
For 1st wave,
Wave top lies at 2.00 V, at this point time period = 2.25 mS
Wave feet lies at -2.00 V, at this point time period = 1.75 mS
For 2nd wave,
Wave top lies at 495.63 mV, at this point time period = 2.25 mS
Wave feet lies at -495.63 mV, at this point time period = 1.75 mS

Again,
Output Signal -

Wave top lies at 4.50V, at this point time period = 1.75 mS
Wave feet lies at -4.50V, at this point time period = 2.25 mS

41 Experiment no: 06

42 Experiment Name:

Inverting summing amplifier

43 Objective:

- **Inversion of Input Signal:** Produce an output voltage that is the opposite polarity of the input signal.
- **Variable Gain:**Offer adjustable amplification or attenuation of the input signal.
- **High Input Impedance:** Avoid loading effects on the input signal source.
- **Low Output Impedance:** Facilitate driving loads with minimal signal loss.
- **Linear Operation**Ensure linear amplification within the op-amp's operational range.
- **Stability:**Prevent oscillations and maintain circuit stability.

44 Theory:

The inverting summing operational amplifier configuration is a circuit arrangement that combines multiple input voltages and produces an output voltage that is proportional to the sum of these inputs, with each input weighted by a specific gain factor. In this configuration, the operational amplifier (op-amp) is configured with negative feedback, where the input signals are applied to the inverting terminal through resistors. The output voltage is then fed back to the inverting terminal through a feedback resistor. By adjusting the values of the input resistors, the circuit can provide different weighting to each input signal, allowing for a customizable linear combination of input voltages at the output. This configuration finds extensive use in applications requiring signal mixing, such as audio mixers, analog computing, and instrumentation circuits.

45 Required apparatus:

- Resistor
- Alternator
- IC 741
- Oscilloscope

46 Circuit Diagram:

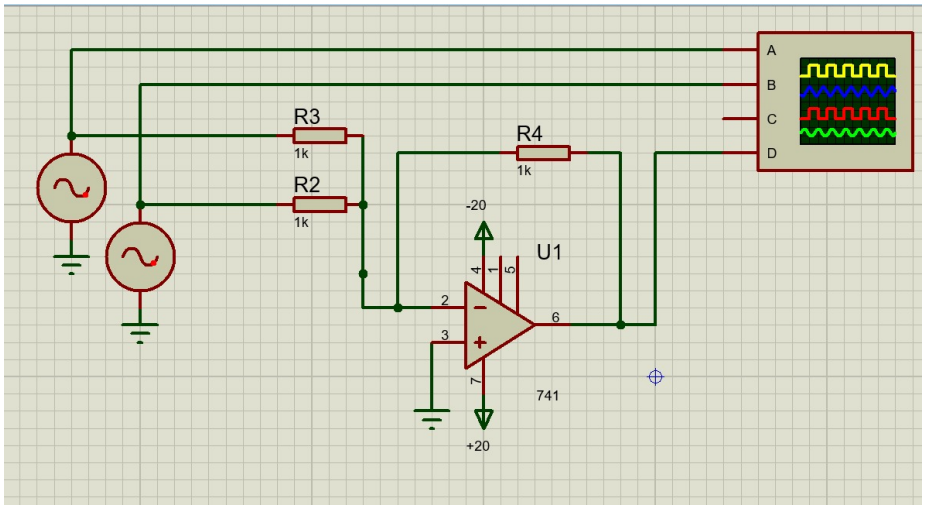


Figure 11: Circuit Diagram

47 Output:

Input Signal, Output Signal-

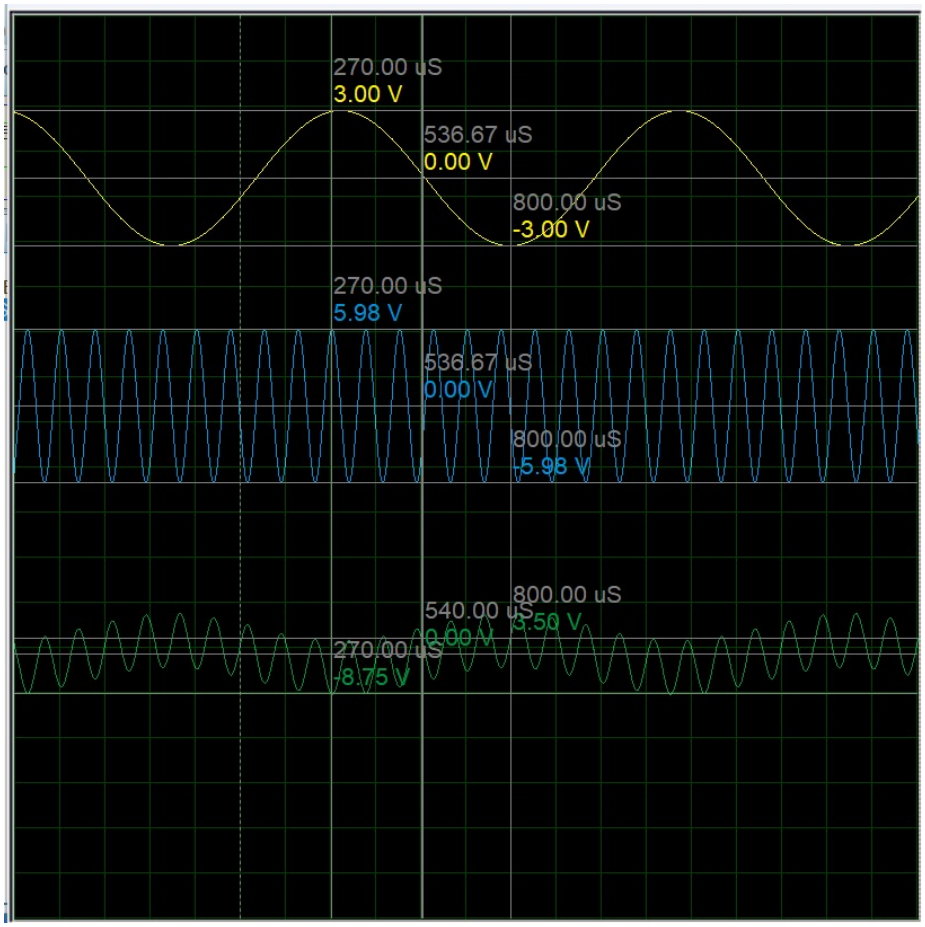


Figure 12: Input and output Signal

48 Discussion:

Here,
Input signal-
For 1st wave,
Wave feet lies at 3.00 V, at this point time period = 270.00 uS
Wave feet lies at -3.00 V, at this point time period = 800.00 uS

For 2nd wave,
Wave top lies at 5.98 V, at this point time period = 270.00 uS
Wave feet lies at -5.98 V, at this point time period = 800.00 uS

Again,

Output Signal -
Wave top lies at 3.50V, at this point time period = 800.00 uS
Wave feet lies at -8.75 V, at this point time period = 270.00 uS

49 Experiment no: 07

50 Experiment Name:

Non-inverting summing amplifier

51 Objective:

- **Unity Gain Buffering:** To provide unity gain (voltage follower) with high input impedance and low output impedance, isolating the input from the load and maintaining signal integrity.
- **Signal Amplification:** To amplify input signals with a gain greater than one, providing signal amplification while maintaining the same polarity as the input.
- **High Input Impedance:** To present a high input impedance, minimizing loading effects on the signal source and ensuring accurate signal measurement.
- **Low Output Impedance:** To present a low output impedance, enabling the amplifier to drive loads with minimal signal loss.
- **Stability and Linearity:**To ensure stable and linear amplification of input signals, minimizing distortion and maintaining fidelity.

52 Theory:

The non-inverting summing operational amplifier configuration combines multiple input signals into a single output signal with each input contributing proportionally to the final output voltage. In this setup, each input signal is connected through a resistor to the non-inverting terminal of the operational amplifier, while the inverting terminal is grounded. The non-inverting input serves as a virtual ground, maintaining a stable reference point for the inputs. The output voltage of the amplifier is the sum of the input voltages, each multiplied by a scaling factor determined by the ratio of the input resistor to the feedback resistor. This configuration provides signal summation without inverting the polarity of any input signal, making it useful in applications such as audio mixing, signal processing, and instrumentation where multiple signals need to be combined without phase inversion. Additionally, the non-inverting configuration offers high input impedance, minimizing loading effects on the input sources, and provides voltage gain determined by the feedback resistor network.

53 Required apparatus:

- Resistor
- Alternator
- IC 741
- Oscilloscope

54 Circuit Diagram:

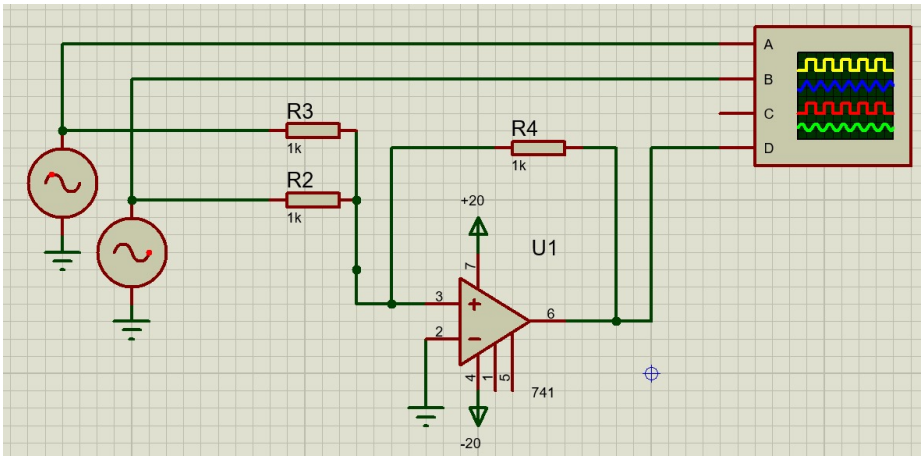


Figure 13: Circuit Diagram

55 Output:

Input Signal, Output Signal-

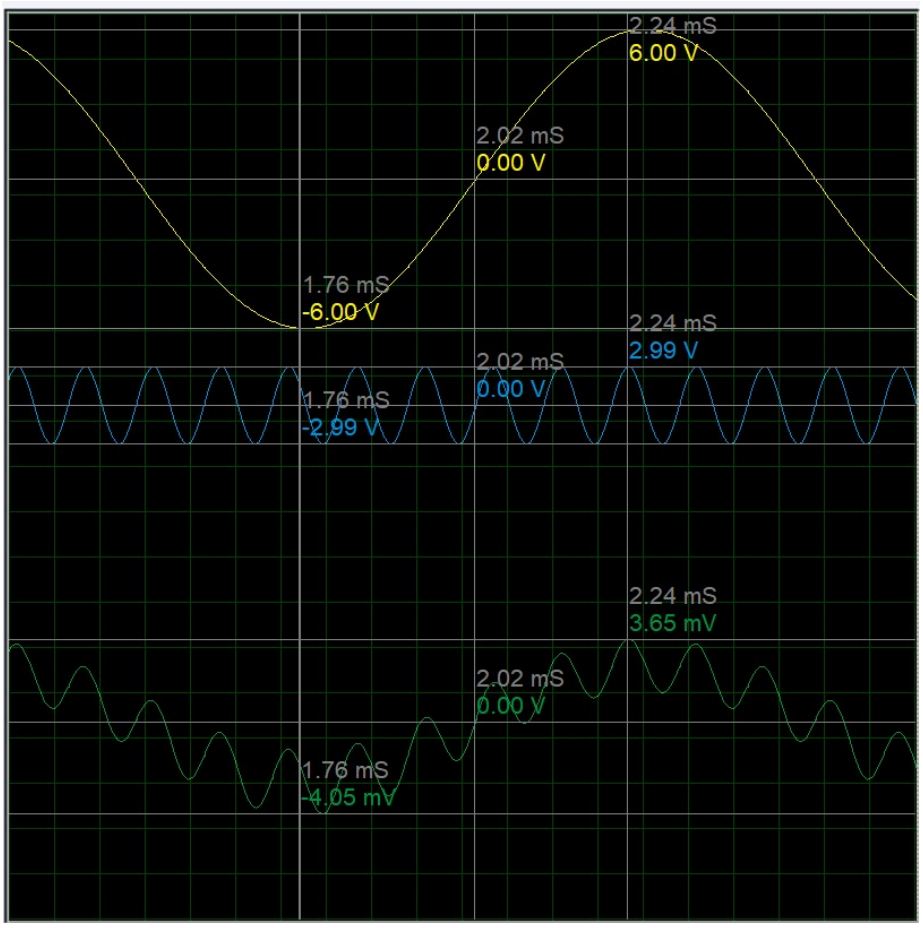


Figure 14: Input and output Signal

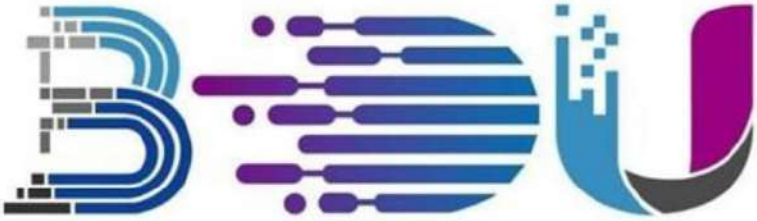
56 Discussion:

Here,
Input signal-
For 1st wave,
Wave feet lies at 6.00 V, at this point time period = 2.24 mS
Wave feet lies at -6.00 V, at this point time period = 1.76 mS

For 2nd wave,
Wave top lies at 2.99 V, at this point time period = 2.24 mS
Wave feet lies at -2.99 V, at this point time period = 1.76 mS

Again,

Output Signal -
Wave top lies at 3.65 V, at this point time period = 2.24 mS
Wave feet lies at -4.05 V, at this point time period = 1.76 mS



Bangabandhu Sheikh Mujibur Rahman Digital University

BANGABANDHU SHEIKH MUJIBUR RAHMAN DIGITAL UNIVERSITY, BANGLADESH

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Lab Report-08

N-Channel JFET Parameter Calculation and simulation in Proteus.

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Date of Submission: 02 May, 2024

IRE 106: Electronics Devices and Applications Sessional

Table of Contents

Experiment No: 01

Experiment Name: N-Channel JFET Parameter Calculation and Simulation (for fixed bias configuration) in Proteus.

Objectives:

- **Compare Biasing Methods:** Evaluate the performance and characteristics of the fixed bias configuration in comparison to the self-bias configuration previously examined.
- **Stability Assessment:** Determine the stability of the fixed bias configuration under varying operating conditions, such as changes in temperature or load.
- **Parameter Calculation:** Calculate the key parameters (such as Ig, Id, Vgs, and Vds) associated with the fixed bias configuration manually and compare them with the results obtained from simulation in Proteus.
- **Operating Point Analysis:** Analyze the operating point of the JFET in the fixed bias configuration to understand its impact on device performance and efficiency.
- **Biasing Efficiency:** Assess the efficiency of the fixed bias method in providing a stable quiescent operating point for the JFET while minimizing power dissipation and distortion.
- **Troubleshooting:** Identify any potential issues or limitations encountered during the implementation of the fixed bias configuration and propose possible solutions or improvements.
- **Understanding Circuit Behavior:** Gain insights into the behavior of the JFET circuit under fixed bias conditions, including the relationship between gate-source voltage, drain current, and drain-source voltage.

Theory:

Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum transfer characteristics make ID levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents ID and drain-source voltage VDS, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for JFETs. In fixed bias configuration, a constant DC voltage is directly applied to the

gate terminal of the JFET. This establishes a steady operating point for the device, determining its quiescent drain current (ID) and drain-source voltage (VDS) under static conditions.

Required Apparatus:

- Proteus simulation software
- JFET (NJFET)
- Resistor (8k)
- Power (+24)
- Cell (2.5V)
- DC Voltmeter
- DC Ammeter

Circuit Diagram:

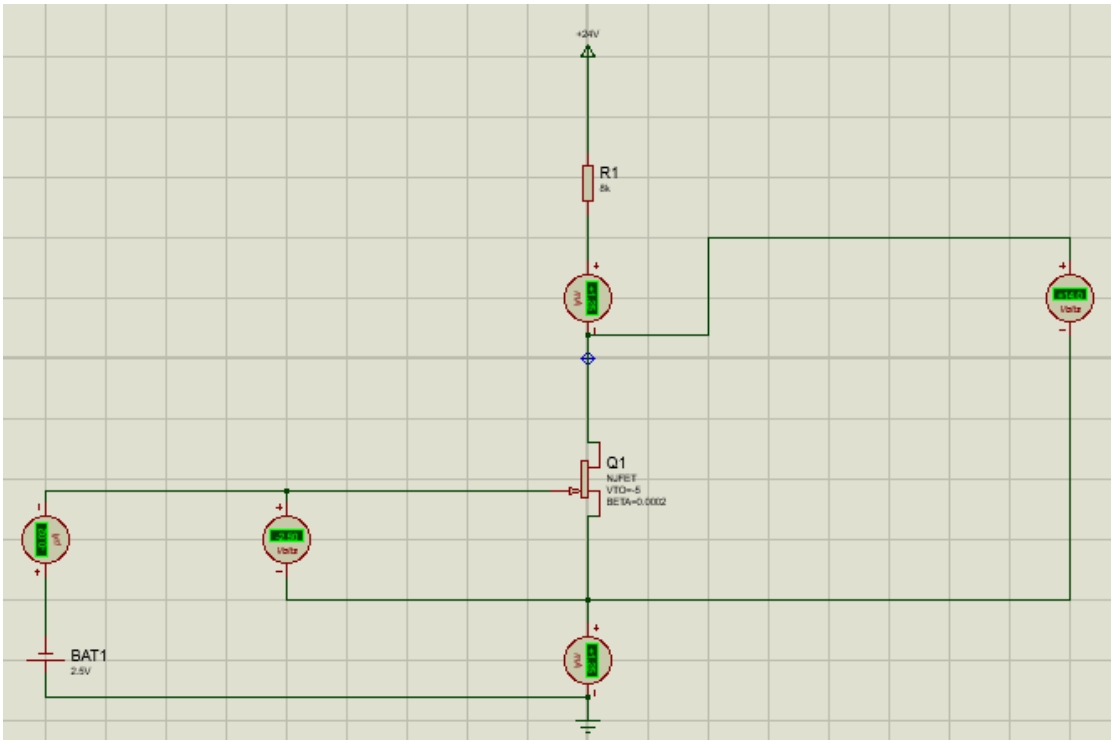

Figure No – 01: Circuit Diagram

Output:

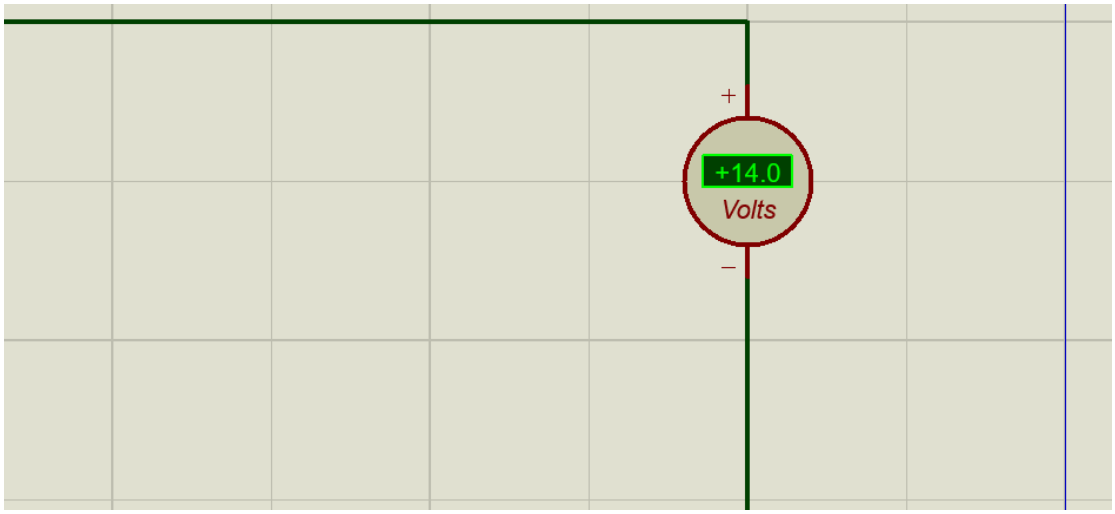

Figure No – 02: Value of V_{DS}

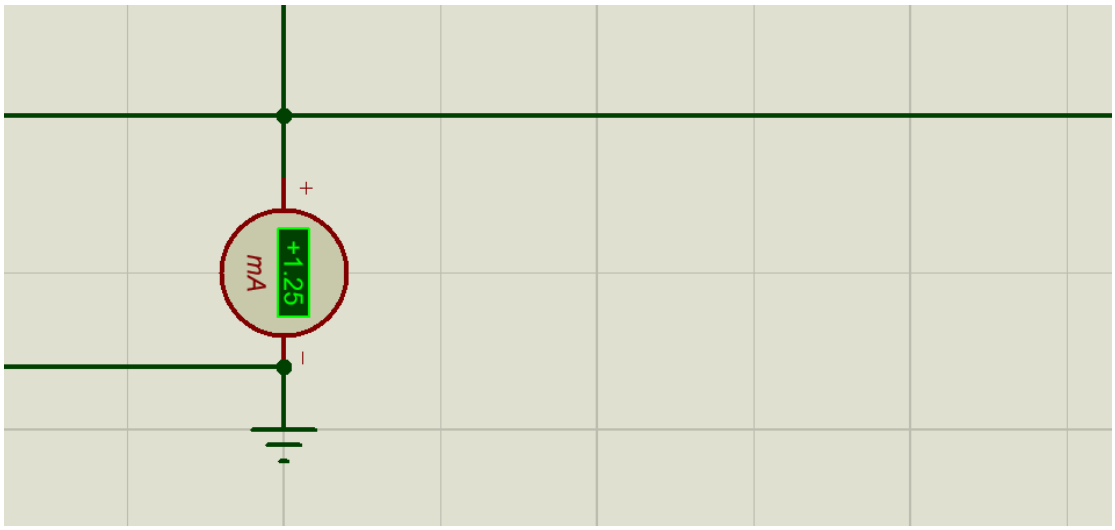

Figure No – 03: Value of Drain Current (I_D)

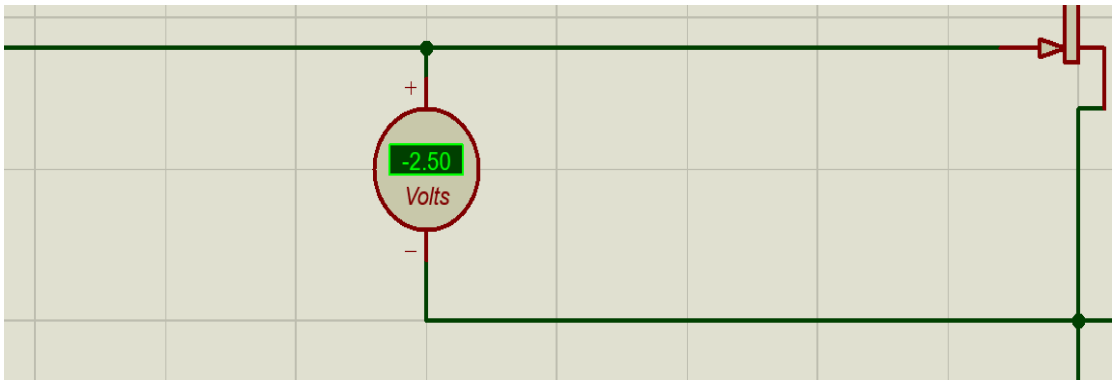

Figure No – 04: Value of V_{GS}

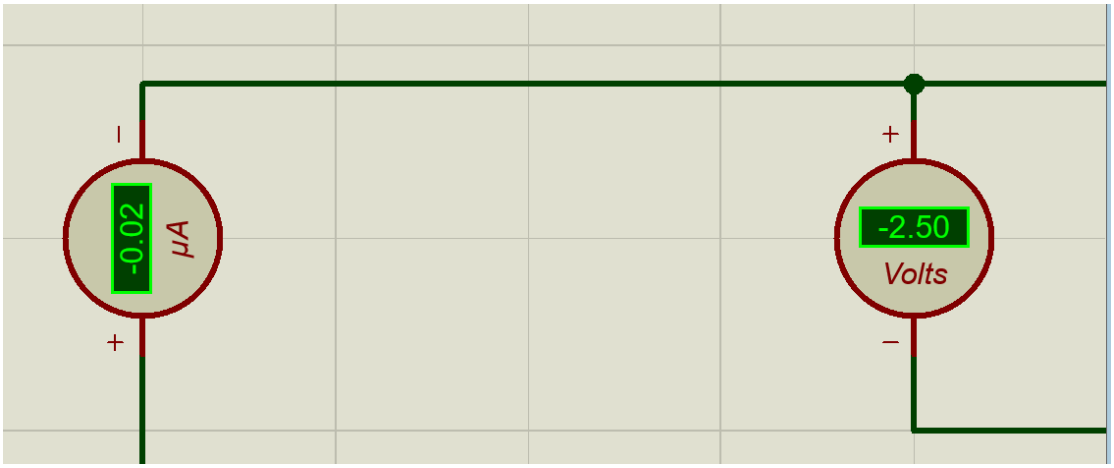

Figure No – 05: Value of I_G (non-zero)

Discussion:

- For simulation, we had set,
  V_p = -5
  We know that,
  BETA = $I_{DSS}\left(\frac{1}{V_p}\right)^2$
  So, **BETA = 0.0002**

- Now if we calculate manually,
  $V_{DD} = 24\text{V}$

  We know that,
  $V_{GS} = -V_{GG}$
  $\boldsymbol{V_{GS} = -2.5\text{V}}$

  We know that,
  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$
  $I_D = 5\text{ mA}\,(1 - \frac{(-2.5)}{(-5)})^2$
  $\therefore \boldsymbol{I_D = 1.25\text{ mA.}}$

  Applying Loop,
  $\boldsymbol{V_{DS} = V_{DD} - I_D R_D}$
  $V_{DS} = 24 - (1.25 * 8\text{K})$
  $V_{DS} = (24 - 10)\text{ V}$
  $\therefore \boldsymbol{V_{DS} = 14\text{V}}$

Experiment No: 02

Experiment Name: N-Channel JFET Parameter Calculation and Simulation (for self-bias configuration) in Proteus.

Objectives:

- **Comparative Analysis:** Compare the performance and characteristics of the self-bias configuration with other biasing methods, such as fixed bias.
- **Stability Assessment:** Evaluate the stability of the self-bias configuration under varying operating conditions, including changes in temperature and load.
- **Parameter Calculation:** Calculate key parameters (such as Ig, Id, Vgs, and Vds) associated with the self-bias configuration both manually and through simulation in Proteus.
- **Operating Point Analysis:** Analyze the operating point of the JFET in the self-bias configuration to understand its impact on device performance and efficiency.
- **Efficiency Evaluation:** Assess the efficiency of the self-bias method in establishing a stable quiescent operating point for the JFET while minimizing power dissipation and distortion.
- **Comparison with Fixed Bias:** Contrast the self-bias configuration with a fixed bias regarding simplicity, stability, and predictability.
- **Understanding Circuit Behavior:** Gain insights into the behavior of the JFET circuit under self-bias conditions, including the relationship between gate-source voltage, drain current, and drain-source voltage.

Theory:

In the self-bias configuration for JFET circuits, a resistor is connected between the gate terminal and the drain terminal. This resistor biases the gate terminal at a voltage determined by the drain current flowing through it, creating a negative feedback loop. As the drain current increases, the voltage drop across the resistor increases, thereby reducing the gate-source voltage and stabilizing the operating point of the JFET. This self-adjusting mechanism ensures a stable quiescent operating point, making self-bias configuration advantageous for its simplicity and inherent stability.

Required Apparatus:

- Proteus simulation software
- 2N3819 (FET) N-Channel JFET
- Resistor 1 (600R)
- Resistor 2 (1000K)
- Resistor 3 (4.7K)
- Resistor 4 (3.5K)
- Resistor 5 (510R)
- Capacitor 1 (0.1uF)
- Capacitor 2 (10uF)
- Capacitor 3 (20uF)
- Battery (30V)
- DC Voltmeter
- VSINE

Circuit Diagram:

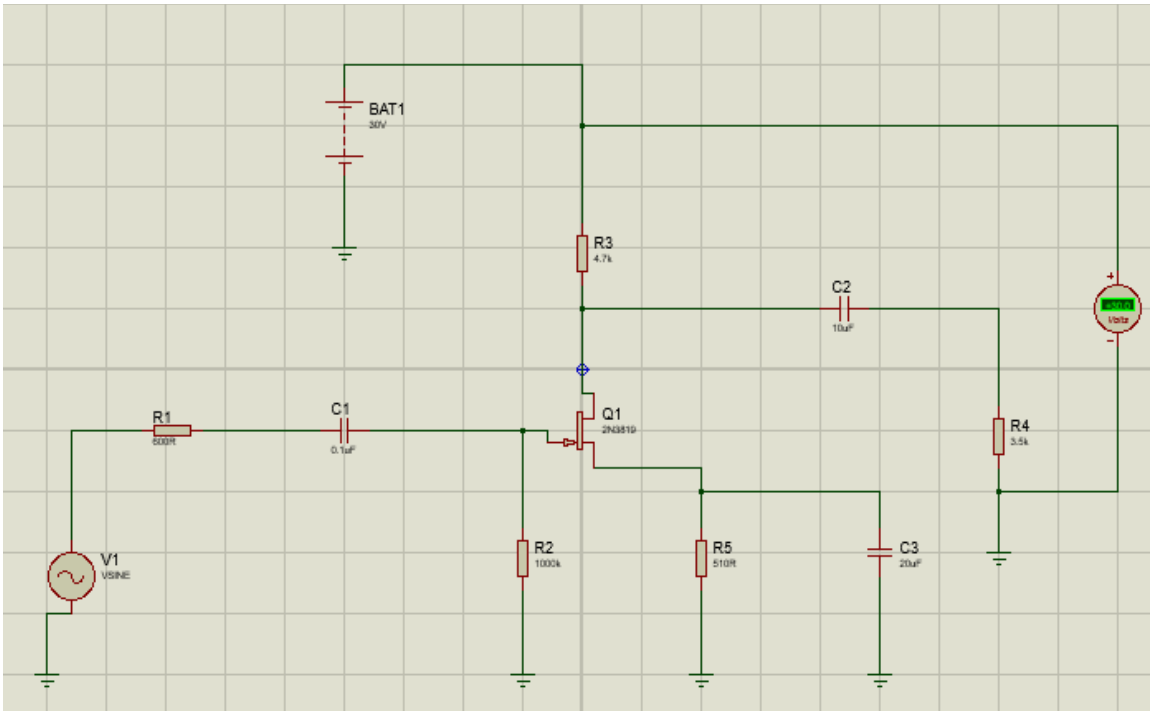

Figure 01: Circuit Diagram

Output:

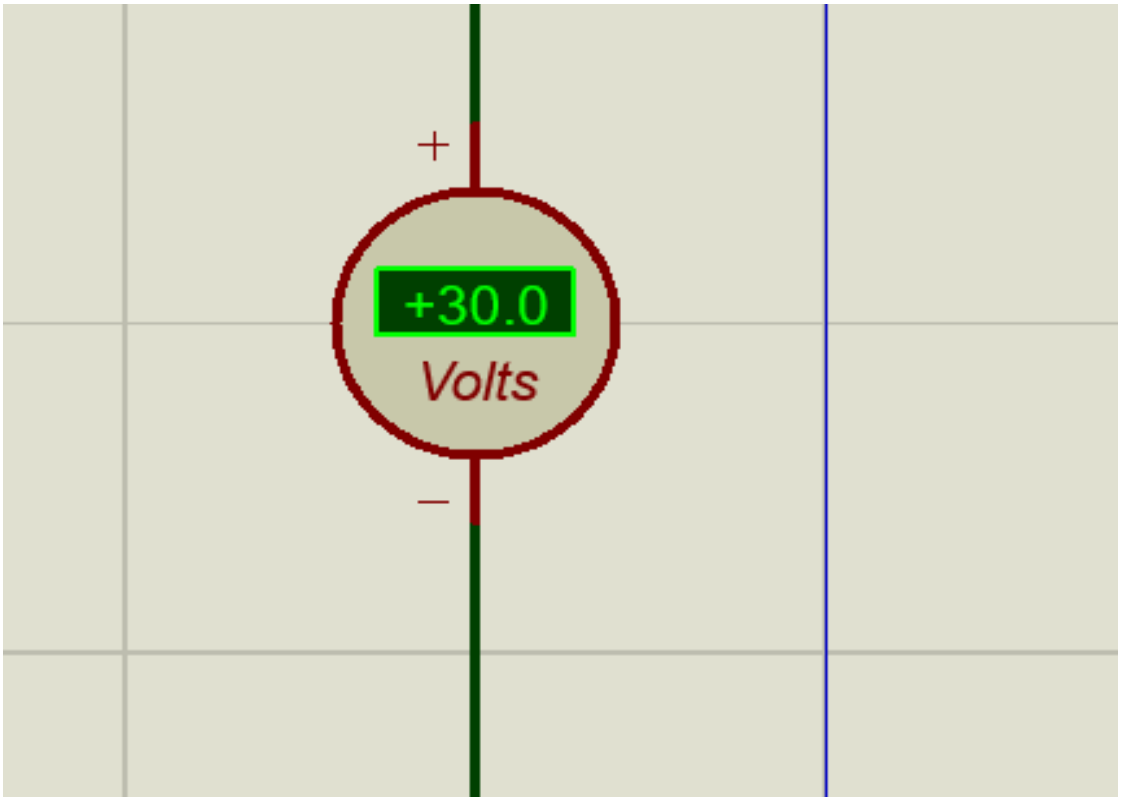

Figure 02: Output Voltage

Discussion:

- **Determination of Quiescent Drain Current (I_{DQ}):** The quiescent drain current (I_{DQ}) can be calculated using Ohm's Law and the voltage divider rule. Assuming the JFET is in the saturation region, where V_{GS} = 0, the voltage across resistor R4 (connected between the drain and ground) can be considered as the supply voltage V_D (which is +30V). Therefore, the I_{DQ} can be calculated as:

$$I_{DQ} = \frac{V_D}{R_4} = \frac{30V}{3.5K\Omega} \approx 8.57\ \text{mA}$$

- **Determination of Gate Bias Voltage (V_{GS}):** The gate bias voltage (V_{GS}) can be determined by analyzing the voltage drop across resistor R3. As per the voltage divider rule:

$$V_{GS} = V_D \times \frac{R_3}{R_3 + R_4} = 30\text{V} \times \frac{4.7k\Omega}{(4.7+3.5)_{k\Omega}} \approx 17.2\text{V}$$

This calculated VGS value sets the operating point of the JFET in the self-bias configuration.

The obtained voltage of +30V is consistent with the battery voltage specified in our components list. In the self-bias configuration, this voltage is effectively divided across resistors R3 and R4, determining the gate bias voltage (V_{GS}) and quiescent drain current ($\boldsymbol{I_{DQ}}$) of the JFET, respectively. This configuration ensures stability and a fixed operating point for the JFET, making it suitable for various applications requiring precise biasing.

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Lab Report-09

MOSFET drain curve

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Date of Submission: 12 MAY,2024

Experiment No: 9.1

Experiment Name: MOSFET drain curve

Objectives:

Understanding Device Operation: Explain how the drain current varies with the drain-source voltage, elucidating the different regions of operation such as cutoff, saturation, and linear (triode) regions.

Parameter Extraction: Use the drain curve to extract important parameters such as threshold voltage (Vth), transconductance (gm), drain conductance (gd), drain-source resistance (rDS), and saturation current (IDSS).

Device Characterization: Characterize the MOSFET's performance under different biasing conditions, highlighting its linearity, saturation behavior, and efficiency.

Verification of Circuit Models: Compare experimental results with theoretical models (such as the MOSFET equations) to verify the accuracy of the models and gain insights into the device's limitations.

Application Insights: Discuss how the drain curve analysis can be applied in various electronic circuits and systems, such as amplifiers, switches, and digital logic circuits.

Troubleshooting: Identify any discrepancies between the expected and measured behavior of the MOSFET, and propose possible reasons for such differences.

Theory:

The drain characteristics of a MOSFET are drawn between the drain current ID and the drain source voltage VDS. The characteristic curve is as shown below for different values of inputs. Actually when VDS is increased, the drain current ID should increase, but due to the applied VGS, the drain current is controlled at certain level. Hence the gate current controls the output drain current.

Required Apparatus:

- Proteus simulation software
  - MOSFET(IRF520)
  - DC voltage source
  - Current probe
- Computer with Proteus installed

Circuit Diagram:

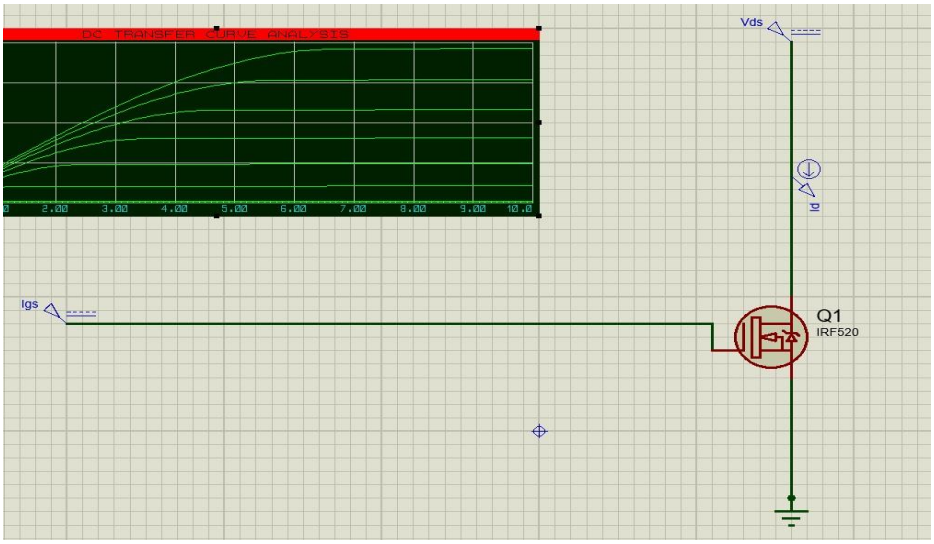
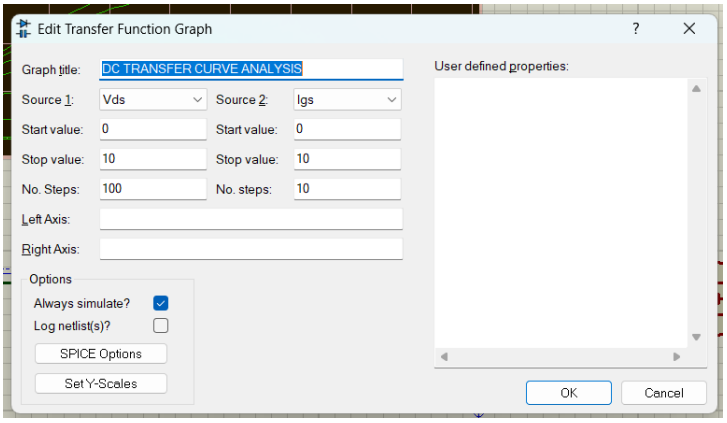


Figure No – 01: Circuit Diagram



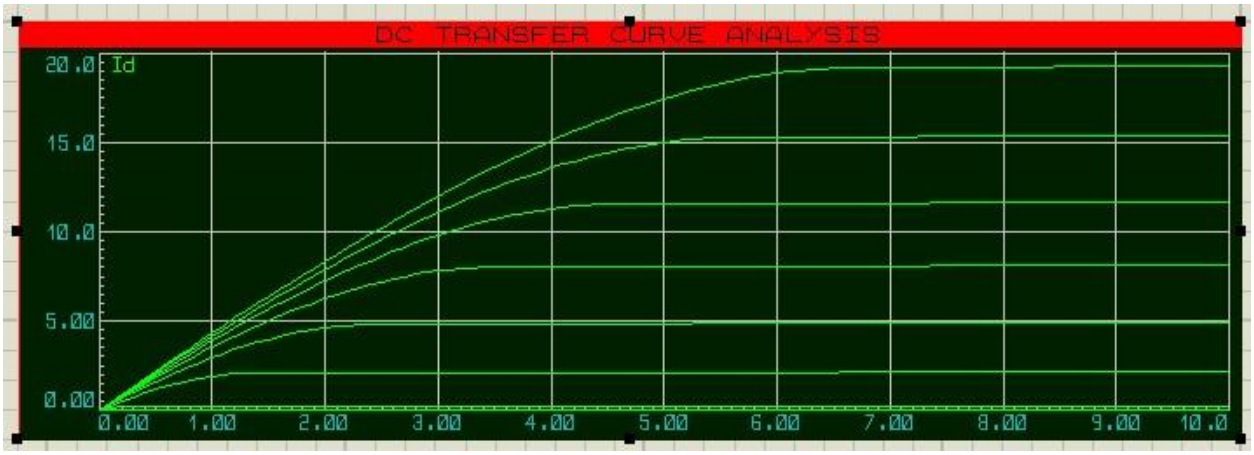


Figure No – 01: graph diagram

Conclusion:

In conclusion, our analysis of the MOSFET drain curve has provided valuable insights into the device's behavior and performance. We successfully extracted key parameters, observed the transitions between different operating regions, and compared our experimental results with theoretical models. Our findings underscore the importance of MOSFET drain curve analysis in understanding device characteristics and its implications for electronic circuit design. Despite some limitations, this experiment has enhanced our understanding of MOSFET operation, paving the way for further exploration and application in various electronic systems.

Experiment No: 9.2

Experiment Name: MOSFET as a Switch

Objectives:

Switching Behavior: Investigate the MOSFET's ability to act as an electronic switch by controlling the flow of current between its drain and source terminals under different biasing conditions.

On/Off States: Explore the transition between the "on" and "off" states of the MOSFET switch, understanding how changes in the gate-source voltage affect the conductivity of the device and determine whether it allows current flow or not.

Threshold Voltage: Determine the threshold voltage required to switch the MOSFET between its on and off states, and analyze how this parameter influences the switching characteristics of the device.

Switching Speed: Measure and analyze the switching speed of the MOSFET switch, including rise and fall times, to assess its suitability for high-speed switching applications.

Power Dissipation: Investigate the power dissipation characteristics of the MOSFET switch in both its on and off states, understanding how they affect the efficiency and reliability of the device in practical circuits.

Switching Applications: Discuss potential applications of MOSFET switches in electronic circuits, such as power supplies, motor control, digital logic gates, and signal amplification, highlighting their advantages and limitations compared to other types of switches.

Performance Optimization: Explore methods to optimize the performance of MOSFET switches, such as proper gate drive techniques, heat sinking, and protection circuitry, to enhance their reliability and longevity in real-world applications.

Theory:

Semiconductor switching in electronic circuit is one of the important aspects. A semiconductor device like a BJT or a MOSFET are generally operated as switches i.e., they are either in ON state or in OFF state.

Ideal Switch Characteristics For a semiconductor device, like a MOSFET, to act as an ideal switch, it must have the following features:

• During ON state, there should not be any limit on the amount of current it can carry.

• In OFF state, there should not be any limit on the blocking voltage.

• When the device is in ON state, there should be zero voltage drop.

• OFF state resistance should be infinite.

• Operating speed of the device has no limits

Practical Switch Characteristics But the World isn't ideal and it is applicable even to our semiconductor switches. In a practical situation, a semiconductor device like a MOSFET has the following characteristics.

During ON state, the power handling capabilities are limited i.e., limited conduction current. The blocking voltage during OFF state is also limited.

• Finite turn on and turn off times, which limit the switching speed. Maximum operating frequency is also limited.

• When the device is ON, there will be a finite on state resistance resulting in a forward voltage drop. There will also be a finite off state resistance which results in a reverse leakage current.

• A practical switch experiences power loses during on state, off state and also during the transition state (on to off or off to on).

he operation of a MOSFET as a switch by considering a simple example circuit

This is a simple circuit, where an N-Channel Enhancement mode MOSFET will turn ON or OFF a light. In order to operate a MOSFET as a switch, it must be operated in cut-off and linear (or triode) region. Assume the device is initially OFF. The voltage across Gate and Source i.e., VGS is made appropriately positive (technically speaking, VGS > VTH), the MOSFET enters linear region and the switch is ON. This makes the Light to turn ON. If the input Gate voltage is 0V (or technically < VTH), the MOSFET enters cut-off state and turns off. This in turn will make the light to turn OFF.

Required Apparatus:

- Proteus simulation software
    - MOSFET(2N6660)
    - Resistor (10k)
    - Motor
    - DC supply (12V)
- Computer with Proteus installed

Circuit Diagram:

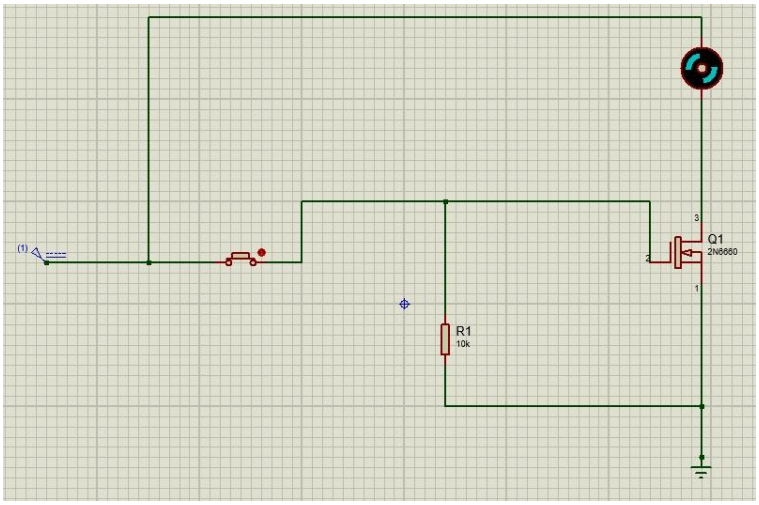


Figure No – 01: Circuit Diagram

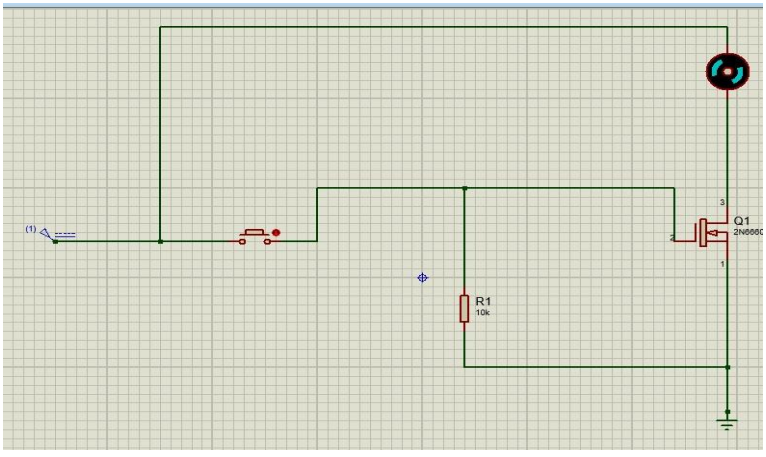


Figure No – 02: Circuit Diagram

Conclusion:

In conclusion, our analysis of MOSFETs as switches has provided valuable insights into their switching behavior and characteristics. We successfully determined the threshold voltage for switching and observed the device's performance in terms of speed and power dissipation. Our findings underscore the versatility of MOSFET switches in various electronic applications, while also highlighting considerations for optimization and practical implementation. This experiment enhances our understanding of semiconductor devices and their role in modern electronics.

Experiment No: 9.3

Experiment Name: MOSFET as a Switch with lamp brightness control.

Objectives:

Switching Functionality: Investigate the MOSFET's capability to function as a switch to control the lamp's state, turning it on and off based on the gate-source voltage.
Analog Control: Explore how the MOSFET can be used to provide analog control over the lamp's brightness by modulating the duty cycle of the switching signal or adjusting the gate voltage.
PWM Technique: Implement Pulse Width Modulation (PWM) technique to control the lamp's brightness, understanding how varying the duty cycle of the PWM signal affects the average power delivered to the lamp.
Characterization of Brightness Levels: Experimentally characterize the relationship between the duty cycle of the PWM signal and the corresponding brightness levels of the lamp, quantifying the range of brightness control achievable.
Efficiency Analysis: Assess the efficiency of the MOSFET-based lamp brightness control system by analyzing power losses in the MOSFET and lamp, and comparing them to alternative control methods.
Stability and Reliability: Evaluate the stability and reliability of the MOSFET switch in controlling lamp brightness over extended periods, considering factors such as heat dissipation, thermal management, and long-term performance.

Applications and Adaptability: Discuss potential applications of MOSFET-based lamp brightness control systems in real-world scenarios, such as home lighting, automotive lighting, and industrial automation, highlighting their advantages and limitations.

Required Apparatus:

- Proteus simulation software
    - MOSFET(IRFZ44N)
    - POT HG
    - Power (6V)
    - Lamp
    - Battery
    - DC voltmeter
    - DC ammeter
- Computer with Proteus installed

Circuit Diagram:

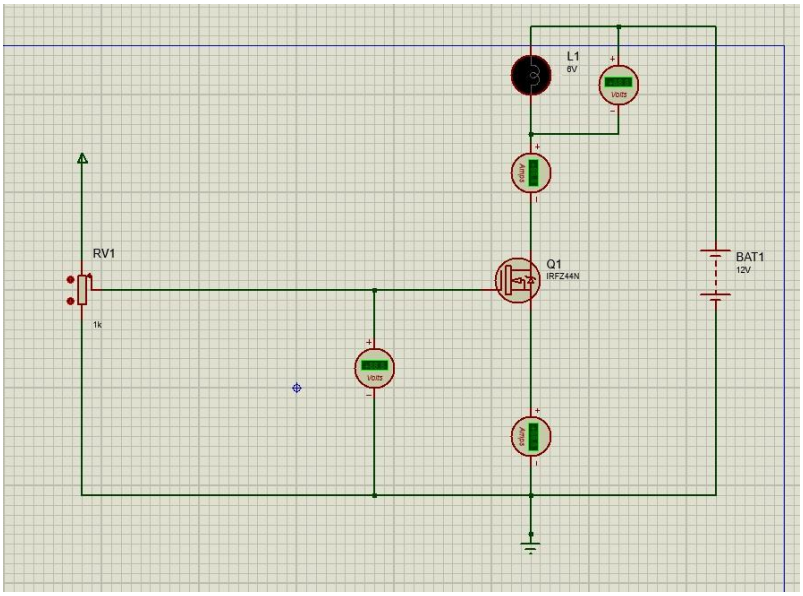


Figure No – 01: Circuit Diagram

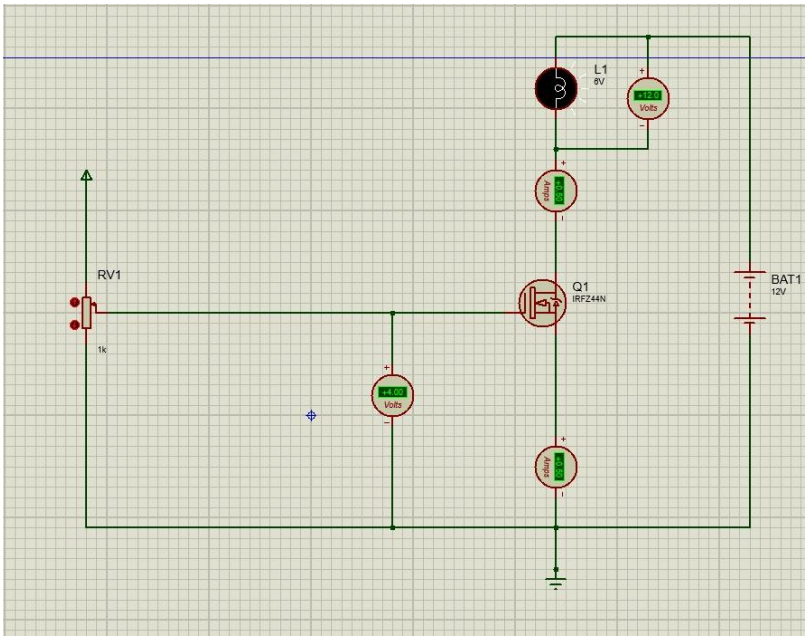


Figure No – 02: Circuit Diagram

Conclusion:

In conclusion, our investigation into MOSFETs as switches with lamp brightness control has demonstrated their efficacy in regulating the intensity of illumination with precision and efficiency. Through Pulse Width Modulation (PWM) techniques, we successfully achieved analog control over the lamp's brightness by modulating the MOSFET's conductivity. Our experiment revealed a direct relationship between the duty cycle of the PWM signal and the corresponding brightness levels of the lamp, showcasing the versatility of MOSFETs in providing adjustable lighting solutions.

Questions and Exercises:

1.What are the advantages of using a MOSFET as a switch compared to other devices?

MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) offer several advantages as switches:

Fast Switching Speed: MOSFETs can switch on and off rapidly, making them suitable for high-frequency applications like switching power supplies and motor control.

Low Power Consumption: They have low gate current requirements, leading to efficient power usage, especially in battery-powered devices.

High Input Impedance: MOSFETs have high input impedance, meaning they require minimal input current to control the switching operation, reducing the load on driving circuits.

High Power Handling Capability: They can handle high currents and voltages, making them ideal for power electronics applications.

Miniaturization: MOSFETs can be fabricated in very small sizes, enabling compact designs in integrated circuits and devices.

Overall, MOSFETs offer a balance of speed, efficiency, and power-handling capability, making them preferred switches in a wide range of electronic applications.

2.What are the key parameters to consider when selecting a MOSFET for switching applications?

When selecting a MOSFET for switching applications, consider these key parameters:

RDS(on) (On-state resistance): Lower RDS(on) results in less power dissipation and higher efficiency.

Gate Threshold Voltage (VGS(th)): Determines the minimum voltage required to turn the MOSFET on. Ensure compatibility with your driving circuit.

Gate Charge (QG): Lower gate charge indicates faster switching speed and reduced switching losses.

Maximum Drain-Source Voltage (VDS): Should exceed the maximum voltage in your application to prevent breakdown.

Maximum Drain Current (ID): Should be higher than the maximum current in your application to avoid overloading.

Continuous Drain Current (ID): Specifies the maximum current the MOSFET can handle continuously without overheating.

Temperature Coefficient: Indicates how the device's characteristics change with temperature. Ensure suitability for your operating conditions.

Package Type: Consider package size, thermal characteristics, and ease of mounting based on your application requirements.

By evaluating these parameters, you can select a MOSFET that meets the needs of your switching application in terms of efficiency, speed, and reliability.

3. How does the gate voltage affect the switching behavior of a MOSFET?

The gate voltage controls the switching behavior of a MOSFET:
Turn-On: Increasing the gate voltage above the threshold voltage (VGS(th)) turns the MOSFET on. This allows current to flow from the drain to the source.
Turn-Off: Decreasing the gate voltage below the threshold voltage turns the MOSFET off. This blocks current flow from the drain to the source.
Threshold Voltage: Below the threshold voltage, the MOSFET remains off, regardless of the gate voltage applied.
Gate Overdrive: Applying a higher gate voltage than necessary can speed up switching but may increase power dissipation and stress on the device.
In summary, the gate voltage dictates whether the MOSFET is in an on or off state, influencing its switching behavior and overall performance.

4. What is the difference between enhancement-mode and depletion-mode MOSFETs in switching applications?

In switching applications, the key difference between enhancement-mode and depletion-mode MOSFETs lies in their default behavior without a gate voltage applied:
Enhancement-Mode MOSFETs: These MOSFETs are normally off without a gate voltage applied. They require a positive gate voltage to enhance the channel conductivity and allow current flow between the drain and the source. They are commonly used in most switching applications due to their ease of control and lower power consumption.
Depletion-Mode MOSFETs: Unlike enhancement-mode MOSFETs, depletion-mode MOSFETs are normally on without a gate voltage applied. They require a negative gate voltage to deplete the channel and reduce conductivity, thus turning them off. Depletion-mode MOSFETs are less common in switching applications but can be useful in certain specialized circuits where an "on" state by default is desired.
In summary, enhancement-mode MOSFETs require a gate voltage to turn on, while depletion-mode MOSFETs require a gate voltage to turn off in switching applications.

5. What are some common applications of MOSFET switches?

MOSFET switches find applications in various electronic systems due to their advantageous characteristics:

Power Supplies: MOSFETs are used in voltage regulation circuits, DC-DC converters, and inverters due to their high efficiency and fast switching speeds.

Motor Control: They are employed in motor drives for speed control and direction switching in appliances, robotics, and industrial automation systems.

LED Lighting: MOSFETs switch high currents in LED drivers, allowing for dimming and efficient power management in lighting systems.

Audio Amplifiers: They serve as switches in Class-D amplifiers for audio signals, providing high efficiency and low distortion.

Computing and Data Communication: MOSFET switches are vital in digital circuits, memory arrays, and communication devices, facilitating signal routing and processing.

Battery Management: In battery-powered devices, MOSFETs manage charging and discharging processes efficiently to prolong battery life and ensure safety.

RF Switching: They are used in radio-frequency applications for signal routing, modulation, and amplification in wireless communication systems.

Automotive Electronics: MOSFETs are integral to automotive systems for controlling lights, fans, motors, and power distribution, benefiting from their high power-handling capabilities and reliability.

Overall, MOSFET switches are versatile components deployed across numerous industries and technologies, enhancing performance, efficiency, and functionality in electronic systems.