# METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

PREPARED BY-

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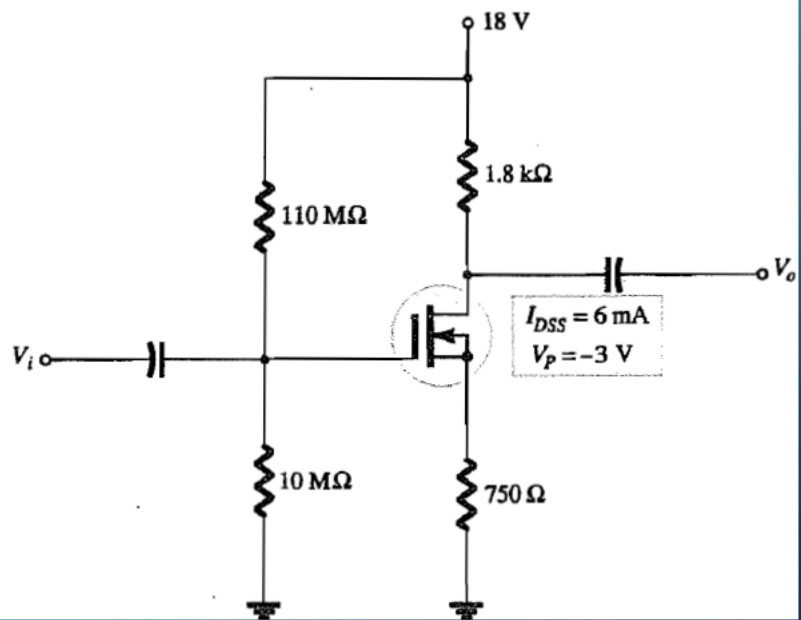
# FOR DEPLETION TYPE MOSFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

**EXAMPLE 7.7** For the $n$-channel depletion-type MOSFET of Fig. 7.30, determine:

a. $I_{D_Q}$ and $V_{GS_Q}$.
b. $V_{DS}$.




For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of $V_P$ and the fact that Shockley's equation defines a curve that rises more rapidly as $V_{GS}$ becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778) \\ &= 10.67\text{ mA} \end{aligned}$$

# FOR DEPLETION TYPE MOSFET

$$V_G = \frac{10\,\text{M}\Omega(18\,\text{V})}{10\,\text{M}\Omega + 110\,\text{M}\Omega} = 1.5\,\text{V}$$

$$V_{GS} = V_G - I_D R_S = 1.5\,\text{V} - I_D(750\,\Omega)$$

Setting $I_D = 0\,\text{mA}$ results in

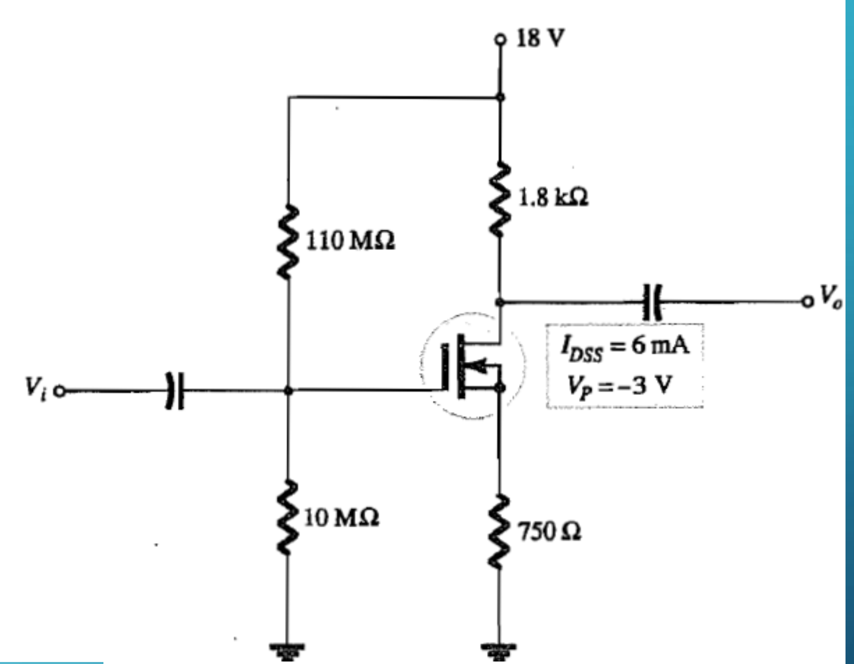
$$V_{GS} = V_G = 1.5\,\text{V}$$

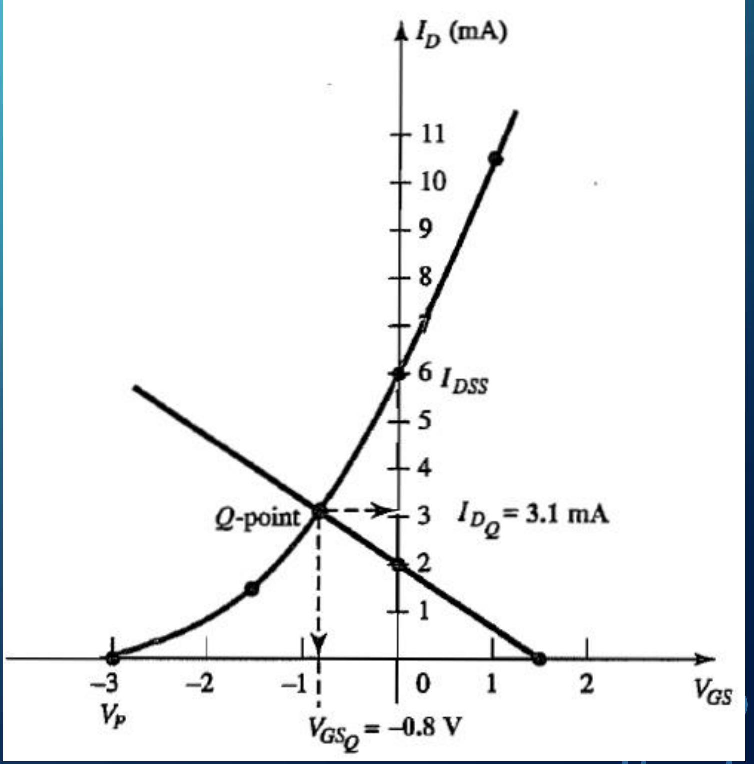
Setting $V_{GS} = 0\,\text{V}$ yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\,\text{V}}{750\,\Omega} = 2\,\text{mA}$$

$$\mathbf{I_{D_Q} = 3.1\,mA}$$
$$\mathbf{V_{GS_Q} = -0.8\,V}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 18\,\text{V} - (3.1\,\text{mA})(1.8\,\text{k}\Omega + 750\,\Omega) \\ &\cong \mathbf{10.1\,V} \end{aligned}$$



# FOR ENHANCEMENT TYPE MOSFET

For Vgs>Vt, the drain current is to related to the applied gate to source voltage by the following non linear relationship_

$$I_D = kV_{GS} - V_t)^2$$

In an enhancement-type MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), "k" typically refers to the transconductance parameter. Transconductance (often denoted as "k" or "gm") represents the relationship between the input voltage and the output current of the MOSFET, essentially indicating how effectively the device can amplify an input signal.

The transconductance parameter ($k$) in terms of its relationship with the drain current ($ID(on)$) and the gate-source voltage ($VGS(on)$) at the point of MOSFET turn-on, and the threshold voltage ($VT$). This equation is typically derived from the MOSFET small-signal model and is used to estimate the transconductance parameter based on device characteristics.

The equation you've provided can be rearranged as follows to express $k$ in terms of the given parameters:

$$k = \frac{I_D(on)}{(V_{GS}(on) - V_T)^2}$$

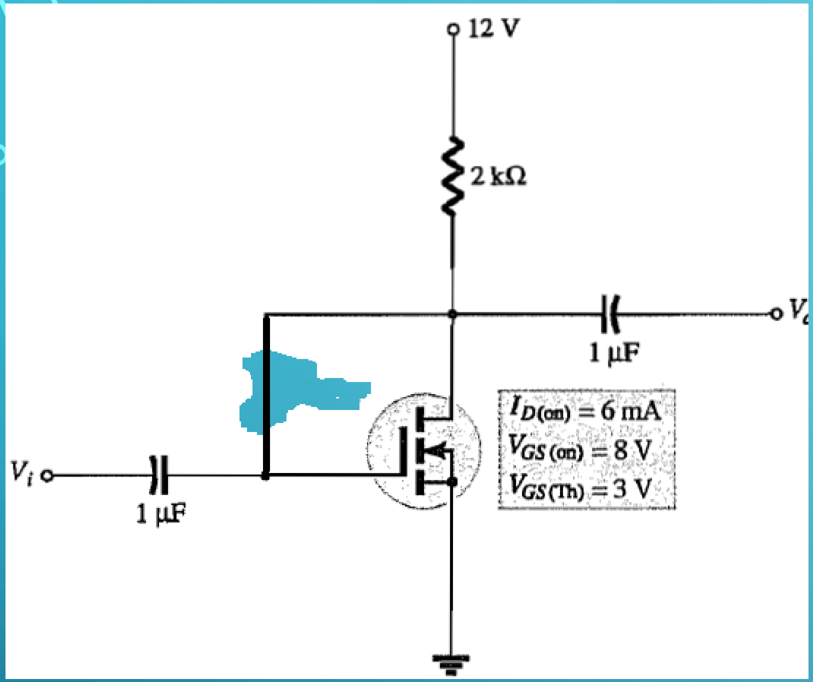
Where:

- $k$ is the transconductance parameter.
- $ID(on)$ is the drain current at the point of turn-on.
- $VGS(on)$ is the gate-source voltage at the point of turn-on.
- $VT$ is the threshold voltage of the MOSFET.

This equation gives you the transconductance parameter based on the device's characteristics at the point of turn-on, which can be useful in MOSFET circuit design and analysis.

# FOR ENHANCEMENT TYPE MOSFET

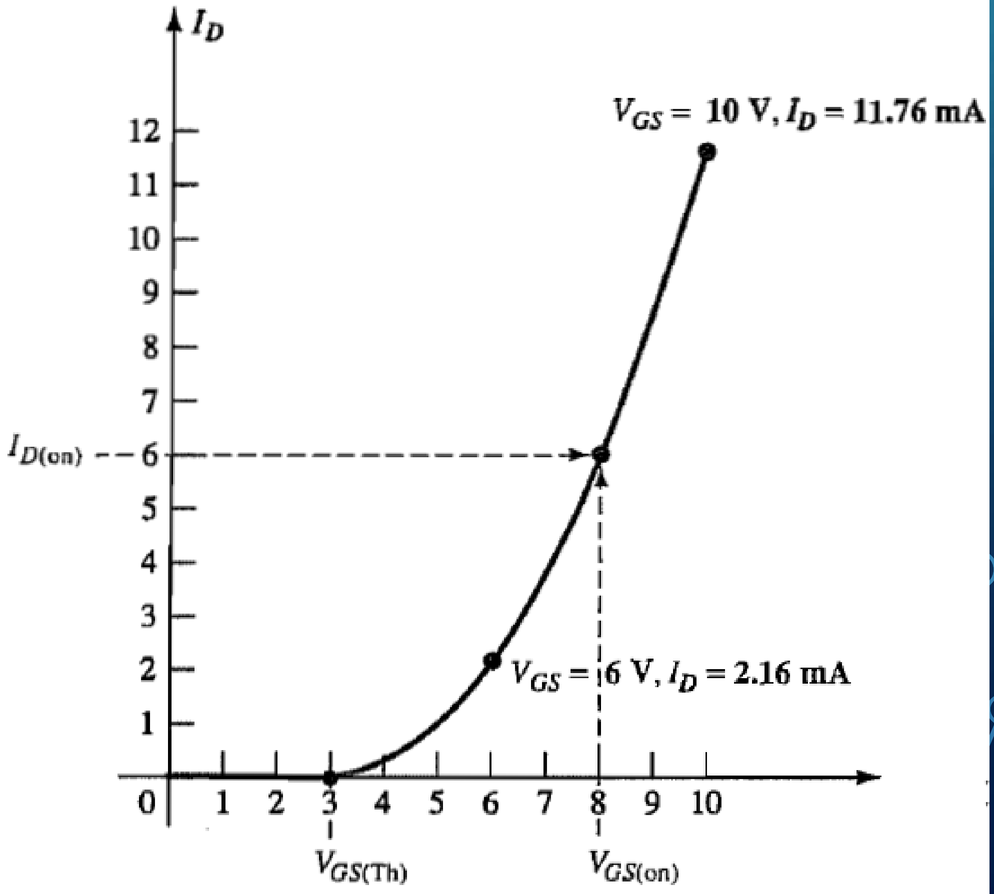
Determine $I_{D_Q}$ and $V_{DS_Q}$ for the enhancement-type MOSFET




$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$
$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{ A/V}^2$$
$$= \mathbf{0.24 \times 10^{-3}\ A/V^2}$$

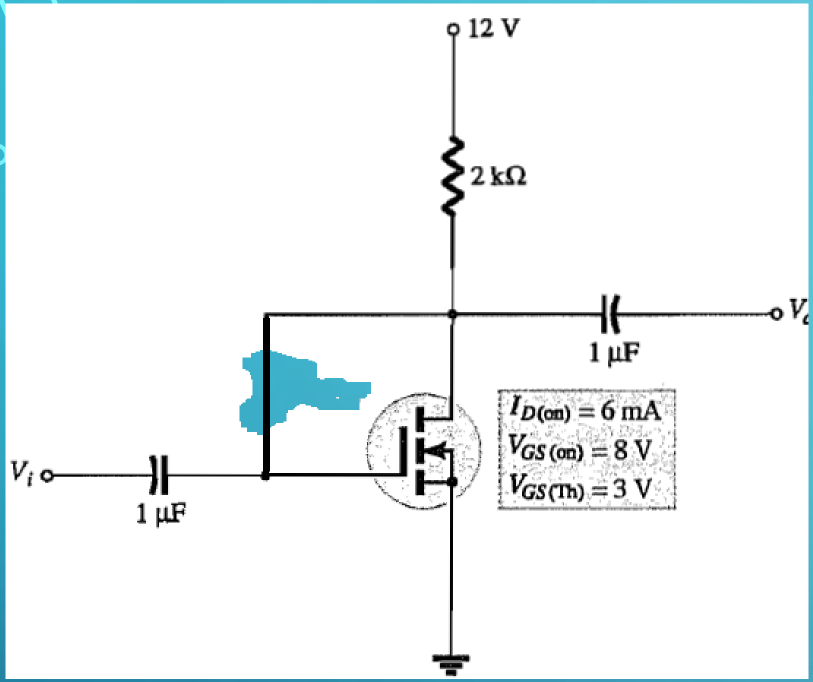
For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$
$$= 2.16\text{ mA}$$



# FOR ENHANCEMENT TYPE MOSFET

Determine $I_{D_Q}$ and $V_{DS_Q}$ for the enhancement-type MOSFET




For $V_{GS} = 10\text{ V}$ (slightly greater than $V_{GS(Th)}$),

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\text{ mA}$$

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$
$$V_{GS} = V_{DD} = 12\text{ V}\big|_{I_D = 0\text{ mA}}$$
$$I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}\big|_{V_{GS}=0\text{ V}}$$

At the operating point,

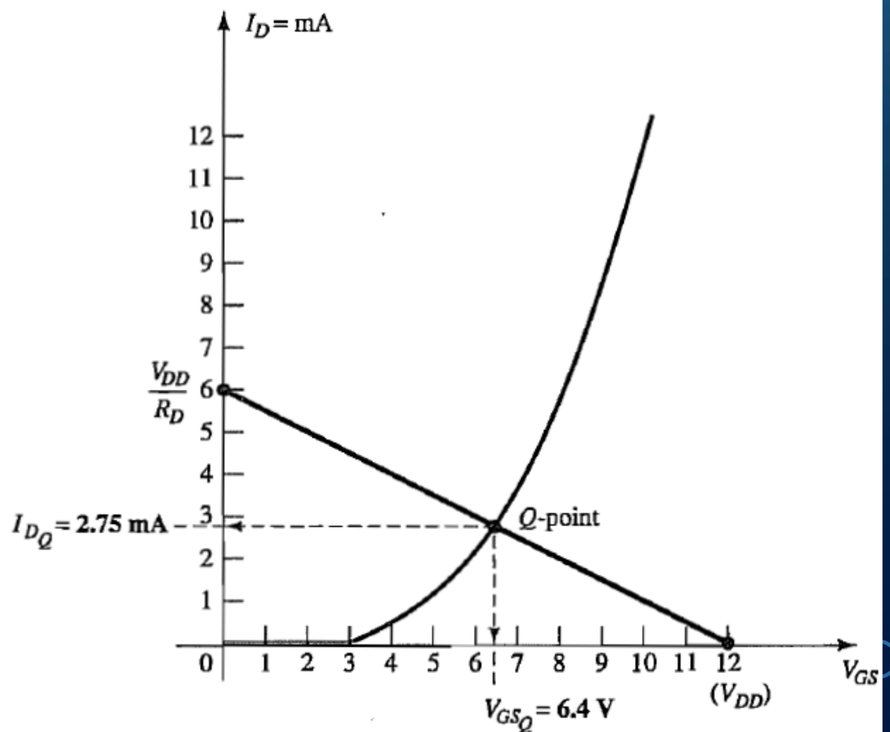
$$I_{D_Q} = \mathbf{2.75\ mA}$$

and

$$V_{GS_Q} = 6.4\text{ V}$$

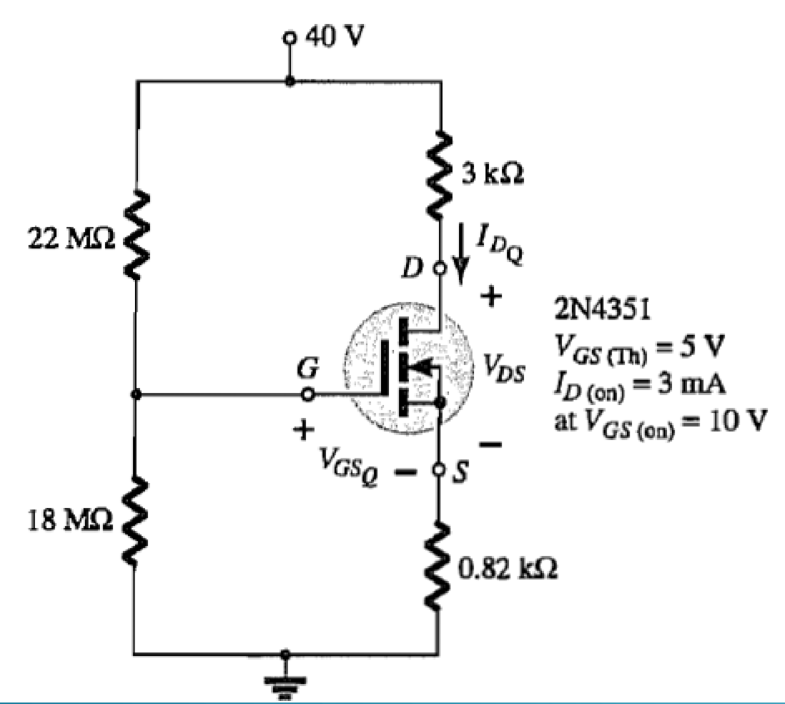
with

$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\ V}$$



# FOR ENHANCEMENT TYPE MOSFET

Determine $I_{D_Q}$, $V_{GS_Q}$, and $V_{DS}$ for the network




$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

When $I_D = 0$ mA,

$$V_{GS} = 18\,\text{V} - (0\,\text{mA})(0.82\,\text{k}\Omega) = 18\,\text{V}$$

When $V_{GS} = 0$ V,

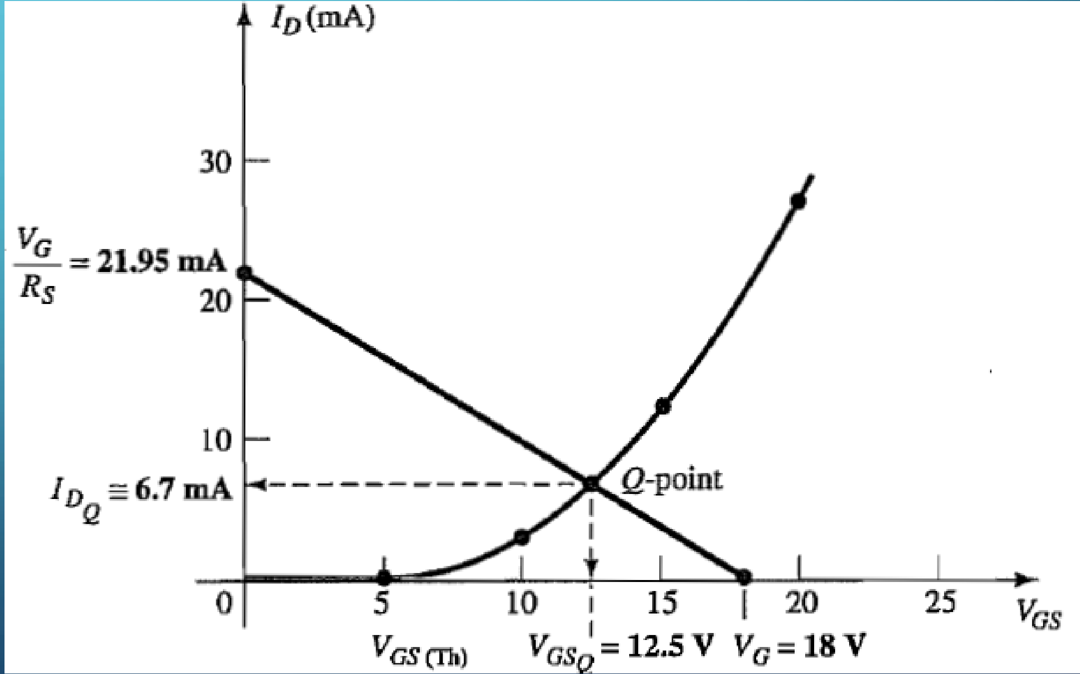
$$V_{GS} = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

$$0 = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

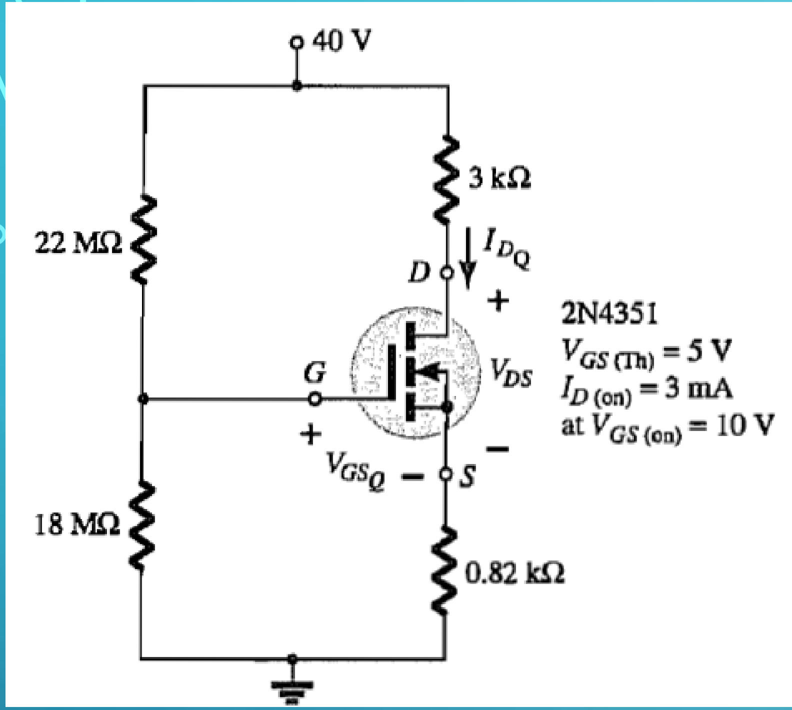
$$I_D = \frac{18\,\text{V}}{0.82\,\text{k}\Omega} = 21.95\,\text{mA}$$

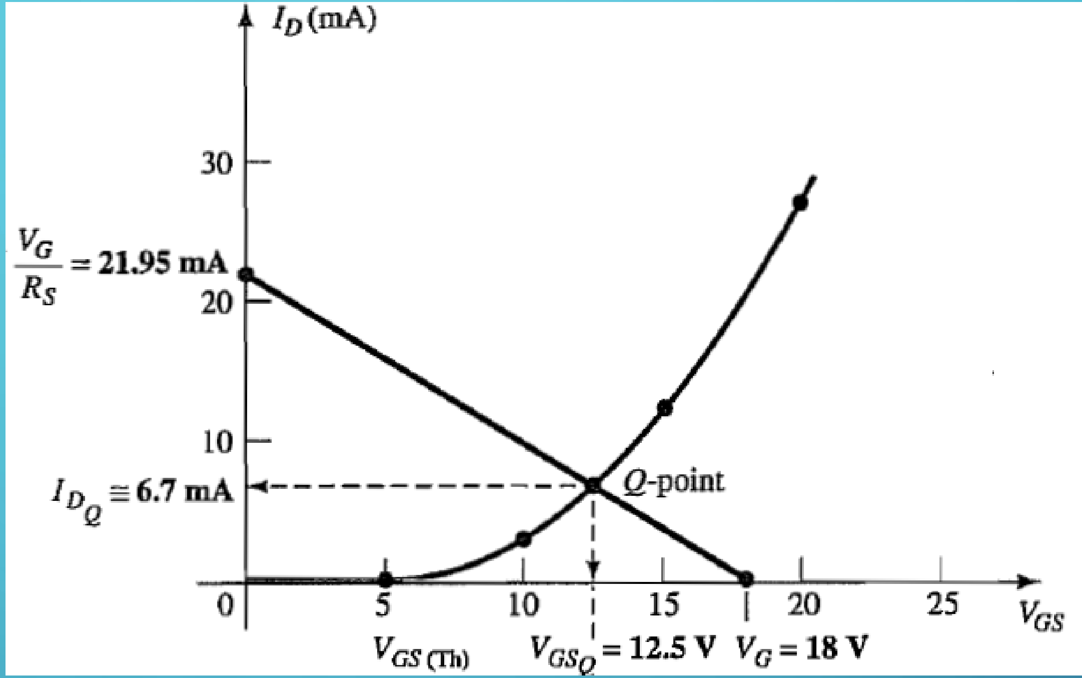
**Device**

$V_{GS(\text{Th})} = 5$ V, $\quad I_{D\,(\text{on})} = 3$ mA with $V_{GS(\text{on})} = 10$ V



# FOR ENHANCEMENT TYPE MOSFET




$$k = \frac{I_{D(\mathrm{on})}}{(V_{GS(\mathrm{on})} - V_{GS(\mathrm{Th})})^2}$$

$$= \frac{3\ \mathrm{mA}}{(10\ \mathrm{V} - 5\ \mathrm{V})^2} = 0.12 \times 10^{-3}\ \mathrm{A/V^2}$$

$$I_D = k(V_{GS} - V_{GS(\mathrm{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

$$I_{D_Q} \cong \mathbf{6.7\ mA}$$

$$V_{GS_Q} = \mathbf{12.5\ V}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\ \mathrm{V} - (6.7\ \mathrm{mA})(0.82\ \mathrm{k\Omega} + 3.0\ \mathrm{k\Omega})$$

$$= 40\ \mathrm{V} - 25.6\ \mathrm{V}$$

$$= \mathbf{14.4\ V}$$

# FOR ENHANCEMENT TYPE MOSFET

- For ‘ON’ or saturation region Vgs>Vt
- For ‘OFF’ or cut off region Vgs<Vt
- For triode/linear/ohmic region Vds<(Vgs-Vt)
- For saturation region of operation Vds≥(Vgs-Vt)

| Condition | Operation region | Formula of Id |
|---|---|---|
| Vds<(Vgs-Vt) | triode/linear/ohmic region | $I_D = \mu_n C_{ox}\frac{W}{L}\left((V_{GS}-V_t)V_{DS}-\frac{1}{2}V_{DS}{}^2\right)$ |
| Vds≥ (Vgs-Vt) | saturation region | $I_D = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2\ \frac{1}{2}$ |

# FOR ENHANCEMENT TYPE MOSFET

**Mobility of the electrons at the surface of the channel** $\mu_n$

**Oxide capacitance** $C_{ox}$

**Width of the channel** W

**Length of the channel** L

**Gate to source voltage** $V_{GS}$

**Drain to source voltage** $V_{DS}$

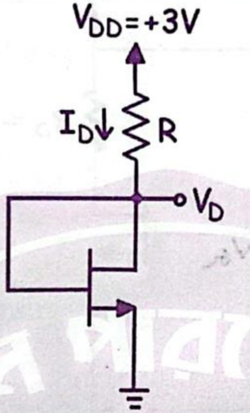
**Threshold voltage** $V_t$

**MOSFET trans-conductance parameter** $k_n{}' = \mu_n C_{ox}$

**MOSFET trans-conductance parameter** $k_n = \mu_n C_{ox} \frac{W}{L}$

**Aspect ratio**= $\frac{W}{L}$

6 Design the circuit in figure to obtain a current $I_D$ of 80 µA. Find the value required for R and find the dc voltage $V_D$. Let the NMOS transistor have $V_t = 0.6$ V, $\mu_n C_{ox} = 200\ \mu A/V^2$, L=0.8 µm and W = 4 µm. Neglect the channel length and modulation effect (i.e., assume $\lambda = 0$ ) *[Example 4.3, Sedra-smith, 5th Edition, Page-264]*




As Source is grounded and Gate & Drain is shorted, $V_{GS} - V_t < V_{DS}$

Here, $V_{DS} = V_{GS}$

$V_t = 0.6$ V

So, $V_{GS} - V_t < V_D$ ; the MOSFET is being operated in sturation region. So,

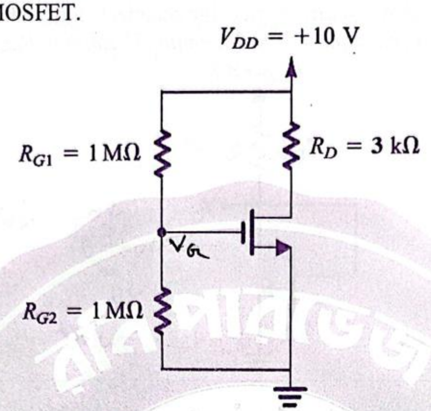
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$\Rightarrow V_{GS} - V_t = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} = \sqrt{\frac{2\times 80}{200\times(4/0.8)}} = 0.4\text{ V}$$

or, $V_{GS} = 0.4 + V_t = 0.4 + 0.6 = 1$ V

So, $V_D = V_{DS} = V_{GS} = 1$ V

So, $R = (V_{DD} - V_D) / I_D = (3 - 1) / 0.08 = 25\ k\Omega$ **Ans.**

| | |
|---|---|
| 7 | Find $I_{Dmax}$ that can flow through the ideal N-MOSFET. Also find $V_{DS}$ at $I_{Dmax}$. Given $V_{tn}$ = 1.5 V and $K_n'(W/L) = 2.76 \times 10^{-6}$ A/V$^2$. Also Find the power dissipated in the MOSFET.  |



**Solution:**

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 1-MΩ resistors

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10 \times \frac{1}{1+1} = +5\text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. If our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Since the voltage at the gate is 5 V and source is grounded,

$V_{GS} = 5$ V

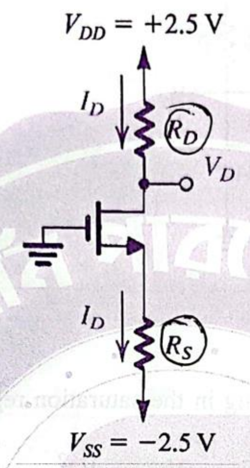
$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_{tn})^2$$

$= ½ * 2.76 * 10^{-6} * (5- 1.5)^2 = 16.9$ µA

$V_D = V_{DS} = V_{DD} - I_D R_D = 10 - (16.9*10^{-6})*(3*10^3) = 9.9493$ V.

Since, $V_{DS} > V_{GS} - V_{tn}$; the transistor is operating in saturation, as initially assumed.

| | |
|---|---|
| 3 | Design the circuit of Fig., that is, determine the values of $R_D$ and $R_S$, so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 1\ \mu m$, and $W = 32\ \mu m$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$). *[Example 5.3, Sedra-Smith]* |




To establish a dc voltage of + 0.5 V at the drain, we must select $R_D$ as follows:

So, $R_D = (V_{DD} - V_D) / I_D = (2.5 - 0.5) / 0.4 = 5\ k\Omega$ **Ans.**

To determine the value required for $R_S$, we need to know the voltage at the source, which can be easily found if we know $V_{GS}$. This in turn can be determined from $(V_{GS} - V_t)$. Toward that end, we note that since $V_D = 0.5$ V is greater than $V_G$, the NMOS transistor is operating in the saturation region, and we can use the saturation-region expression of $I_D$ to determine the required value of $(V_{GS} - V_t)$,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Then substituting $I_D = 0.4$ mA $= 400\ \mu A$, $\mu_n C_{ox} = 100\ \mu A/V^2$, and $W/L = 32/1$ gives

$400 = ½ * 100 * (32/1) * (V_{GS} - V_t)^2$

⇨ $(V_{GS} - V_t) = 0.5$

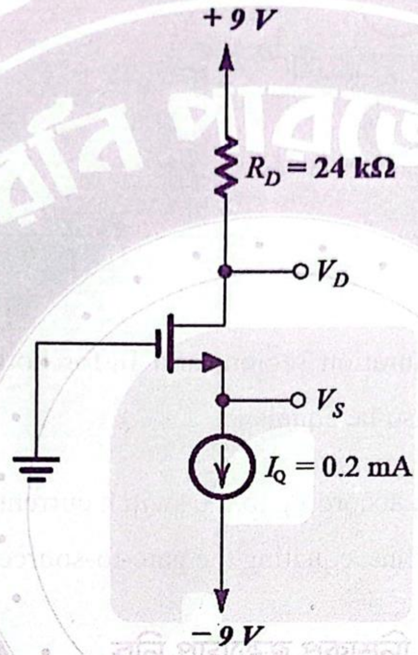
⇨ $V_{GS} = 0.5 + V_t = 0.5 + 0.7 = 1.2$ V

Now, $V_{GS} = V_G - V_S$

⇨ $V_S = V_G - V_{GS} = 0 - 1.2 = -1.2$ V

So, $R_S = (V_S - V_{SS}) / I_D = \{(-1.2) - (-2.5)\} / 0.4 = 3.25\ k\Omega$ **Ans.**

In the following NMOS Transistor $V_t = 0.6$ V and $K_n'(W/L) = 200\ \mu A/V^2$. Determine the value of $V_S$ and $V_D$.




**Solution:**

Here, $V_G = 0$ V & $V_t = 0.6$ V. So, $V_G - V_t = 0 - 0.6 = -0.6$ V

$V_D = V_{DD} - I_D R_D = 9 - 0.2 * 24 = 4.2$ V **Ans.**

As $V_D > V_G - V_t$ ; $V_{DS} > V_{GS} - V_t$. So, the MOSFET will be operated in saturation region and

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

or, $(0.2*10^{-3}) = ½ * (200*10^{-6})*(V_{GS} - 0.6)^2$ $[K_n' = \mu_n C_{ox}]$

or, $(V_{GS} - 0.6)^2 = 2$

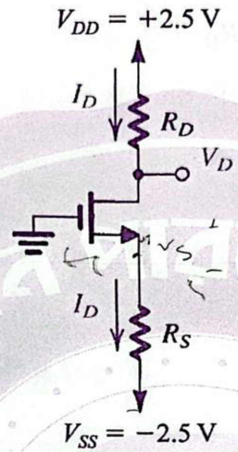
or, $(V_{GS} - 0.6) = \sqrt{2} = 1.414$

or, $V_{GS} = 1.414 + 0.6 = 2.01$ V

Again, $V_{GS} = V_G - V_S$

So, $V_S = V_G - V_{GS} = 0 - 2.01 = -2.01$ V **Ans.**

| | |
|---|---|
| 4 | A NMOS transistor in the circuit of Fig., has $R_D = 5\ k\Omega$, and $R_S = 3.25\ k\Omega$. The transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. It has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 1\ \mu m$. Determine the value of gate width, $W$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$). *[Similar to Example 5.3, Sedra-Smith]* |




$V_{DS}$ $V_{GS} - V_t$

$V_{DS}$ ?

$V_S$ =

$I_D = \frac{V_{DD} - V_D}{R_D}$

$\frac{V_{SS} - V_S}{R}$

$V_S - I_D R_S - 2.5$

$V_S = 2.5 +$

To establish a dc voltage of +0.5 V at the drain, we must select $R_D$ as follows:

So, $I_D = (V_{DD} - V_D) / R_D = (2.5 - 0.5) / 5000 = 0.4$ mA

Again, $I_D = (V_S - V_{SS}) / R_S$

⇨ $V_S = V_{SS} + I_D R_S = \{ (-2.5) + (0.4*10^{-3})*(3.25*10^{3})\} = -1.2$ V.

So, $V_{GS} = V_G - V_S = 0 - (-1.2) = 1.2$ V ✓

So, $V_{GS} - V_t = 1.2 - 0.7 = 0.5$ V. ✓

But, $V_D = 0.5$ V.

As, $V_D = V_{GS} - V_t$; the MOSFET is being operated in saturation region. So,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

or, $(0.4*10^{-3}) = ½ * (100*10^{-6}) * \{W/(1*10^{-6})\} * (0.5)^2$

So, $W = 32\ \mu m$ **Ans.**

# Thank You!