



APLM

(Automated Piano Learning Module)

Project semester 8 2024-2025



Contents

- I. Reminder and brief presentation of the project
- II. Demonstration
- III. Additional schematic and PCB Design
- IV. Digital audio signal processing



I. Reminder and brief presentation of the project

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Figure 1: Representation of the project generated by IA

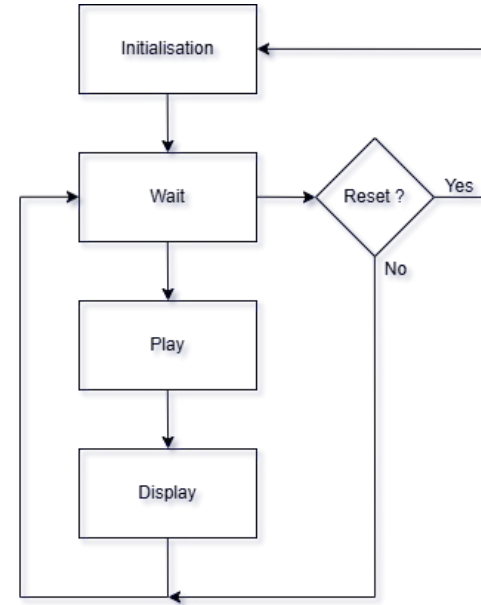


Figure 2: Project function diagram

I. Reminder and brief presentation of the project

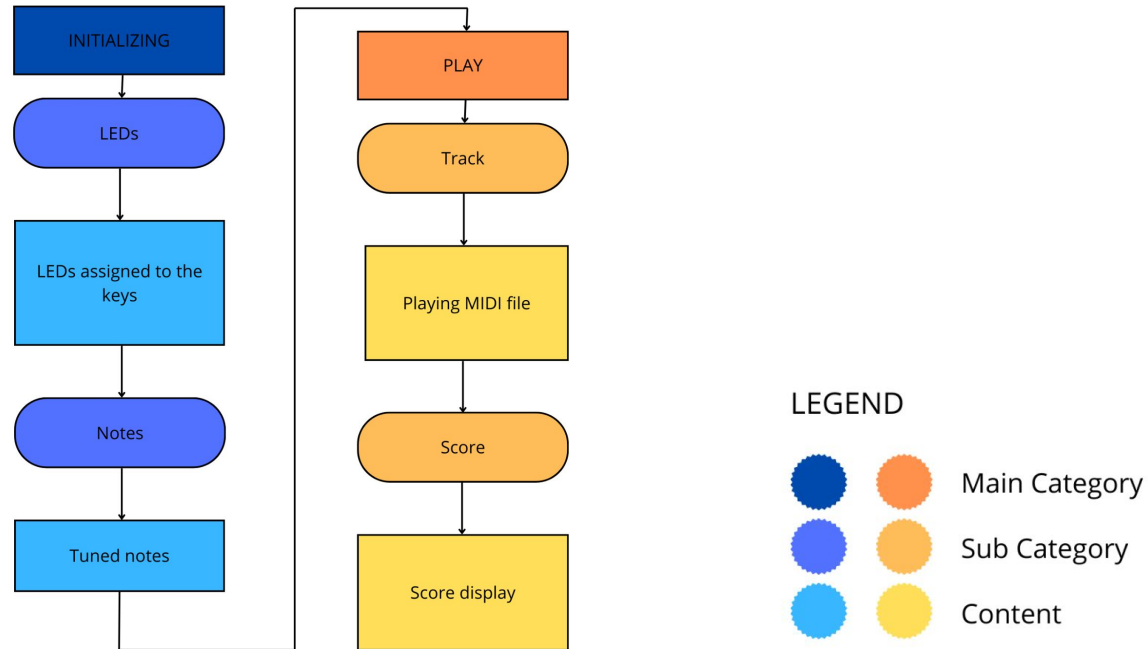


Figure 3: Initializing and Play



II. Demonstration

II. Demonstration

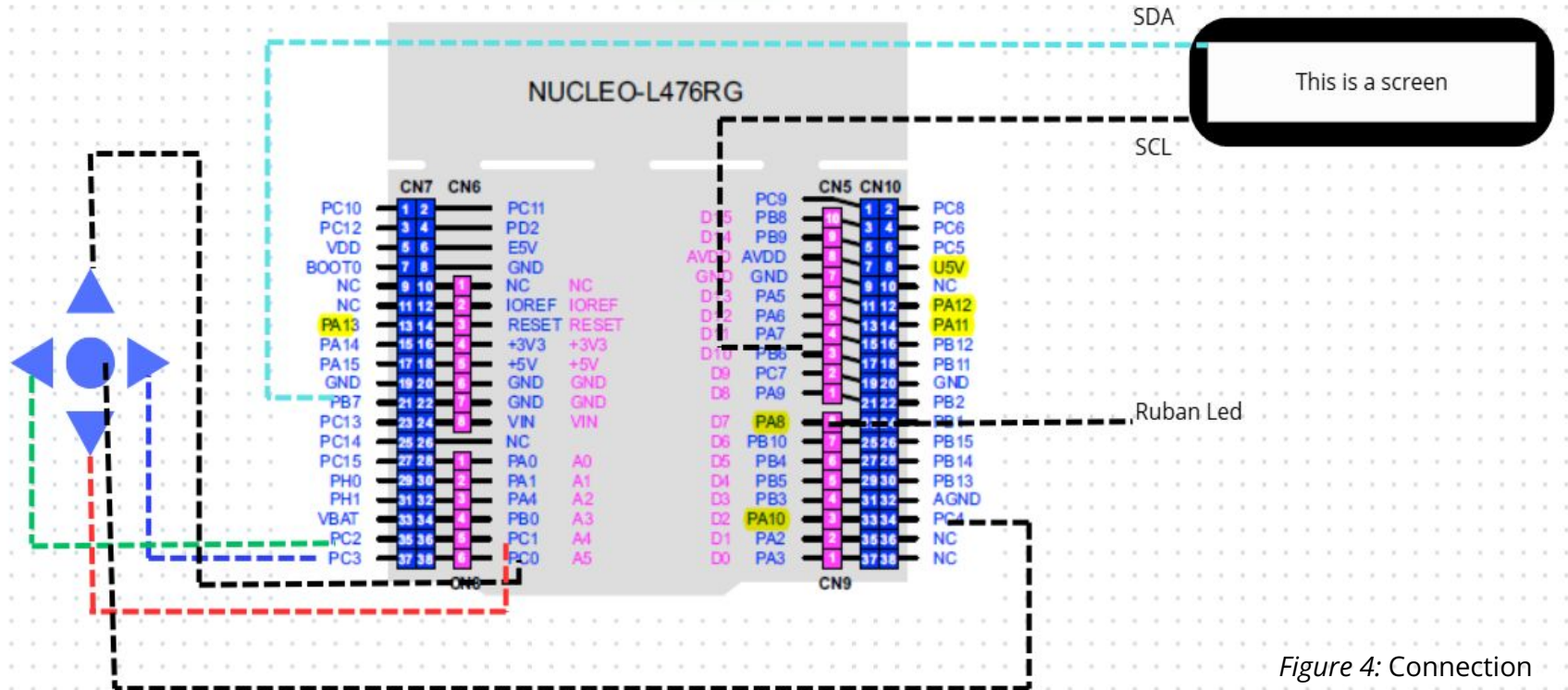


Figure 4: Connection

1) Initialization

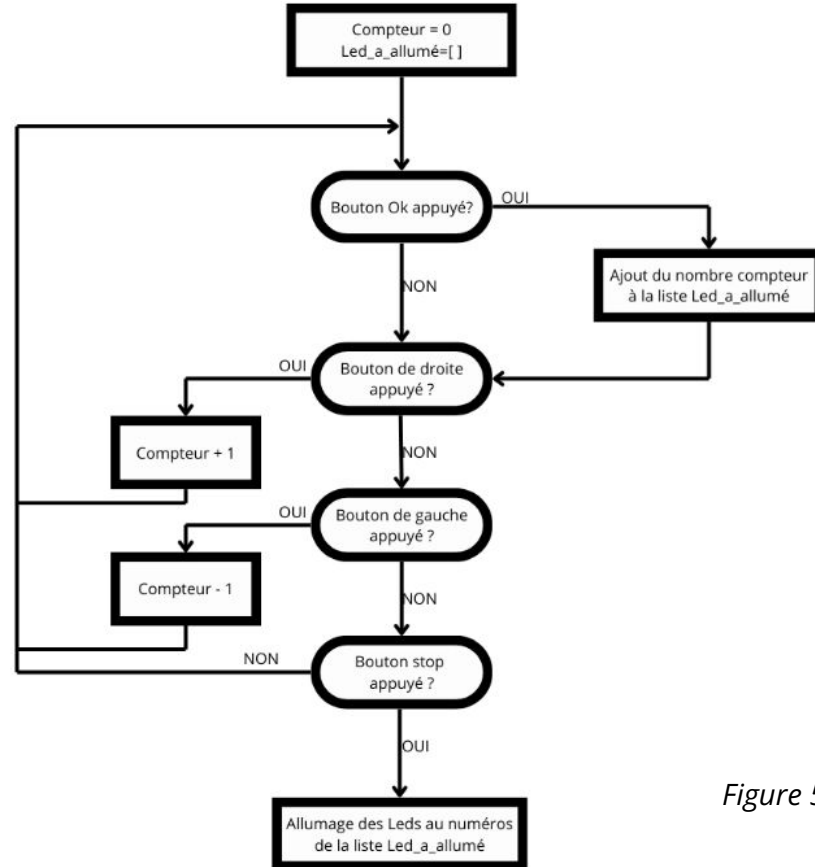


Figure 5: Decision diagram of Led assign

2) Menu

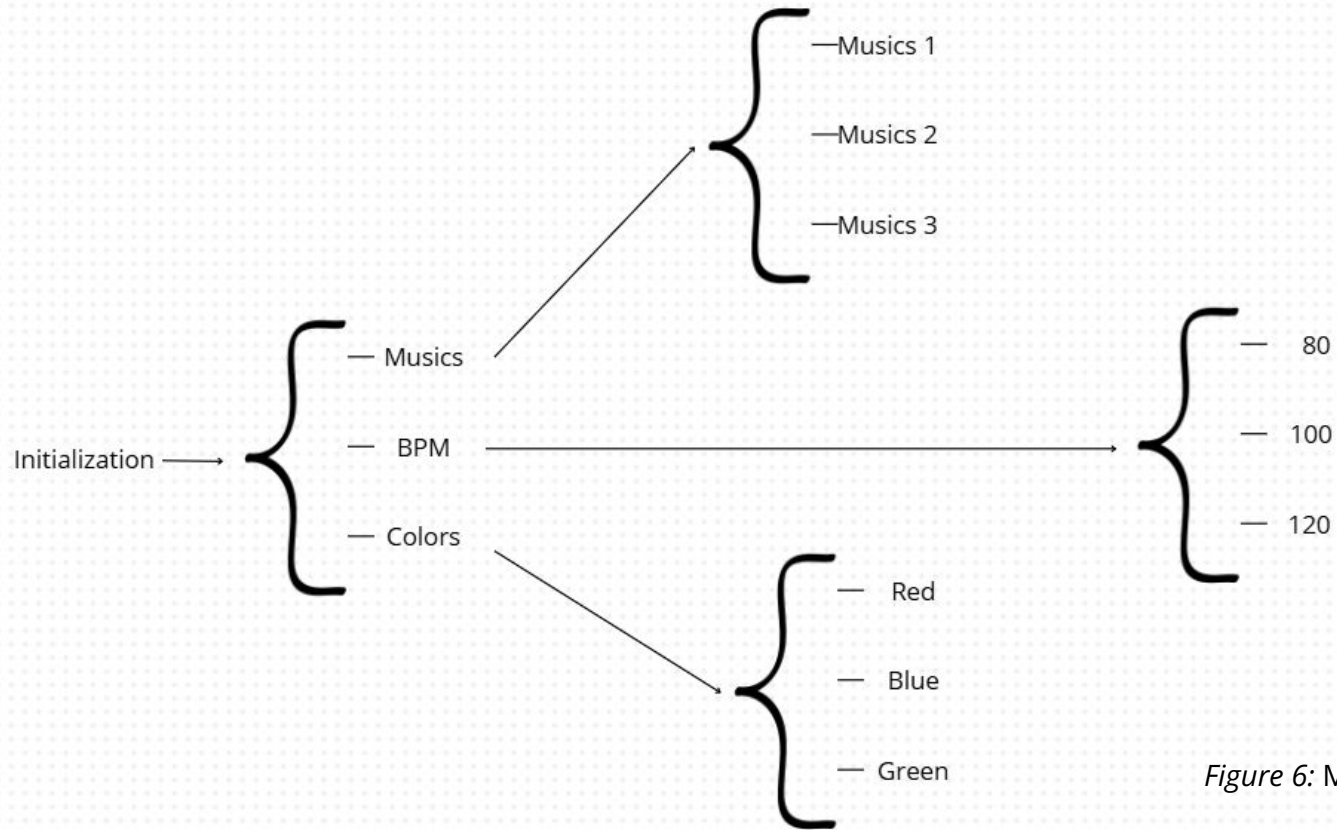


Figure 6: Menu navigation

3) Possible Ameliorations

- Do the test for an entire piano and not just an octave
- Store more MIDI file in a SD card to play different music
- Increase the number of floors
- Complete the User Interface and functionality (Colors,BPM,...)
- Correct the initialization list with the real list played when there are several floors



III. Additional schematic and PCB Design

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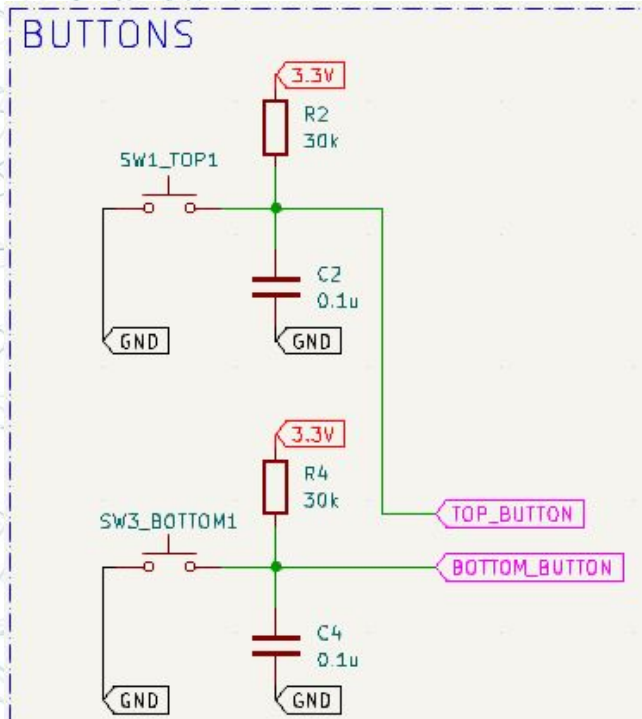


Figure 7: Buttons schematic

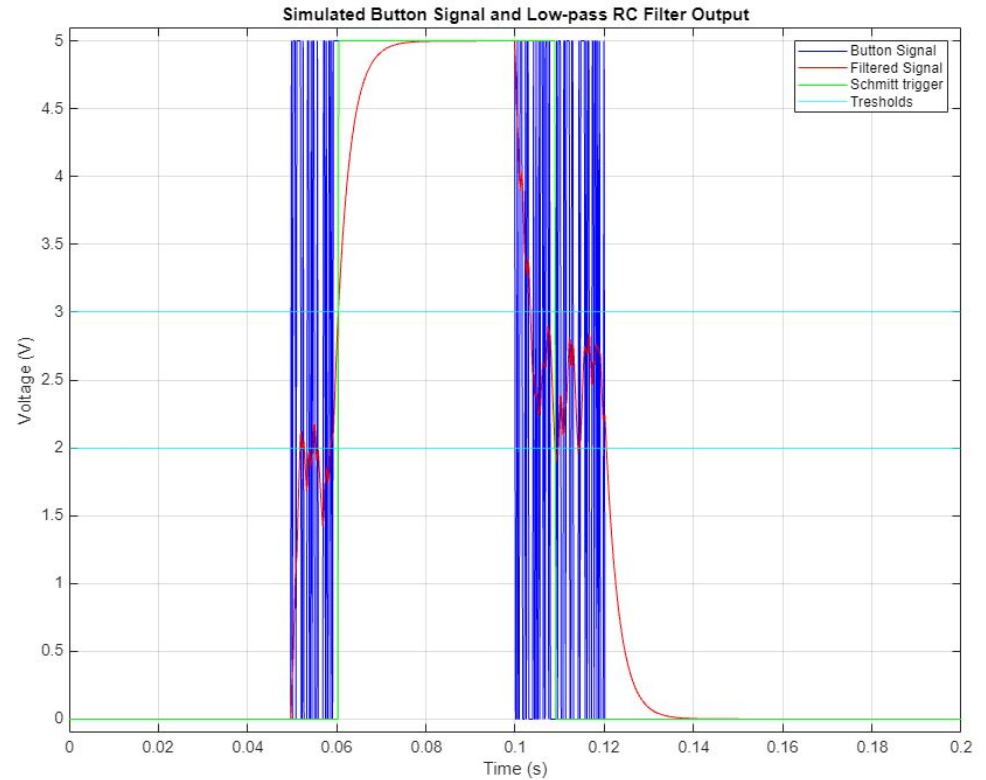


Figure 8: Button simulation

III. Additional schematic and PCB Design

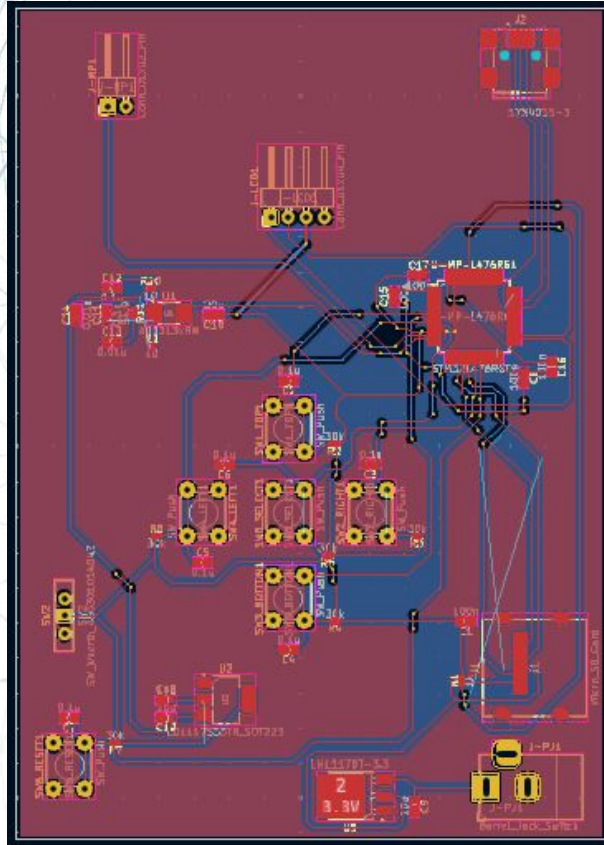


Figure 9: APLM PCB

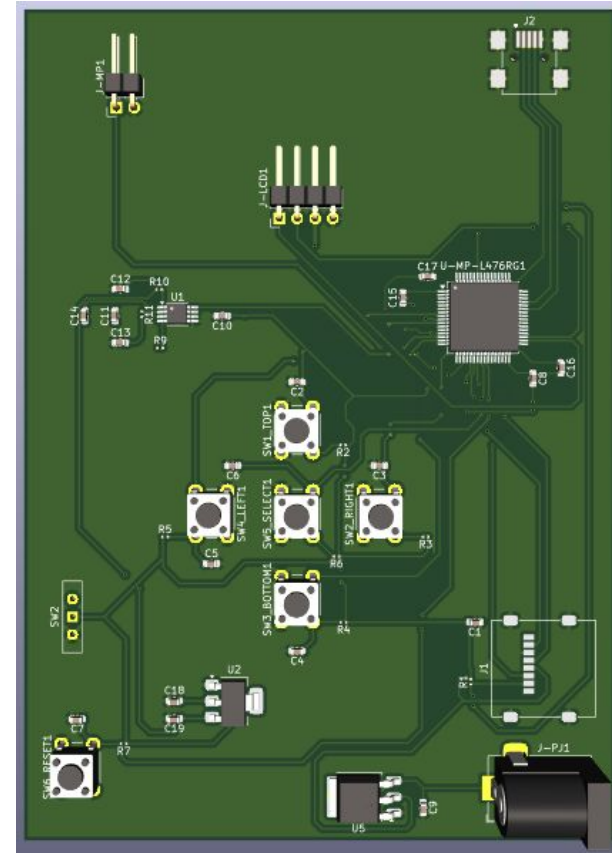


Figure 10: APLM 3D view

III. Additional schematic and PCB Design

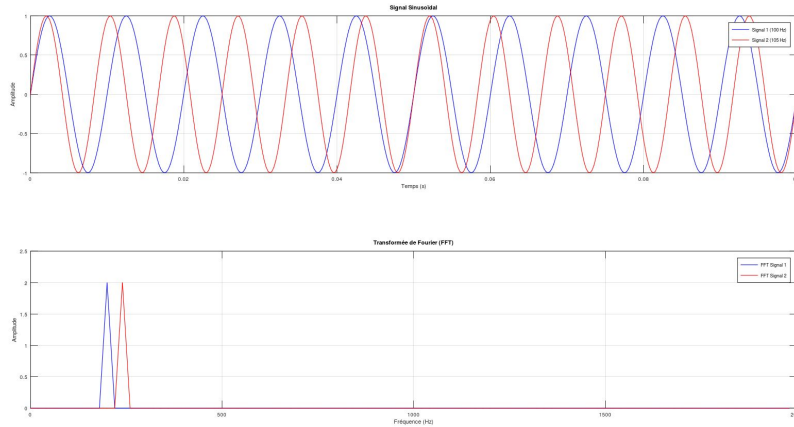
What's left to do as of today :

- Fix the issue with certain components on the PCB
- Print the PCB
- Solder the components onto the board



IV. Digital audio signal processing

IV. Digital audio signal processing



$$S_{Tn} = \left(1 - \frac{|f_{OnTH} - f_{OnMS}|}{f_{OnTH}}\right) * \frac{100}{100}$$

=>

$$S_{Final} = \frac{1}{N_0} * \sum_{i=1}^{N_0} S_{Ti}$$

T_N : Le N-ième temps joué

N_0 : le nombre de temps du morceau

Figure 11: Method for evaluating the user score



Figure 12: Useful libraries for the project

V. Digital audio signal processing

Solutions

Solution	Conditions d'estimation des temps	Temps d'acquisition (ms)	Temps de calcul FFT (ms)	Total (ms)	Impact sur CPU STM32	Complexité d'implémentation	Prix supplémentaire	Conclusion
STM32L476RG (CMSIS-DSP)	Cortex-M4 à 80 MHz avec FPU Deux FFT exécutées séquentiellement avec CMSIS-DSP	3	4	7	Fort	Nécessite l'implémentation d'un code à partir de la bibliothèque CMSIS qui est difficile d'utilisation avec un temps de développement supplémentaire plus long.	0,00 €	Sélectionné
X-NUCLEO-IKS02A1	Temps d'acquisition via I ² C/SPI estimé à ~1-2 ms Calcul FFT effectué sur STM32 avec CMSIS-DSP	1-2	4-6	5-8	Moyen	Ne nécessite pas de code complexe et trop de temps de développement supplémentaire.	29,39 €	Recalé
ADS1299	Temps d'acquisition via SPI à 16 S/S Calcul FFT effectué sur STM32 avec CMSIS-DSP	0,2	3,2-4,2	3,4-4,4	Moyen	Ne nécessite pas de code complexe et trop de temps de développement supplémentaire.	29,87 €	Recalé
AD7768	Temps d'acquisition via SPI ou LVDS (256 kS/S) Calcul FFT réalisé à un FPGA ou un DSP dédié	0,05	~0,5 (via FPGA/DSP)	0,55	Faible	Ne nécessite pas de code complexe et trop de temps de développement supplémentaire.	20,96 €	Recalé

Figure 13: Options in numbers

V. Digital audio signal processing

Paradigm shift

When initialising, record every FFT of every note on the piano!

V. Digital audio signal processing

Advantages:

- Frees up the processor for a real-time FFT
- Simplifies programming (no need to search for a maximum, cross-correlation of theoretical and measured signals)
 - Gives the processor extra room to manoeuvre

V. Digital audio signal processing

Physical simulation of the new process

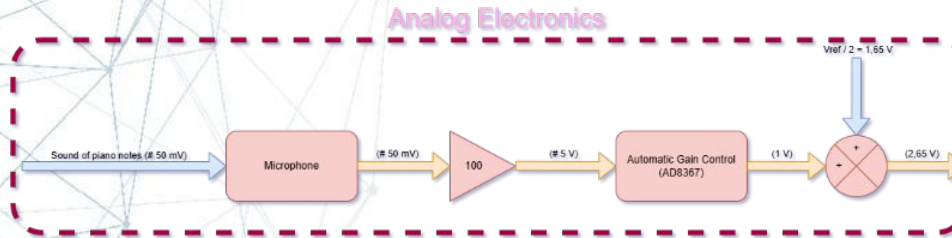


Figure 14: Function diagram of the DSP section

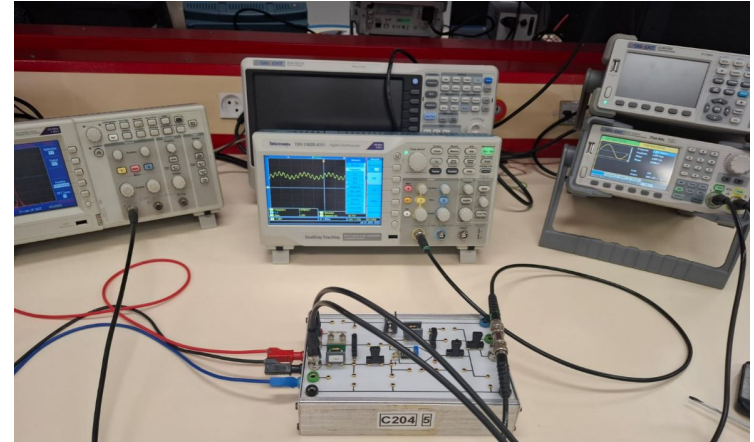


Figure 15: Representative electronic circuit for the new process

V. Digital audio signal processing

Physical simulation of the new process

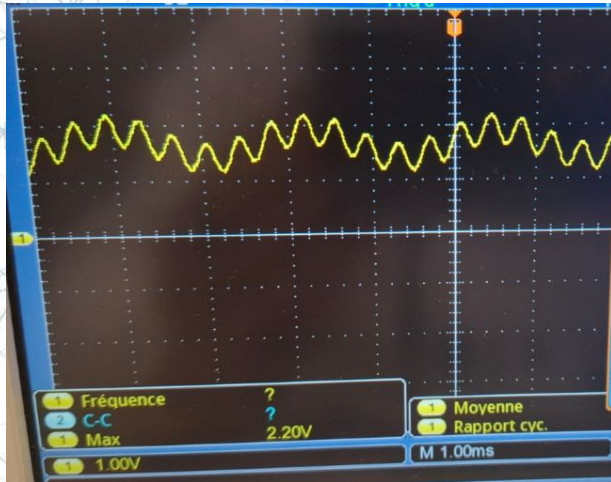


Figure 16: Sum of signals

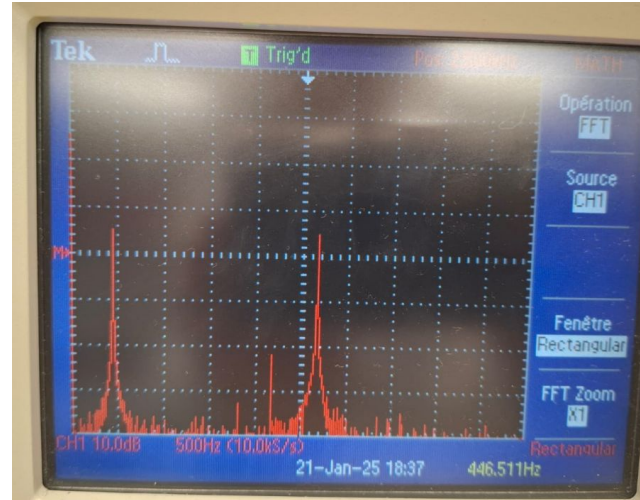


Figure 17: FFT of the sum

V. Digital audio signal processing

Introduction of white noise

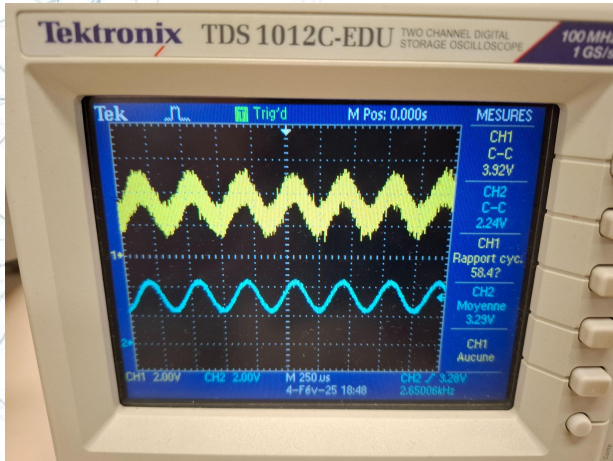


Figure 18: Noisy and filtered signal

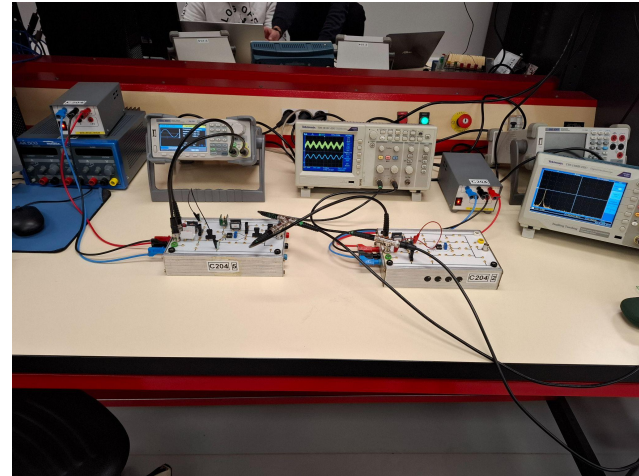


Figure 19: Electrical installation

V. Digital audio signal processing

Averaging filter

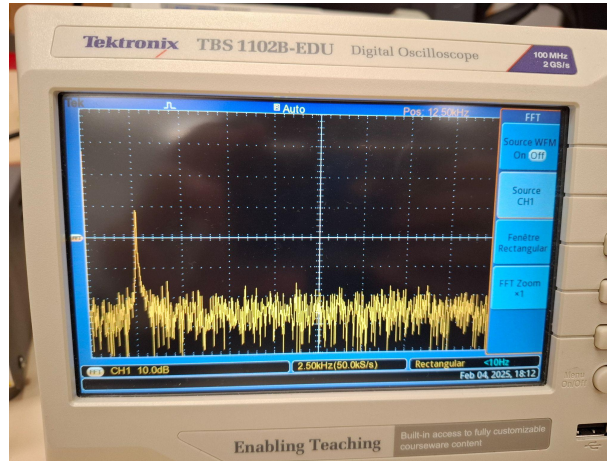


Figure 20: Filtered FFT

V. Digital audio signal processing

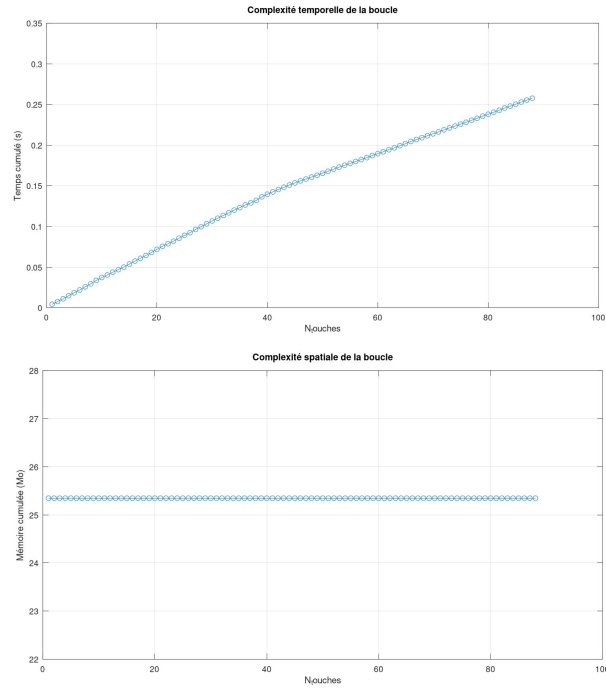


Figure 21: Temporal and spatial complexity for the greedy algorithm

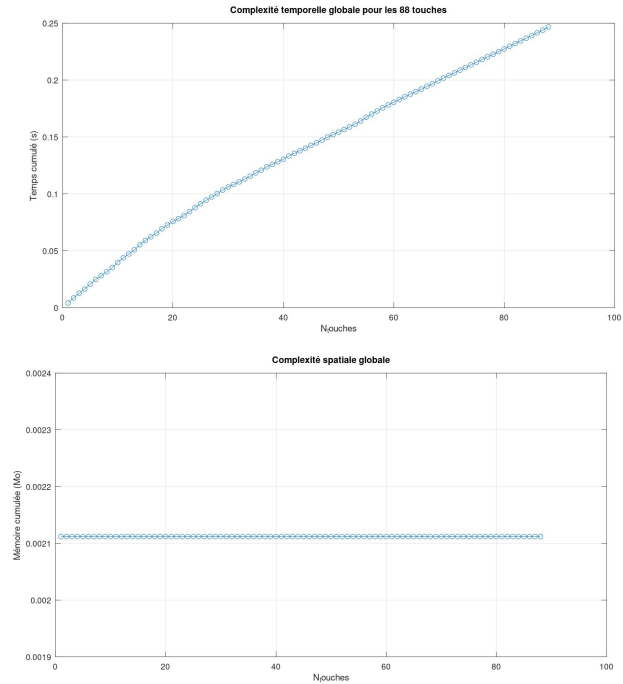


Figure 22: Time and space complexity for the finer algorithm

V. Digital audio signal processing

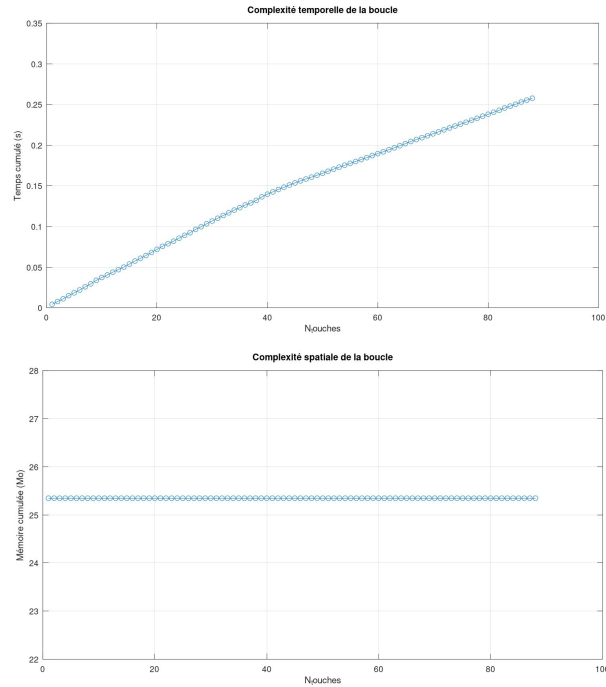


Figure 23: Temporal and spatial complexity for the greedy algorithm

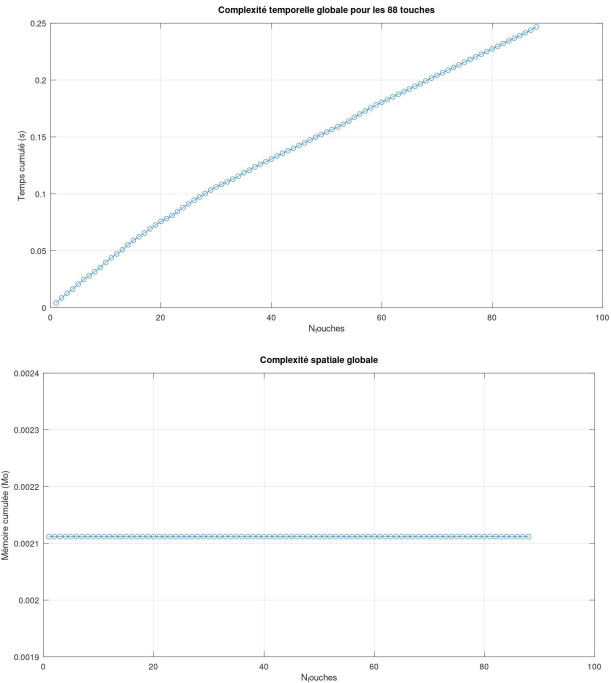


Figure 24: Time and space complexity for the finer algorithm



Beyond Engineering

Thank you for
your time and
attention!