Latches, Flip-Flops, and Registers

By Jake D. Karas

Lab 8 - Latches, Flip-Flops, and Registers

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Objective:

The goal of this lab was to design three key components useful both in general and in the 4-bit CPU. The first of these, the D Latch, stores the previous output state of a section of a logic circuit, updating on a particular input level (0 or 1) of a clock input. A D Flip-Flop, however, functions similar to a D Latch, except for the fact that it only updates on a particular edge (a change in level) of said clock. The D Flip-Flop designed in this lab is negative-edge triggered, meaning that the output updates when the clock input changes from 1 to 0. Lastly, nine D-Flip-Flops were then connected to the same clock, but with separate D inputs and Q outputs. This formation serves as the instruction register for the 4-bit CPU.

Verilog Code:

D Latch:

```
module DLatch(D, En, Q);
input D, En;
output Q;
wire Dbar, T1, T2, Qbar;
not (Dbar, D);
nand (T1, D, En);
nand (T2, Dbar, En);
nand (Q, T1, Qbar);
nand (Qbar, T2, Q);
endmodule
```

D Flip-Flop:

```
module DFlipFlop(D, En, Q);
input D, En;
output Q;
wire EnBar, Y;
not (EnBar, En);
DLatch DL1 (D, En, Y);
DLatch DL2 (Y, EnBar, Q);
endmodule
```

D Flip-Flop Testbench:

```
module DFlipFlop_tb();
wire Q_out;
reg D_in, CLK;

DFlipFlop uut(.Q(Q_out), .D(D_in), .En(CLK));

initial
begin
D_in=1'b0;
CLK=1'b1;
end

always #50 CLK=~CLK;
always #85 D_in=~D_in;

endmodule
```

9-Bit Register:

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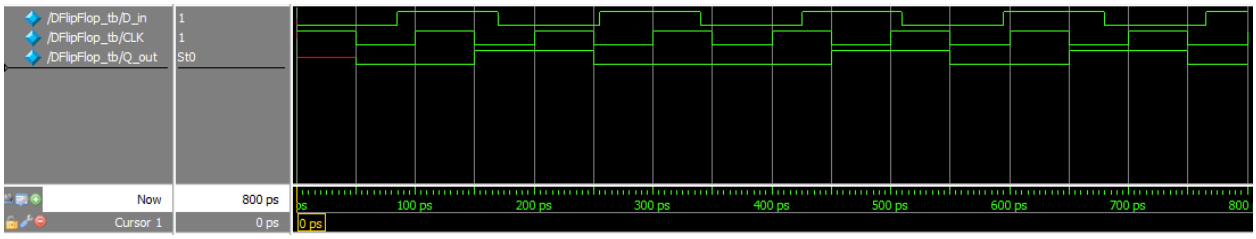
```
1  module NineBitRegister (In, CLK, Out);
2  input[8:0] In;
3  input CLK;
4  output[8:0] Out;
5  DFlipFlop DFF0 (In[0], CLK, Out[0]);
6  DFlipFlop DFF1 (In[1], CLK, Out[1]);
7  DFlipFlop DFF2 (In[2], CLK, Out[2]);
8  DFlipFlop DFF3 (In[3], CLK, Out[3]);
9  DFlipFlop DFF4 (In[4], CLK, Out[4]);
10 DFlipFlop DFF5 (In[5], CLK, Out[5]);
11 DFlipFlop DFF6 (In[6], CLK, Out[6]);
12 DFlipFlop DFF7 (In[7], CLK, Out[7]);
13 DFlipFlop DFF8 (In[8], CLK, Out[8]);
14 endmodule
```

Simulation Waveform:



Discussion:

As demonstrated by the output waveform, the output of the D Flip-Flop designed in this lab is only updated at the negative edge of the clock. When it does update, the output is set to the same state as the D input. This allows logic circuit designers to store a particular signal state as well as delay the timing of when another circuit component receives a state change to synchronize input changes so that don't care states aren't achieved.