Semester project

TTT4201 - Radio System Design and
RF/Microwave Measurement Techniques

This years' semester project will focus on the design of a radio frequency power amplifier based on a packaged, discrete transistor by Wolfspeed. The semester project will consist of two parts: 1) the design of the RF power amplifier with the help of Advanced Design Systems (ADS), and 2) measurements of your designed RF power amplifier at the department's microwave laboratory. At the end of the semester, you are expected to hand in a full report. The report should, as a minimum, include the design process for your design, and a comparison of your simulated and measured results, followed by a discussion and a conclusion. **The length of the report should not exceed 15 pages, including the appendix**. Also, the project report counts for 40 % of the total grade in the course.

1 Device technology and components

Following is a short overview of the device technology you will be using in your design, and some practical considerations you should be aware of.

1.1 Transistor technology

As mentioned, the transistor you will be using in the design is a packaged, discrete transistor by Wolfspeed, CG2H40010 [2]. This device is a powerful 10 W device, which, if matched properly, can deliver as much as 13 W to 15 W when operated in deep compression. The CAD-model for the transistor is provided in Blackboard/Teams. After installation of the CAD-model in ADS [3], you will find the transistor in the **Cree_Wlfspd_ADS_v16p0** library. The name of the component is **CG2H40010F**.

1.2 Microstrip substrate

The substrate you will be using for your printed circuit board (PCB) is a standard FR-4 substrate with parameters as summarized in table 1. These parameters should be entered into the **MSUB** component found in the **TLines-Microstrip** library in ADS. You can ignore the the rest of the parameters in the MSUB component which are not listed in the table (use the default values).

Table 1: Electrical properties for the available FR-4 substrate.

H	Er	Mur	Cond	T	TanD
1.6×10^{-3} m	4.4	1.0	5.96×10^{7}	35×10^{-6} m	0.02

1.3 Passive components

Besides microstrip lines, you will also have to use some passive components, such as resistors, capacitors, or inductors. For the resistors, you can use the standard, ideal resistors found in the **Lumped-Components** library in ADS. During optimization in ADS, you can use continuous values, however, at the department's laboratory you will only have access to surface-mount resistors that come in 0603 and 0805 packages [6], with values according to the E12 series [1].
As for the capacitors and the inductors, you must use the CAD-models provided on Blackboard. These CAD-models describe the behavior of a set of high quality RF capacitors [4, R14S on pp. 2-3] and inductors [5, L-14 on pp. 2] from Johanson Technology, that are available at the laboratory. Again, you may use continuous values for these components during optimization in ADS, but as with the resistors, the capacitors and the inductors are only available in the values given in tables 2 and 3. You **may** use the ideal capacitor model found in the **Lumped Components** library in ADS for

Table 2: Available component values for the R14S capacitors in pico farad.

0.3	0.5	0.8	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.6	3.9	4.7
5.6	6.8	7.5	8.2	9.1	10	12	15	18	20	22	24	27
30	33	36	39	43	47	56	68	82				

decoupling in your bias networks. If you decide to use the ideal capacitors, the part of your biasing network that includes the decoupling capacitors should have a structure like the one depicted in fig. 1 in order to avoid the ideal capacitors short-circuiting everything, making the simulation environment far too idealistic compared what you will experience at the lab. If you have designed a good bias network, the parasitic

Table 3: Available component values for the L-14 inductors in nano henry.

1.0	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
10	12	15	18	22	27	33	39	47	56	68	82
100	120	150	180	220						

effects in the decoupling capacitors (only applies if you use the Johanson capacitors) should not affect the RF performance of your amplifier design.

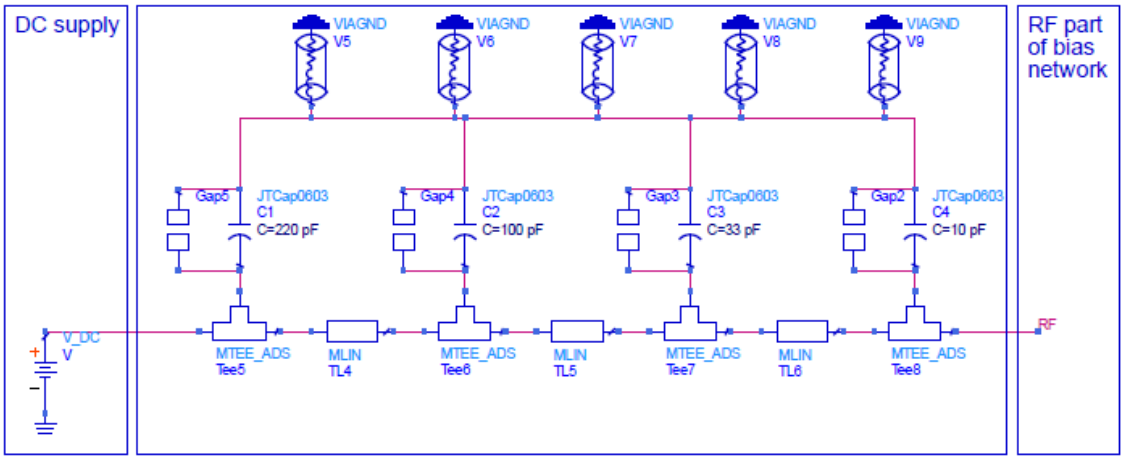

Figure 1: One **possible** arrangement of decoupling capacitors in bias network. If all the (ideal) capacitors are placed at the same node ADS will automatically calculate the equivalent capacitance at that specific node, which will lead to different short-circuiting abilities than what you expect/want. If you have designed your biasing network to present a short circuit/low impedance at DC/baseband frequencies at the node called 'RF' in the figure, you should minimize the distance between the 'RF' node and the decoupling capacitors; e.g., don't add a long line that introduces a phase change.

Before you finalize your design, you **must** select component values for your passive components that correspond to actual component values available at the laboratory. This means that your simulation results *might* change. In some cases, the changes are small and negligible, whereas in other cases you will have to adjust other parts of your circuit to retain the results, i.e. change the impedance of a line (change its width). **If you skip this step, you can end up with measurements that do not correspond with your simulations at all**.

2 Design restrictions and specifications

Your power amplifier design should satisfy a set of predefined design specifications. Some of the values given in the specifications are selected based on experience with the device (from both simulations and measurements), and some are given to make the whole process easier for everyone. Thus, you will discover that some decisions are already made for you, whereas others are left for you to decide.

2.1 Design restrictions

- The frequency of operation (f_c) is 2.4 GHz.
- The device must be biased with a drain voltage (V_D) of 28 V.
- The drain current (I_D) should be no less than 50 mA. This implies that gate voltages (V_G) below approximately −3.0 V cannot be used.

2.2 Small-signal specifications

- The device must be unconditionally stable, e.g. the stability factor (μ) must be greater than unity for all frequencies.
- The small-signal bandwidth (f_{bw}) should be at least 100 MHz within 1dB.
- The small-signal gain (S_{21}) should be at least 14 dB throughout the bandwidth (2.35 GHz to 2.45 GHz).

2.3 Large-signal specifications

2.3.1 Common specifications

- The device should produce an output power (P_{out}) of at least 39 dBm with a maximum single-tone input power (P_{in}) of 27 dBm.
- For a two-tone peak output power of 38 dBm, the intermodulation distortion (IMD) should be as little as possible. The tone spacing should be 5 MHz for the two-tone test.

2.3.2 Target specifications

Each group should target ***either***

- Maximum output power (maximizing P_{out} compared to the common specification) for single tone input.
- Maximum power added efficiency (η_{pae}) for a single-tone input, keeping the common specifications.

3 Layout restrictions

The following restrictions are given to shorten the time of the production process. Producing custom heatsinks for each design is a costly, and time-consuming process, so the goal is to minimize both these factors. Your layout should fit on a 62.5 mm-by-62.5 mm area, as depicted in fig. 2. The bigger circles depicted are the locations of the screw holes in the heat sink plate; these are used for two reasons: 1) provide mechanical stability, and

2) for ensuring a good ground connection. SMA connectors for both RF in and RF out are to be placed at the edge of the circuit board outside the heatsink. An ADS layout of the board will be provided.

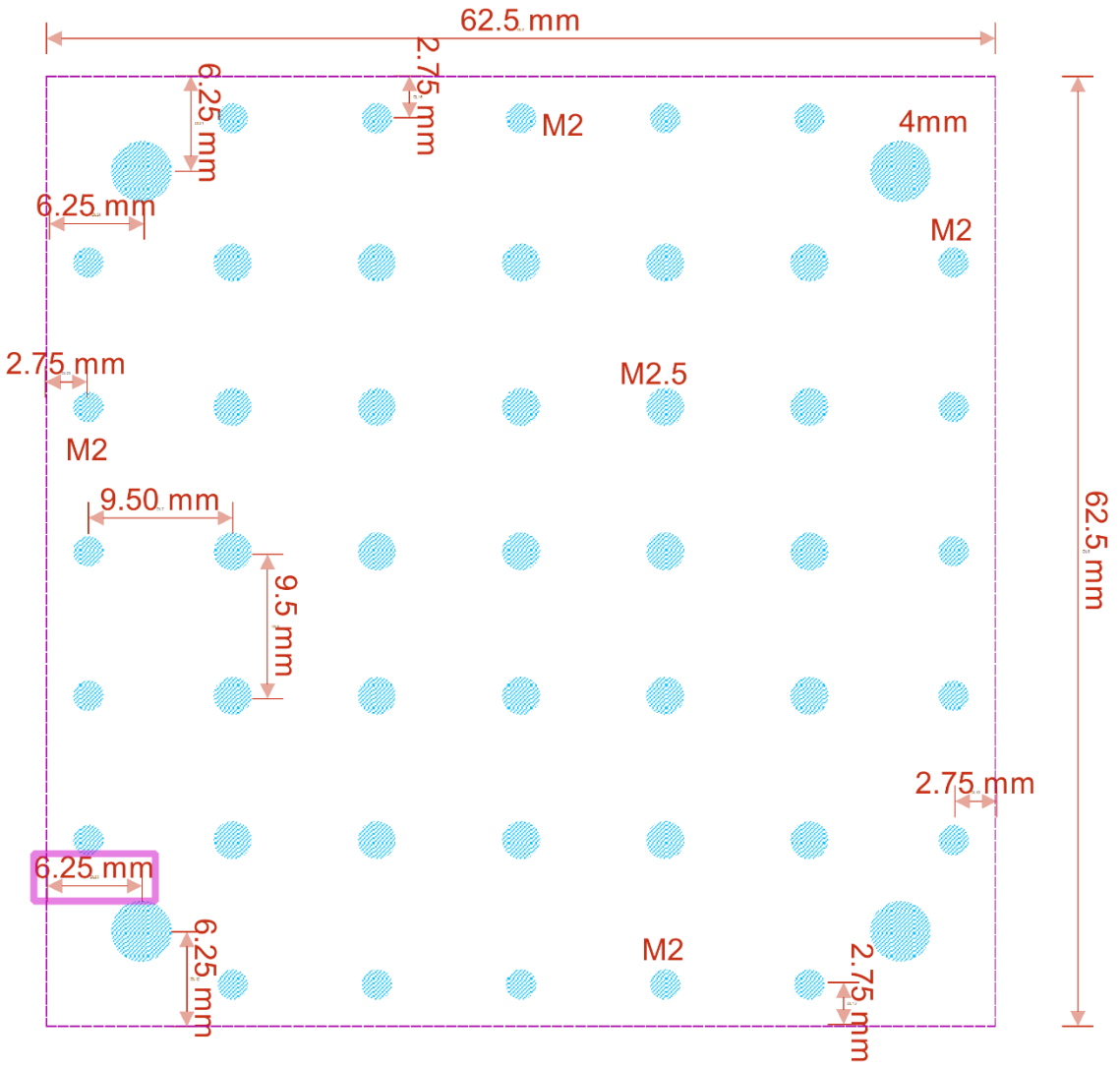

Figure 2: Illustration of heat sink, and the placement of the screw holes. **Note that you only must adjust your layout to agree with the placement of the screw holes for the transistor.**

4 Presentations and design contest

At the end of the semester all the groups should give a **short** presentation of their design and summarize the main results from both simulations and measurements. The best overall design will be awarded after all the presentations are given.

5 Getting started with ADS 201x.xx

5.1 Installing libraries

To install the CAD-tool libraries for the transistor and the passive components (capacitors and inductors), first extract the content of the zip-files provided on Blackboard to a directory on your computer.

5.2 Creating a new workspace

When you have added the library definition files, you may create a new workspace. It is important that you follow **all** the steps in the new workspace wizard. This is because you must include the libraries you just installed in ADS to your new workspace manually, and because you must select a technology, (you should select **Standard ADS Layers, 0.0001 millimeter layout resolution** in order to avoid having to manually change all dimensions in both the circuit schematic and the layout schematic from mils to millimeters).

5.3 DC simulations

In order to determine the bias point of your amplifier design you should run a DC simulation to see how the transistor behaves with different operating voltages. In ADS, there is a design guide available for this, which can be found under the **DesignGuide** menu. Select **Amplifier**->**DC and Bias Point Simulations**->**FET I-V Curves, Class A Power, Eff,....** Another alternative to is set up the simulations by yourself, e.g. as depicted in fig. 3.

5.4 Linear S-parameter simulations

After you have decided the operating point for your amplifier design, the next step is usually to design a biasing network, and evaluate the *S*-parameters of the am plifier. Again there is a design guide available to perform an *S*-parameter simulation. Under the **DesignGuide** menu, select **Amplifier**->**S-Parameter Simulations**->**S-params., Noise Fig., Gain, ...** Alternatively, you can easily set up your own simulation schematic as depicted in fig. 4. To make it easier to navigate in your simulation schematic it is recommended to use sub-designs that you can push into.

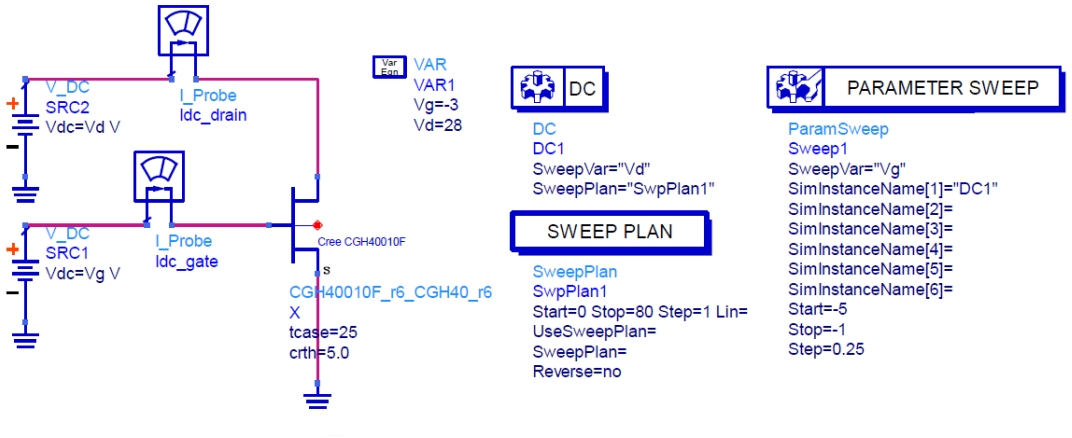

Figure 3: Schematic of DC simulation setup.

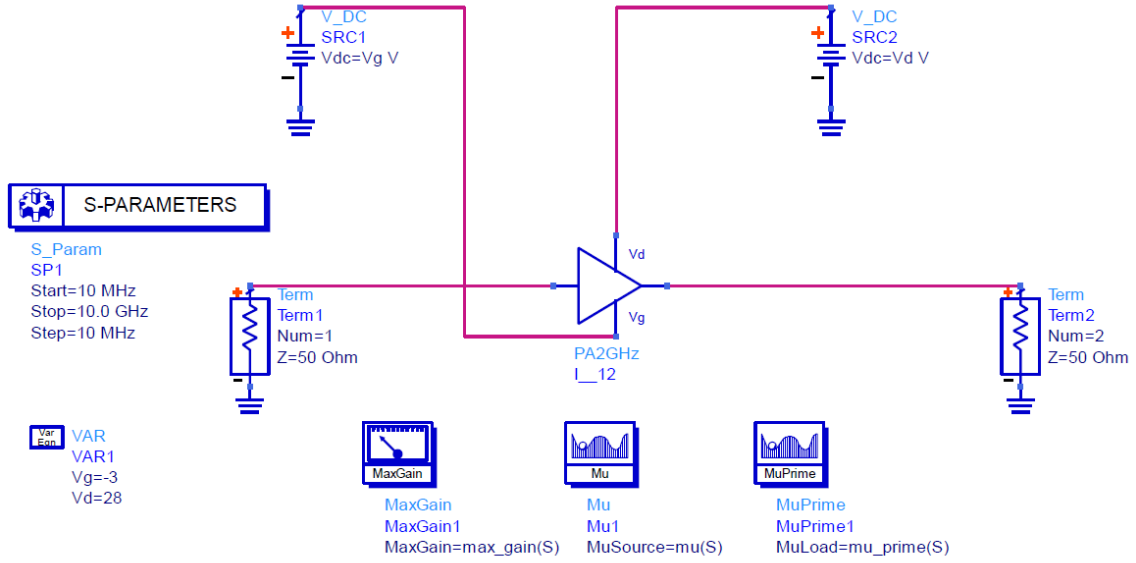

Figure 4: Schematic of *S*-parameter simulation setup.

In fig. 4 the component named **PA2GHz** contains the actual amplifier schematic. If you select the component and then click the **Push Into Hierarchy** button, you will get to the amplifier schematic, e.g., as depicted in fig. 5.

5.5 Nonlinear harmonic balance simulations

To analyze the large signal performance of your amplifier design you have to perform a harmonic balance (or envelope) simulation. There are multiple design guides available for this purpose; some only sweeps the RF power of the input signal at a single frequency; some sweep both the RF power and the frequency of the input signal to allow you to verify the performance over a larger bandwidth. These design guides can be found under the **DesignGuide** menu. Select an appropriate

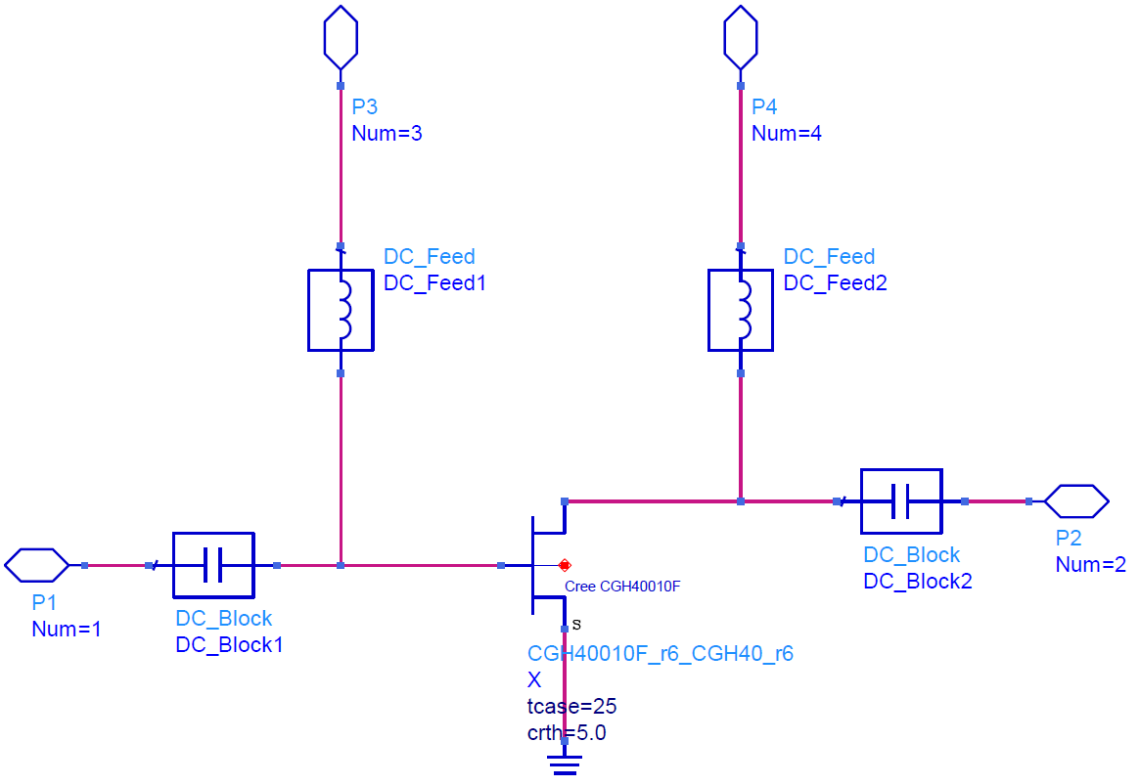

Figure 5: Amplifier schematic using ports to allow for a hierarchical structure.

guide from **Amplifier->1-Tone Nonlinear Simulations**. For the semester project it suffices to use the guide named **Spectrum, Gain, Harmonic Distortion vs. Power (w/PAE)** for 1-tone simulations, and the guide named **Spectrum, Gain, TOI, and 5thOI Points vs. Power (w/PAE)** under **2-Tone Nonlinear Simulations** for the 2-tone simulations.
Alternatively, you can setup your own simulation test bench as depicted in fig. 6. To be able to plot data from the schematic window in the data display window you have to define **Measurement equations** inside the **MeasEqn**-components. Node voltages are accessed by giving the node a name. This can be done pushing the **Insert Wire/Pin Label** button (next to the **Insert Wire**-button). To access currents you must place a current probe at the desired location. Both node voltages and current probes save data for all simulated frequencies including their harmonic frequencies (up to and including the order you have specified in the harmonic balance simulator). To use the data for harmonic frequency n at node X, you must specify $X[n]$ in your equation (for current probes you must use $X.i[n]$). It is also possible to define the same equations inside the data display window, but here you have to pay respect to the dimensions of the simulated data. E.g., if you have performed a power sweep with 20 different points, and specified the maximum order to be $N = 8$, you will notice that a node voltage X will have dimensions 20×9 (including DC). Thus, to plot the magnitude of the second harmonic voltage vs. the input power you will have to specify an equation similar to **plot_vs(mag(X[::,2]),RFpower)**.
By defining measurement equations in the schematic window, you can easily export the data to Matlab for further analysis by using the **MatlabOutput** component (located under **Simulation-HB**).

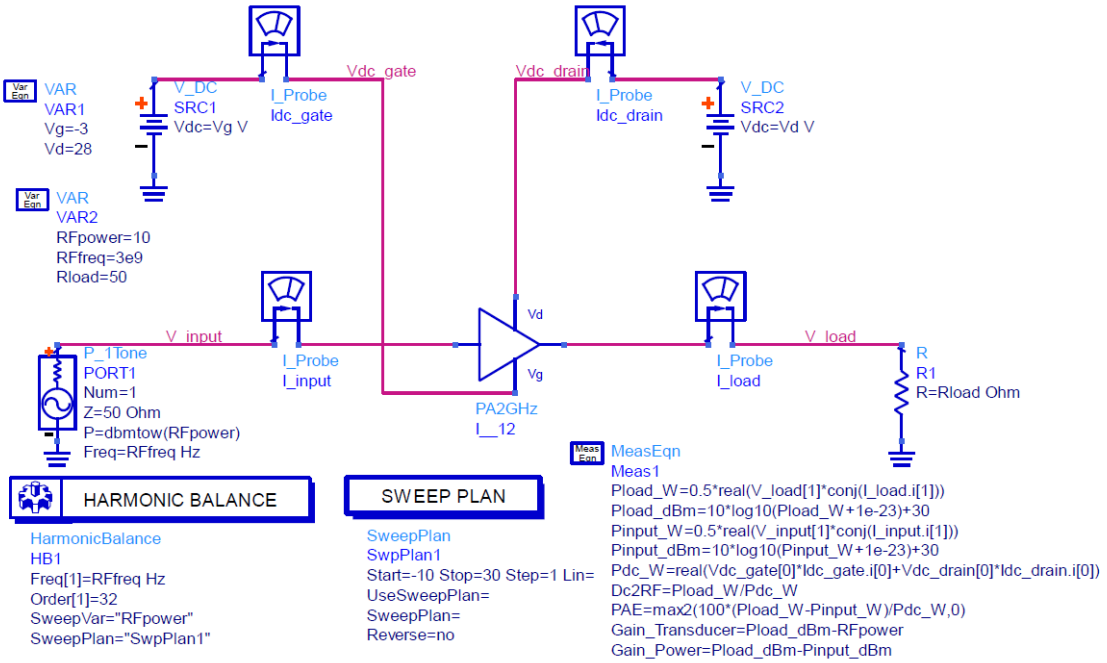

Figure 6: Schematic of harmonic balance simulation setup.

6 Measurements

At the lab you will measure both the small-signal and the large-signal response of your amplifier.

6.1 Small-signal measurements

The small-signal characterization is performed with a vector network analyzer (VNA) that allows you to save the S-parameters for your device. For this measurement, it is **very important** that you use a coupler and an attenuator at the output of your amplifier in order to protect the instrument from too large output signals (e.g., in case your device oscillates). Hence, in order to get accurate measurements you will have to calibrate the VNA with the coupler and the attenuator attached to port 2. Attaching these two components will introduce a total attenuation of approximately X dB in each direction, implying that the signals for your $\boldsymbol{S}_{22}$ measurement will be attenuated with about $2X$ dB. Thus, the accuracy of your $\boldsymbol{S}_{22}$ measurement may not be as good as for e.g. $\boldsymbol{S}_{11}$ or $\boldsymbol{S}_{21}$. To improve the accuracy it is possible to reduce the IF filter bandwidth before calibration, at the cost of an increased sweep time.

6.2 Large-signal measurements

The large-signal characterization is performed with a vector signal generator (VSG) and a spectrum analyzer. The VSG can output a single-tone signal with a peak envelope power (PEP) of 27 dBm, and a two-tone signal with a PEP of 23 dBm. These limitations in the VSG requires you to use a driver amplifier (available at the lab) to amplify the signals from the VSG in order to be able to drive your amplifier into compression. The measurement setup for the large-signal measurements is as illustrated in fig. 7. In order to characterize your amplifier, you will first have to measure all the passive losses in the measurement setup, and the driver amplifier. The passive losses (components in green boxes in the illustration) can be characterized with a VNA, whereas the driver amplifier must be characterized with the VSG and the spectrum analyzer. Before you compare the measured and simulated

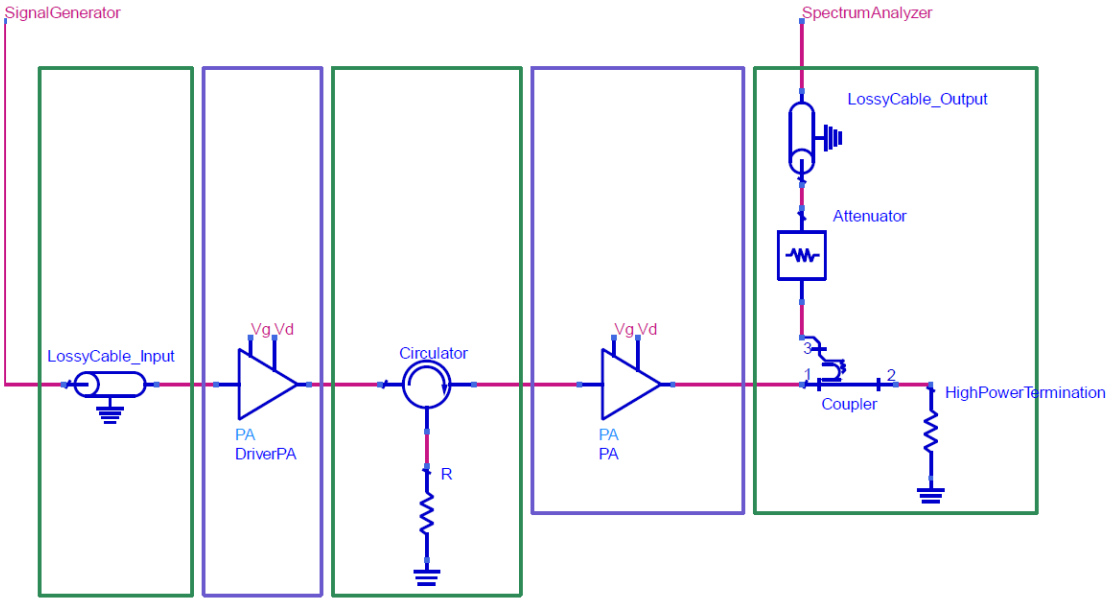

Figure 7: Schematic of large signal measurement setup.

data for your amplifier you will have to correct the measured data so you evaluate it at the correct reference plane. This means that the input power of your amplifier will not be the same as the power generated by the VSG, but the output power of the driver amplifier plus the passive loss in the circulator at the measurement frequency. In the same manner the output power of your device will be the power measured by the spectrum analyzer minus the passive losses between your amplifier and the spectrum analyzer.

References

[1] AnaLog. *Standard EIA Decade Resistor Values Table*. 2010. http://www.logwell.com/tech/components/resistor_values.html (visited on 24/01/2018).

[2] Wolfspeed. *CG2H40010 Rev 1.4 – June 2021*. https://d3rx8y505vv2z0.cloudfront.net/uploads/2020/12/CG2H40010.pdf

[3] Agilent Technologies. *Advanced Design System Software*.

[4] Johanson Technology. *Multi-Layer High-Q Capacitors*. 2012. http://www.johansontechnology.com/images/stories/catalog/JTI_CAT_2012_MLCC_HighQ.pdf (visited on 01/21/2013).

[5] Johanson Technology. *RF Ceramic Chip Inductors*. 2012. http://www.johansontechnology.com/images/stories/rf-inductors/cci/JTI_CAT_2012_Inductors_Chip.pdf (visited on 01/21/2013).

[6] Wikipedia. *Surface-mount technology*. 2013.

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