Diego A. Méndez
19673

Tabla 1
Mux8 a 1

ABC	Y
VCD info: c	
000	0
001	1
010	1
011	0
100	1
101	0
110	0
111	1

Tabla 1
Mux4 a 1

ABC	Y
000	0
001	1
010	1
011	0
100	1
101	0
110	0
111	1

Tabla 1
Mux2 a 1

ABC	Y
000	0
001	1
010	1
011	0
100	1
101	0
110	0
111	1

Tabla 2
Mux8 a 1

ABC	Y
000	1
001	0
010	0
011	0
100	0
101	1
110	1
111	0

Tabla 2
Mux4 a 1

ABC	Y
000	1
001	0
010	0
011	0
100	0
101	1
110	1
111	0

Tabla 1
Mux2 a 1

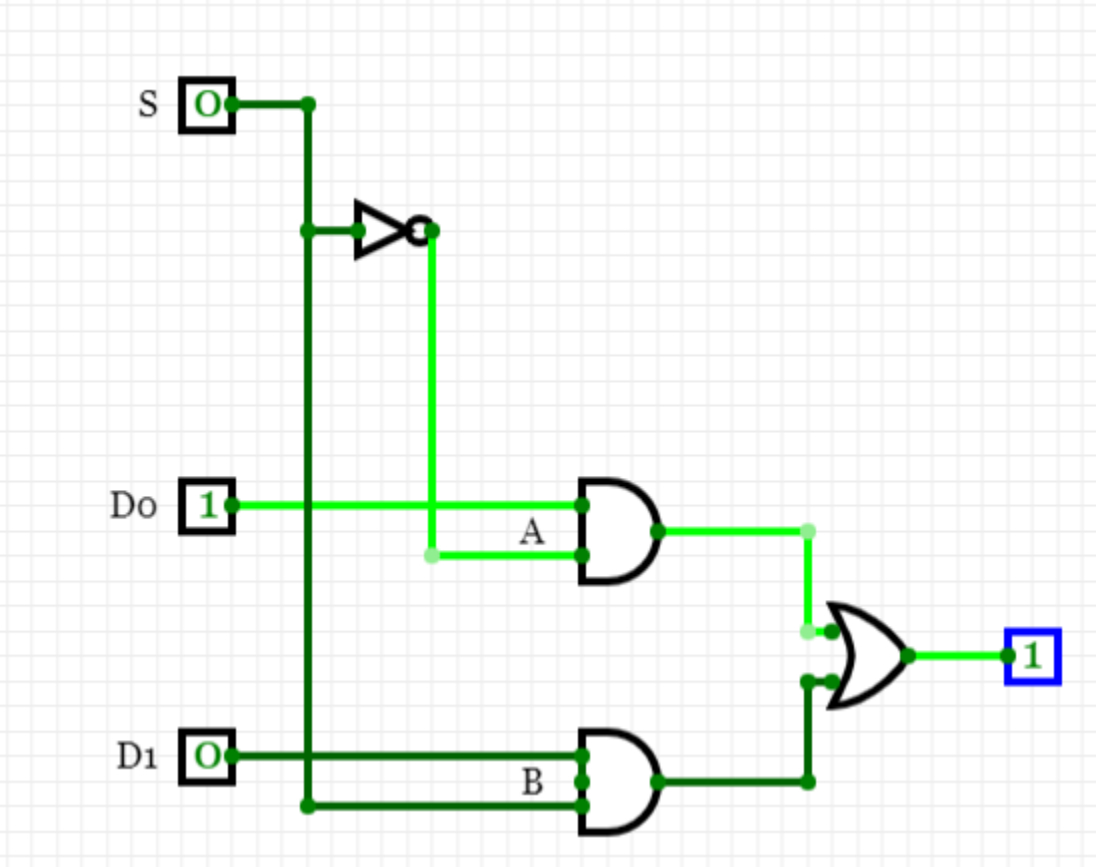
ABC	Y
000	1
001	0
010	0
011	0
100	0
101	1
110	1
111	0

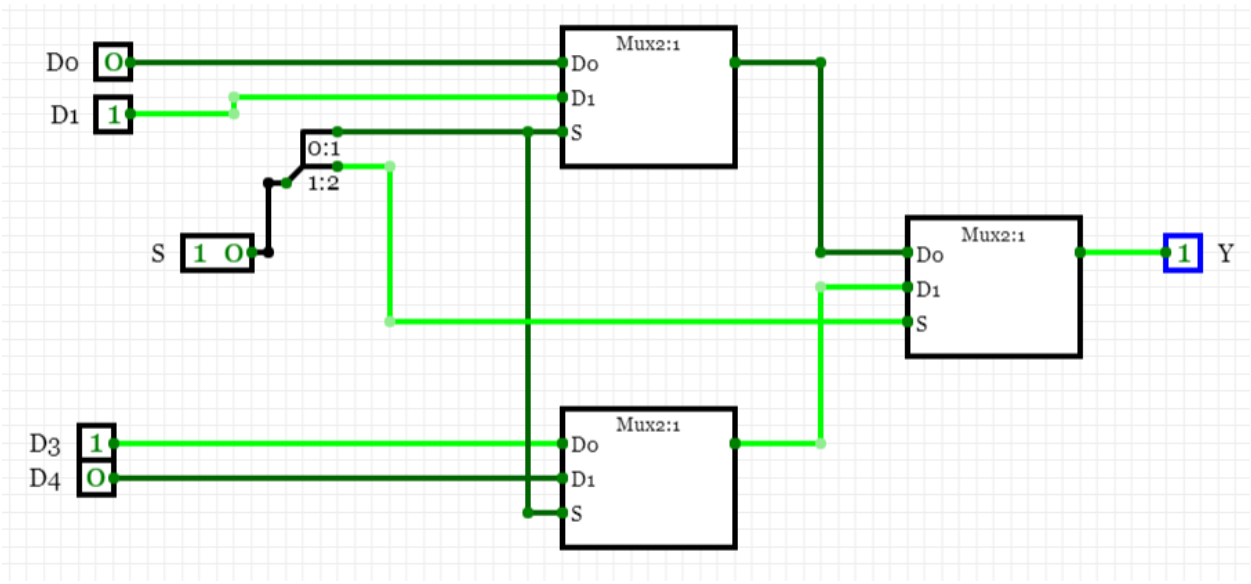
```
//Diego A. Méndez
//19673
//Ejercicio 04

module mux2_1(input wire inA, inB, inS, output wire Y);

  assign Y=inS?inB:inA;

endmodule

module mux4_1(input wire inA, inB, inC, inD, input wire[1:0] inS, output wire Y);
//Creacion de un mux 4 a 1 basado
  wire Y1, Y2;
  mux2_1 U1(inA, inB, inS[0], Y1);
  mux2_1 U2(inC, inD, inS[0], Y2);
  mux2_1 U3(Y1, Y2, inS[1], Y);

endmodule


module mux8_1(input wire inA, inB, inC, inD, inE, inF, inG, inH, input wire[2:0] inS, output wire Y);
//Creacion de un mux 8 a 1 basado
  wire Y1, Y2;
  mux4_1 U1(inA, inB, inC, inD, inS[1:0], Y1);
  mux4_1 U2(inE, inF, inG, inH, inS[1:0], Y2);
  mux2_1 U3(Y1, Y2, inS[2], Y);
```

```
module tabla1mux8(input wire[2:0] inS, output wire Y);
//modulo para mux 8 tabla 1

//registrar cables
  wire inA1, inB1, inC1, inD1, inE1, inF1, inG1, inH1;

//asignar valores
  assign inA1=0; assign inB1=1; assign inC1=1; assign inD1=0;
  assign inE1=1; assign inF1=0; assign inG1=0; assign inH1=1;

  mux8_1 U1(inA1, inB1, inC1, inD1, inE1, inF1, inG1, inH1, inS, Y);
endmodule


module tabla1mux4(input wire inC, input wire[1:0] inS, output wire Y);
  //aplicando la primera tabla con un mux4a1 y compuertas
  wire NC;

  not N1(NC,inC);
// la compuerta not nos sirve para trabajar unicamente con una entrada C y el mux 4
  mux4_1 U1(inC,NC,NC,inC,inS, Y);
endmodule
```

```
module tabla1mux2(input wire inS, inB, inC, output wire Y);
//aplicacion de mux2 en tabla1
  wire Y1, Y2;

  assign Y1= inB ^ inC ;
  assign Y2= inB ~^ inC;

  mux2_1 U1(Y1, Y2, inS, Y);


endmodule

//Tabla2

module tabla2mux8(input wire[2:0] inS, output wire Y);
//modulo para mux 8 tabla 2

//registrar cables
  wire inA1, inB1, inC1, inD1, inE1, inF1, inG1, inH1;

//asignar valores
  assign inA1=1; assign inB1=0; assign inC1=0; assign inD1=0;
  assign inE1=0; assign inF1=1; assign inG1=1; assign inH1=0;

  mux8_1 U1(inA1, inB1, inC1, inD1, inE1, inF1, inG1, inH1, inS, Y);
endmodule
```

```
module tabla2mux4(input wire inC, input wire[1:0] inS, output wire Y);
  //aplicando la segunda tabla con un mux4a1 y compuertas
  wire NC, P;
  assign P=0;
  not N1(NC,inC);
// la compuerta not nos sirve para trabajar unicamente con una entrada C y el mux 4
  mux4_1 U1(NC,P,inC,NC,inS, Y);
endmodule

module tabla2mux2(input wire inS, inB, inC, output wire Y);
//aplicacion de mux2 en tabla1
  wire Y1, Y2;

  assign Y1= inB ~| inC ;
  assign Y2= inB ^ inC;

  mux2_1 U1(Y1, Y2, inS, Y);


endmodule
```




D0
0
D1
1
0:1
1:2
S
1 0
Mux2:1
D0
D1
S
Mux2:1
D0
D1
S
1
Y
Mux2:1
D0
D1
S
D3
1
D4
0

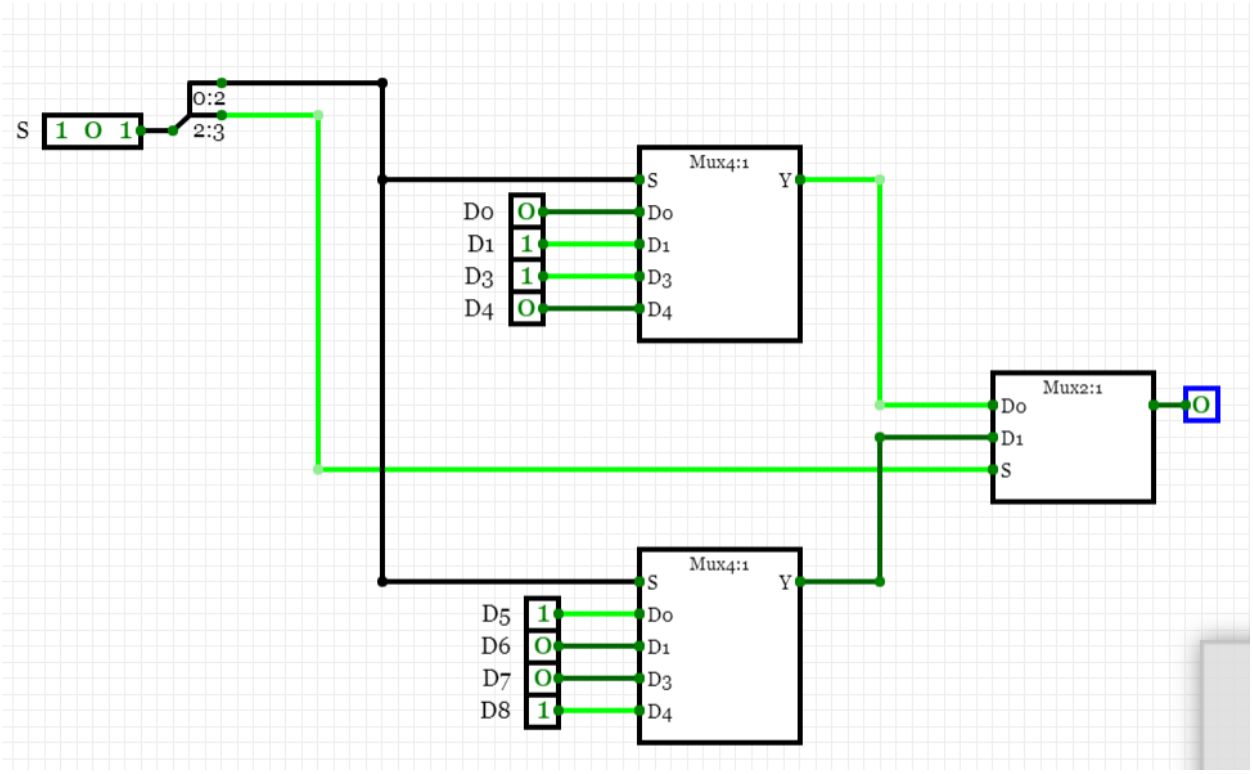

S
1 0 1
0:2
2:3
Mux4:1
S
Y
D0
0
D1
1
D3
1
D4
0
D0
D1
D3
D4
Mux2:1
D0
D1
S
0
Mux4:1
S
Y
D5
1
D6
0
D7
0
D8
1
D0
D1
D3
D4

Tabla 01

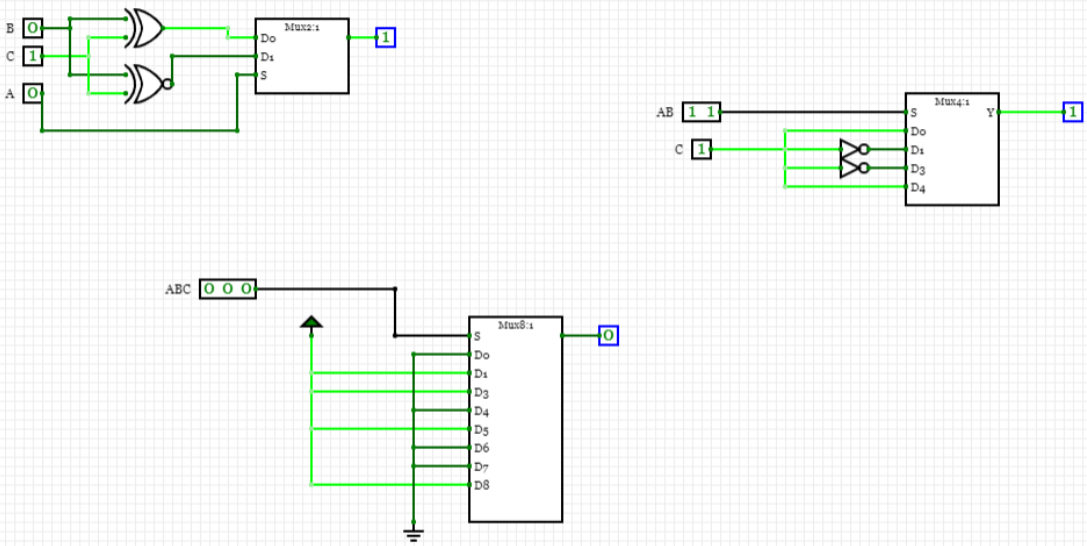
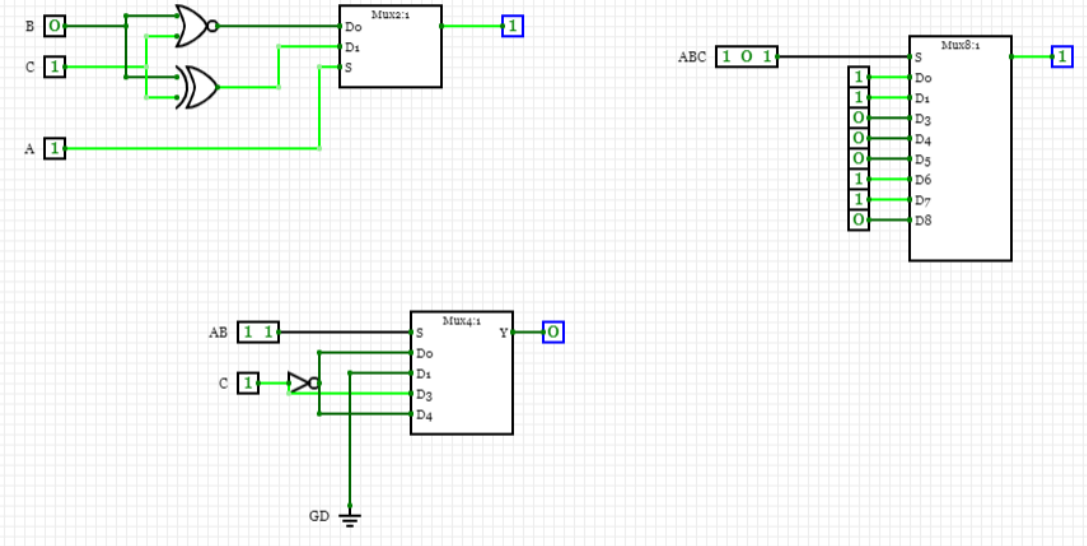
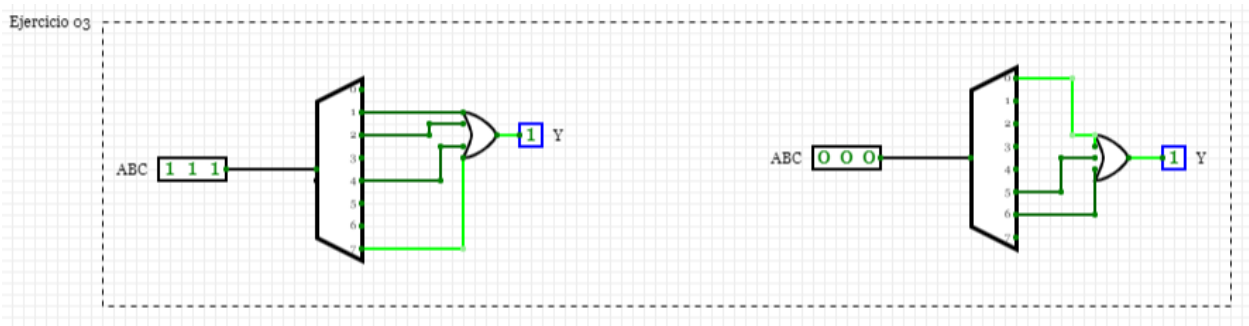


Tabla 02




Ejercicio 03
ABC
1 1 1
1
Y
ABC
0 0 0
1
Y

```
//Diego A. Méndez
//19673
//Testbench

module testbench();
// registrar entradas

  reg inC2;
  reg inB3, inC3;
  reg inC5;
  reg inB6, inC6;


  reg[2:0] inS1, inS4;
  reg[1:0] inS2, inS5;
  reg inS3, inS6;
  wire Y1, Y2, Y3, Y4, Y5, Y6;

  //Llamando a los modulos
    tabla1mux8 U1(inS1, Y1);
    tabla1mux4 U2(inC2, inS2, Y2);
    tabla1mux2 U3(inS3, inB3, inC3 ,Y3);
    tabla2mux8 U4(inS4, Y4);
    tabla2mux4 U5(inC5, inS5, Y5);
    tabla2mux2 U6(inS6, inB6, inC6, Y6);
```

```
initial begin //iniciamos el mux8_1
  $display(" ");
  $display(" Tabla 1 ");
  $display("Mux8 a 1");
  $display("ABC | Y");
  $display("----------");
  $monitor("%b | %b",inS1 ,Y1);

      inS1=000;
    #1 inS1=001;
    #1 inS1=010;
    #1 inS1=011;
    #1 inS1=100;
    #1 inS1=101;
    #1 inS1=110;
    #1 inS1=111;
    end
```

```
initial begin //iniciamos el mux8_1
#8
    $display(" ");
    $display(" Tabla 1 ");
    $display("Mux4 a 1");
    $display("ABC | Y");
    $display("----------");
    $monitor("%b%b | %b",inS2, inC2 ,Y2);
         inS2=00; inC2=0;
      #1 inS2=00; inC2=1;
      #1 inS2=01; inC2=0;
      #1 inS2=01; inC2=1;
      #1 inS2=10; inC2=0;
      #1 inS2=10; inC2=1;
      #1 inS2=11; inC2=0;
      #1 inS2=11; inC2=1;
      end
```

```
initial begin //iniciamos el mux8_1
#16
    $display(" ");
    $display(" Tabla 1 ");
    $display("Mux2 a 1");
    $display("ABC | Y");
    $display("----------");
    $monitor("%b%b%b | %b",inS3, inB3, inC3 ,Y3);
         inS3=0; inB3=0; inC3=0;
      #1 inS3=0; inB3=0; inC3=1;
      #1 inS3=0; inB3=1; inC3=0;
      #1 inS3=0; inB3=1; inC3=1;
      #1 inS3=1; inB3=0; inC3=0;
      #1 inS3=1; inB3=0; inC3=1;
      #1 inS3=1; inB3=1; inC3=0;
      #1 inS3=1; inB3=1; inC3=1;
      end
```

```
initial begin //iniciamos el mux8_1
#25
  $display(" ");
  $display(" Tabla 2 ");
  $display("Mux8 a 1");
  $display("ABC | Y");
  $display("----------");
  $monitor("%b | %b",inS4 ,Y4);

      inS4=000;
    #1 inS4=001;
    #1 inS4=010;
    #1 inS4=011;
    #1 inS4=100;
    #1 inS4=101;
    #1 inS4=110;
    #1 inS4=111;
    end
```

```
initial begin //iniciamos el mux8_1
#33
    $display(" ");
    $display(" Tabla 2 ");
    $display("Mux4 a 1");
    $display("ABC | Y");
    $display("----------");
    $monitor("%b%b | %b",inS5, inC5 ,Y5);
        inS5=00; inC5=0;
      #1 inS5=00; inC5=1;
      #1 inS5=01; inC5=0;
      #1 inS5=01; inC5=1;
      #1 inS5=10; inC5=0;
      #1 inS5=10; inC5=1;
      #1 inS5=11; inC5=0;
      #1 inS5=11; inC5=1;
      end
```

```
initial begin //iniciamos el mux8_1
#41
    $display(" ");
    $display(" Tabla 1 ");
    $display("Mux2 a 1");
    $display("ABC | Y");
    $display("----------");
    $monitor("%b%b%b | %b",inS6, inB6, inC6 ,Y6);
        inS6=0; inB6=0; inC6=0;
      #1 inS6=0; inB6=0; inC6=1;
      #1 inS6=0; inB6=1; inC6=0;
      #1 inS6=0; inB6=1; inC6=1;
      #1 inS6=1; inB6=0; inC6=0;
      #1 inS6=1; inB6=0; inC6=1;
      #1 inS6=1; inB6=1; inC6=0;
      #1 inS6=1; inB6=1; inC6=1;
      end
```

```
  initial

  #49 $finish;

initial begin

    $dumpfile("Ejercicio4_tb.vcd");
    $dumpvars(0,testbench);
end

endmodule
```