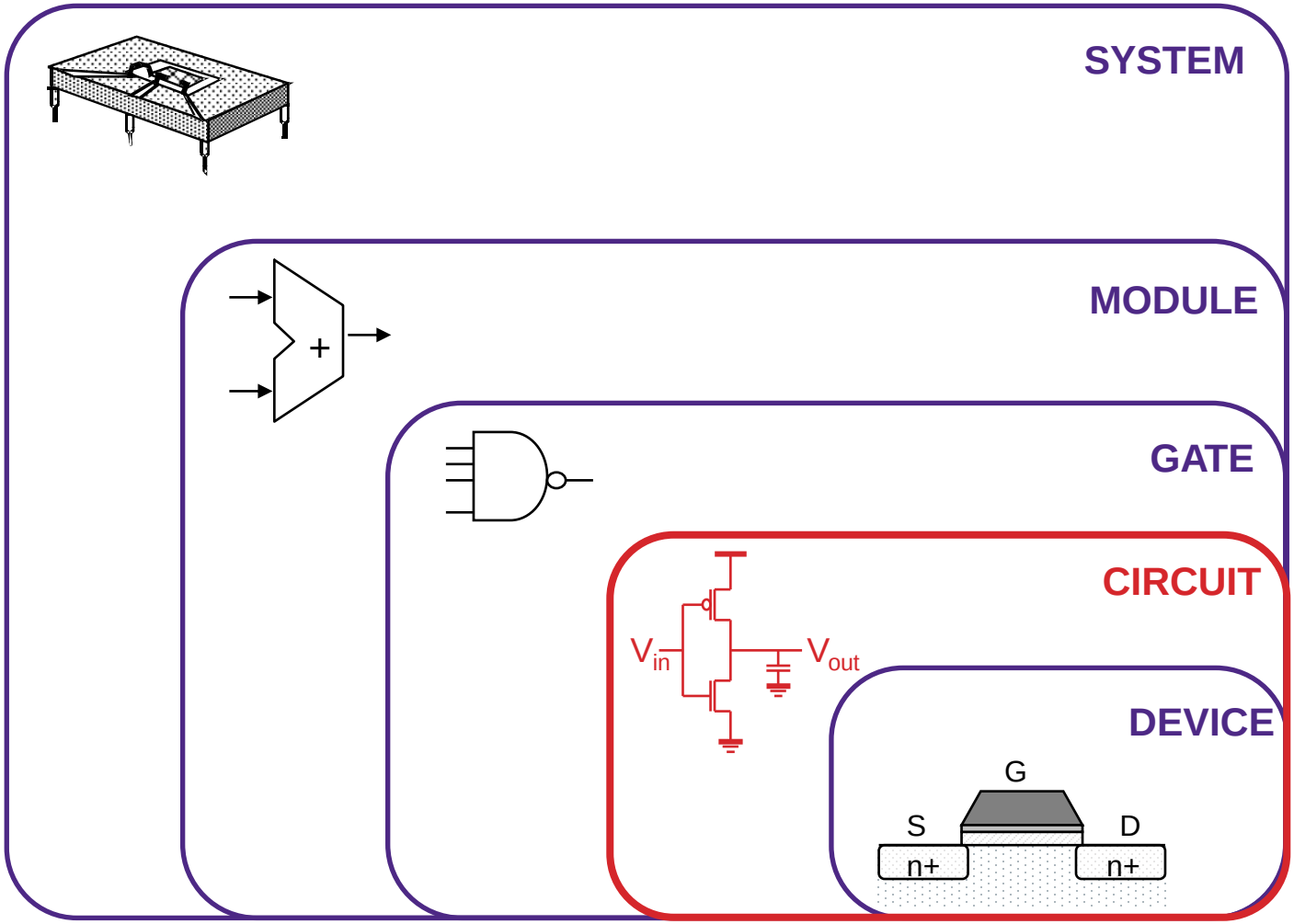
Budapest University of Technology and Economics
Department of Electron Devices

Microelectronics, BSc course

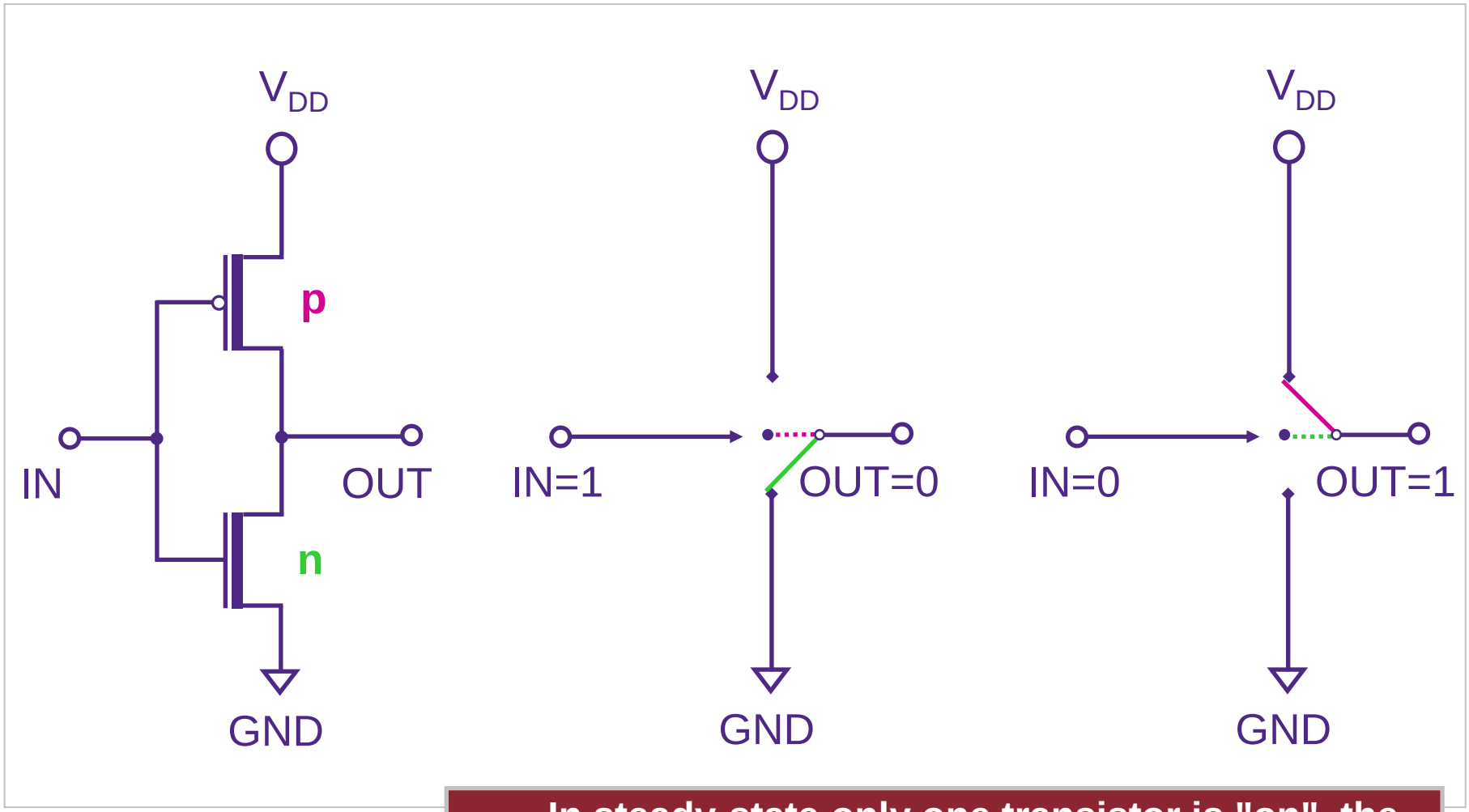
nMOS/CMOS Logic Gates II:

Schematic, layout, x-section, std cells

The abstraction level of our study:

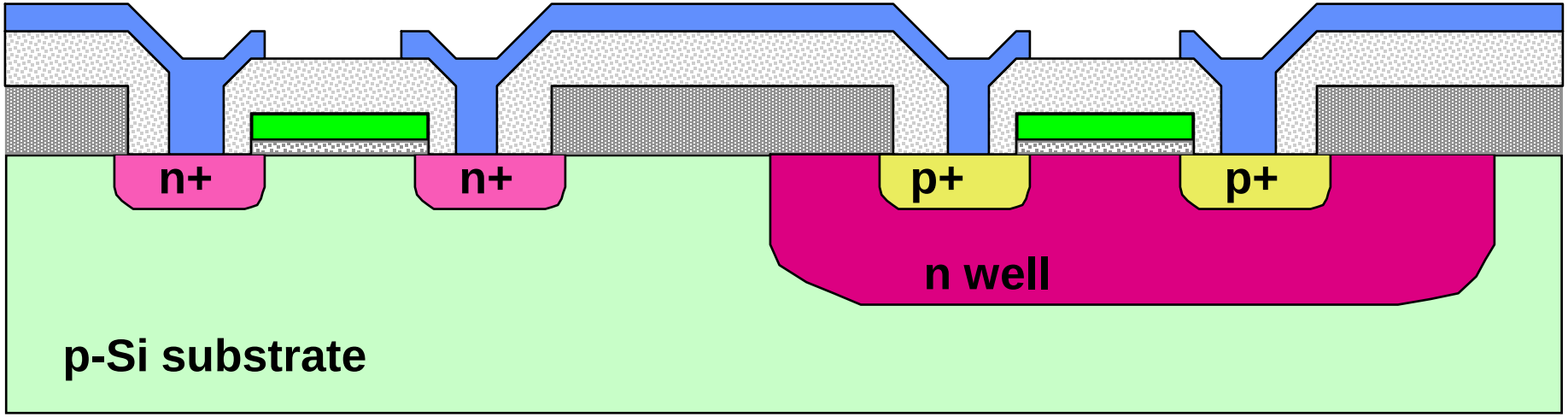


The CMOS inverter – recall



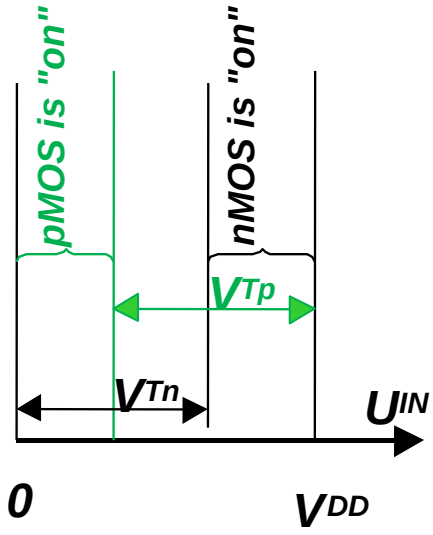
In steady-state only one transistor is "on", the other one is always "off"

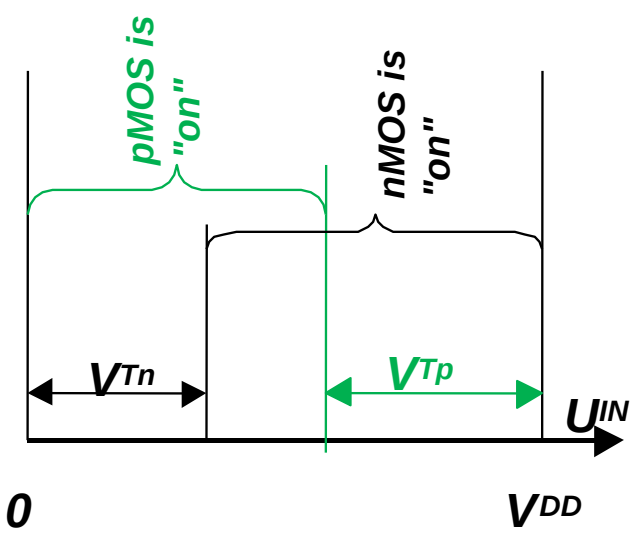
X-sectional view of a CMOS inverter

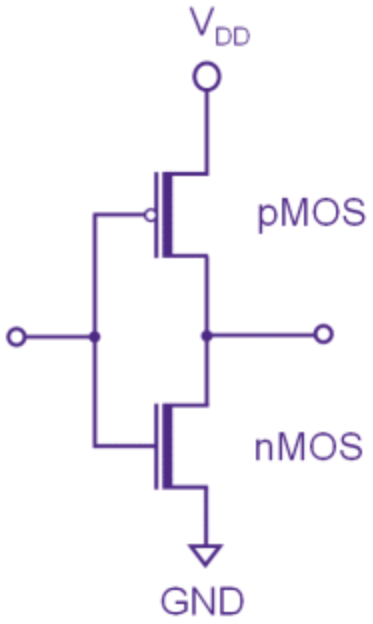


Characteristic of the CMOS inverter

2 basic cases, depending on the supply voltage and threshold voltages of the transistors







1. small supply voltage:

$$V_{DD} < V_{Tn} + |V_{Tp}|$$

only one transistor is "on" at a time

2. larger supply voltage:

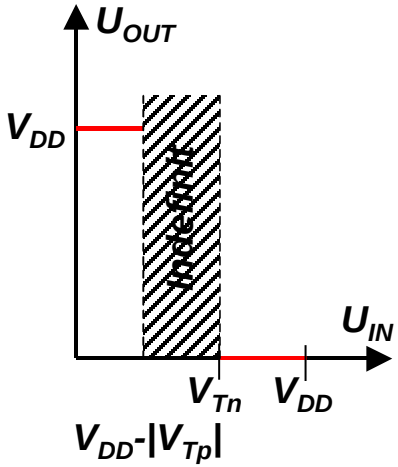
$$V_{DD} > V_{Tn} + |V_{Tp}|$$

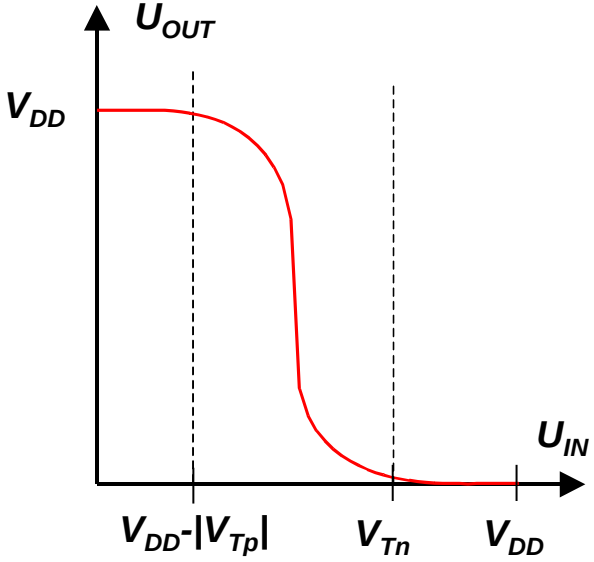
when switching over, both transistors are "on" at the same time

Characteristic of the CMOS inverter

- 1. small supply voltage: $V_{DD} < V_{Tn} + |V_{Tp}|$

the characteristics: $U_{OUT} = \begin{cases} V_{DD} & \text{if } \ldots\ldots\ldots\ldots\ldots\ldots U_{IN} < V_{DD} - |V_{Tp}| \\ \text{indefinit} & \text{if } \ldots\ldots\ldots\ldots V_{Tn} < U_{IN} < V_{DD} - |V_{Tp}| \\ 0 & \text{if } \ldots\ldots\ldots\ldots\ldots\ldots U_{IN} > V_{Tn} \end{cases}$





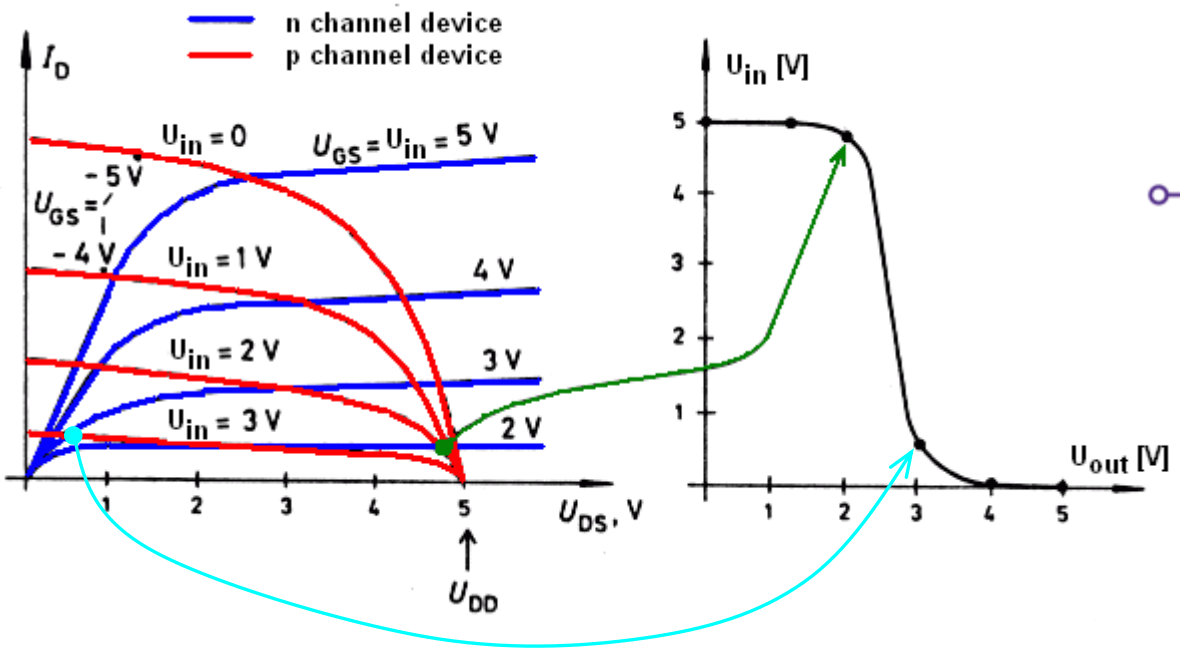
The middle part of the transfer characteristic is very steep, this is the specific advantage of CMOS inverters.

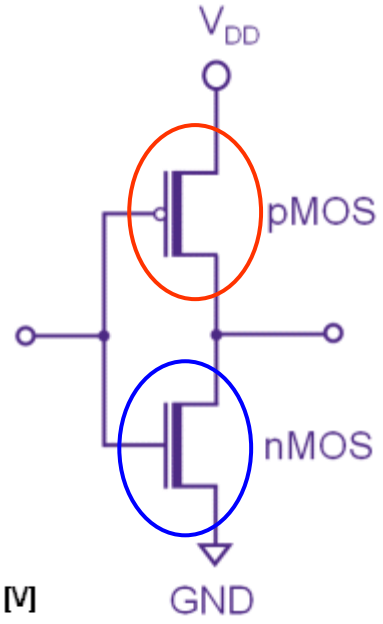
Characteristic of the CMOS inverter

- 2. large supply voltage: $V_{DD} > V_{Tn} + |V_{Tp}|$

  Switching over? - "mutual conduction"

▶ Constructing the characteristic:





The CMOS inverter

Design for symmetrical operation:

If $U_{IN}=U_{inv}$ logic threshold voltage, both transistors have equal current:

$$K_n(U_{inv}-V_{Tn})^2 = K_p(U_{DD}-U_{inv}-|V_{Tp}|)^2$$

$$U_{inv} = \frac{U_{DD}-|V_{Tp}|+V_{Tn}\sqrt{K_n/K_p}}{1+\sqrt{K_n/K_p}}$$

$$K_X = \left(\frac{W}{L}\right)_X \frac{\mu_X C_{ox}}{2}$$

$U_{GSn}=U_K$

$U_{GSp}=V_{DD}-U_K$

The inverter logic threshold voltage depends on the ratio of the current constants of the transistors.
To have U_{inv} at $V_{DD}/2$ and $V_{Tn}=|V_{Tp}|$, then $K_n=K_p$ has to be set.

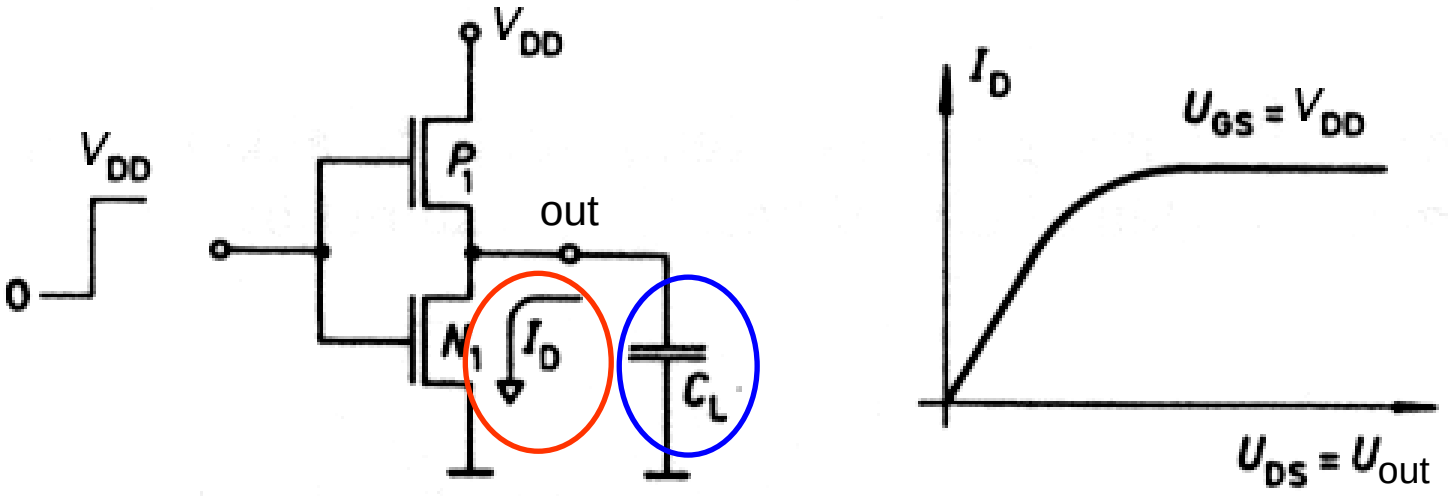
$$\left(\frac{W}{L}\right)_P = 2..2.5\times\left(\frac{W}{L}\right)_n$$

since hole mobility is 2 ... 2.5 times less

The logic threshold voltage can be set by the W/L ratios

The CMOS inverter / dynamic char.

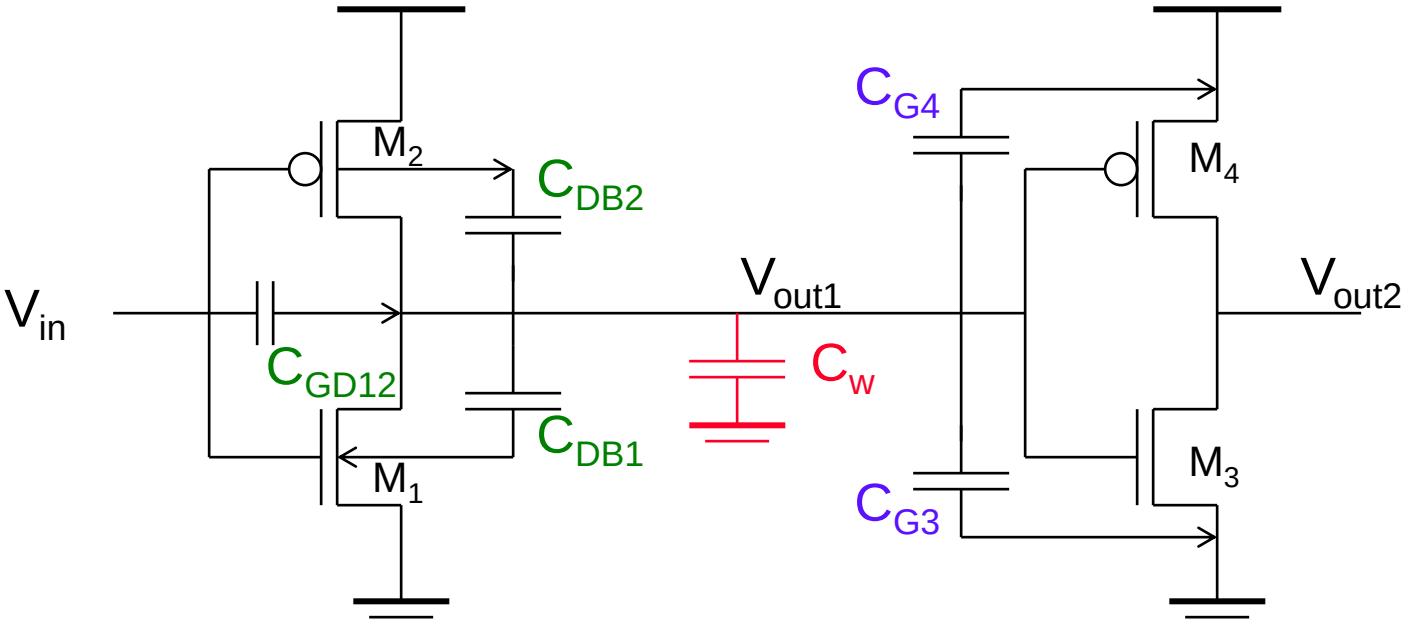
- Calculation of the switching times
  - What do they depend on?
    - the current driving capability of the output
    - the capacitive load on the output



- If the characteristics of the two transistors are exactly complementary ($K_n=K_p$ and $V_{Tn}=|V_{Tp}|$), rising and falling times will be equal

The capacitances

- Intrinsic capacitances of the driving stage
- Input capacitance of the loading stage (next gate) – extrinsic or fanout capacitances
- wiring (interconnect) capacitance

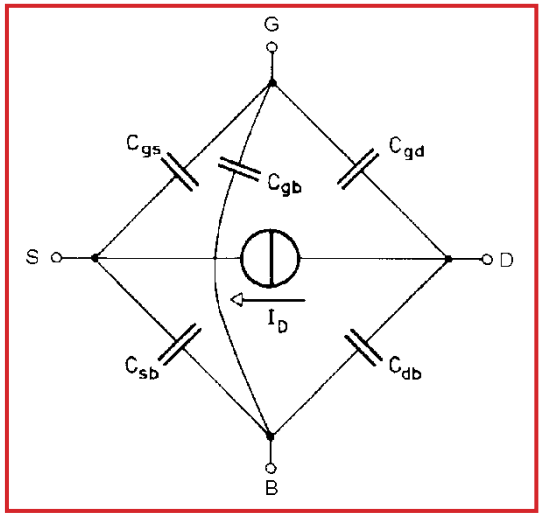


intrinsic MOS transistor capacitances

extrinsic MOS transistor (fanout) capacitances

wiring (interconnect) capacitance

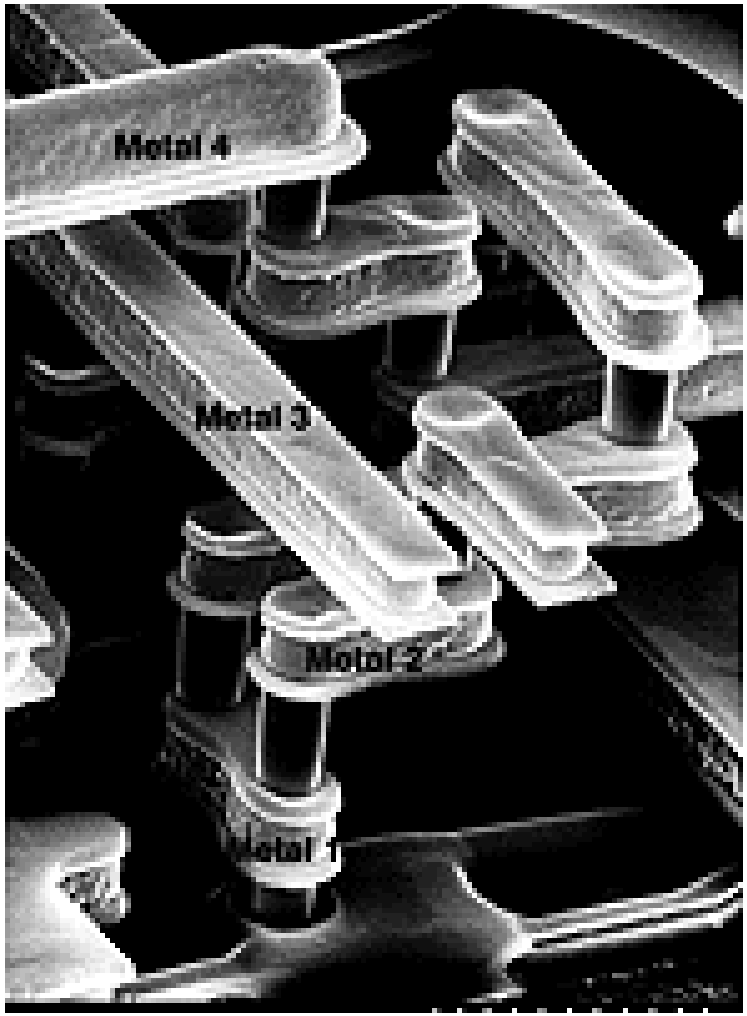
The capacitances

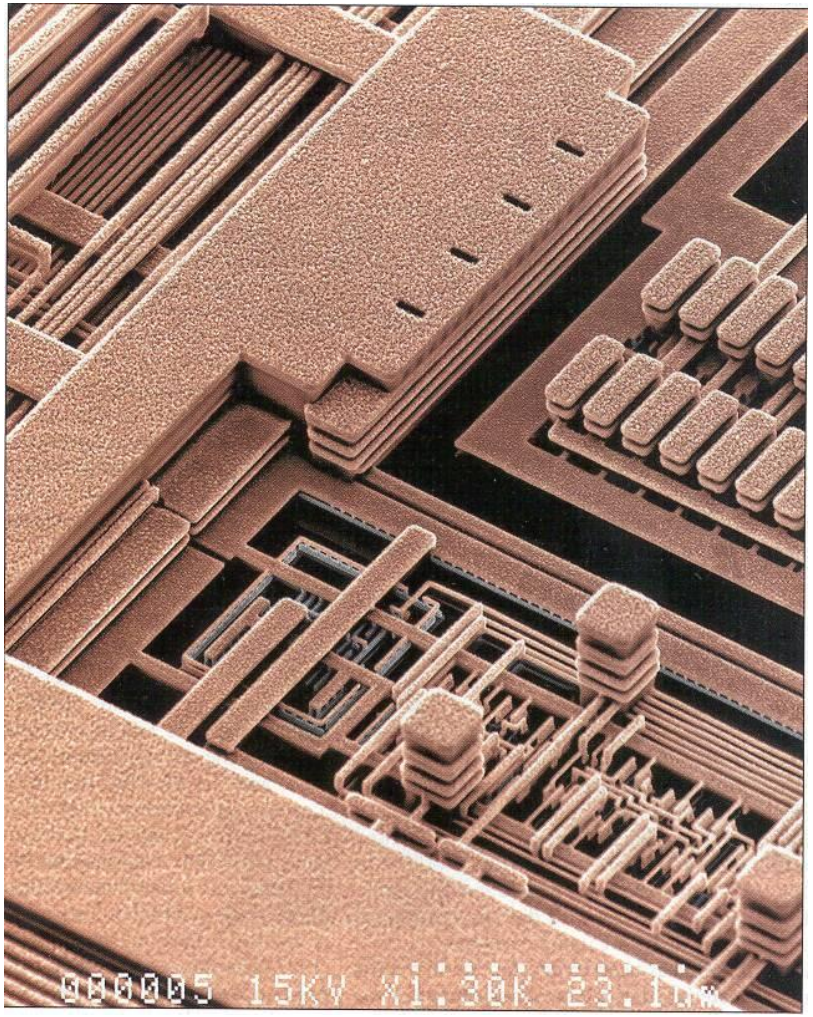


- The intrinsic capacitances:
  - S-G G-D overlap capacitances
  - the MOS capacitance of the channel
  - capacitances of pn junctions

- The wiring capacitance
  - depends on the interconnect geometry (width, length)
  - with the advance of manufacturing processes this capacitance tends to increase

Modern metallization



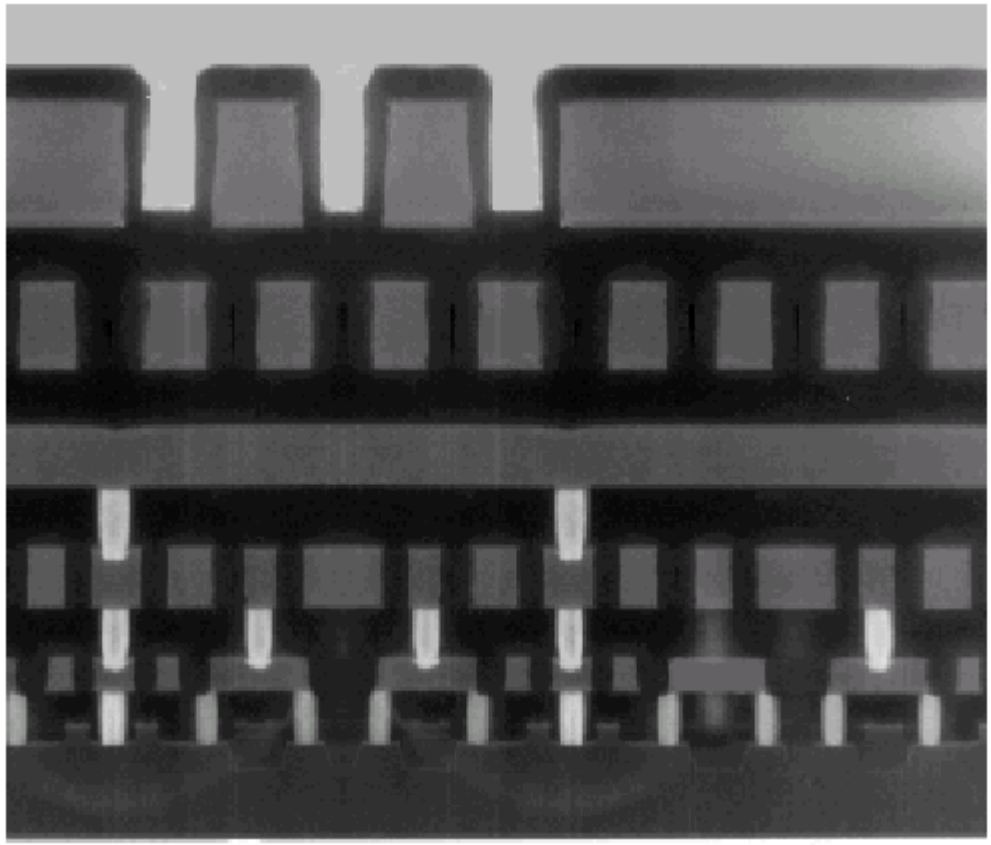


Intel 0.25 µm process

5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

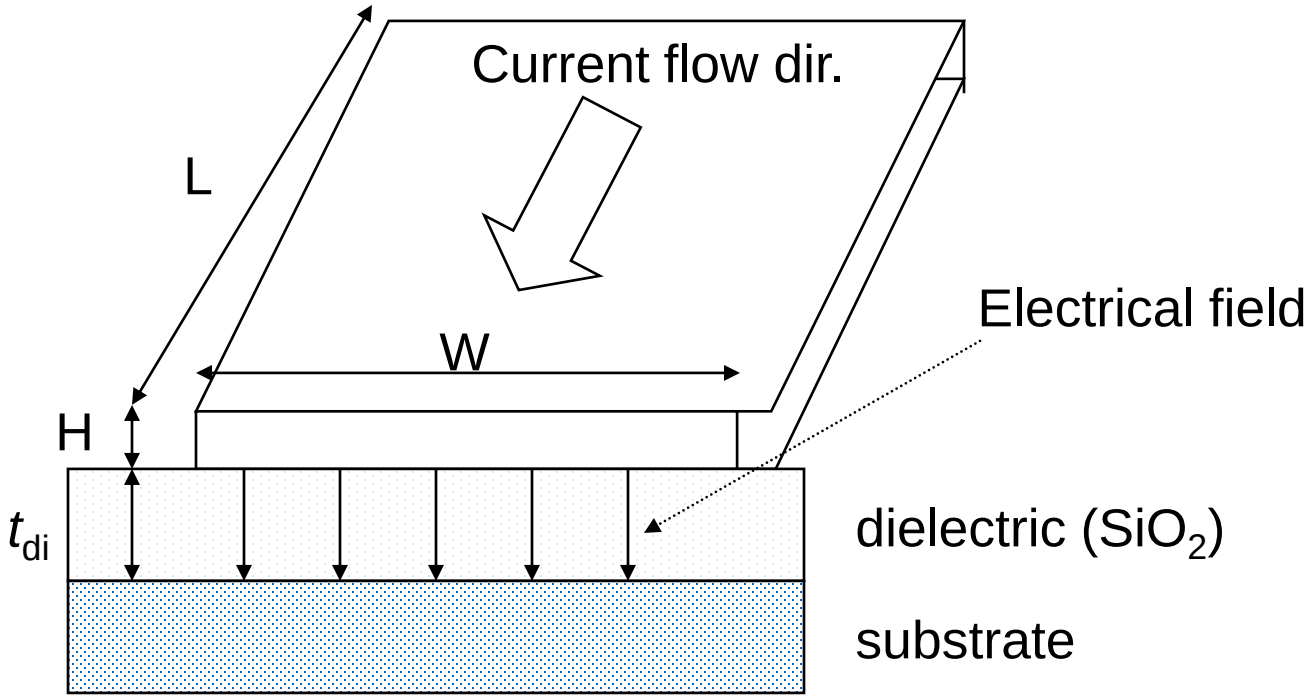
LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

Layer pitch, thickness and aspect ratio



Interconnect capacitances

Interconnect - substrate: *parallel plate capacitance*

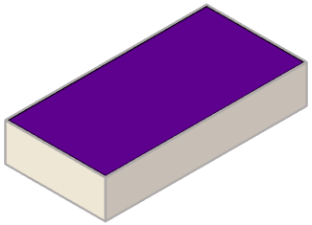


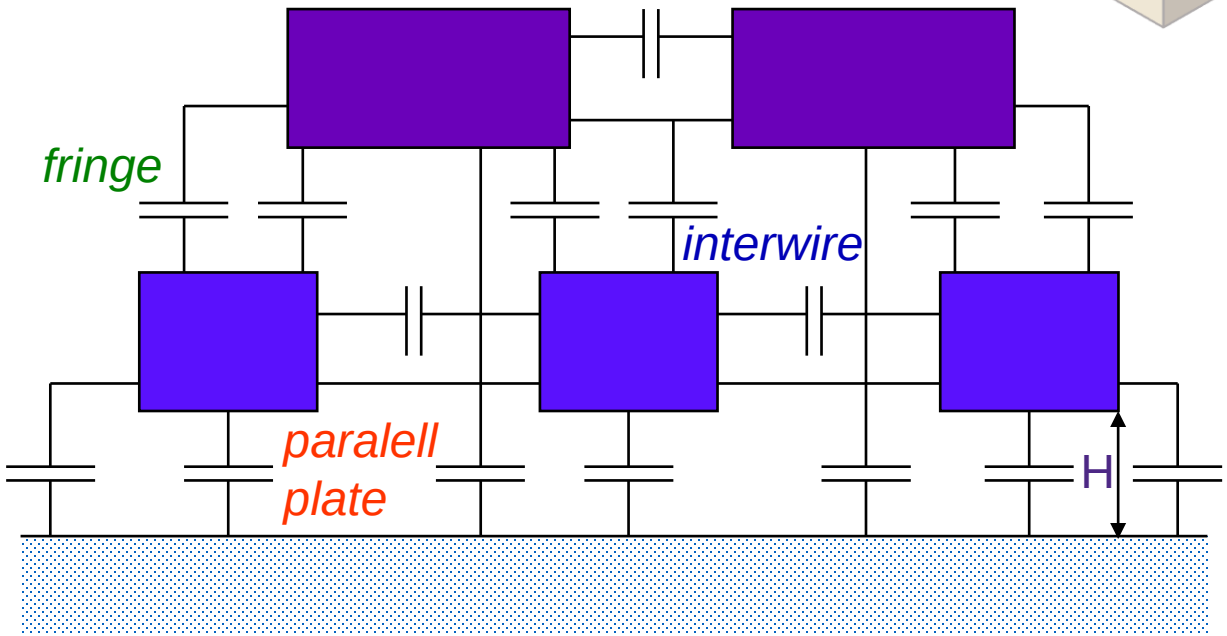
Dielectric constant (SiO_2 => 3.9)

$$C_{pp} = (\varepsilon_{di}/t_{di})\ WL$$

Interconnect capacitances

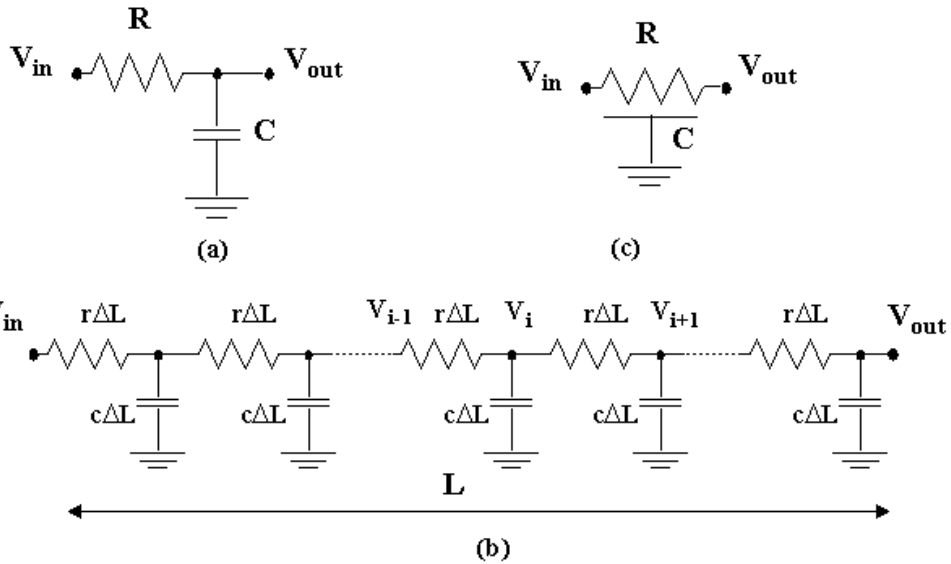
$$C_{wire} = C_{pp} + C_{fringe} + C_{interwire}$$
$$= (\varepsilon_{di}/t_{di})WL + (2\pi\varepsilon_{di})/\log(t_{di}/H) + (\varepsilon_{di}/t_{di})HL$$





Other issues of interconnects

- Series resistance
- Distributed parameter RC line (see transmission lines)



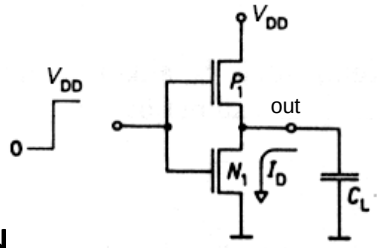
$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

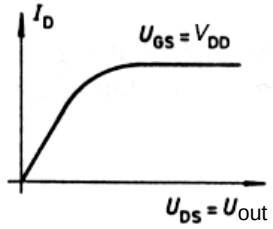
$$\tau(V_{out}) = \frac{rc\,L^2}{2}$$

Sort of a representation of the diffusion equation

The CMOS inverter / dynamic char.

- Calculation of switching times
  - identical times, integration for the extreme values of the voltage of the load capacitance:





$$t_l = \int_{V_{DD}}^{V_{LM}} \frac{C_L}{I_D} dU$$

- If

$$I_D \approx K(V_{DD} - V_T)^2$$

V_{LM} – minimal voltage of the load capacitance

then

$$t_l = \frac{C_L(V_{DD} - V_{LM})}{K(V_{DD} - V_T)^2}$$

Can be reduced by increasing the supply voltage or the W/L ratio

Power consumption of CMOS inv.

- There is no static consumption since there is no static current
- There is dynamic consumption during switching which consists of 2 parts:
  - **Mutual conduction:**
    - During the rise of the input voltage both transistors are "on"

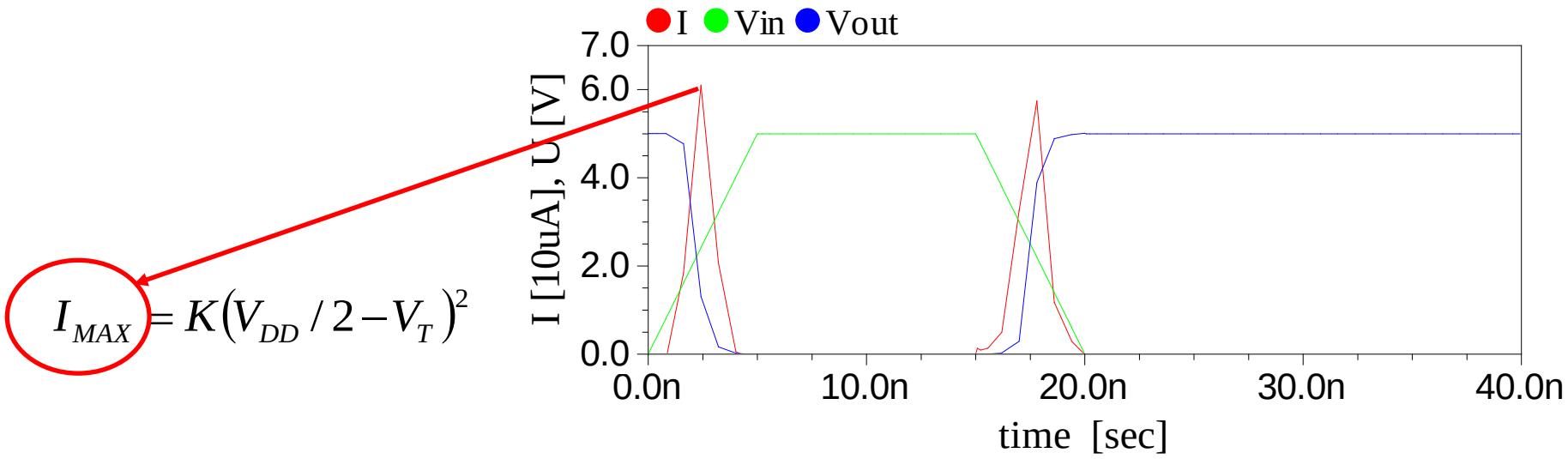
$$V_{Tn} < U_{IN} < V_{DD} - V_{Tp}$$

  - **Charge pumping:**
    - At switching over the output to 1 the $C_{L\ \text{loading}}$ capacitor is charged to the supply voltage through the *p* transistor, then it is discharged towards the ground through the *n* transistor.

Charge is pumped from VDD to GND.

Power consumption of CMOS inv.:

- **Mutual conduction ("short power"):**
  - During a certain period of the rise of the input signal both transistors are "on" if $V_{Tn}<U_{IN}<V_{DD}-V_{Tp}$ this is called mutual conduction



  - *charge flowing through:* $\Delta Q = bt_{UD}I_{MAX}$ *, where* t_{UD} *is the time while current is flowing,* ***b*** *is a constant depending on the signal shape. b≈0.1-0.2*

$$P = f\Delta QV_{DD} = fV_{DD}bt_{UD}K(V_{DD}/2 - V_T)^2$$

$$P \sim f\,V_{DD}^{\,3}$$

Power consumption of CMOS inv.:

- **Charge pumping:**
  - At switching the C_L load capacitance is charged to VDD through the p-channel device when the output changes to 1, later, when switching the output to 0, it is discharged towards GND through the n-channel device.

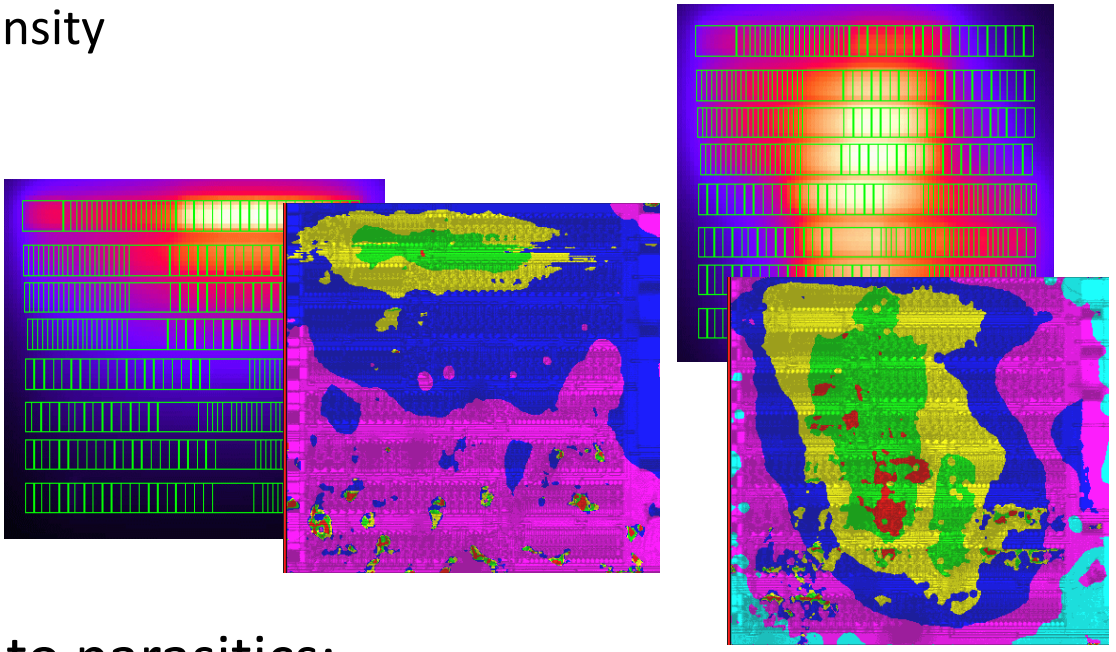
$$\Delta Q_L = C_L V_{DD} \qquad P_{cp} = f\, C_L V_{DD}^2$$

  - **The power consumption due to charge pumping is proportional to the frequency and the square of the supply voltage.**

- **Total consumption:** sum of the two components (if there is mutual conduction), directly proportional to the **frequency** and the 2nd and 3rd power of the supply voltage.

Components of the consumption of CMOS circuits

- Dynamic components – at every switching event
  - mutual conduction, charge pumping
  - proportional to the event density
    - clock frequency
    - circuit activity



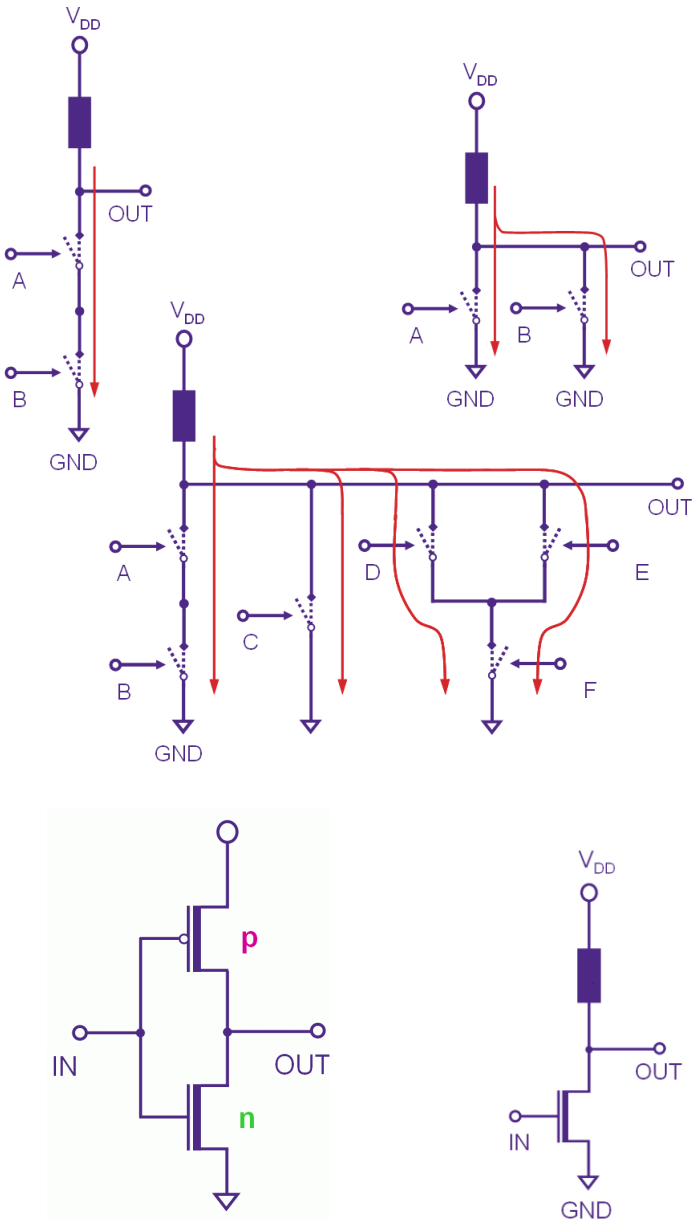
- Further components due to parasitics:
  - subthreshold currents
  - leakage currents of pn junctions – nowadays already significant
  - leakage (tunneling) through the a gate dielectric

Construction

- **Constructing CMOS gates on schematic (circuit) level**
- **Process and layout**
  - Recall the nMOS process and layout
    - Stick diagram layout
    - Full layout
  - Create standard cells

CMOS gates

- **PDN**: Create an nMOS switching circuit (pull down network):
  - series path: NAND function
  - parallel path: NOR function
  - combination of these: complex gate
  - Switches: **nMOS** transistors
- **PUN**: *Load of the former nMOS gates with no active control is replaced by a full network*: the dual circuit of the nMOS pull down network:
  - Dual topology (series → parallel, parallel → series, aka the loop-cut duality)
  - Dual component: **pMOS** transistors
- The transistor gates in the PDN and PUN recieve the **same control signals** (inputs)



CMOS gates

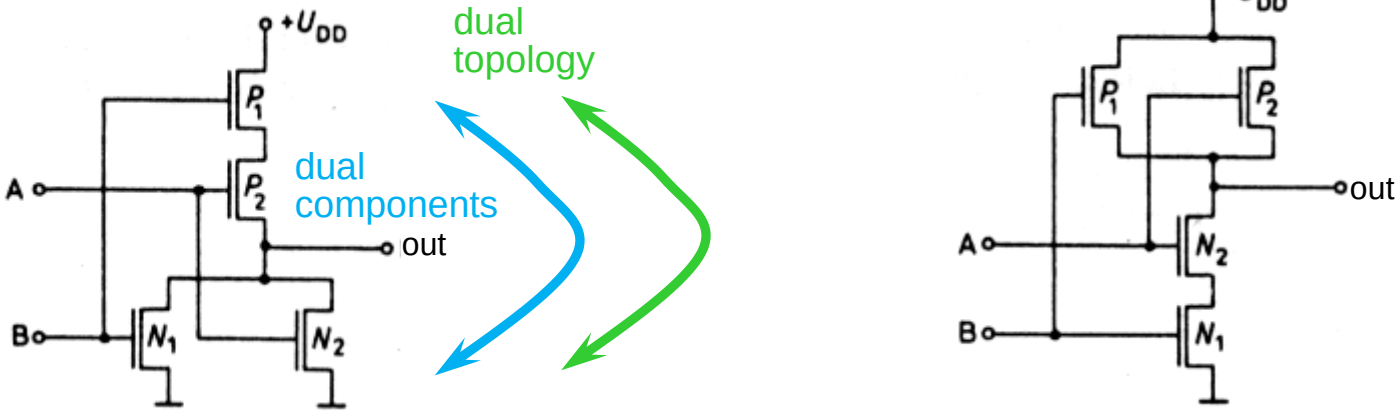
- In a CMOS inverter both transistors are actively controlled
- In case of gates there will be a PUN (pull up network: pMOS circuit) and a PDN (pull down network: nMOS circuit). The number of transistors both in PUN and PDN is equal to the number of inputs of the gate
  - For input combinations where the output is 0, the PDN realizes a short towards GND and the PUN is an open circuit;
  - if the output function is equal to 1, the PDN will be an open circuit and the PUN realizes a short towards VDD.

Circuits with dual topology should be realized from n and p channel transistors

- Gates of transistors receiving the same signal are connected

CMOS gates

- NOR gate ⟷ duality of the logic function ⟷ NAND gate

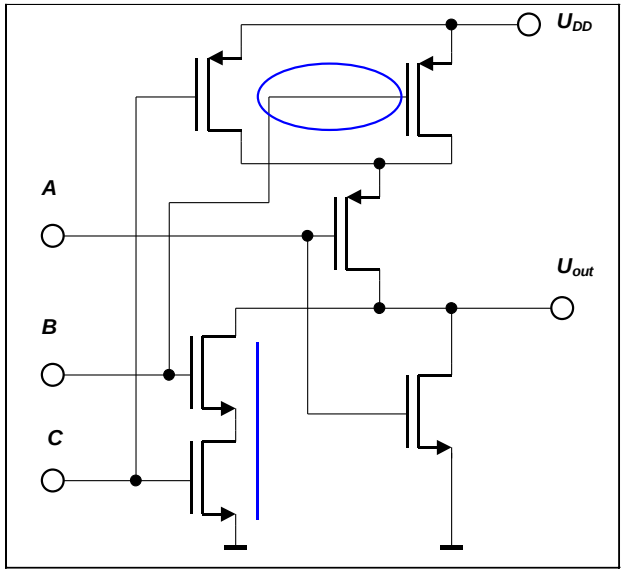


duality of the transistor level circuit

For an *n* input CMOS gate 2*n* transistors are needed
(passive load gates need only n+1 transistors)

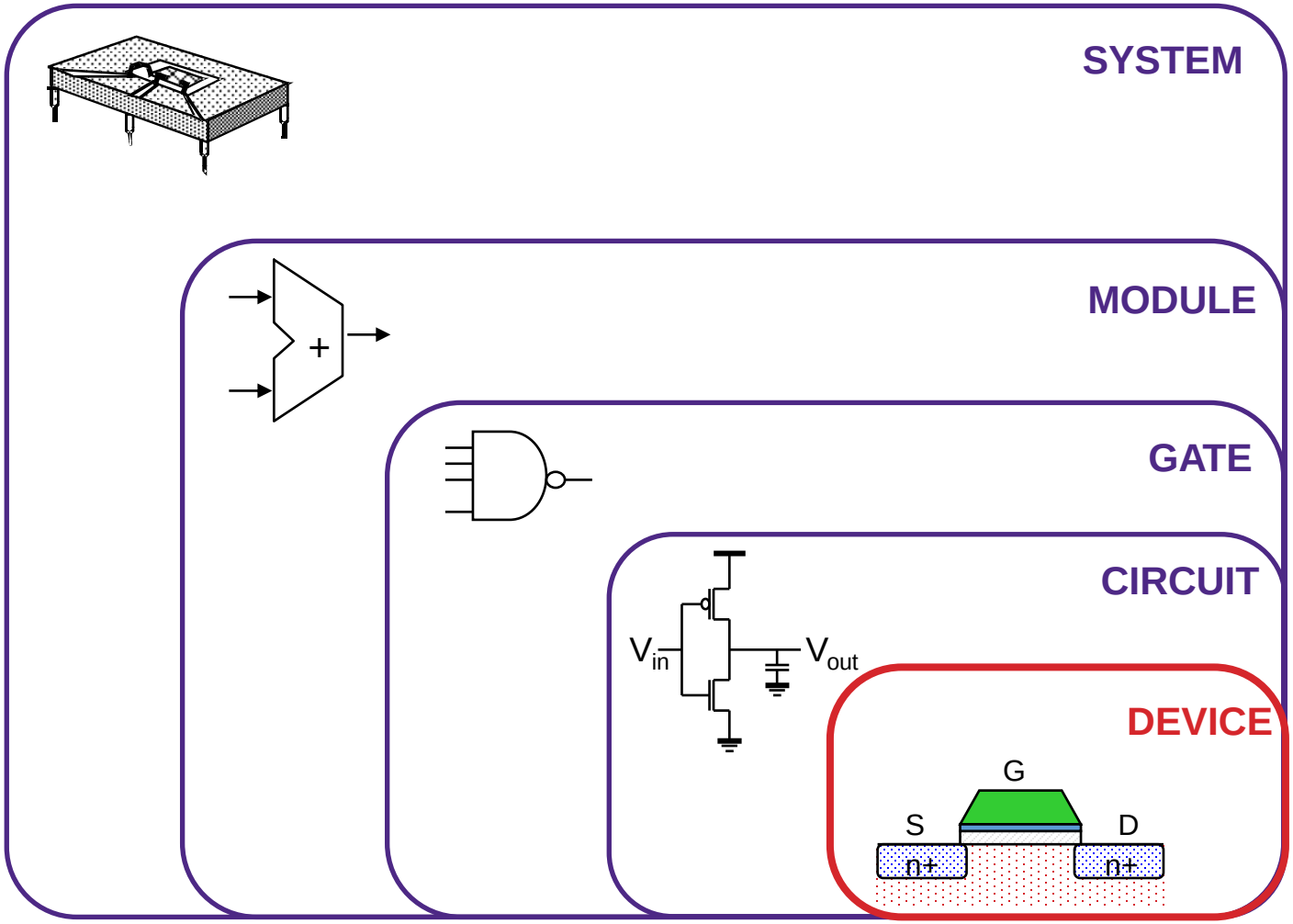
Construction complex CMOS gates

- dual topology (loop $\Rightarrow$ cut, cut $\Rightarrow$ loop)
- dual components: nMOS replaced by pMOS
- transistor gates corresponding to the same signal must be connected
- proper sizing of the W/L ratios (electron/hole mobility mismatch)



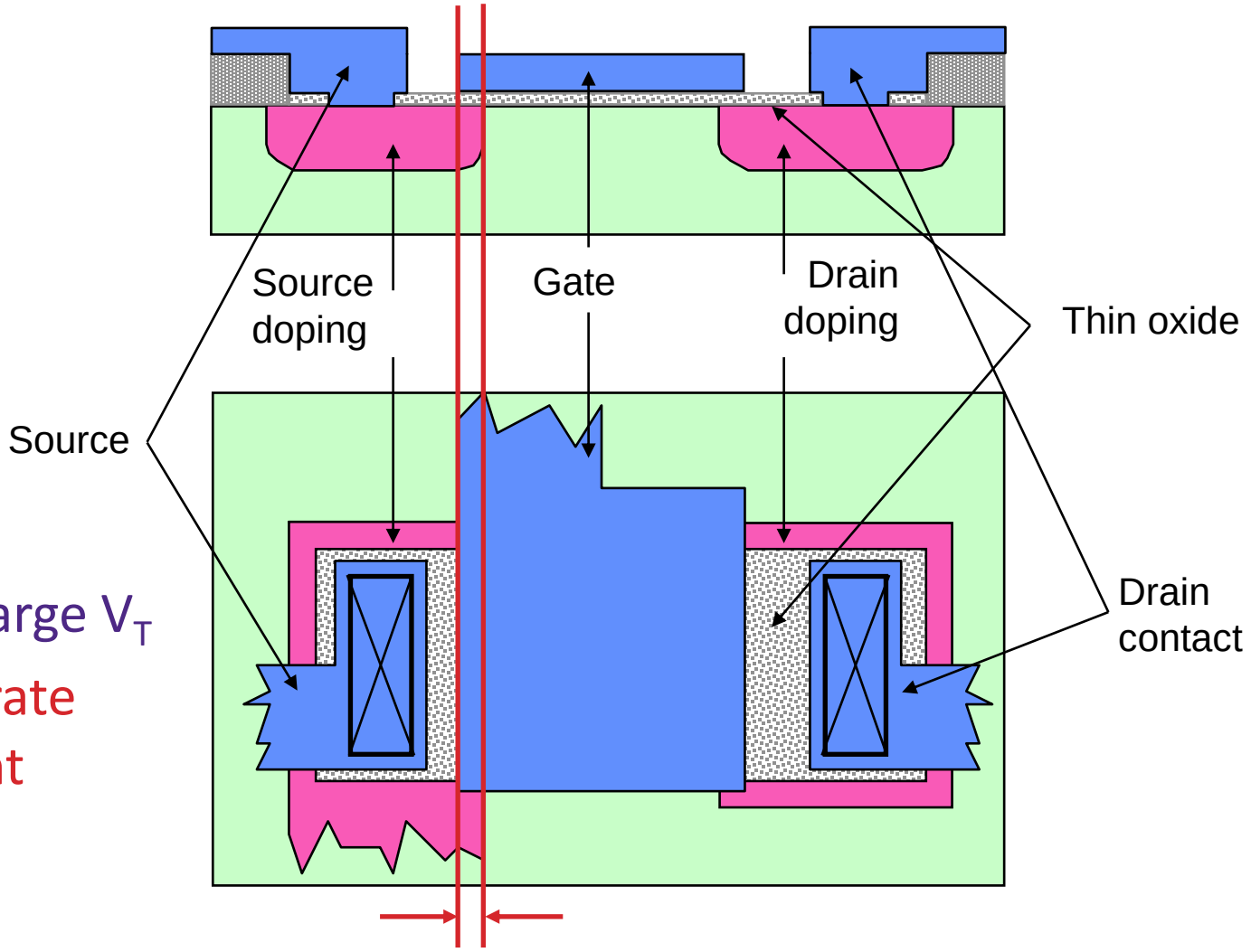
$$F = \overline{A + BC}$$

The abstraction level of our study:



Metal gate MOS transistor

Layout view:



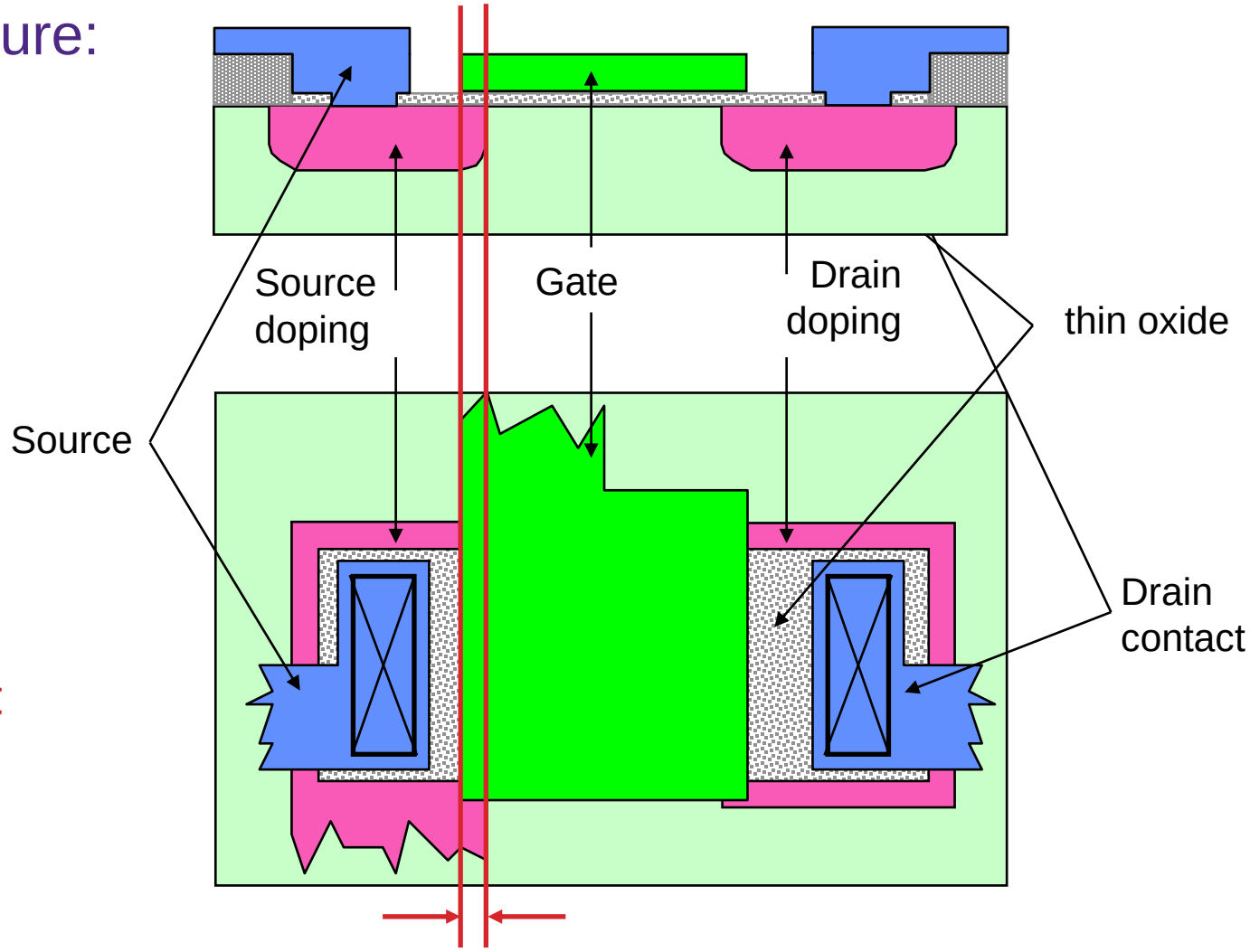
Problems:

- metal gate – large V_T
- requires accurate mask alignment

Poly-Si gate MOS transistor

In-depth structure:

Layout view:

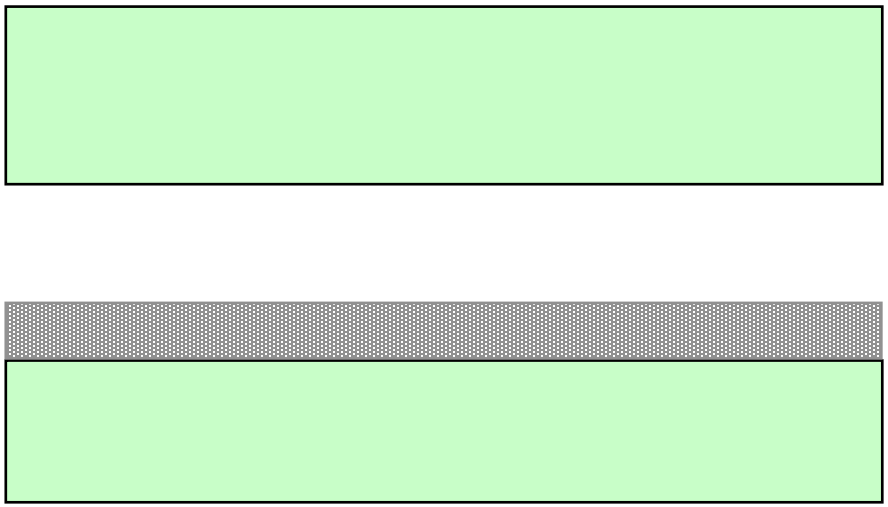


Advantages

- smaller V_T
- self alignment

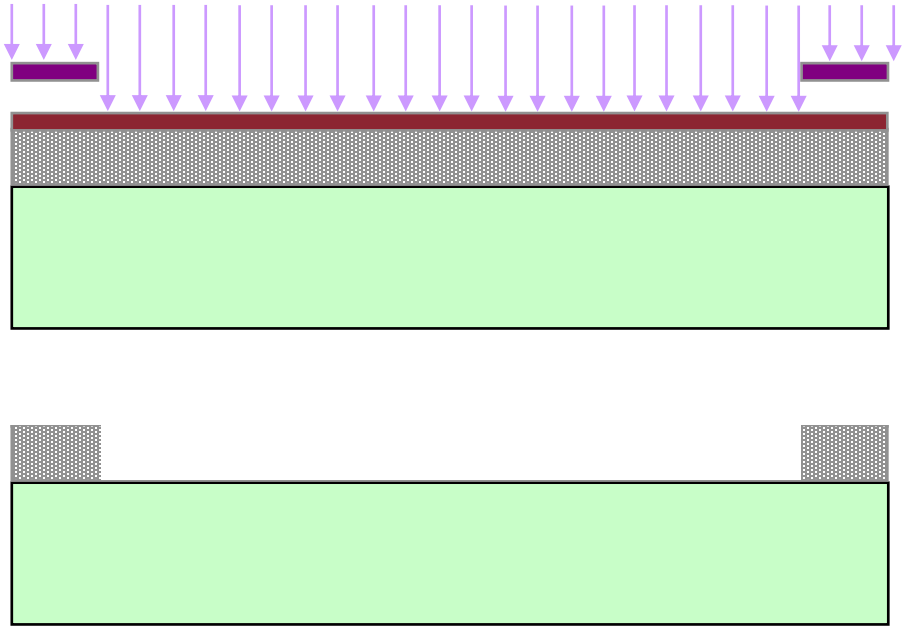
A poli-Si gate nMOS process

- Start with: p type substrate (Si wafer)
  - cleaing,
  - grow thick SiO_2 – this is called *field oxide*



A poli-Si gate nMOS process

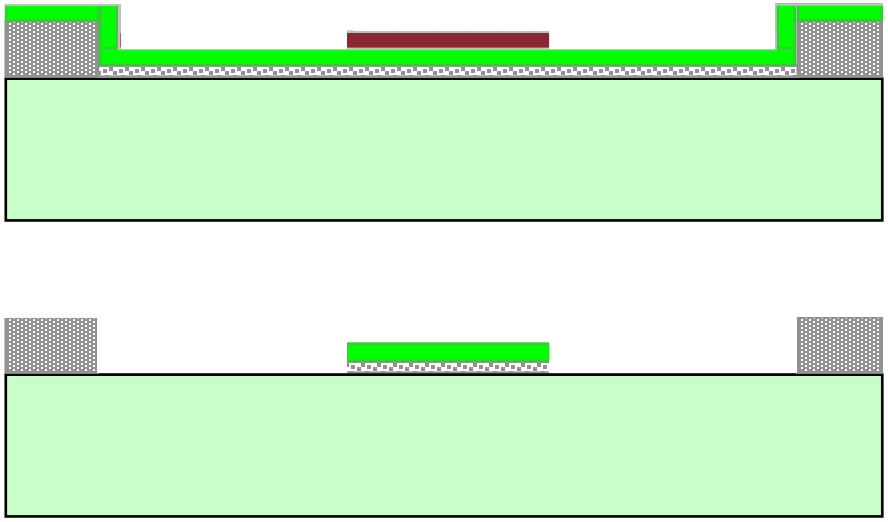
- Create the active zone with photolithography
  - coat with resist,
  - expose to UV light through a mask,
  - development, removal of exposed resists
  - etching of SiO_2 removal of the resist



M1: active zone

A poli-Si gate nMOS process

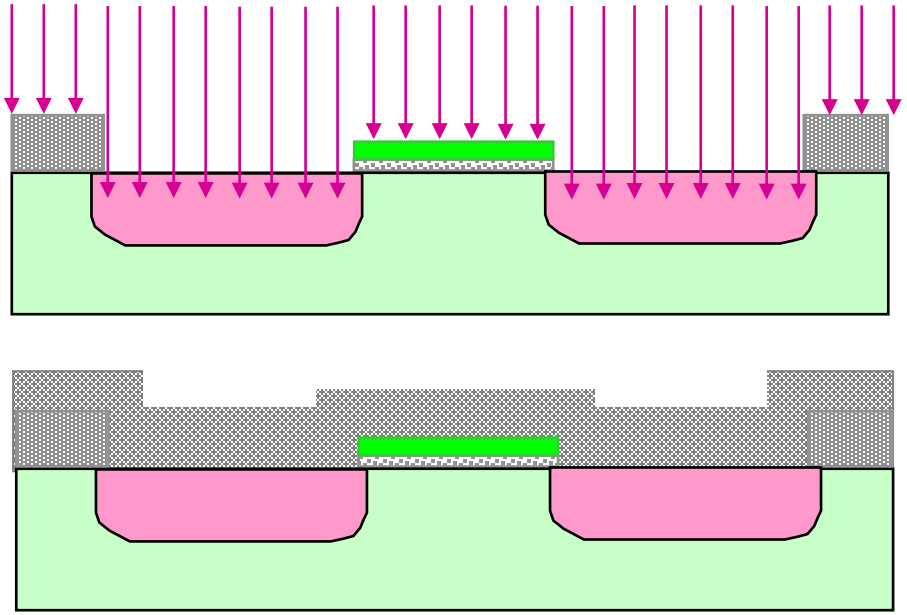
- Create the gate structure:
  - growth of thin oxide
  - deposit poly-Si
  - pattern poly-Si with photolithography (resist, exposure, develop)
  - etch poly-Si, etch thin oxide



M2: poly-Si pattern

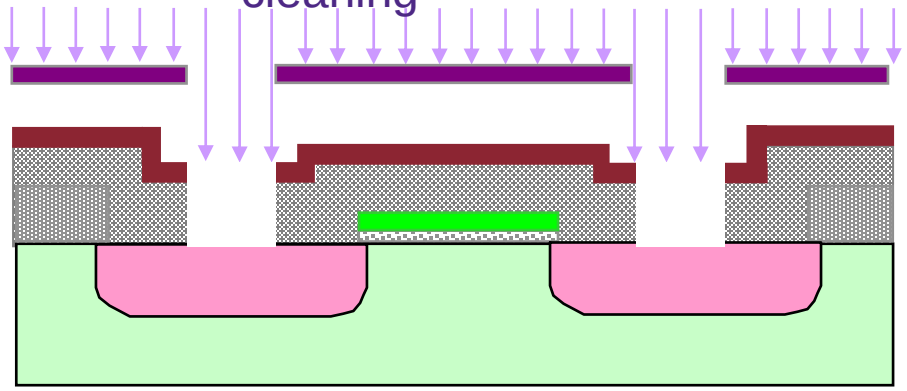
A poli-Si gate nMOS process

- S/D doping (implantation)
  - the exide (thin, thick) masks the dopants
  - this way the self-alignment of the gate is assured
- Passivation: deposit PSG



A poli-Si gate nMOS process

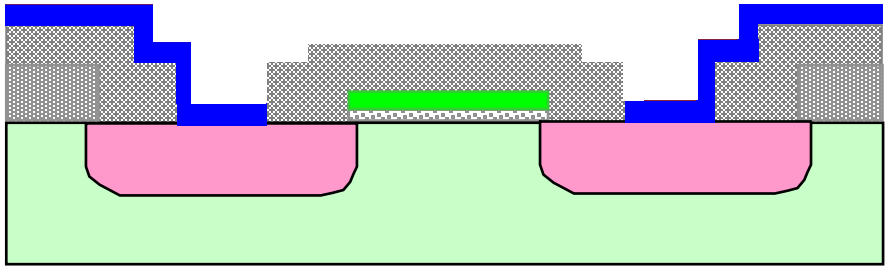
- Open contact windows through PSG
  - photolithography (resist, expose pattern, develop)
  - etching (copy the pattern)
  - cleaning



M3: contact window pattern

A poli-Si gate nMOS process

- Metallization
  - Deposit Al
  - photolithography, etching, cleaning

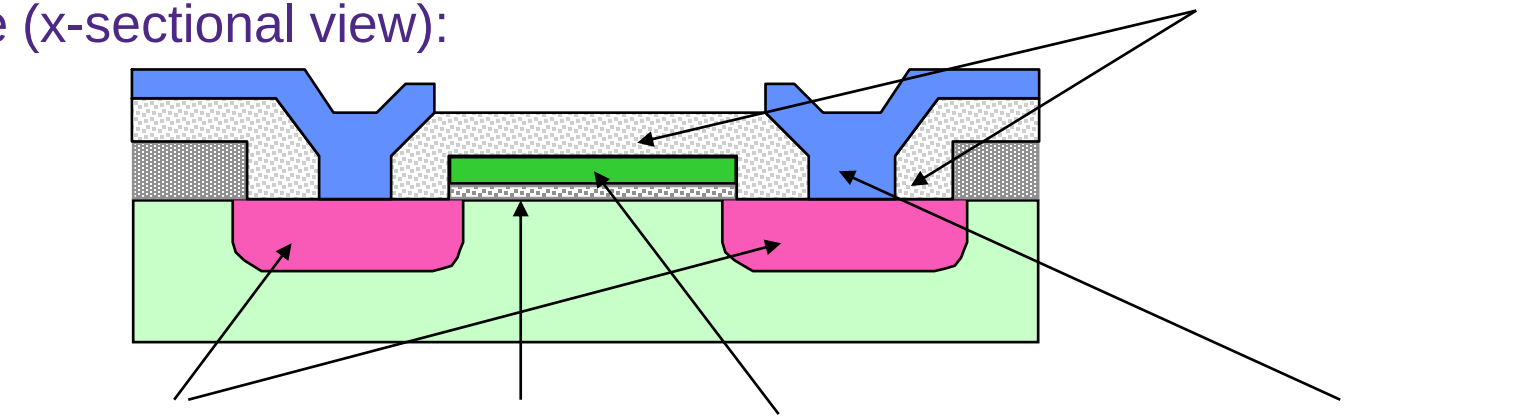


M4: metallization pattern

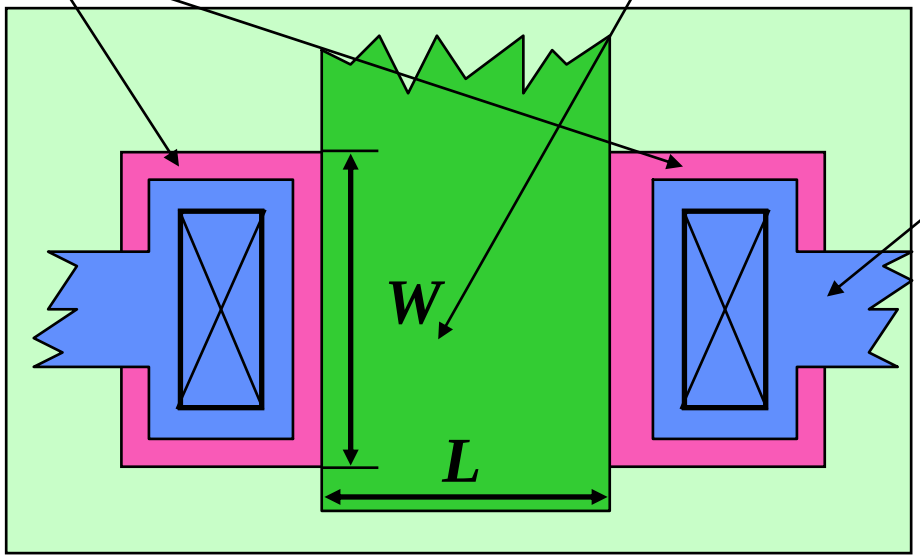
- The recepy of the process is given, the in-depth structure is determined by the sequence of the masks
- One needs to specify the shapes on the masks
  - ***The set of shapes on subsequent masks is called layout***

A poli-Si gate nMOS process

Structure (x-sectional view):



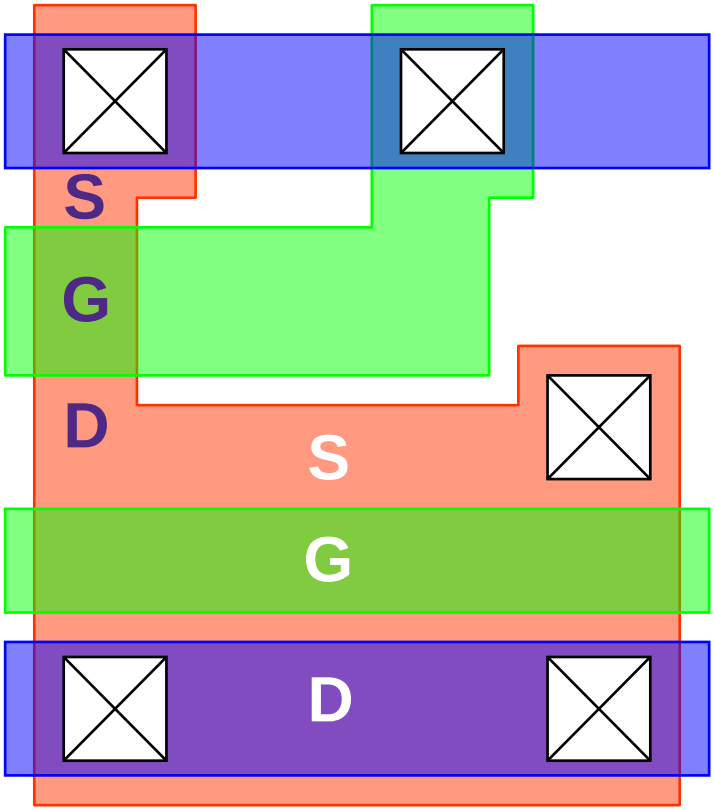
Layout (top view):



Steps of the self-aligned poli-Si gate process

1) Open window for the active region **M**
   - photolitography, field oxide etching
2) Growth of thin oxide
3) Window for hidden contacts **M**
   - Contacts the poli-Si gate (yet to be deposited) with the active region (after doping).
3) Deposit poli-Si
4) Patterning of poli-Si **M**
5) Open window through the thin oxide (etching only)

Layout of a depletion mode inverter

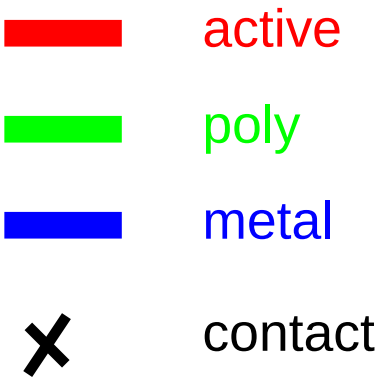


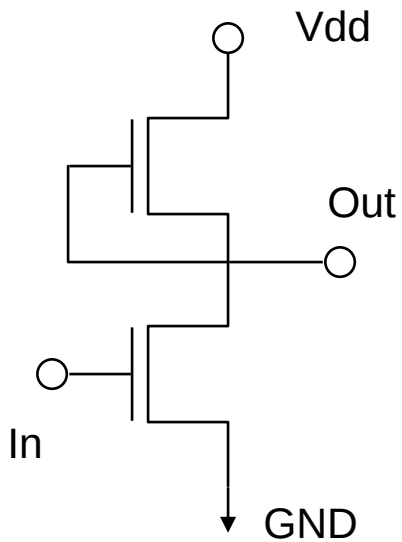
- Layout == set of 2D shapes on subsequent masks
- Masks are color coded:
  - active zone: red
  - poly-Si: green
  - contact windows: black
  - metal: blue
- Mask == layout layer

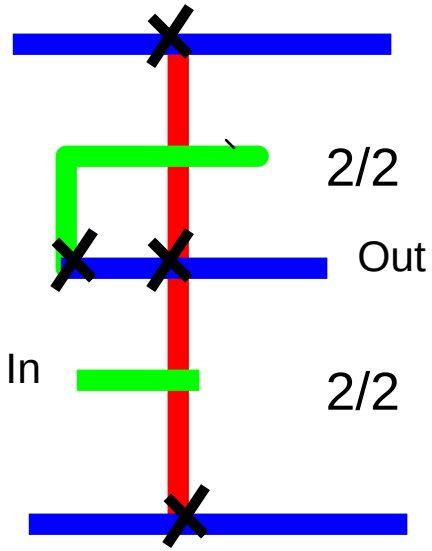
Where is a transistor? Channel between two doped regions:

CHANNEL = ACTIVE AND POLY

Simplified layout: *stick diagram*





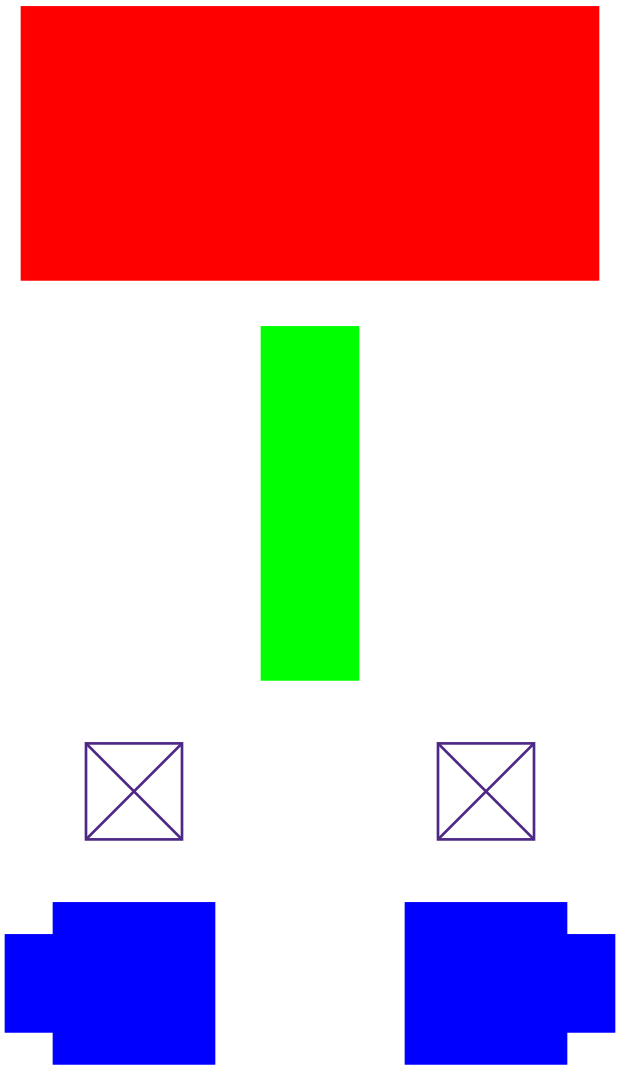


W/L ratios are given

Si-compilers

- Logic schematic / netlist / high level description
- Transistor level schematic with W/L information
- Stick diagram layout
- Actual layout
  - Automatic conversion between these representations
  - HARDWARE SYNTHESIS
  1. From behavioural description structural description
  2. Implementation of the structural description with a given realization mode / manufacturing process: *technology mapping*
     - *We have seen basics of the realization of an application specific integrated circuit (ASIC)*
     - *Designs can also be mapped to an FPGA*

Layout primitives: simple shapes



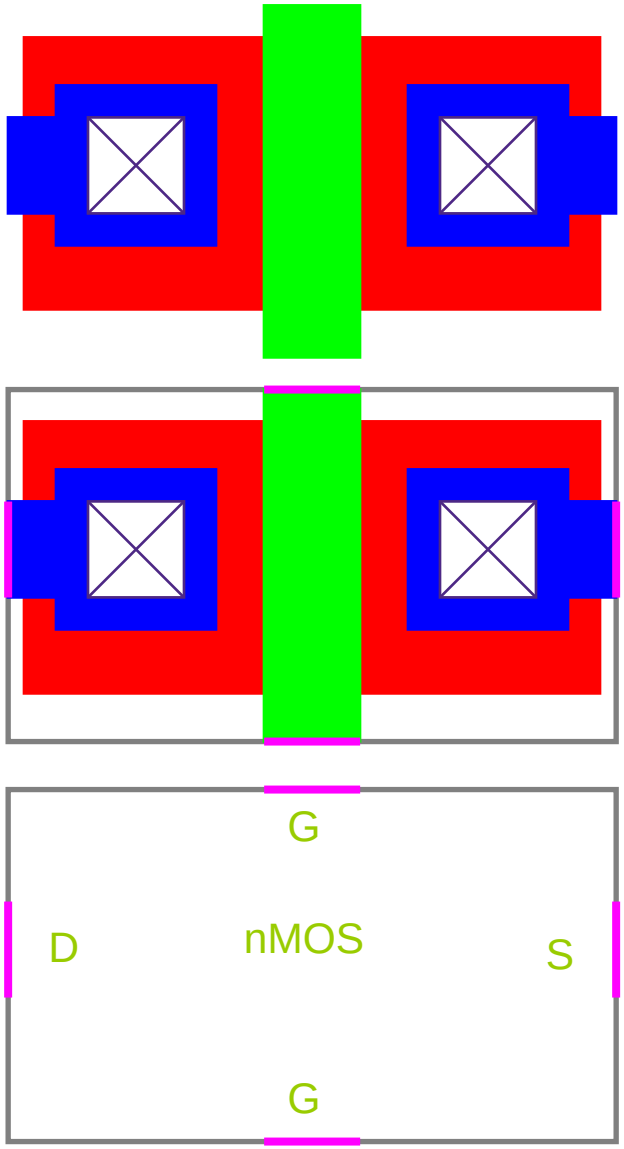
Active zone (window opening through the oxide)

Gate (mask of poly-Si pattern)

Contacts (window opening mask through oxide/PSG)

S/D lines (mask of metallization pattern)

Layout macros – from primitives



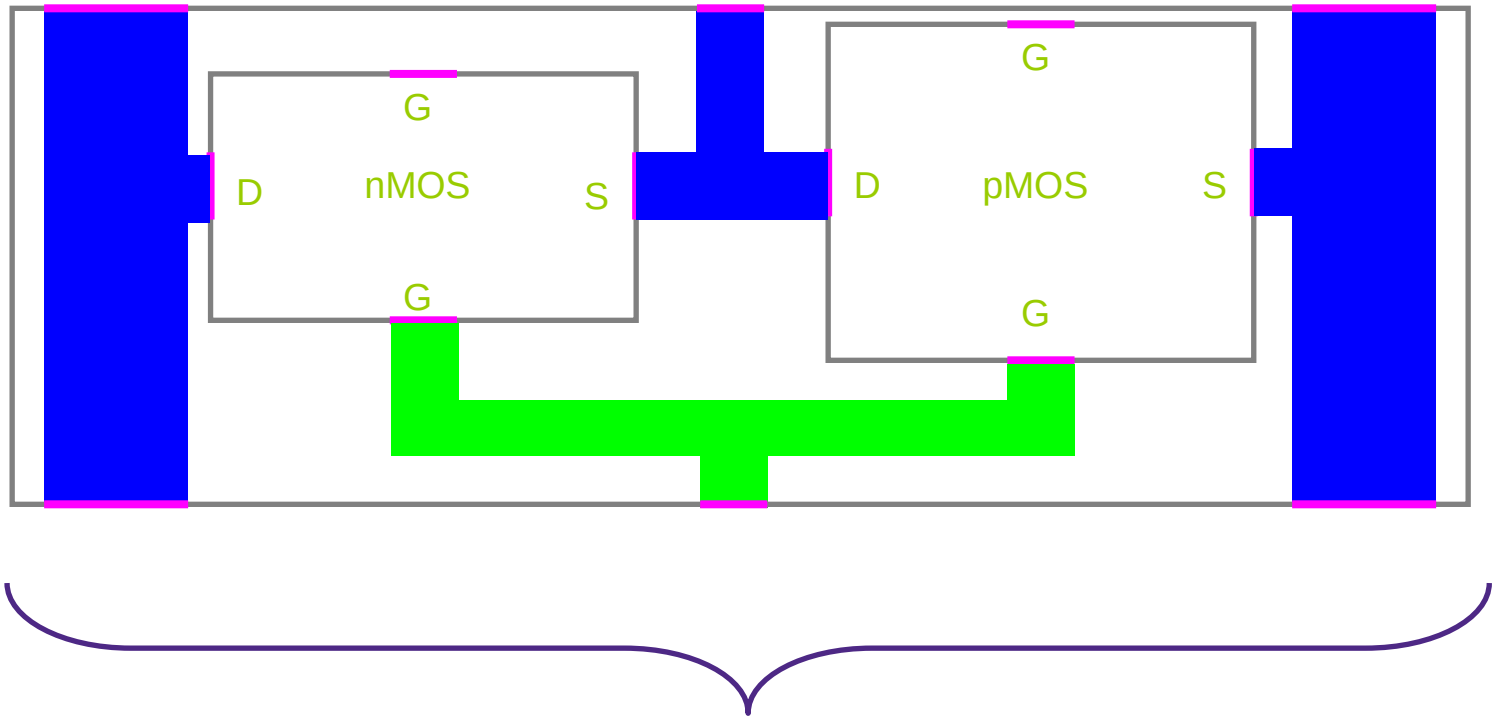
layout of an nMOS transistor: *layout primitives on actual layers corresponding to real masks*

nMOS transistor layout + outline + pins

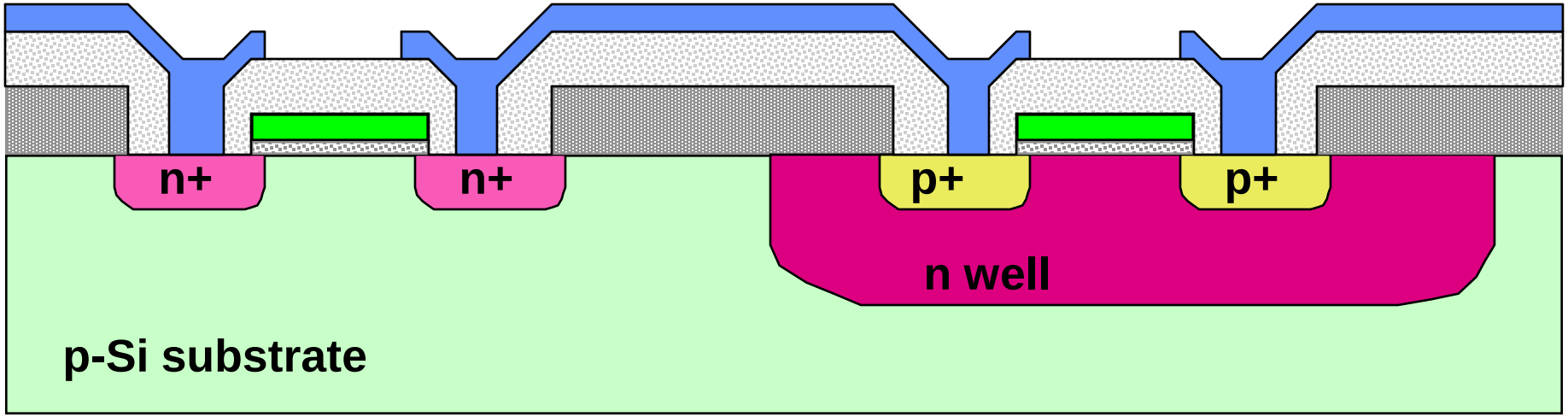
nMOS transistor macro:

outline, pins, scripts: ***pseudo layers***

Layout macros – from macros and primitives



CMOS structure (inverter)

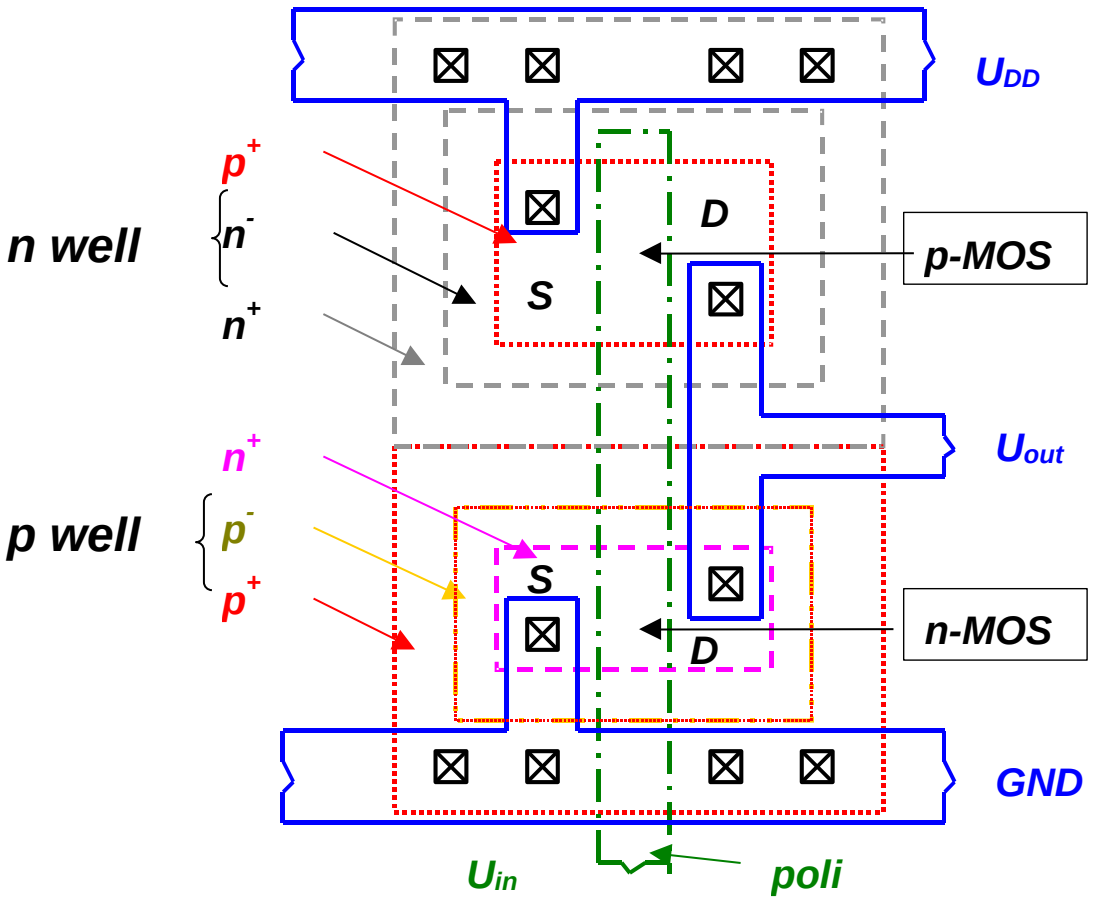


CMOS structures

- Further masks:
  - n-well (or p-well, depending on the substrate)
  - p doping (or n doping, depending on the substrate)
- Multiple metal layer CMOS:
  - each metallization needs own mask,
  - contact windows, vias
- There could be multiple poly-Si layers (analog CMOS)
- Typically: 15..20 masks

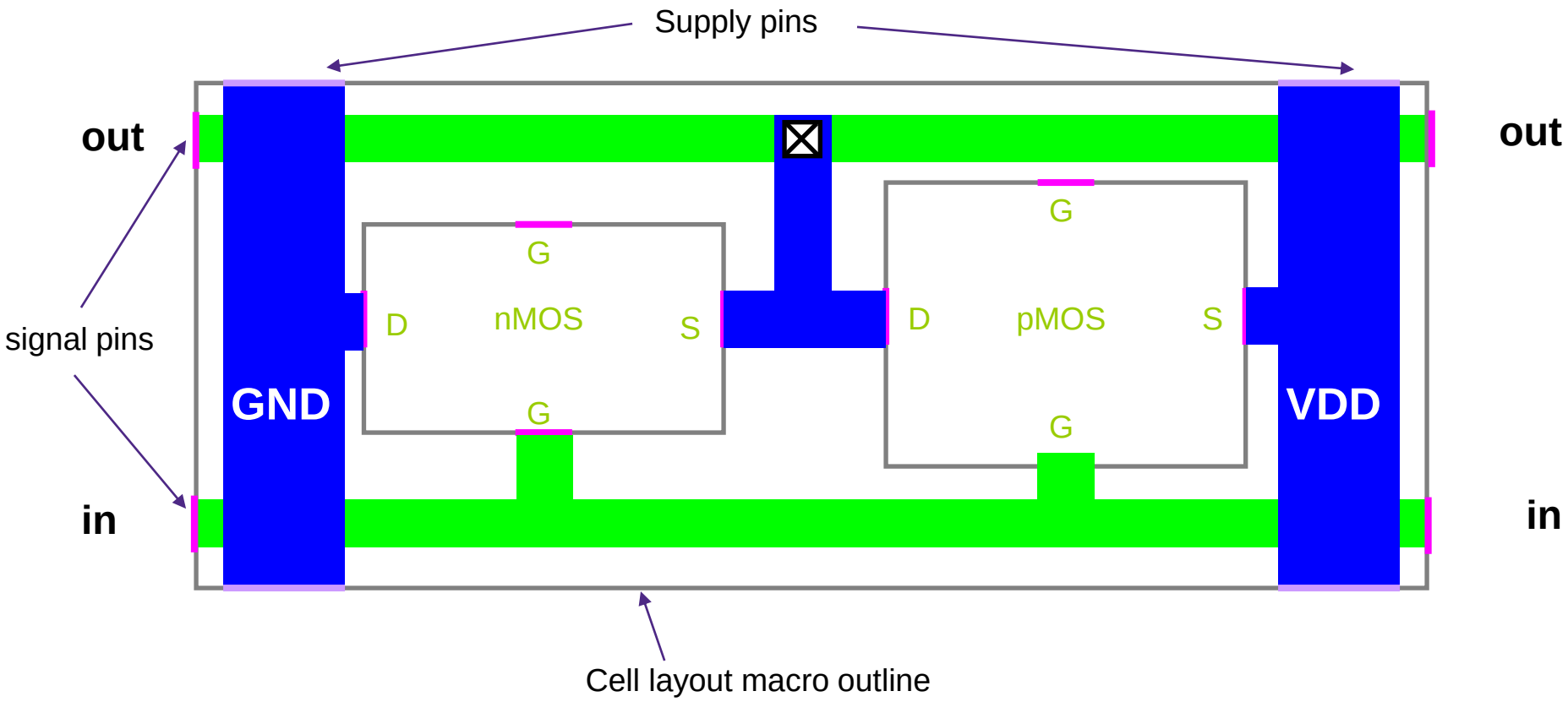
- Certain rules need to be kept for manufacturability: ***design rules***
  - ***come from the process, given by Si-foundry***

Layout of a CMOS inverter



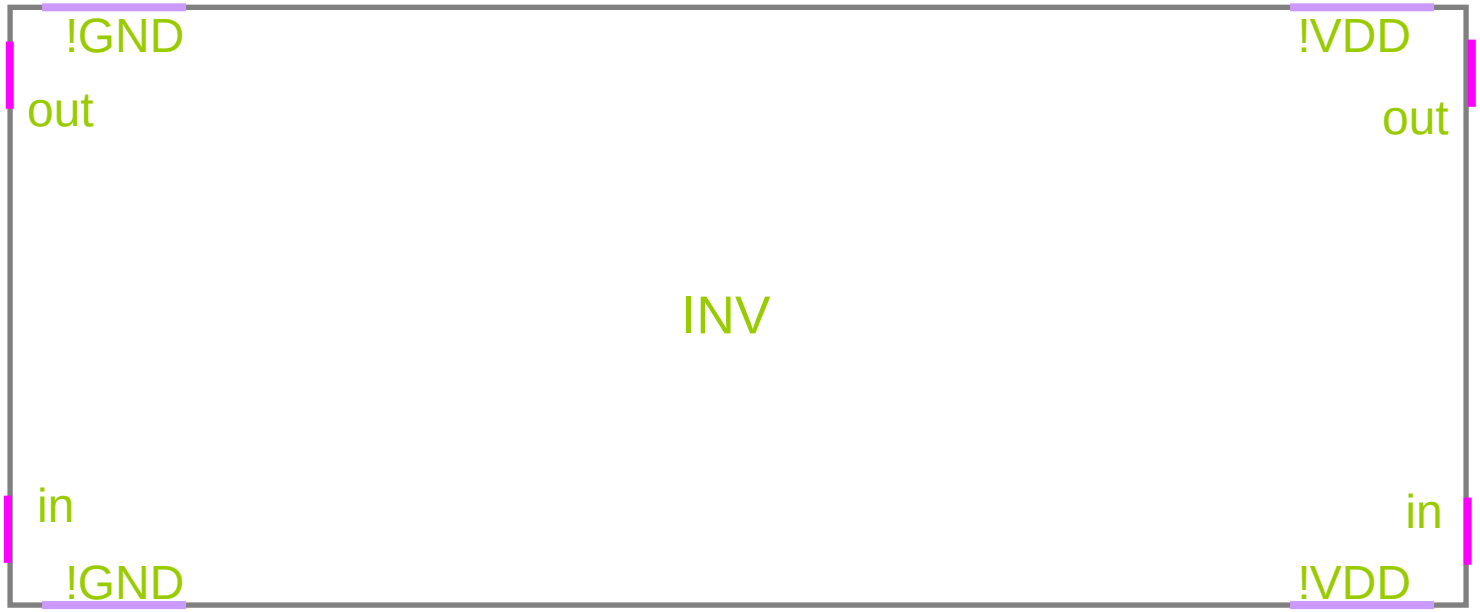
Standard cells of gates

- The CMOS inverter layout shown before has also been created according to conventions of standard cell design

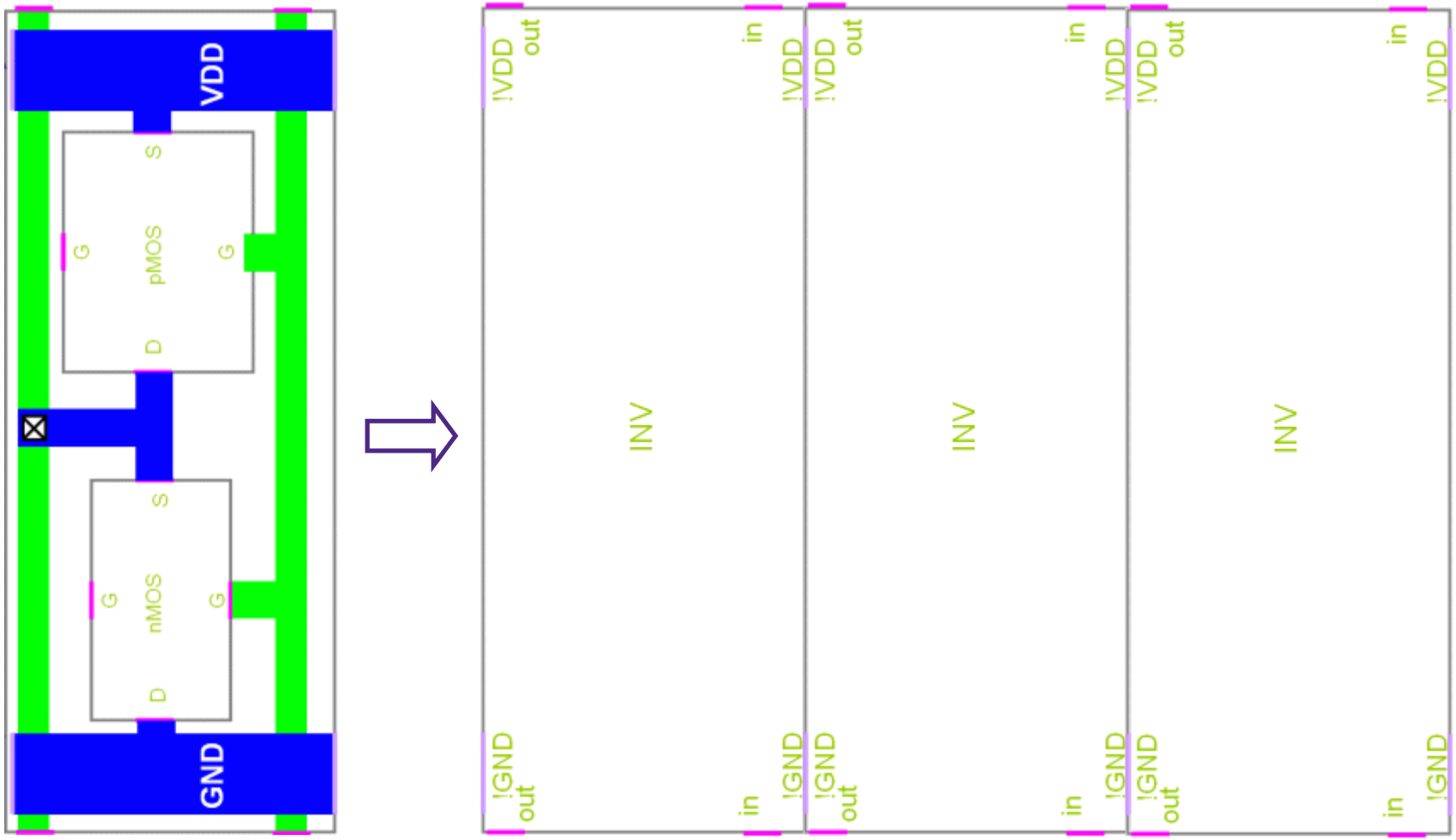


Standard cells

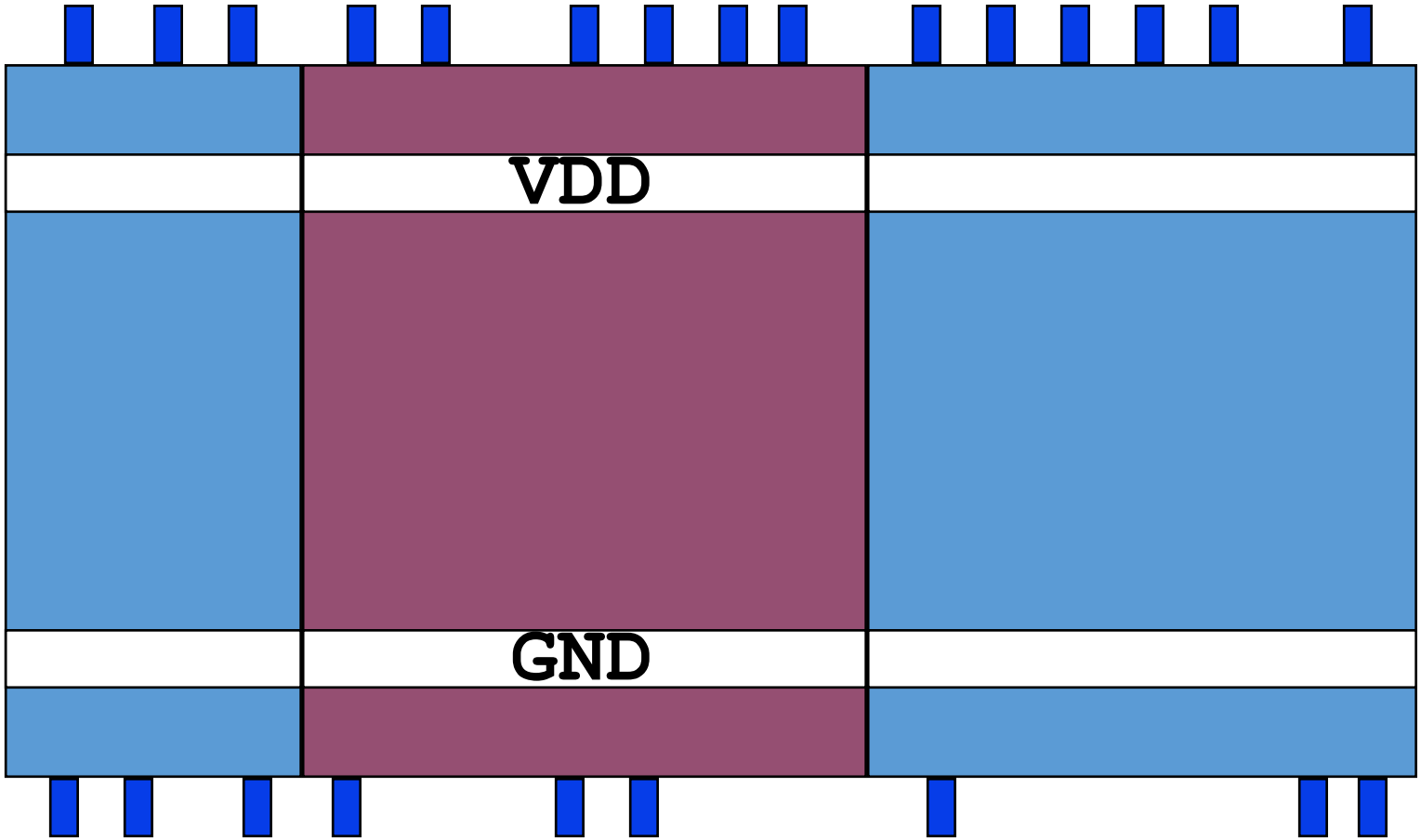
- In layout view on can refer to the inverter through its layout macro (cell outline and pins)



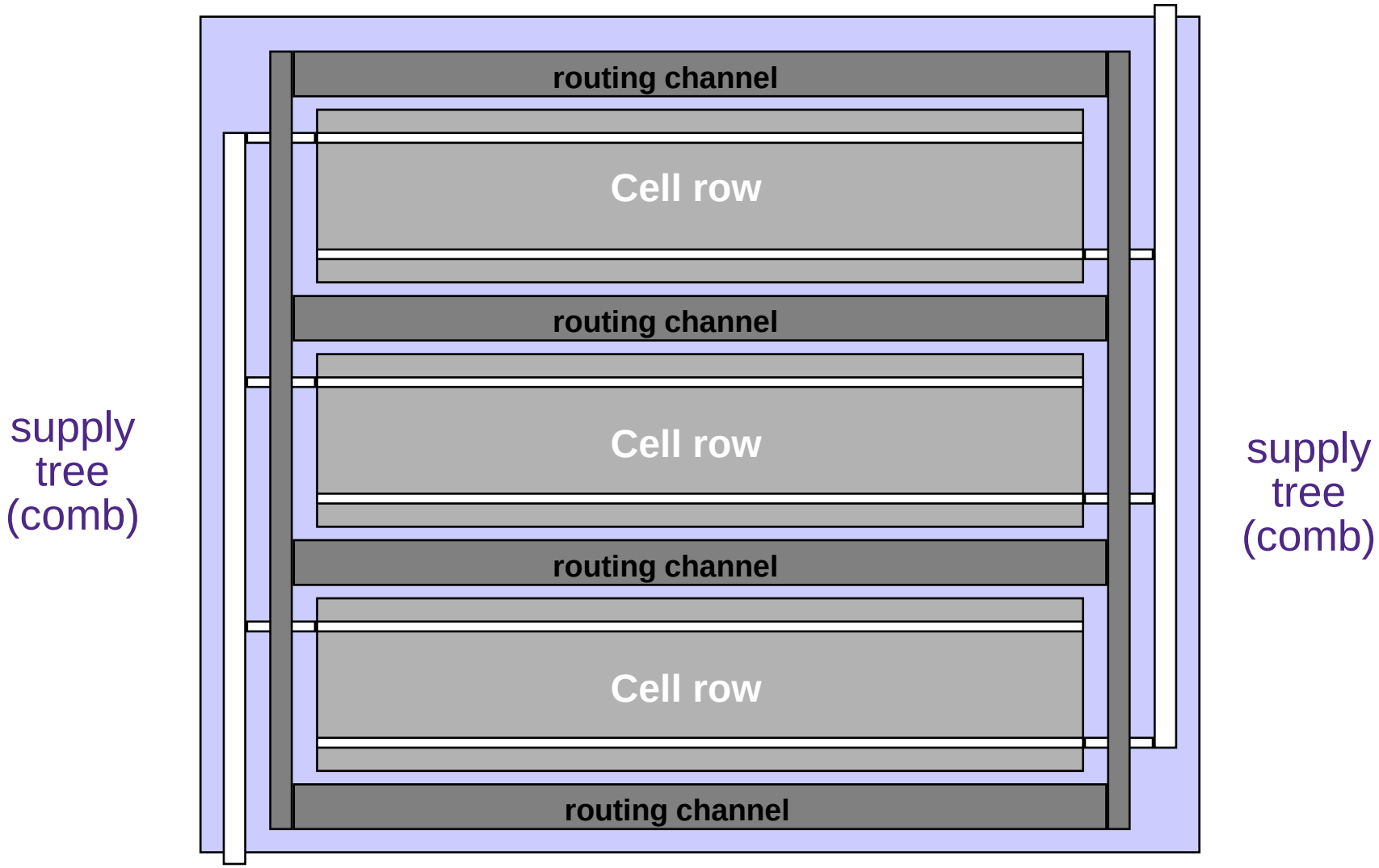
Standard cells



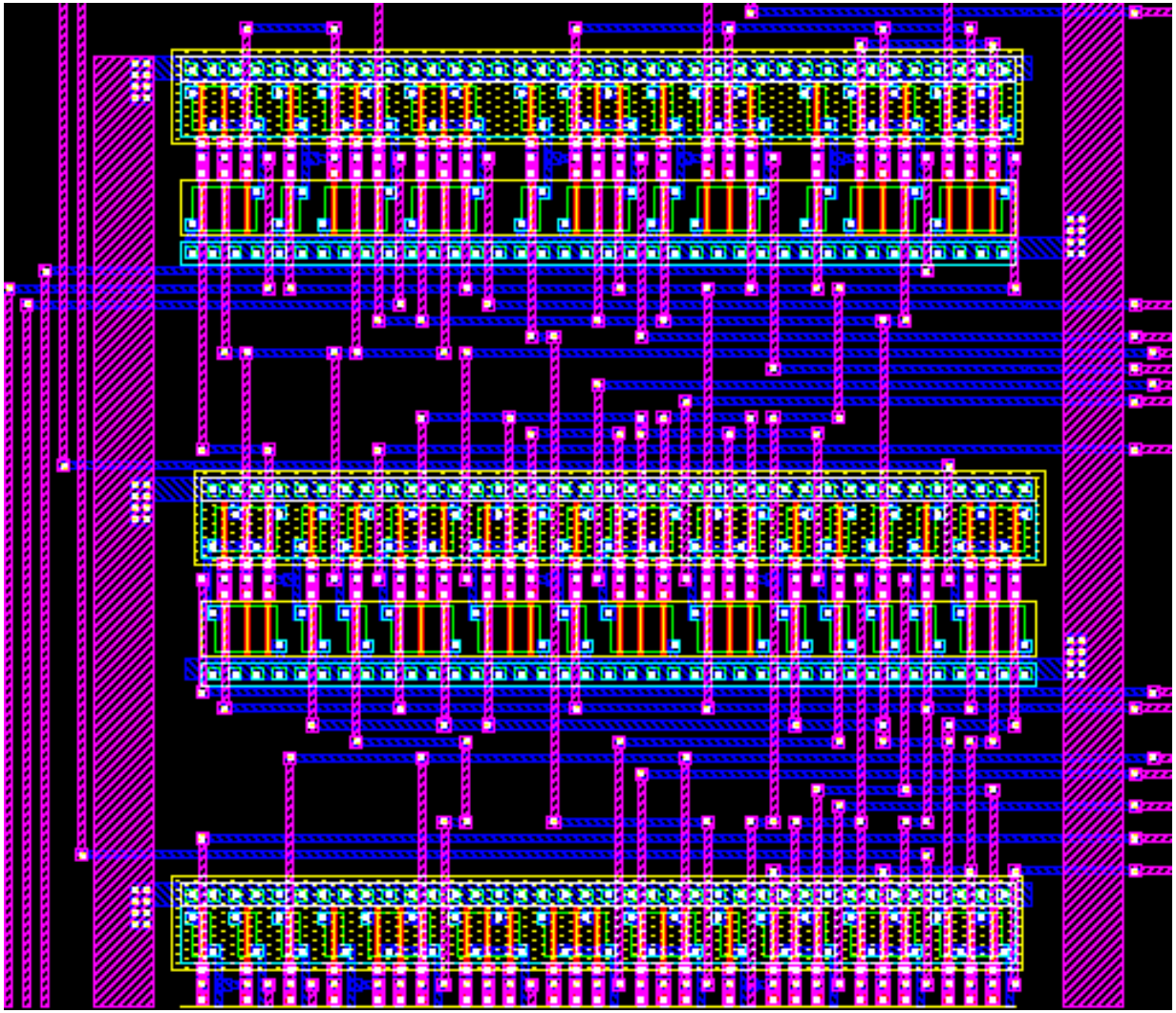
Standard cella in a row:



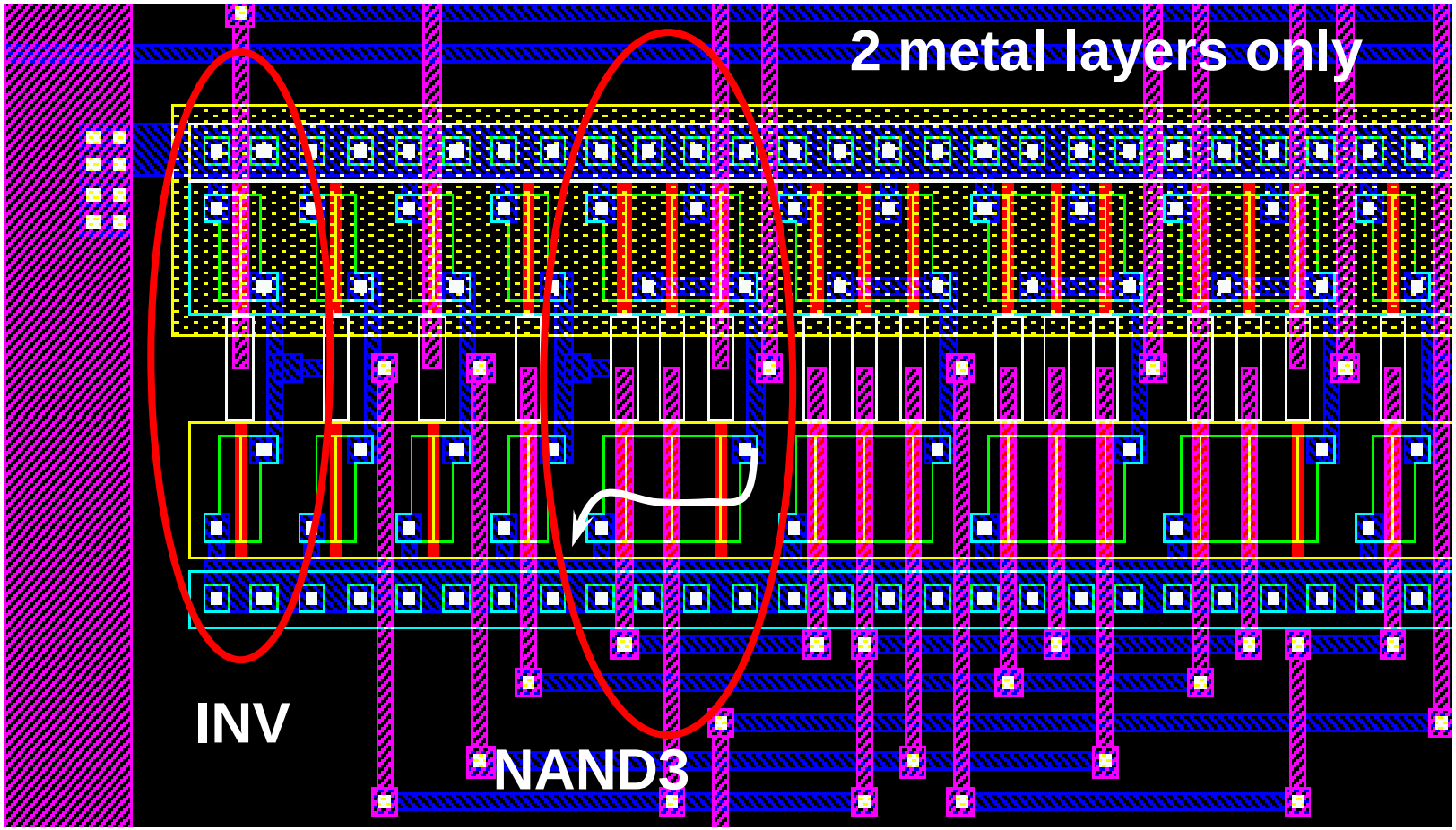
Standard cell IC:



Detail of a standard cell IC:



Details of a CMOS circuit



Layout extraction: checking, real delays

The same in CAD tools of VLSI design