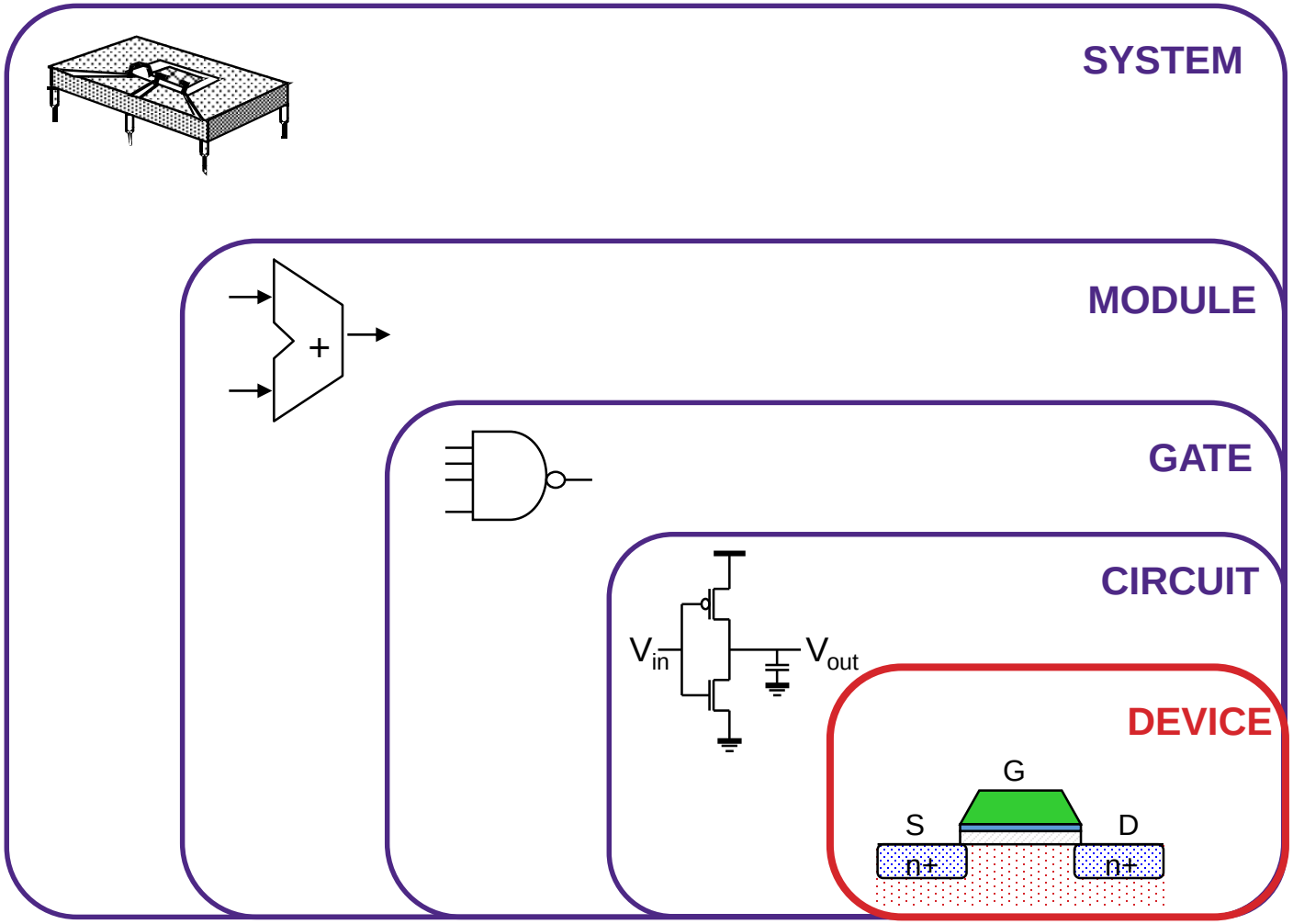
Budapest University of Technology and Economics
Department of Electron Devices

Microelectronics, BSc course

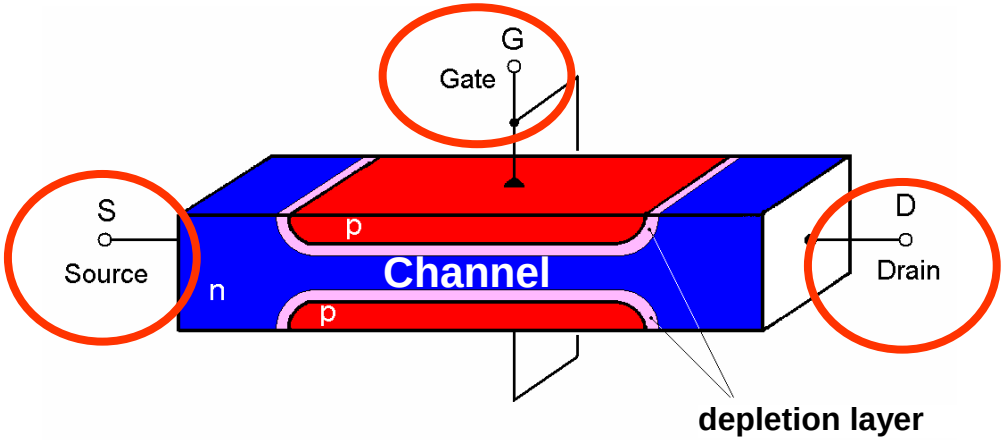
Field effect transistors 2: The MOSFETs

The abstraction level of our study:



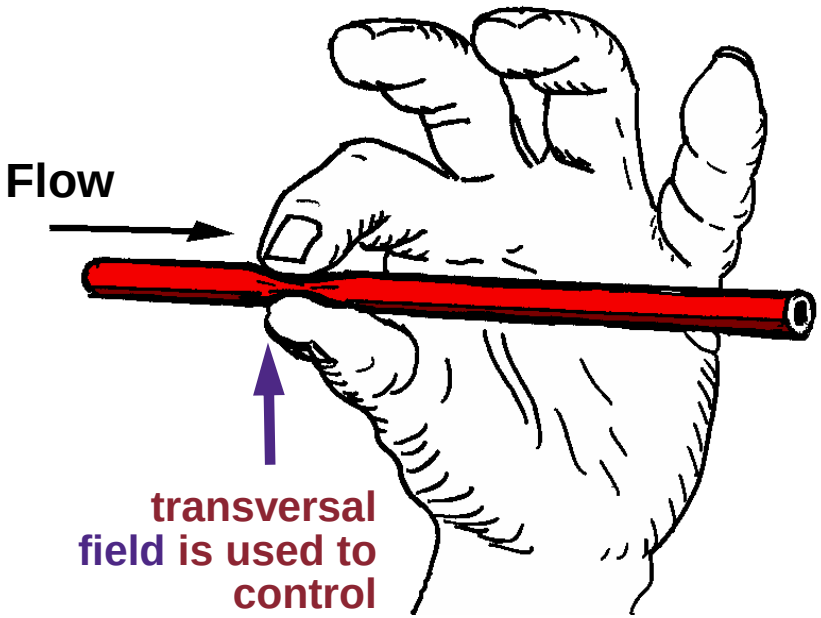
Field effect transistors 1

- FET = **F**ield **E**ffect **T**ransistor – the flow of charge carriers is influenced by electric field



JUNCTION FET: depletion layers of pn-junctions close the channel

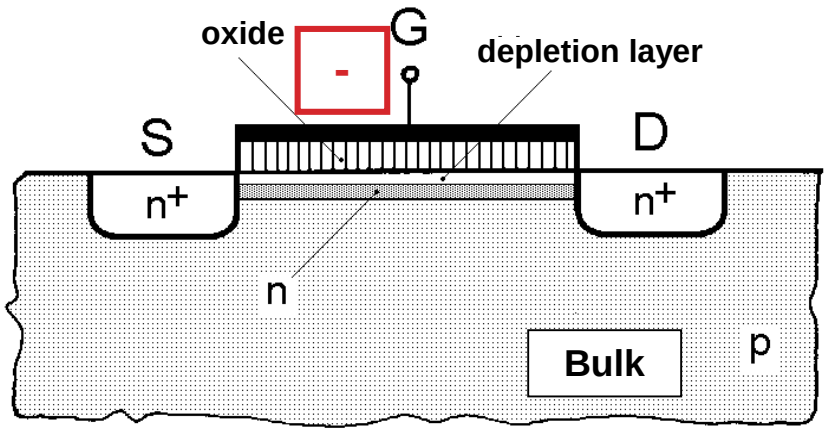
Most important parameter:
U_0 pinch-off voltage



- Unipolar device: current is conducted by majority carriers
- Power needed for controlling the device ≈ 0

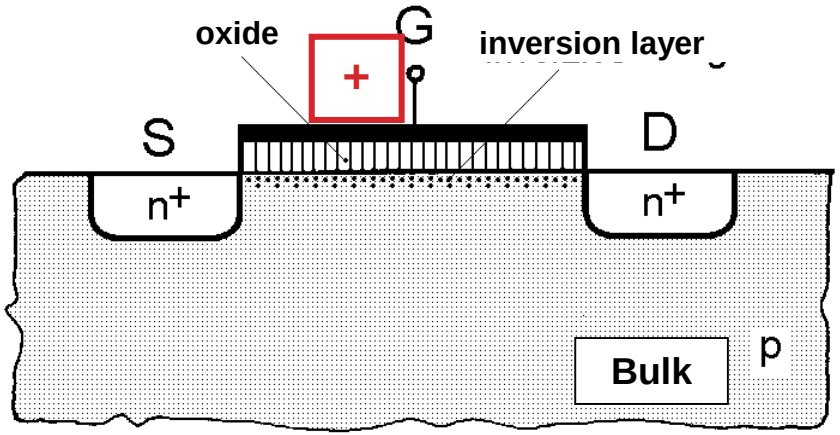
Field effect transistors 2

- MOSFET: **M**etal-**O**xide-**S**emiconductor **FET**



First type: depletion mode device

Most important parameter: U_0 pinch off voltage



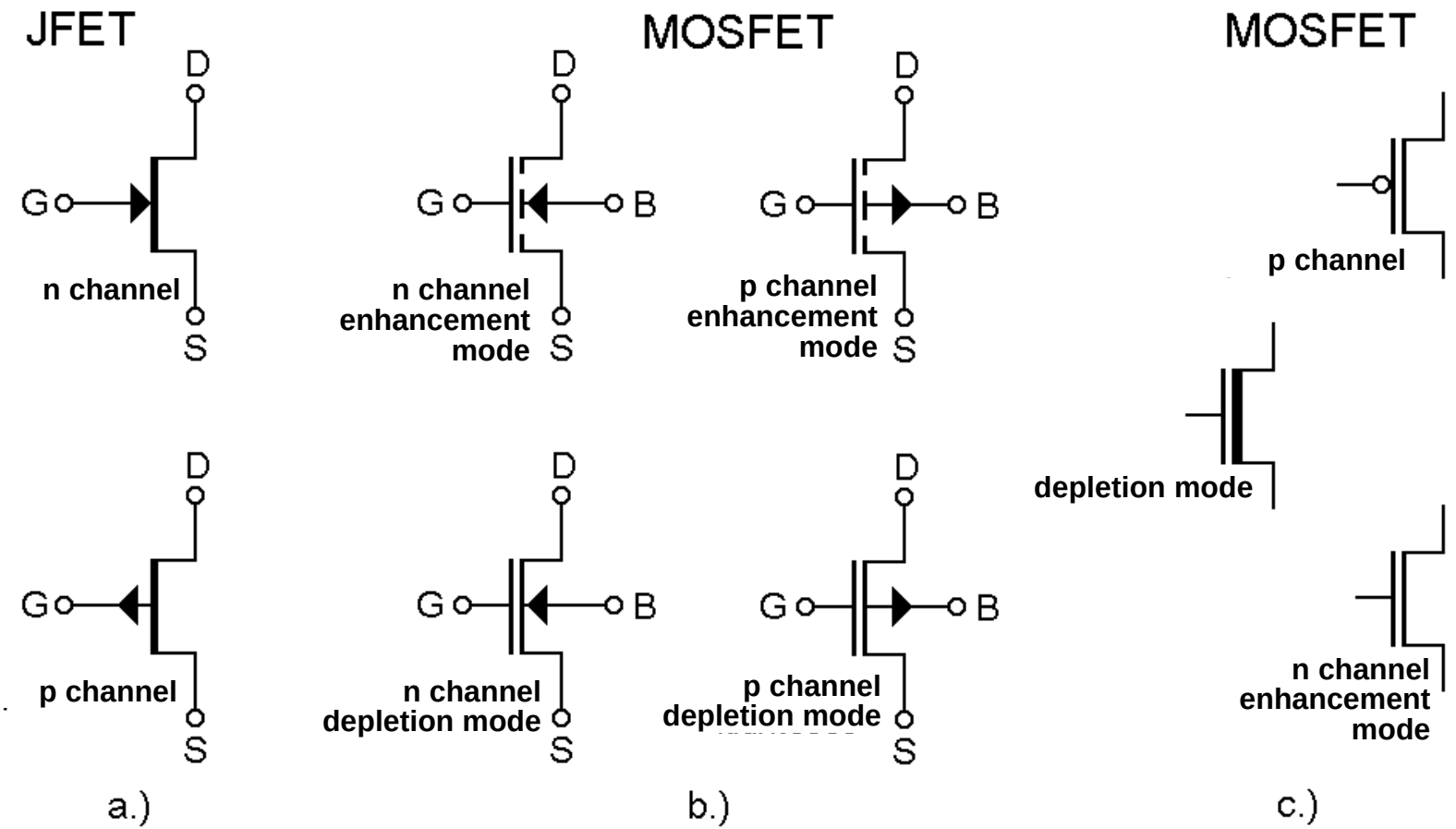
Second type: enhancement mode device

Most important parameter: V_T threshold voltage

Most frequently used today

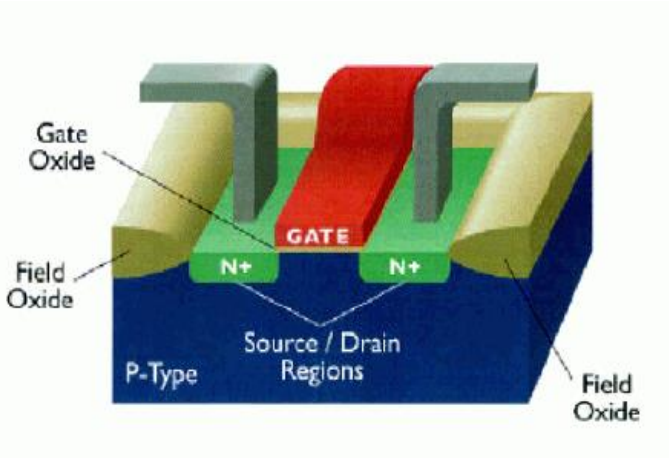
Field effect transistors 3

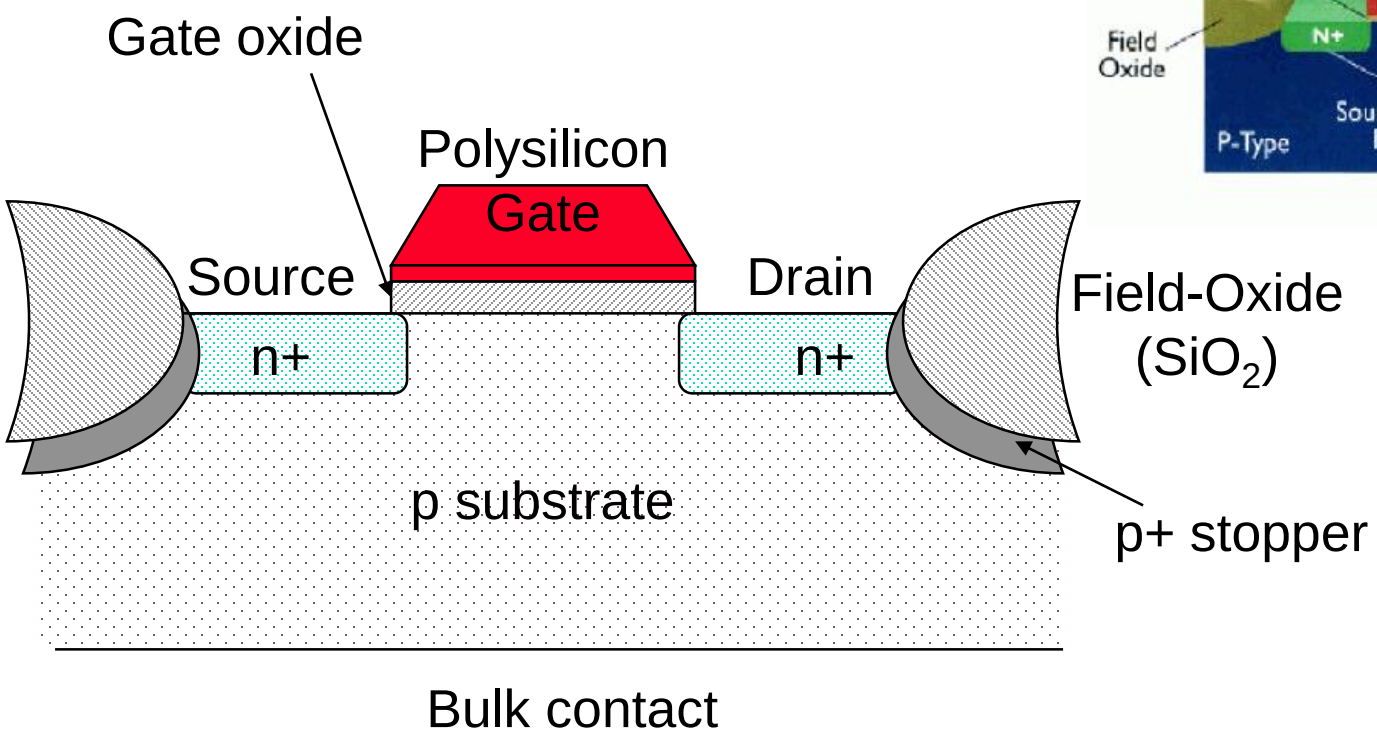
- Symbols:



MOSFETs

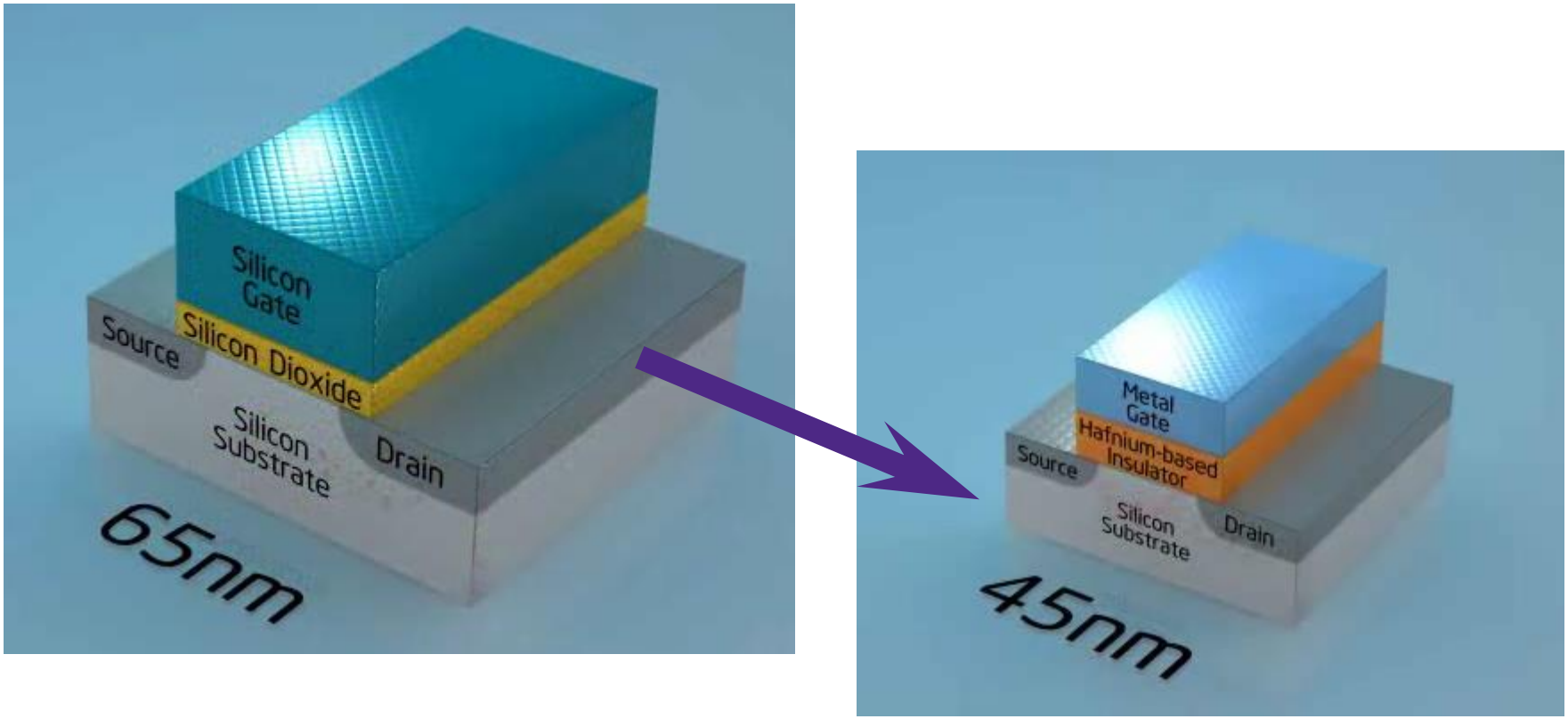
- More realistic cross-sectional view of enhnacement mode MOSFETs:





The most modern MOSFETs:

- **2007/2008 …** Intel:

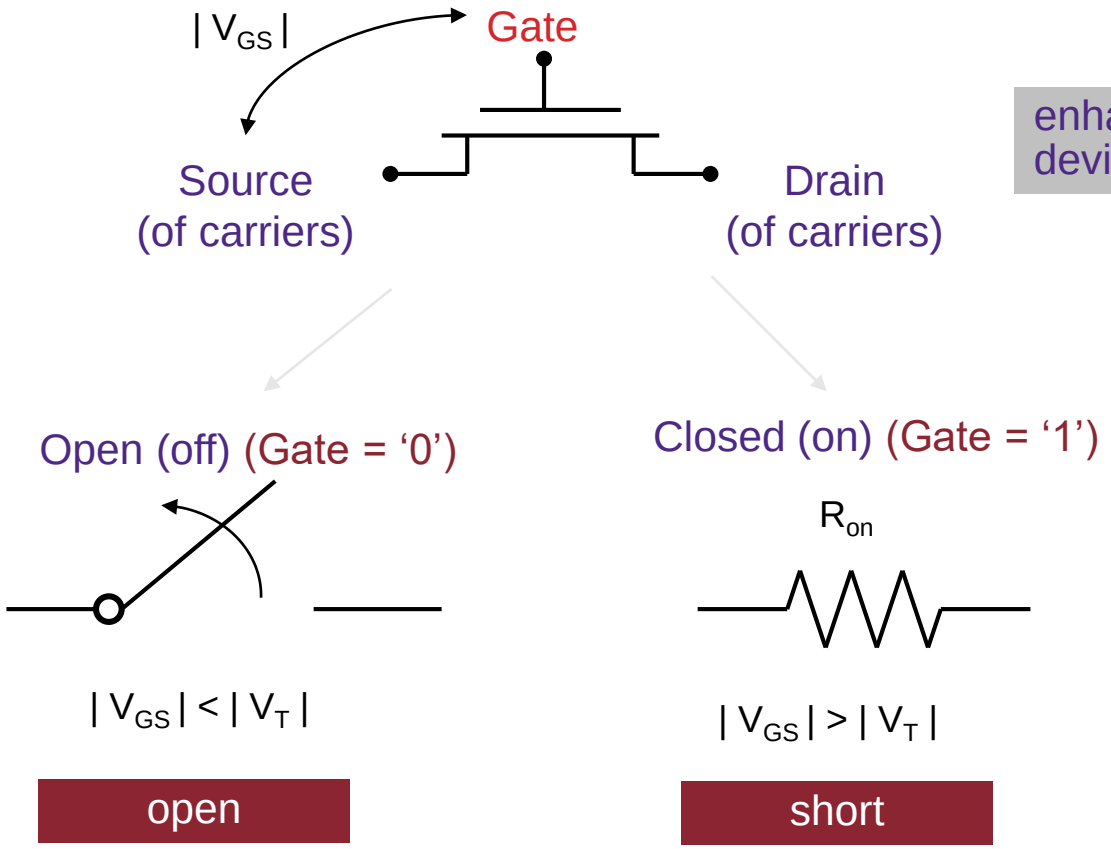


Further topics:

- Overview of operation of MOS transistors
- Characteristics
- Secondary effects
- Models

Operation of MOSFETs

- The simplest (logic) model:
  - open (off) / short (on)

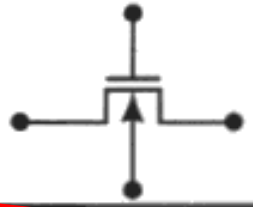
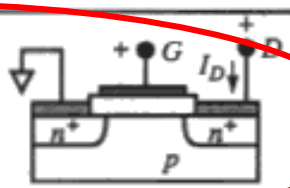
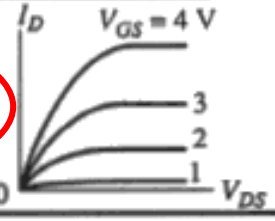
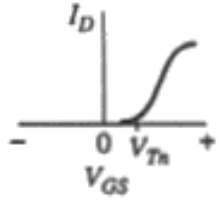
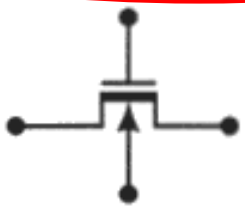
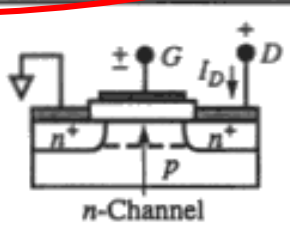
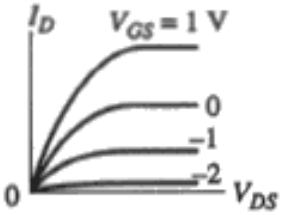
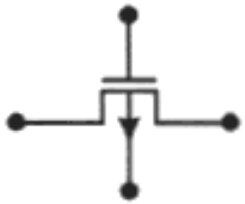
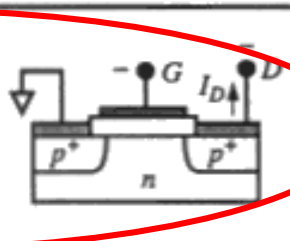
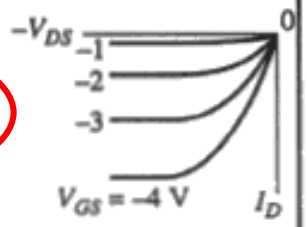
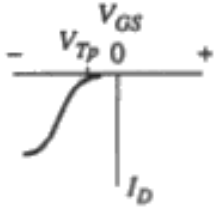
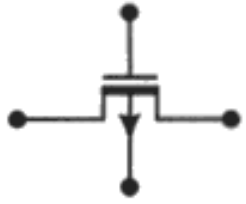
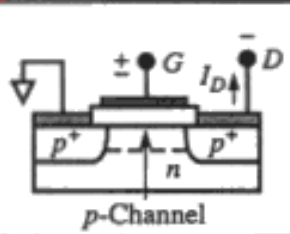
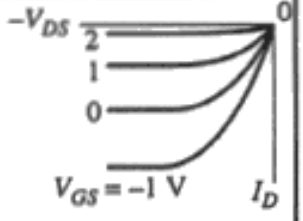
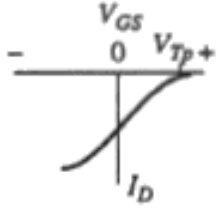


Operation of MOSFETs

- n-channel device:
  - electrons are flowing
- p-channel device:
  - holes are flowing
  - same operation, change of the signs

- **Normally OFF device:** at 0 gate (control) voltage the are "open" (enhancement mode device)
- **Normally ON device:** at 0 gate (control) voltage the are "short" (depletion mode device)

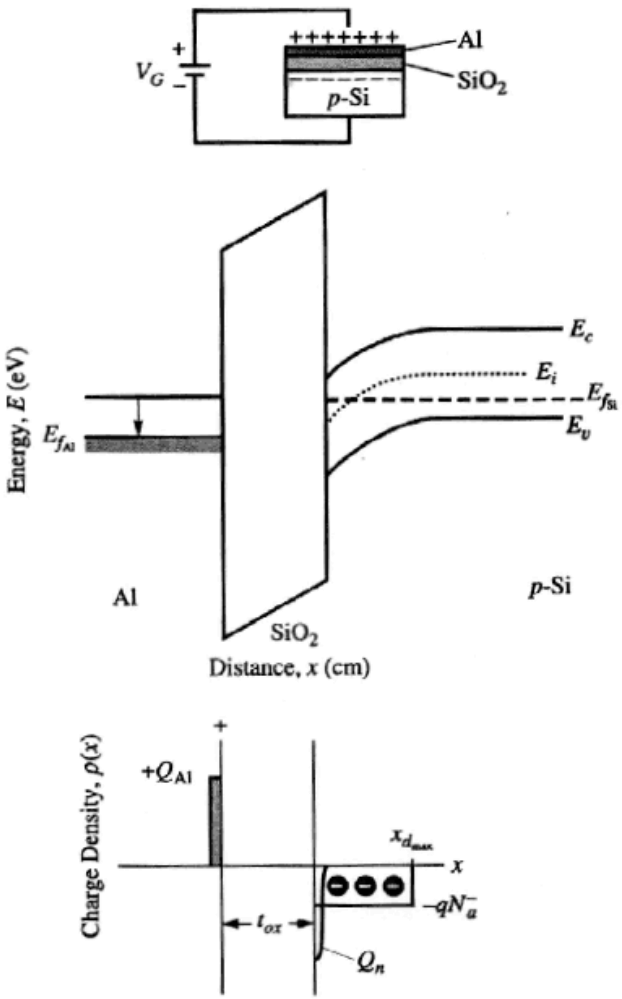
Overview of MOSFET types

Type	Circuit Symbol	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)				
n-Channel Depletion (Normally On)				
p-Channel Enhancement (Normally Off)				
p-Channel Depletion (Normally On)				

Overview of the operation

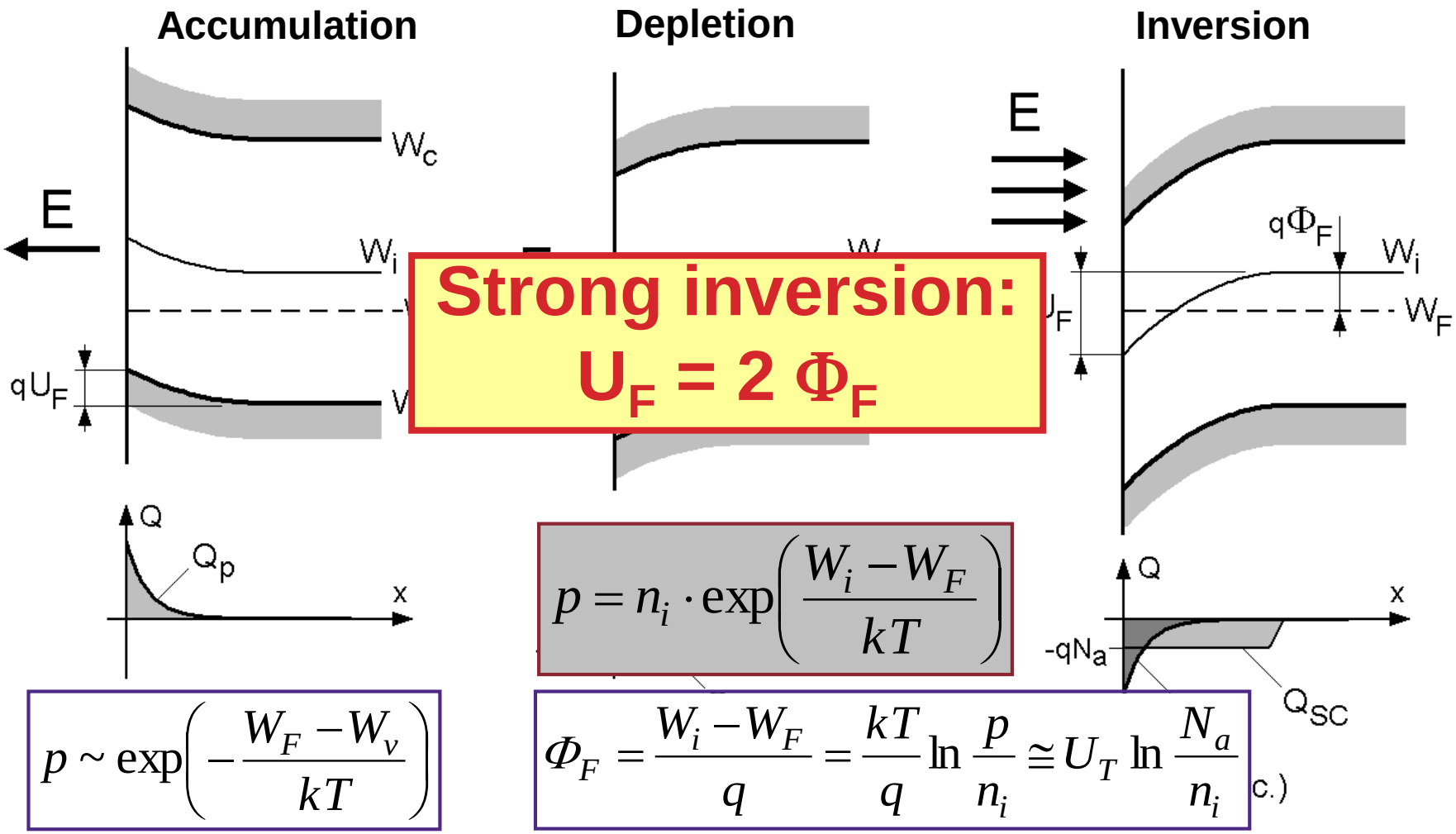
- The operation is based on the so called MOS capacitance:

- As a result of electrical field perpendicular to the gate surface
  - positive charges accumulate at the metal (gate)
  - in the p-type semiconductor
    - first the positive charges are "swept" out and a depletion layer is formed
    - further increasing the electric field, negative carriers are collected from the bulk under the metal
    - if the voltage at the surface exceeds a threshold value, the type of the semiconductor gets „inverted": an ***inversion layer*** is formed
- V_T threshold voltage – the minimal voltage needed to form the inversion layer; depends on:
  - the energy levels of the semiconductor material
  - the thickness and the dielectric constant of the oxide (SiO_2)
  - the doping level and dielectric constant of the semiconductor (Si)



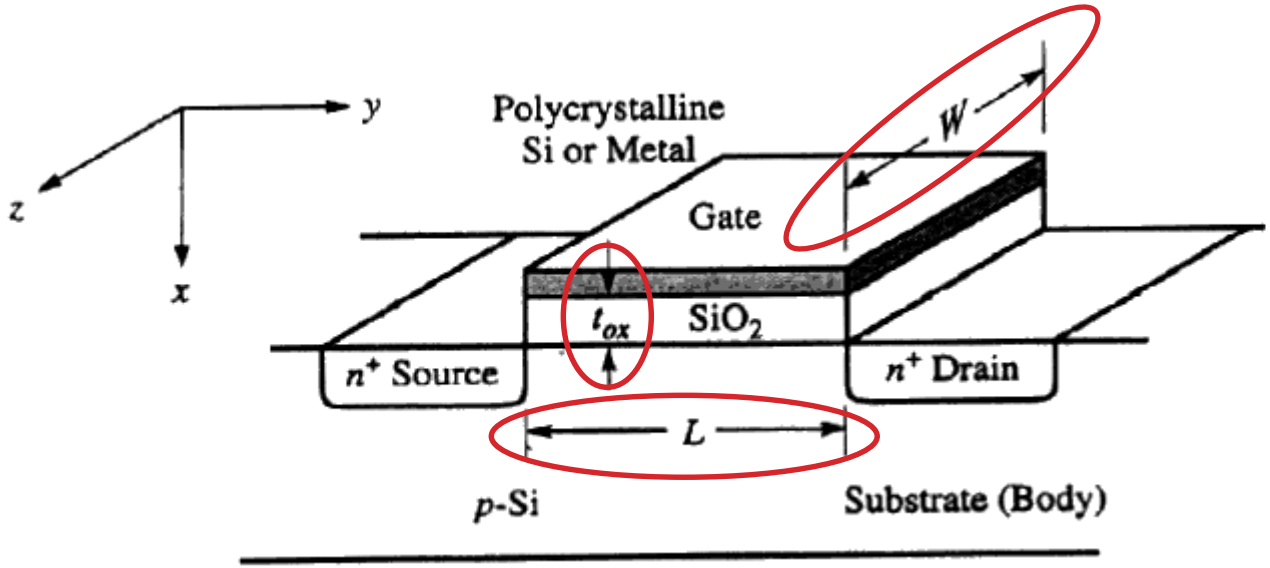
Overview of the operation

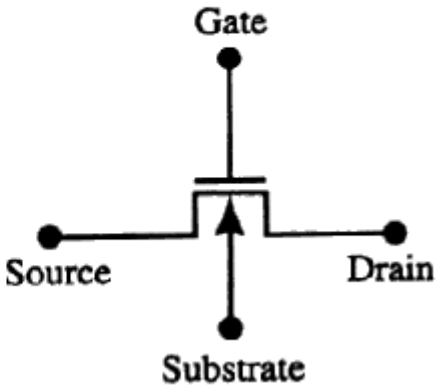
- Surface phenomena in case of the MOS capacitance



The MOS transistor

- MOS capacitance completed by two electrodes at its two sides:

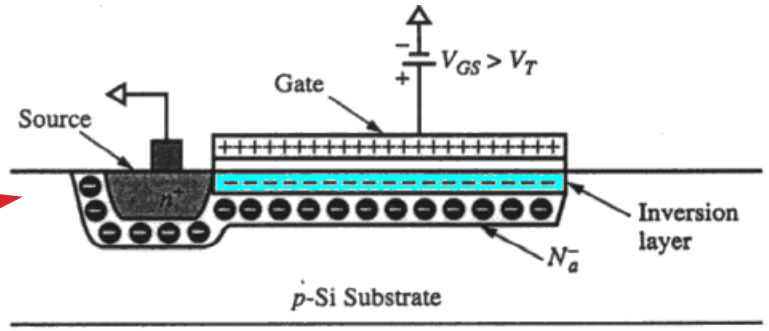


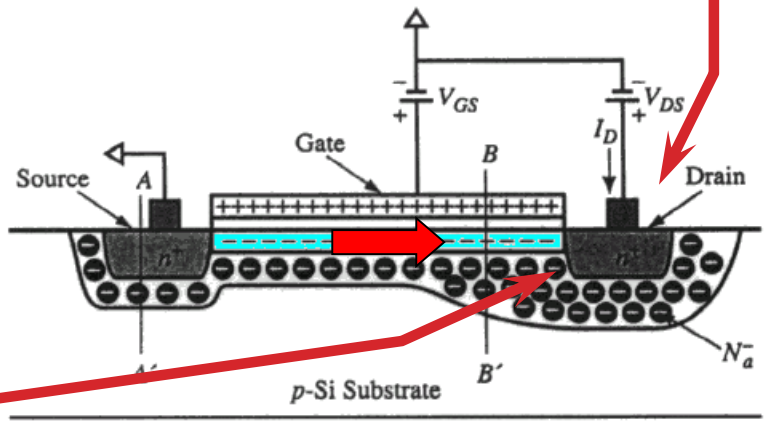


- **n-channel** device: current conducted by **electrons**
- **p-channel** device: current conducted by **holes**

Qualitative operation of the MOSFET

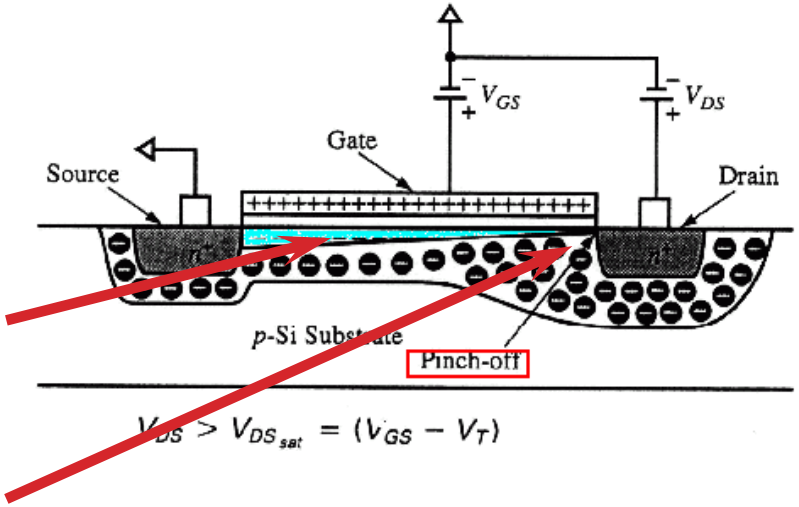
- If $V_{GS} > V_T$, inversion layer is formed
  - the n+ region at the *source* can inject electrons into the inversion channel
  - the positive potential at the *drain* induces flow of electrons in the channel,
  - the positive potential of the drain *reverse biases* the pn junction formed there
  - the electrons drifted there are all sank in the n+ region and the circuit is closed





Qualitative operation of the MOSFET

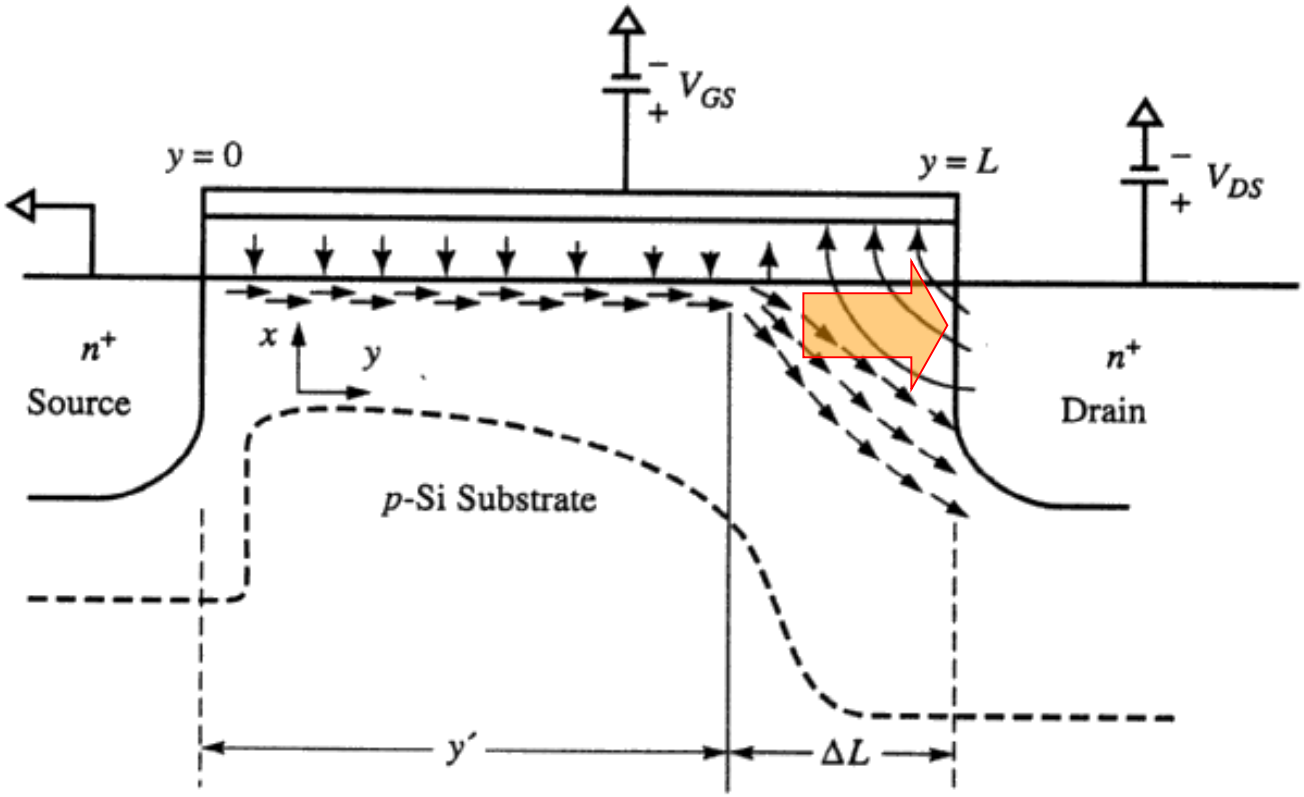
- the charge density in channel depends on the V_{GS} voltage
- there is a *voltage drop* in the channel, thus, the thickness of the inversion layer will deminish along the channel
- at a given V_{DSsat} *saturation voltage* the thickness will reach 0, this is the so called pinch-off



$$V_{DSsat} = V_{GS} - V_T$$

After this voltage is reached, the MOSFET operates ***in saturation mode, the drain voltage does not influence the drain current any longer***.

Qualitative operation of the MOSFET



In the *pinch-off* region the charge transport takes place by means of diffusion current.

I-V characteristics

- output characteristics: $I_D=f(U_{DS})$, parameter: U_{GS}
- input characteristics: $I_D=f(U_{GS})$

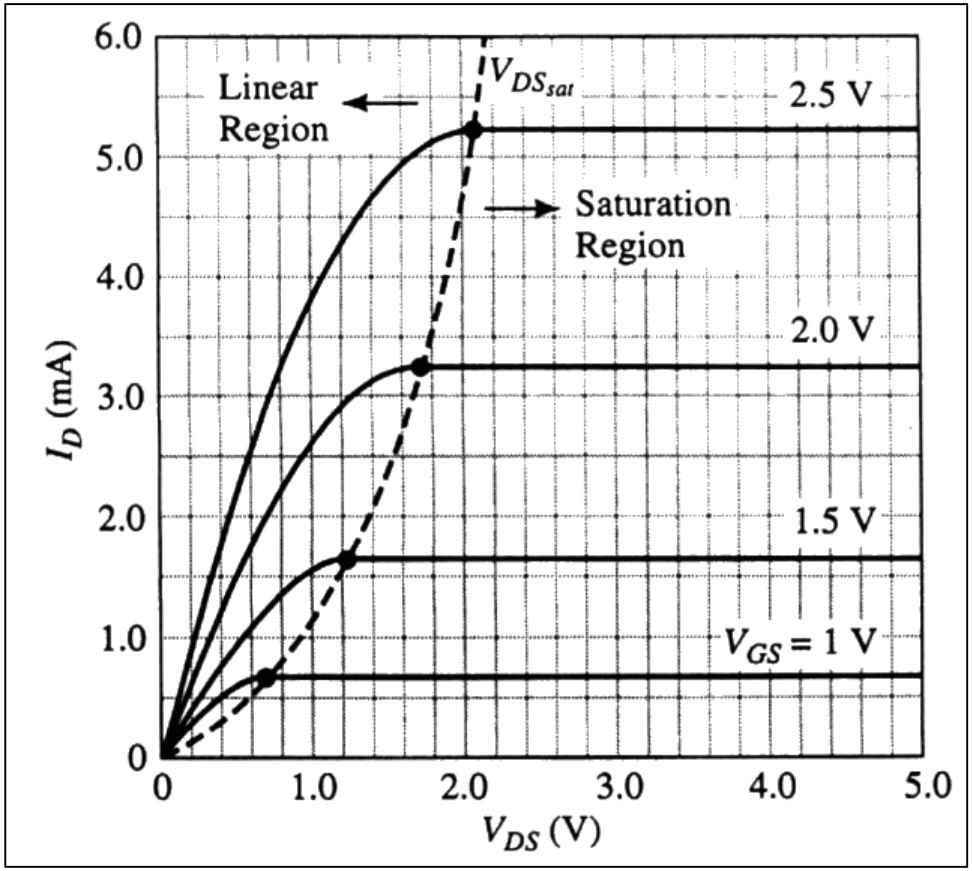
Output characteristics:

In saturation:

$$I_D = \frac{W}{L}\frac{\mu_n}{2}\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{GS}-V_T\right)^2$$

$$K = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$ *current constant*

The circuit designer can change the geometry only: the W width and the L length



Example

Calculate the saturation current of a MOSFET for U_{GS}=5V if

$$K = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} = 110 \mu A/V^2$$

V_T =1V, and the geometry

a) W= 5μm, L=0.4μm ,
b) W= 0.8μm, L=5μm !

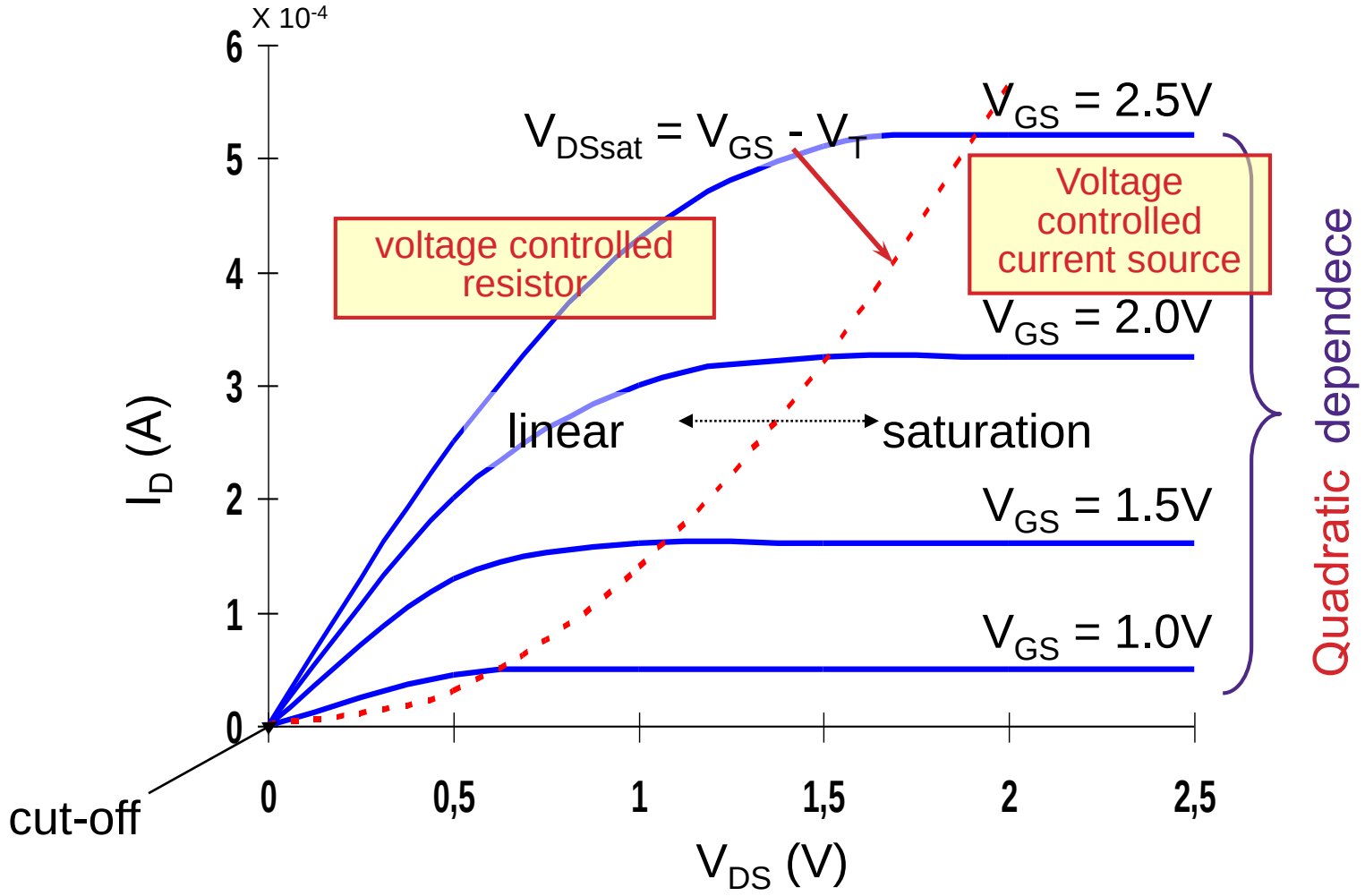
---

a) $$I_D = \frac{W}{L}\frac{K}{2}(U_{GS} - V_T)^2 = \frac{5}{0.4}\frac{110}{2}10^{-6}(5-1)^2 = 11 \cdot 10^{-3} A = \underline{11mA}$$

b) $$I_D = \frac{W}{L}\frac{K}{2}(U_{GS} - V_T)^2 = \frac{0.8}{5}\frac{110}{2}10^{-6}(5-1)^2 = 141 \cdot 10^{-6} A = \underline{141 \mu A}$$

By changing the **W/L ratio** the drain current can be changed by orders of magnitude

I-V characersitics



nMOS transistor, 0.25um, L_d = 10um, **W/L = 1.5**, V_{DD} = 2.5V, V_T = 0.4V

Overview of the physics:

- Charges and potentials at the surface
- The threshold voltage
- The characteristics
- Secondary effects

Potentials of the MOS structure

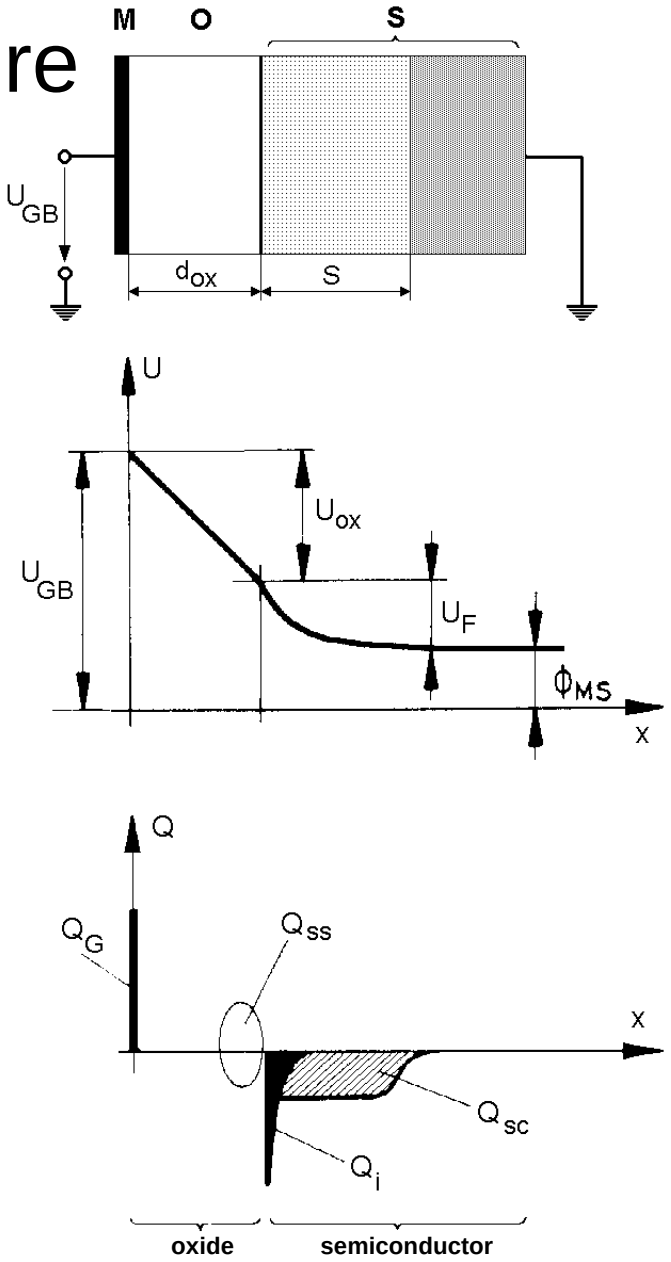
$$U_{GB} = U_{ox} + U_F + \Phi_{MS}$$

$$Q_G = Q_{SC} - Q_{SS} + Q_i$$

$$C_0 = \frac{\varepsilon_{ox}}{d_{ox}}$$

$$Q_G = C_0 U_{ox}$$

$$Q_{SC} = qN_a S$$



Potentials of the MOS structure

$$U_{GB} = U_{ox} + U_F + \Phi_{MS}$$

$$Q_G = Q_{SC} - Q_{SS} + Q_i$$

$$Q_G = C_0 U_{ox}$$

$$Q_{SC} = qN_a S$$

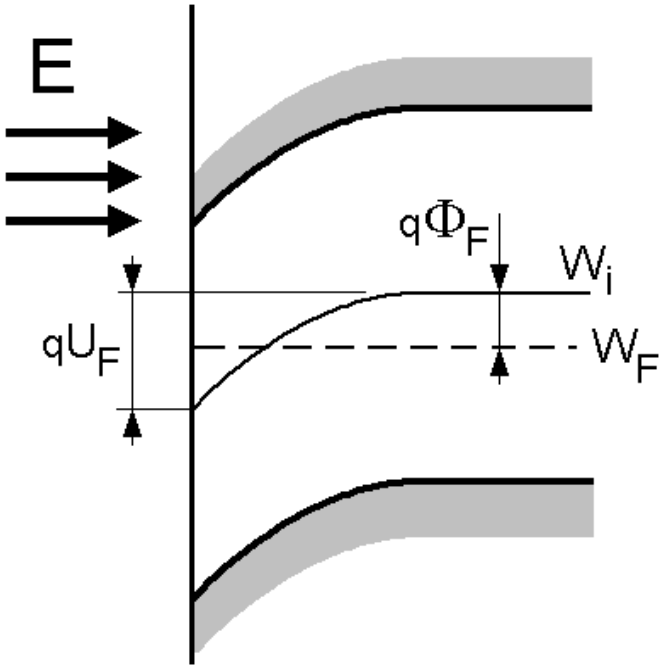
$$Q_i = Q_G - Q_{SC} + Q_{SS} =$$
$$= C_0 U_{ox} - \sqrt{2\varepsilon_s q N_a}\sqrt{U_F} + Q_{SS}$$

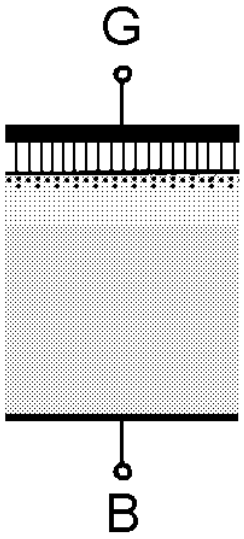
$$Q_i = C_0(U_{GB} - U_F - \Phi_{MS}) -$$
$$- \sqrt{2\varepsilon_s q N_a}\sqrt{U_F} + Q_{SS}$$

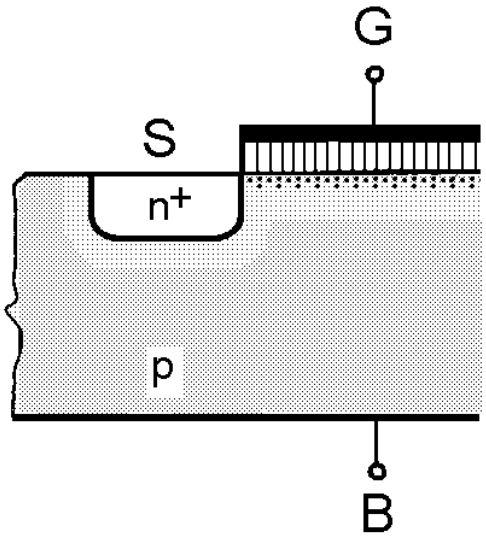
$$Q_{SC} = qN_a\sqrt{\frac{2\varepsilon_s}{qN_a}}\sqrt{U_F} = \sqrt{2\varepsilon_s q N_a}\sqrt{U_F}$$

The threshold voltage of the MOSFET

Inversion







$$U_F = 2\Phi_F$$

$$U_F = 2\Phi_F + U_{SB}$$

The threshold voltage of the MOSFET

$$Q_i = C_0(U_{GB} - 2\Phi_F - U_{SB} - \Phi_{MS}) - \sqrt{2\varepsilon_s q N_a}\sqrt{2\Phi_F + U_{SB}} + Q_{SS}$$

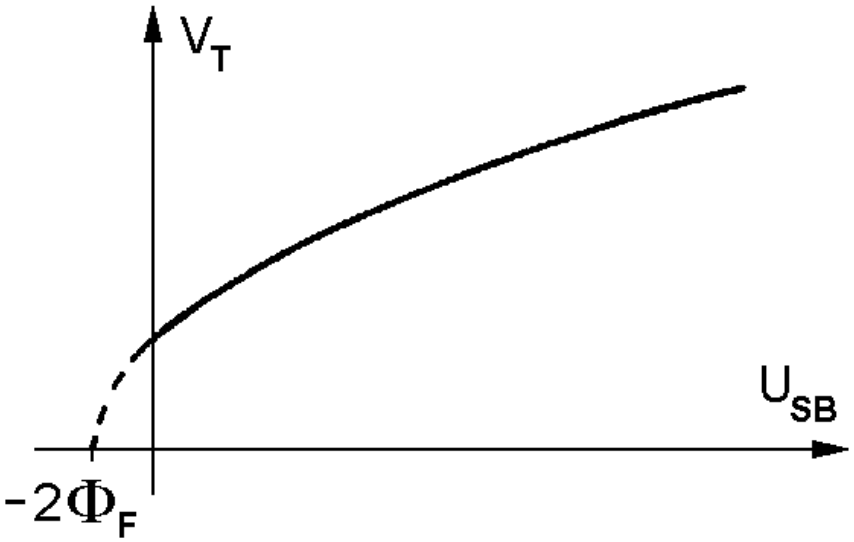
$$V_T = U_{GS}\big|_{Q_i=0}$$

$$Q_i \cong C_0\left(U_{GS} - V_T\right)$$

$$V_T = 2\Phi_F + \Phi_{MS} - \frac{Q_{SS}}{C_0} + \frac{\sqrt{2\varepsilon_s q N_a}}{C_0}\sqrt{2\Phi_F + U_{SB}}$$

The threshold voltage of the MOSFET

$$V_T = 2\Phi_F + \Phi_{MS} - \frac{Q_{SS}}{C_0} + \frac{\sqrt{2\varepsilon_s q N_a}}{C_0}\sqrt{2\Phi_F + U_{SB}}$$



Flat-band potential:

$$\Phi_{FB} = \Phi_{MS} - \frac{Q_{SS}}{C_0}$$

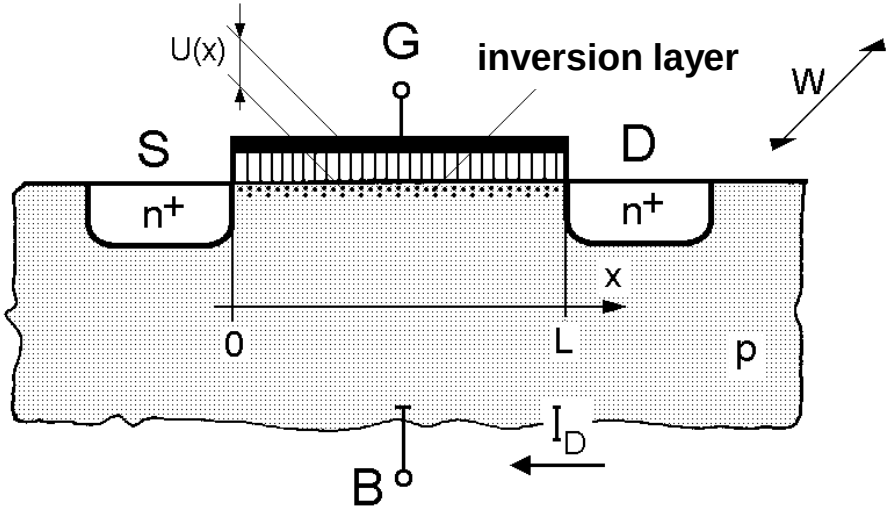
Bulk constant:

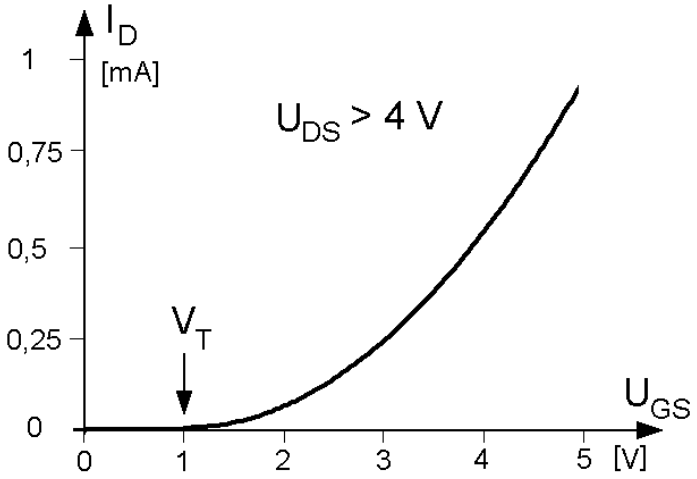
$$P = \frac{\sqrt{2\varepsilon_s q N_a}}{C_0}$$

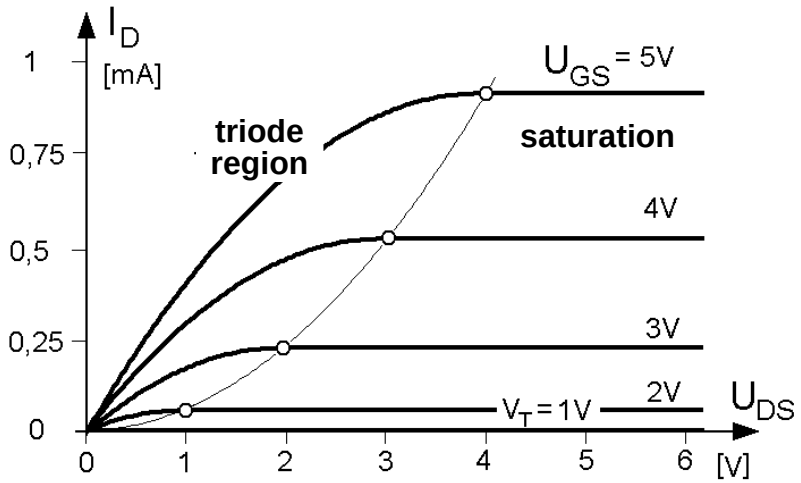
$$V_T = 2\Phi_F + \Phi_{FB} + P\sqrt{2\Phi_F + U_{SB}}$$

The char. of an enhancement mode MOSFET

Later we shall calculate these!



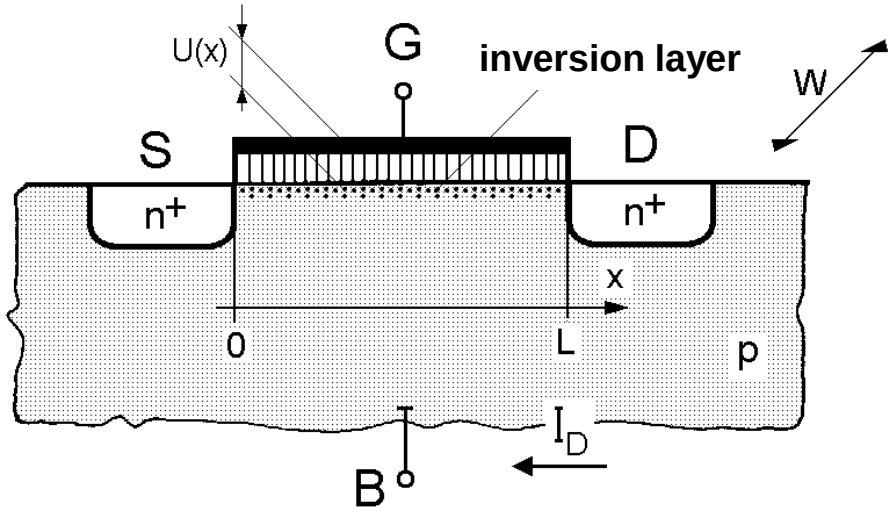




Derivation of the characteristic

$U(0) = U_{GS}$, $U(L) = U_{GD}$

$Q_i(U) = Q_i[U(x)]$



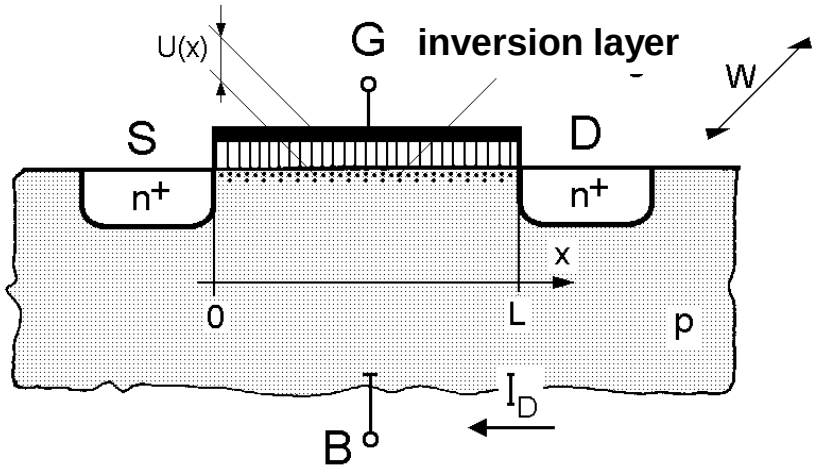
$$I_D = Q_i W v$$

$$v = -\mu E = -\mu \frac{dU}{dx}$$

$$I_D = -Q_i(U) W \mu \frac{dU}{dx} \Rightarrow \int_0^L I_D dx = -W\mu \int_0^L Q_i \frac{dU}{dx} dx$$

Derivation of the characteristic

$$\int_0^L I_D dx = -W\mu \int_0^L Q_i \frac{dU}{dx} dx$$



$$I_D L = -W\mu \int_{U_{GS}}^{U_{GD}} Q_i(U)\, dU$$

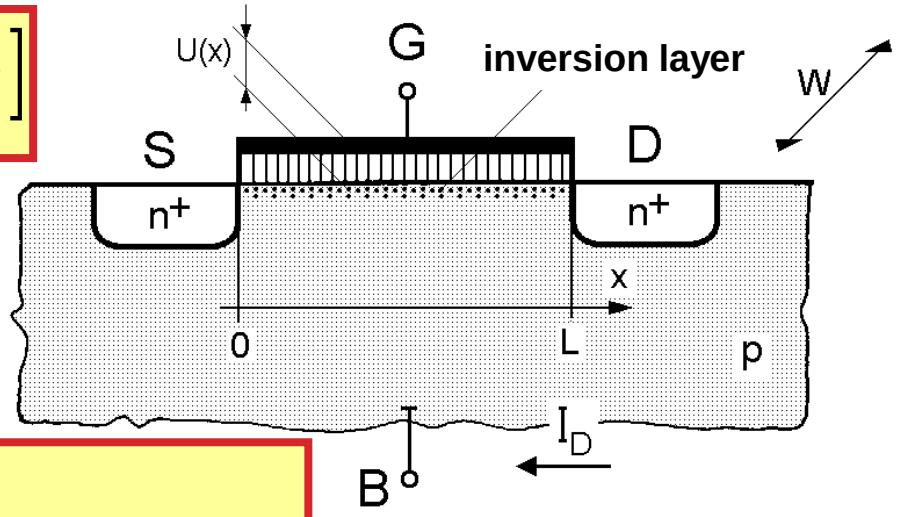
$$Q_i = C_0\left(U(x) - V_T\right)$$

$$I_D = -\frac{W}{L}\mu \int_{U_{GS}}^{U_{GD}} C_0\left(U - V_T\right) dU = \frac{W}{L}\frac{\mu C_0}{2}\left(U - V_T\right)^2 \Big|_{U_{GD}}^{U_{GS}}$$

$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left[\left(U_{GS} - V_T\right)^2 - \left(U_{GD} - V_T\right)^2\right]$$

Derivation of the characteristic

$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left[(U_{GS} - V_T)^2 - (U_{GD} - V_T)^2\right]$$



$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left[F(U_{GS}) - F(U_{GD})\right]$$

$$F(U) = \begin{cases} (U - V_T)^2 & \text{if} \quad U > V_T \\ 0 & \text{if} \quad U \le V_T \end{cases}$$

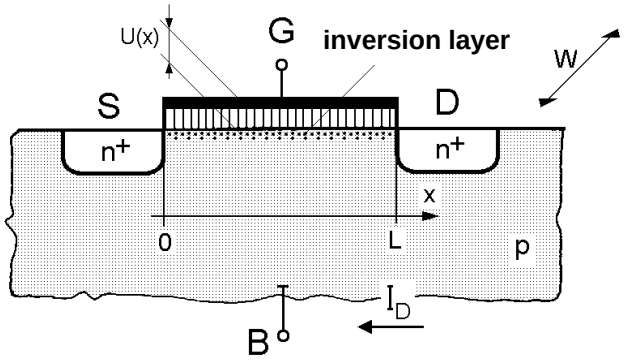
For all regions of operation!

The saturation region

$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left[F(U_{GS}) - F(U_{GD})\right]$$

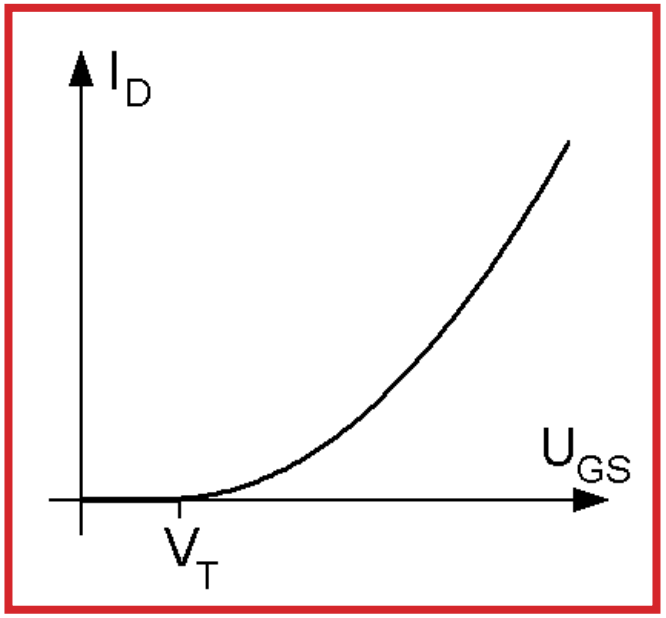
$$F(U) = \begin{cases} (U - V_T)^2 & ha \quad U > V_T \\ 0 & ha \quad U \le V_T \end{cases}$$

For all regions of operation!

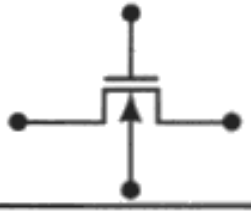
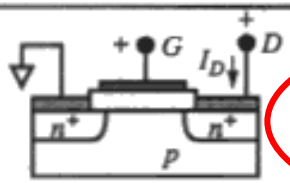
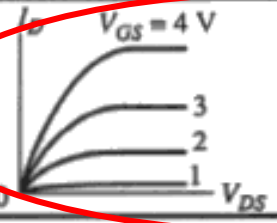
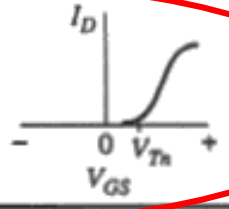
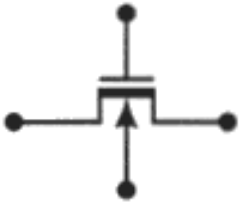
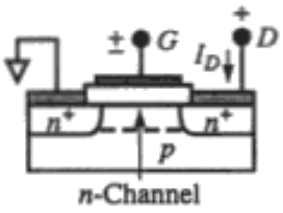
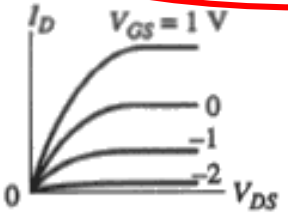
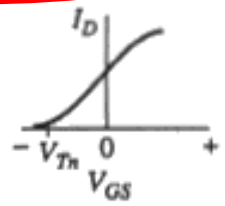
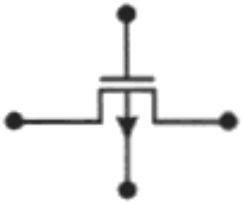
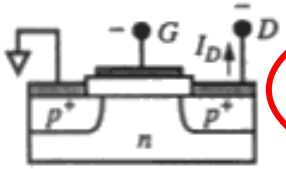
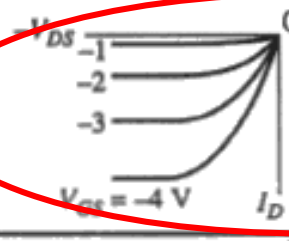
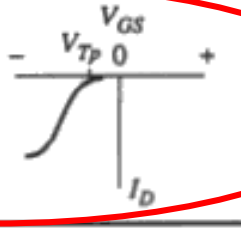
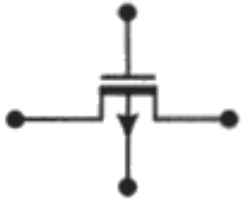
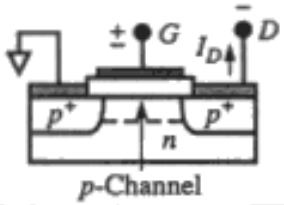
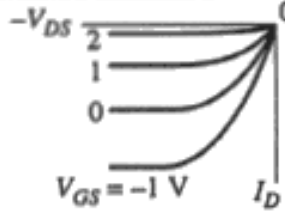
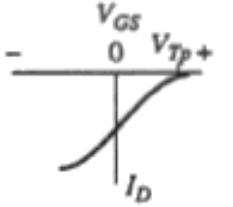


Saturation: $U_{GD} < V_T$

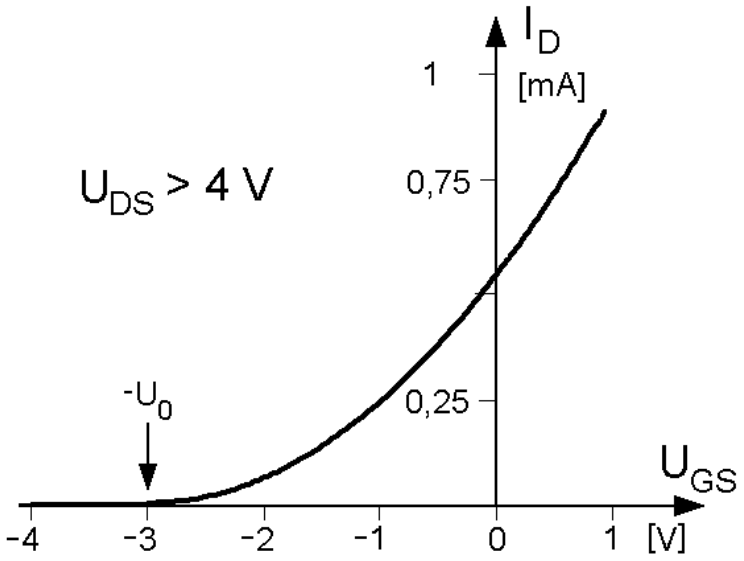
$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left(U_{GS} - V_T\right)^2$$

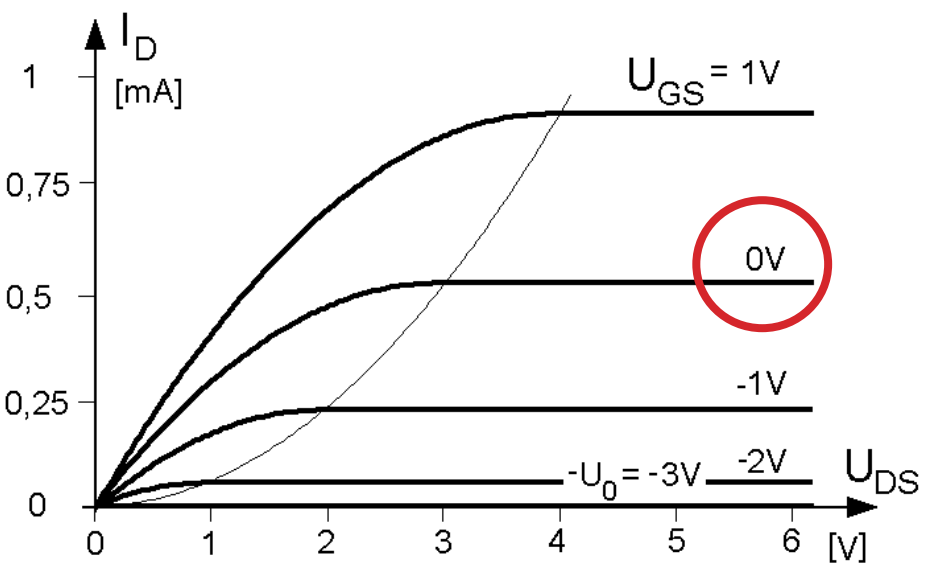


Overview of all types of MOSFETs

Type	Circuit Symbol	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)				
n-Channel Depletion (Normally On)				
p-Channel Enhancement (Normally Off)				
p-Channel Depletion (Normally On)				

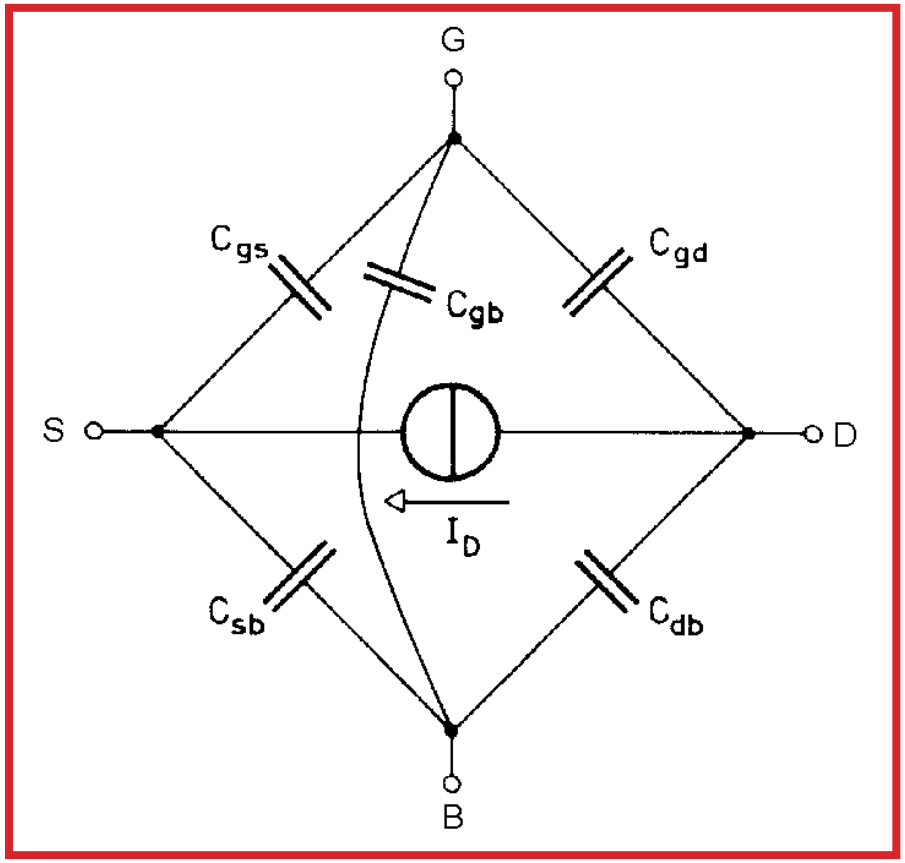
Depletion mode MOSFET

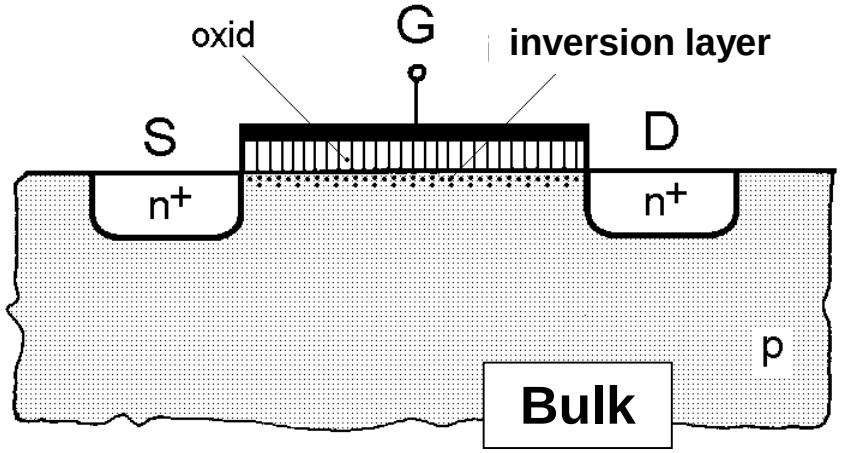




Like an enhance mode MOSFET with a negative threshold voltage

Capacitances of the MOSFET





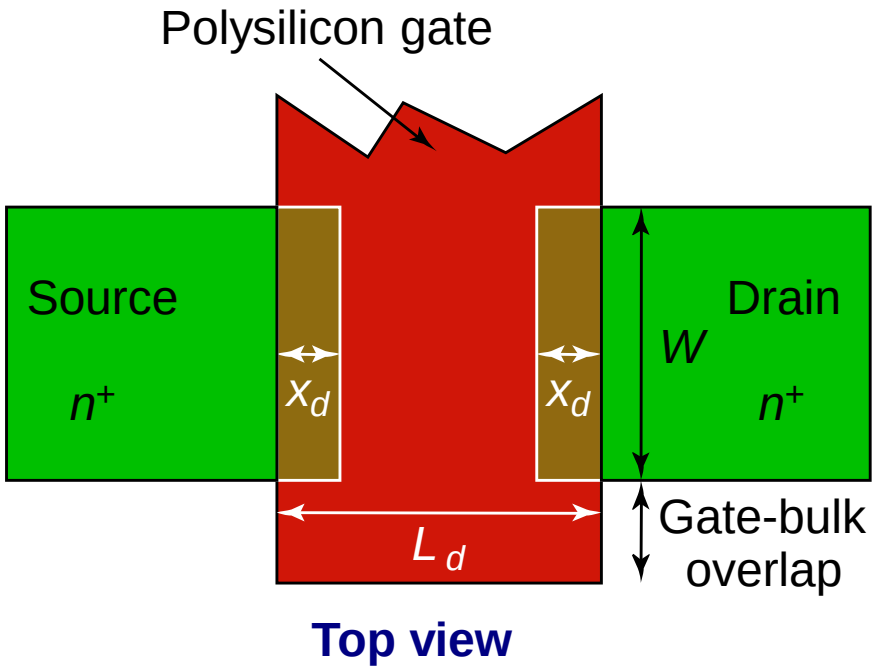
$$Q_G = f_G(U_{GS}, U_{GD}, U_{GB})$$

$$Q_i = f_i(U_{GS}, U_{GD}, U_{GB})$$

S/D – B capacitance: reverse biased PN junction

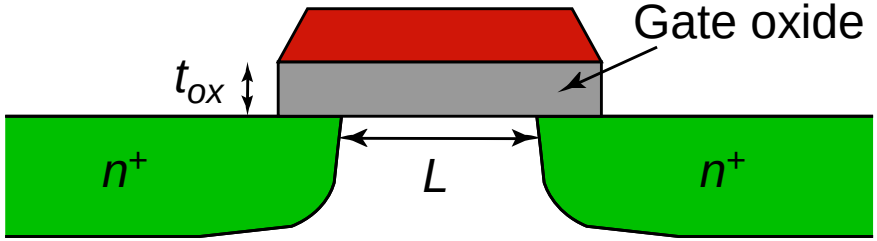
$$C_{gs} = \frac{\partial Q_G}{\partial U_{GS}}$$

The gate capacitance:



Top view

$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

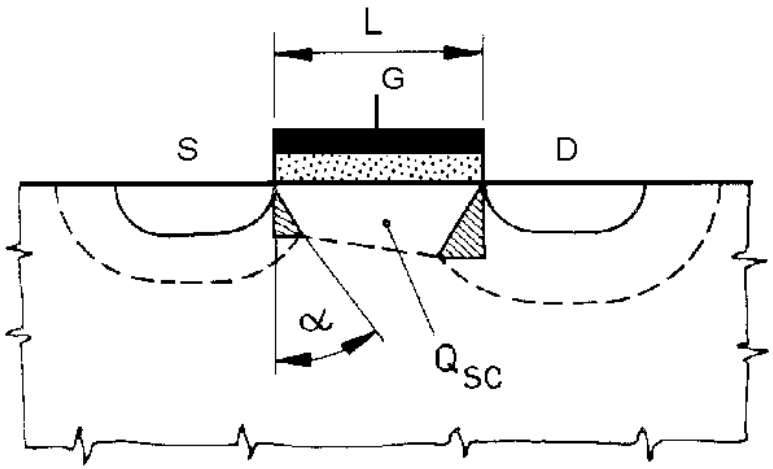


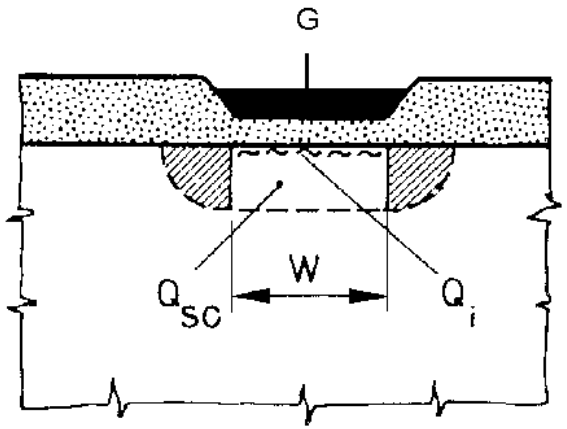
Cross section

Secondary effects

- Short and narrow-channel effects
- Velocity saturation
- Channel length modulation
- Temperature dependence
- Subthreshold current

Dependence of threshold voltage on geometry



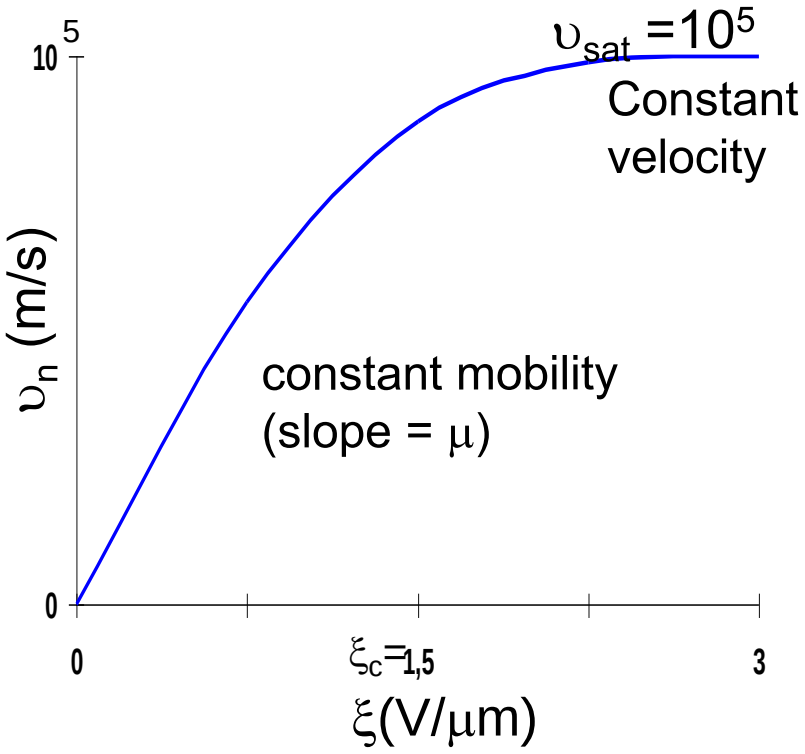


Short channel: V_T decreases

Narrow channel: V_T increases

Velocity saturation

- Influences the operation of short channel devices

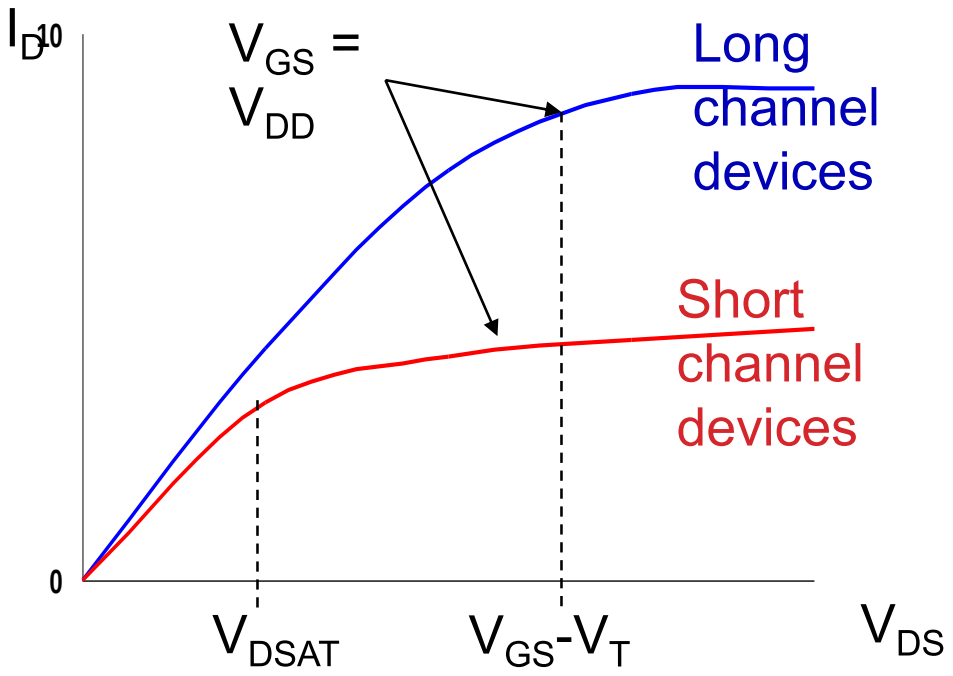


Velocity saturation the speed of carriers (due to the collisions) becomes constant

In a L = 0.25μm channel device a few Volts of D-S voltage may already result in velocity saturation.

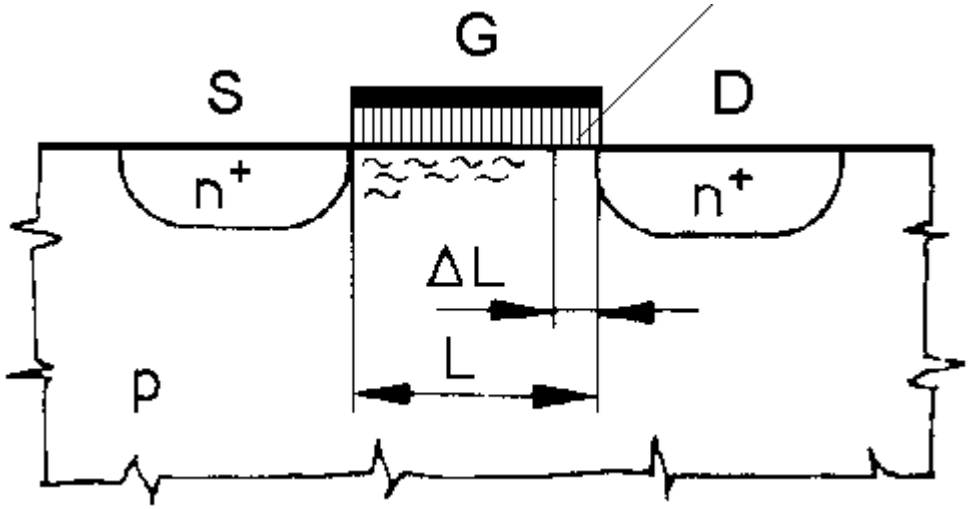
Velocity saturation

- In short channel device velocity saturation takes place sooner (at lower voltage)

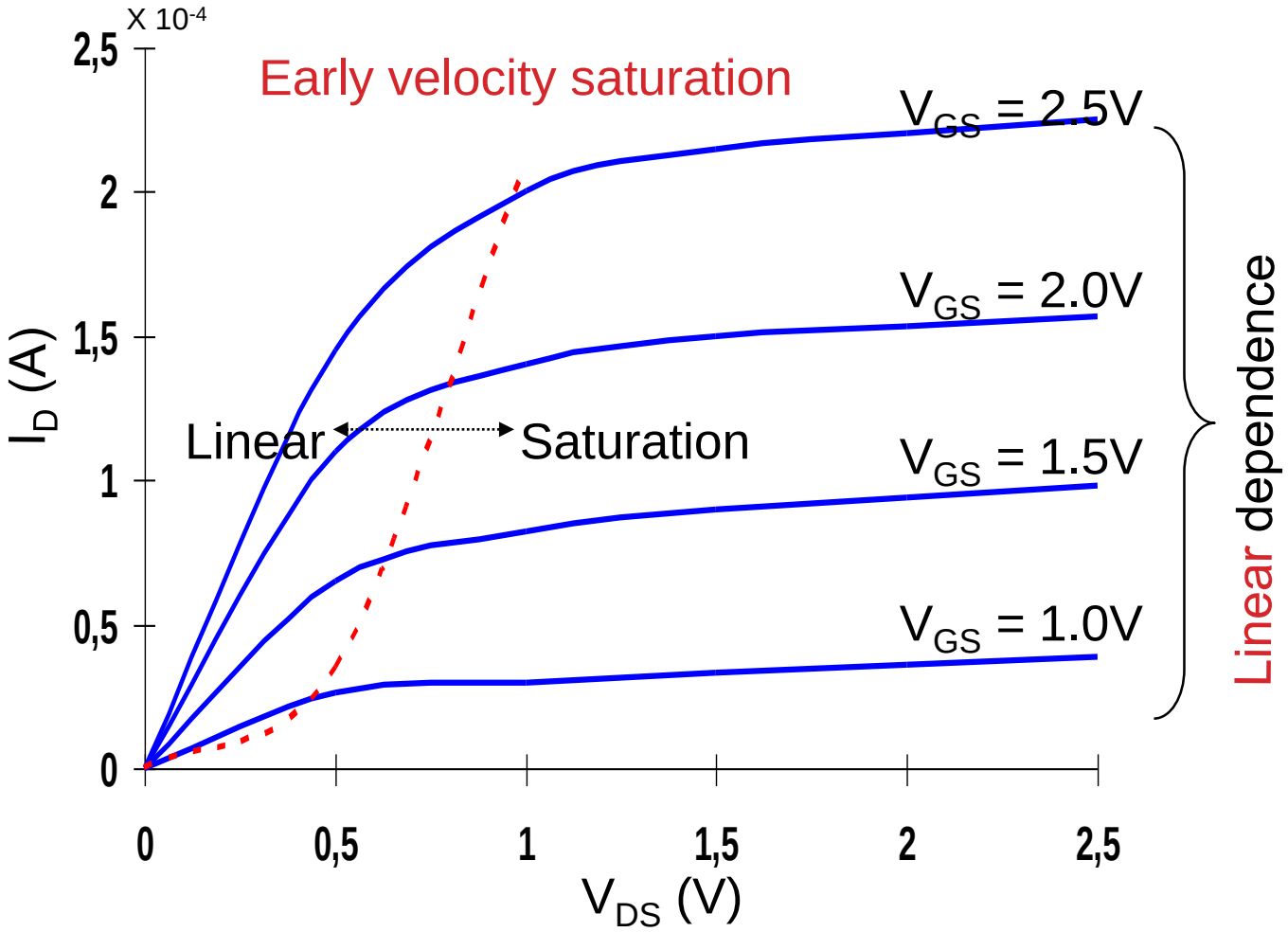


Short channel charactersitics

Channel length modulation



Short channel characersitics



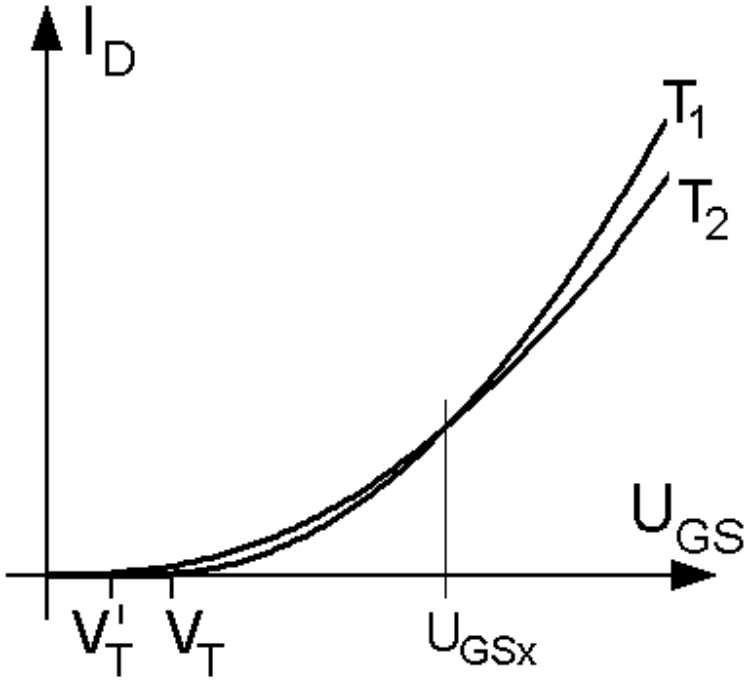
nMOS transistor, 0.25um, L_d = 10um, **W/L = 1.5**, V_{DD} = 2.5V, V_T = 0.4V

Temperature dependence

$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left(U_{GS} - V_T\right)^2$$

$$\frac{1}{\mu}\frac{d\mu}{dT} = -0{,}003 \ldots - 0.006 \ /^o C$$

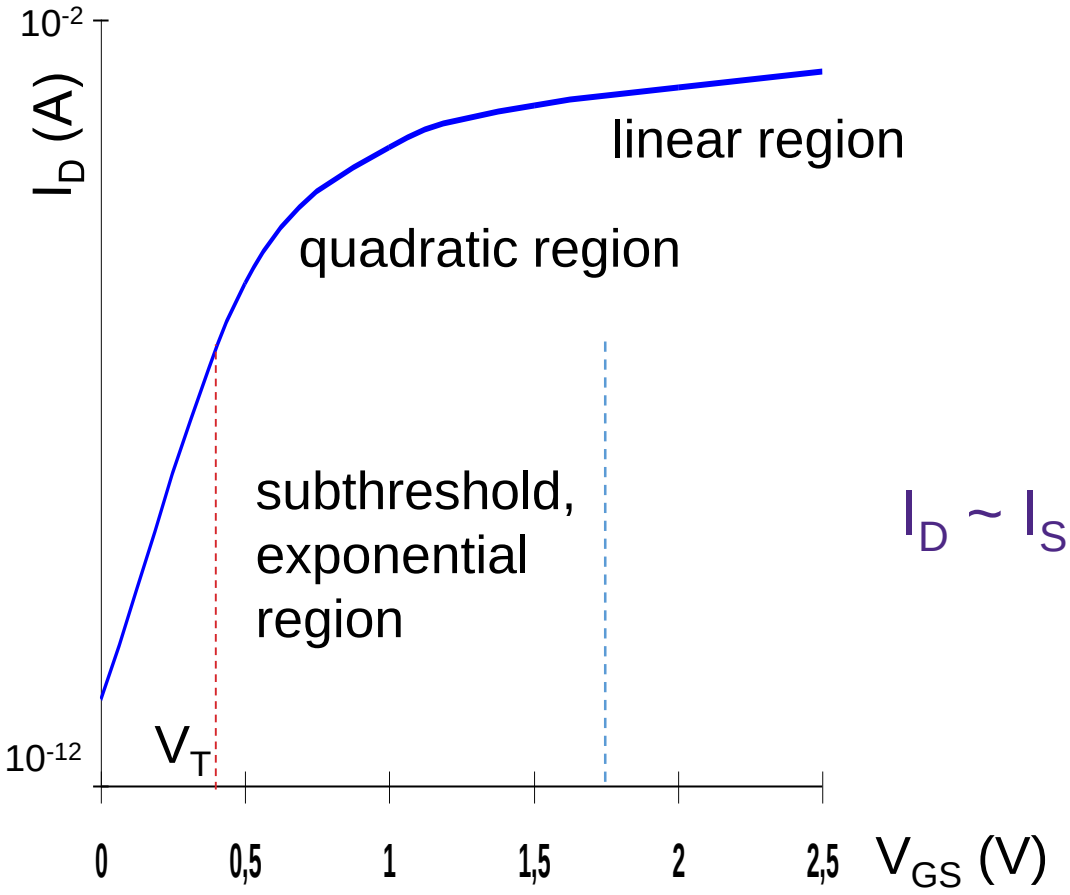
$$\frac{\partial V_T}{\partial T} = -1{,}5 \ldots - 4 \, mV \ /^o C$$



Zero Temperature Coefficient (ZTC) bias point

Subthreshold current

- Assuming a given V_T is rough model; in reality the current vanishes exponentially with the gate voltage:



$$I_D \sim I_S \, e^{(qV_{GS}/nkT)} \quad \text{where} \quad n \geq 1$$

Subthreshold current

- Continuous transition between the ON and OFF states
  - Subthreshold is undesired: strong deviation from the **switch** model

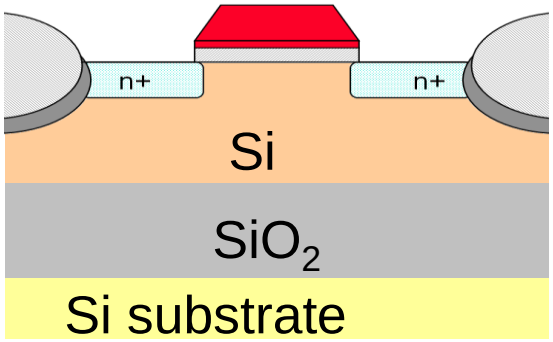
$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

- I_0, n – empirical parameters, n is typically 1.5
- *Slope factor*: S = n (kT/q) ln (10)

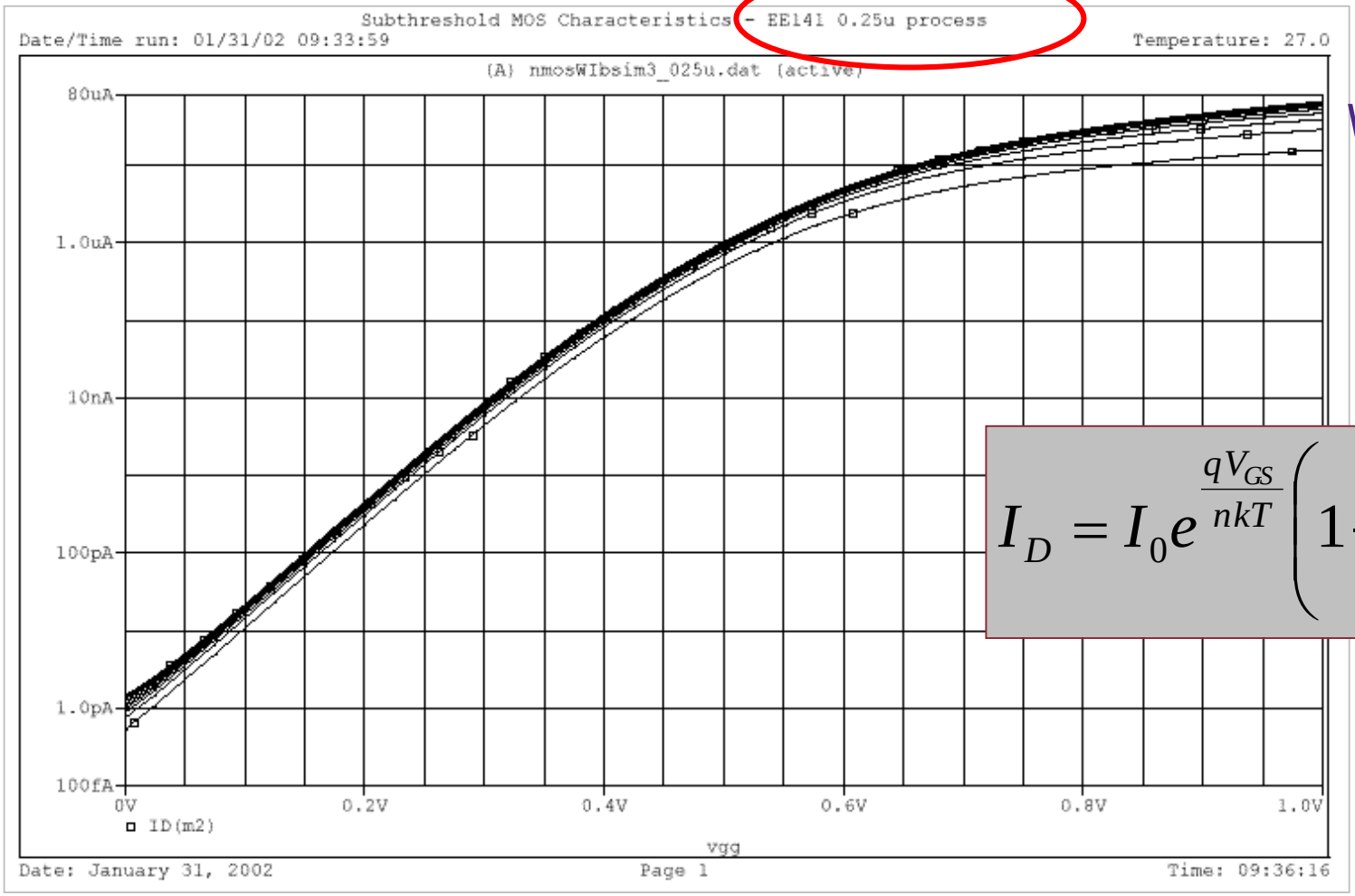
  (typically: 60 ..100 mV/decade) – the smaller the better, depends on.

Can be reduced by SOI:

e.g. SIMOX process



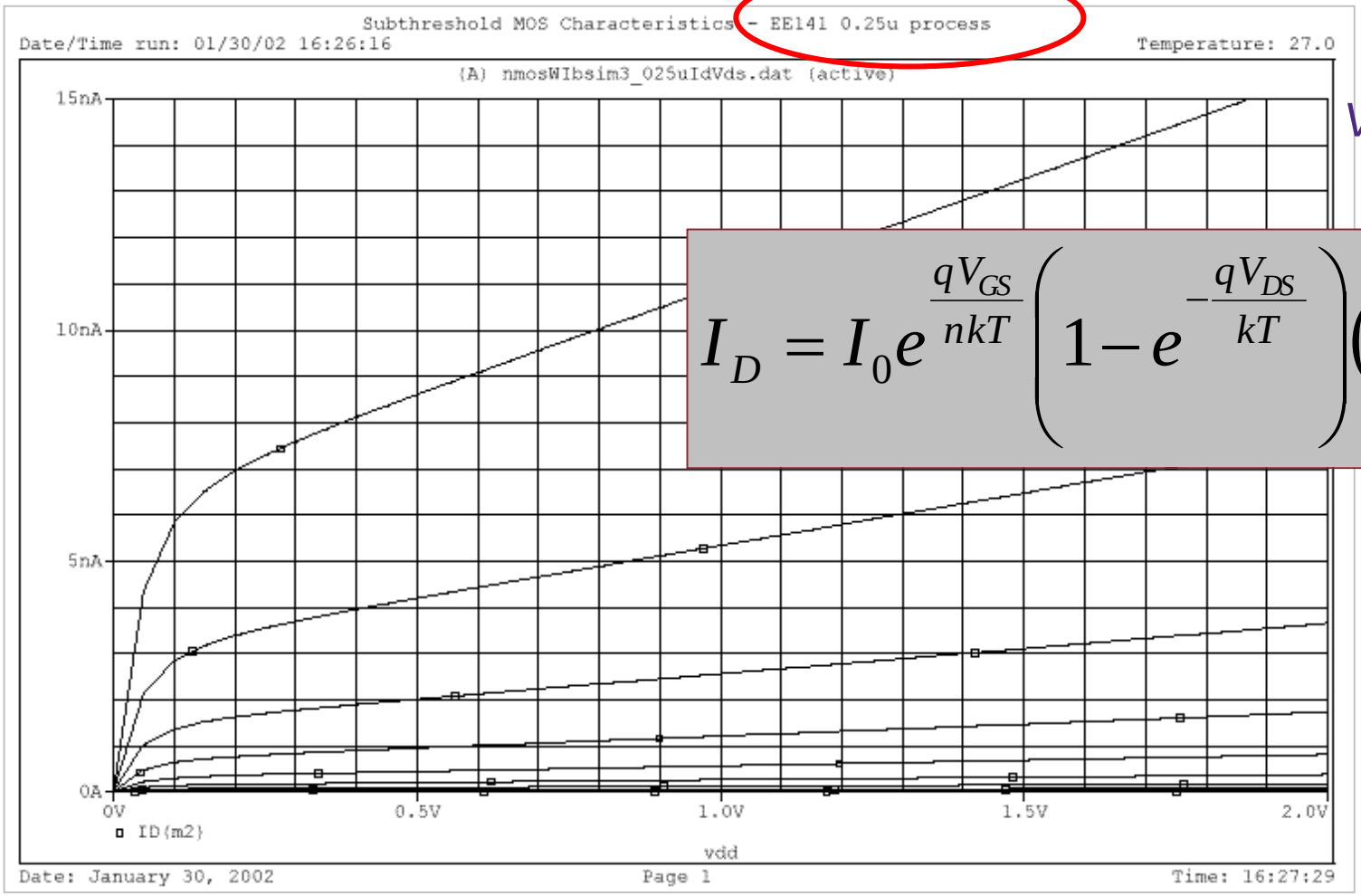
Subthreshold $I_D(V_{GS})$ characersitic



V_{DS} : 0 .. 0.5V

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$

Subthreshold $I_D(V_{DS})$ characersitic



V_{GS} : 0 .. 0.3V

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)\left(1 + \lambda \cdot V_{DS}\right)$$

MOS transistor models

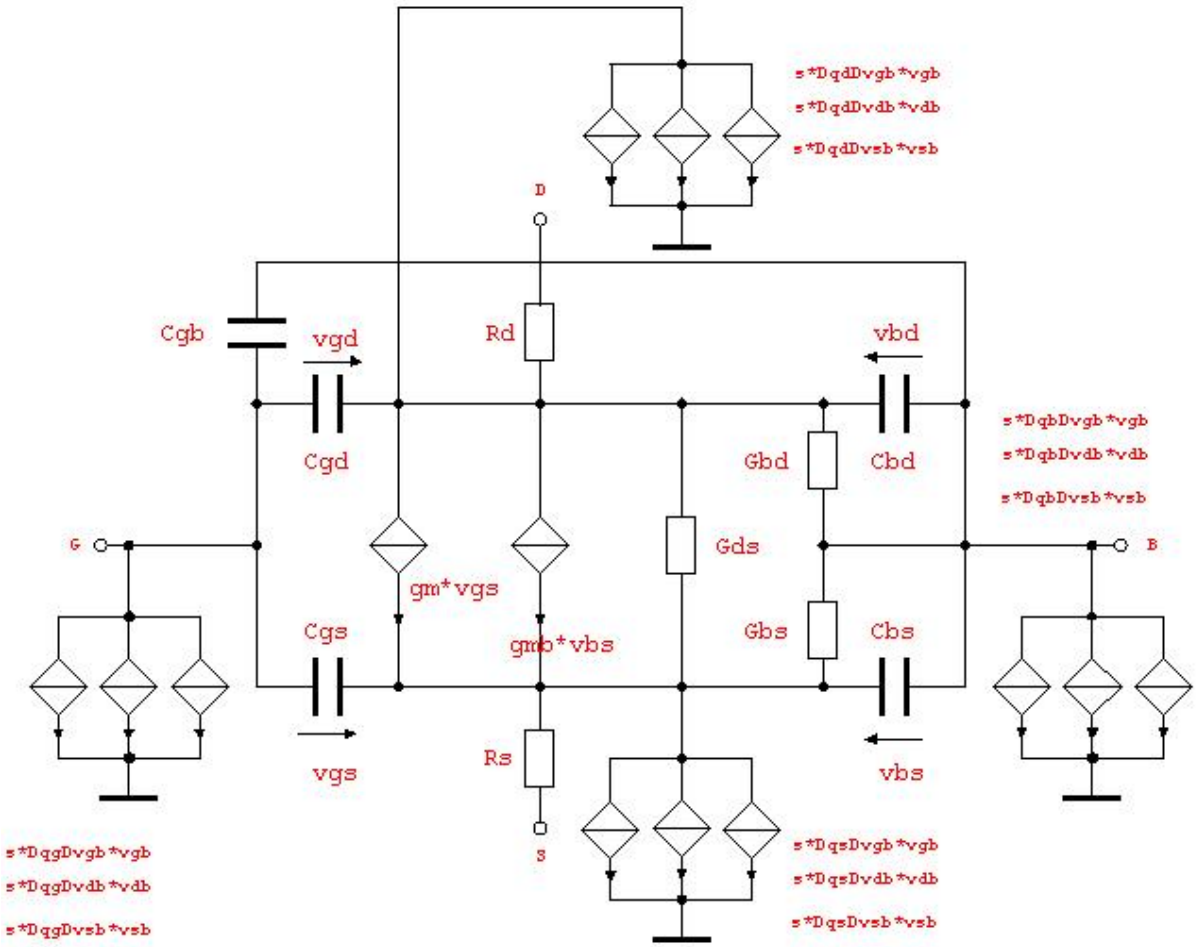
- Needed for circuit simulators (SPICE, TRANZ-TRAN, ELDO, SABER, etc.)
- Different levels of complexity:
  - level0, 1, 2, ...n,
  - EKV,
  - BSIM3, BSIM4

TABLE 8.1 SPICE2 and PSpice MOSFET DC Model Parameters.

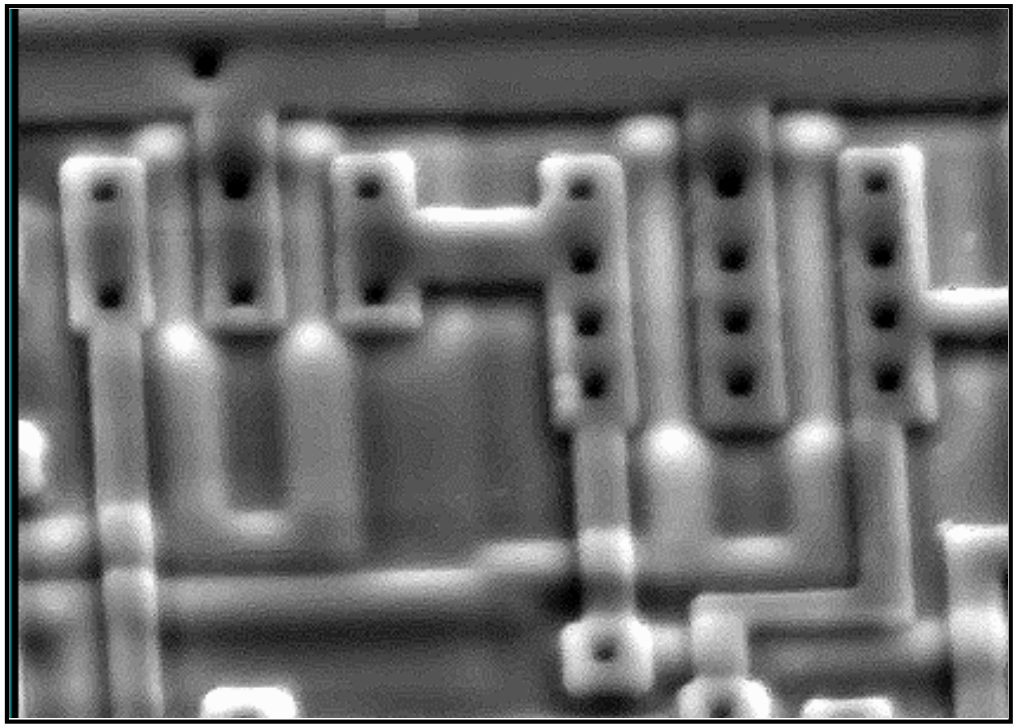
No.	Text Symbol	SPICE Keyword	Level	Parameter Name	Default Value	Units
1	—	LEVEL	1–3	SPICE model 1, 2 or 3	1	—
2	V_T	VTO	1–3	Zero-bias threshold voltage	0.0	V
3	γ	GAMMA	1–3	Bulk space-charge parameter	0.0	$V^{0.5}$
4	ψ_s	PHI	1–3	Surface potential	0.6	V
5	KP	KP	1–3	Transconductance parameter	2.0E-5	A/V^2
6	λ	LAMBDA	1, 2	Channel-length modulation	0	V^{-1}
7	t_{ox}	TOX	1–3	Gate-oxide thickness	1.0E-7	meter
8	N_b	NSUB	1–3	Substrate doping	0.0	cm^{-3}
9	N_f	NSS	2, 3	Fixed oxide charge	0.0	cm^{-2}
10	N_{it}	NFS	2, 3	Interface-trapped charge	0.0	cm^{-2}
11	—	TPG	2, 3	Type of gate material +1 opp. to substrate −1 same as substrate 0 Al gate	1	—
12	μ	UO	1–3	Surface mobility	600	cm^2/Vs
13	U_c	UCRIT	2	Critical electric field for mobility	1E4	V/cm
14	U_e	UEXP	2	Exponential coefficient for mobility	0.0	—
15	U_t	UTRA	2	Transverse field coefficient	0.0	—
16	x_j	XJ	2, 3	Source or drain junction depth	0.0	meters
17	x_{jl}	LD	1–3	Lateral diffusion	0.0	meters
18	v_{max}	VMAX	2, 3	Maximum carrier drift velocity	0.0	meters/s
19	N_{eff}	NEFF	2	Total channel charge coefficient	1	—
20	δ	DELTA	2, 3	Width effect on threshold voltage	0.0	—
21	η	ETA	3	Static feedback on threshold voltage	0.0	—
22	V_{bi}	PB	1–3	Source and drain junction built-in potential	0.80	V
23	θ	THETA	3	Mobility modulation	0.0	—
24	κ	KAPPA	3	Saturation field factor	0.2	—

MOS transistor models

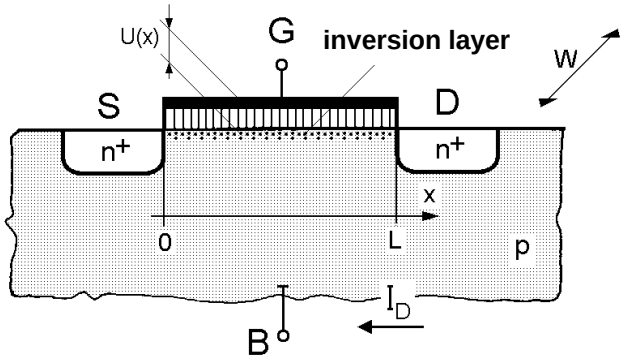
- Needed for circuit simulators (SPICE, TRANZ-TRAN, ELDO, SABER, etc.)
- Different levels of complexity:
  - level0, 1, 2, ...n,
  - EKV,
  - BSIM3, BSIM4



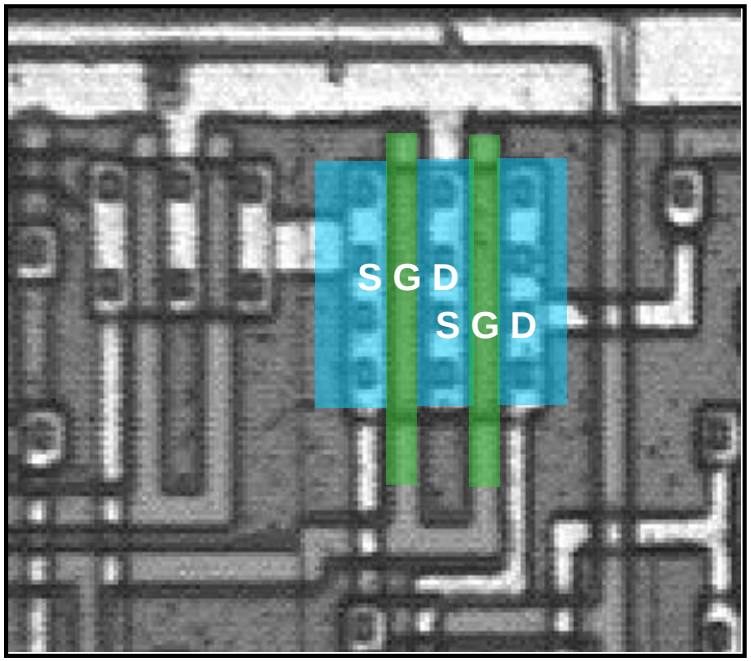
Examples for MOSFETs



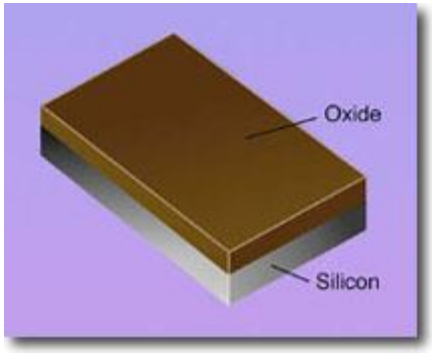
Micro-photograph by SEM

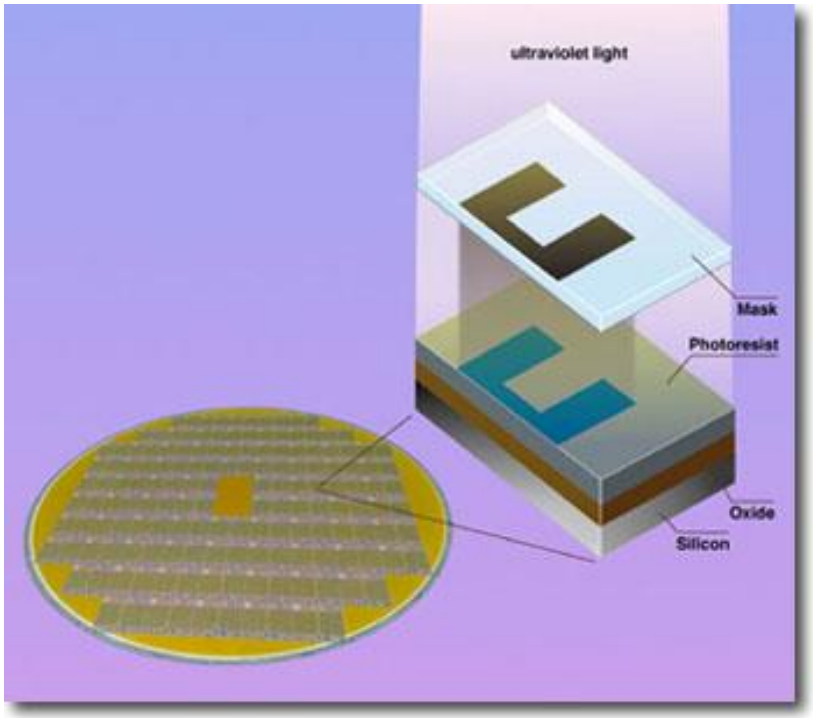


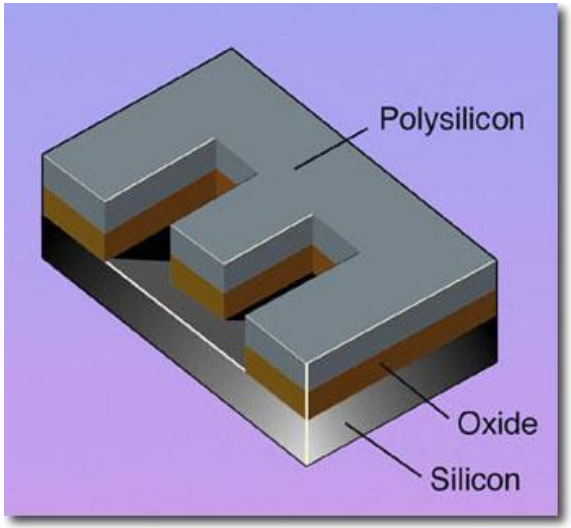
Photograph by optical microscope

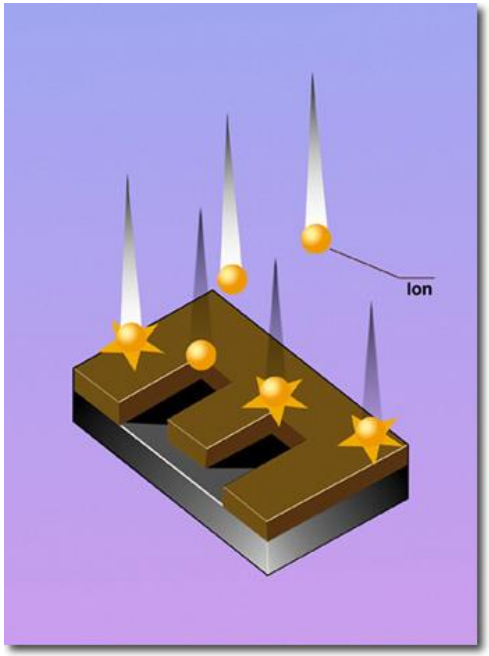


How is it manufactured?





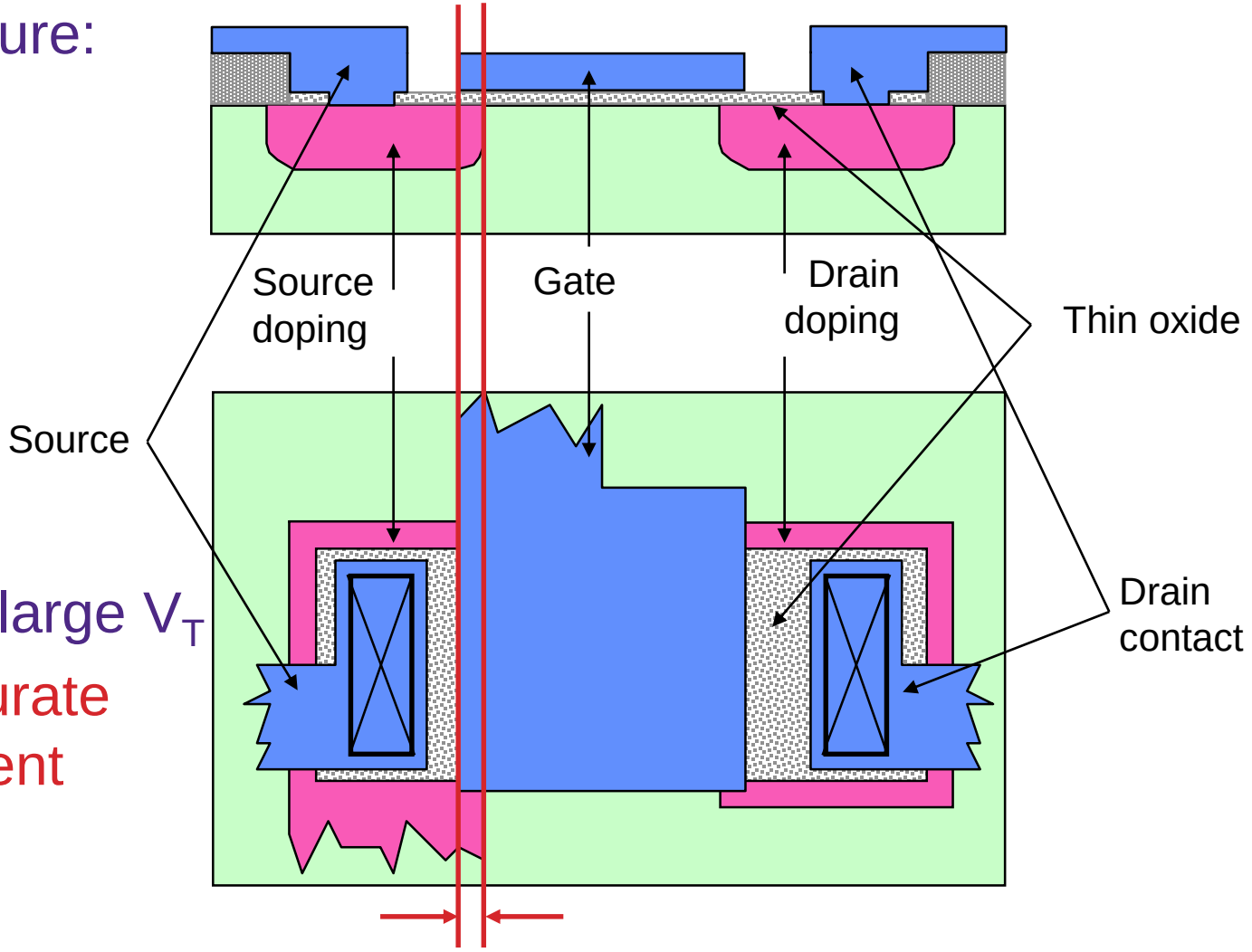




Metal gate MOS transistor

In-depth structure:

Layout view:



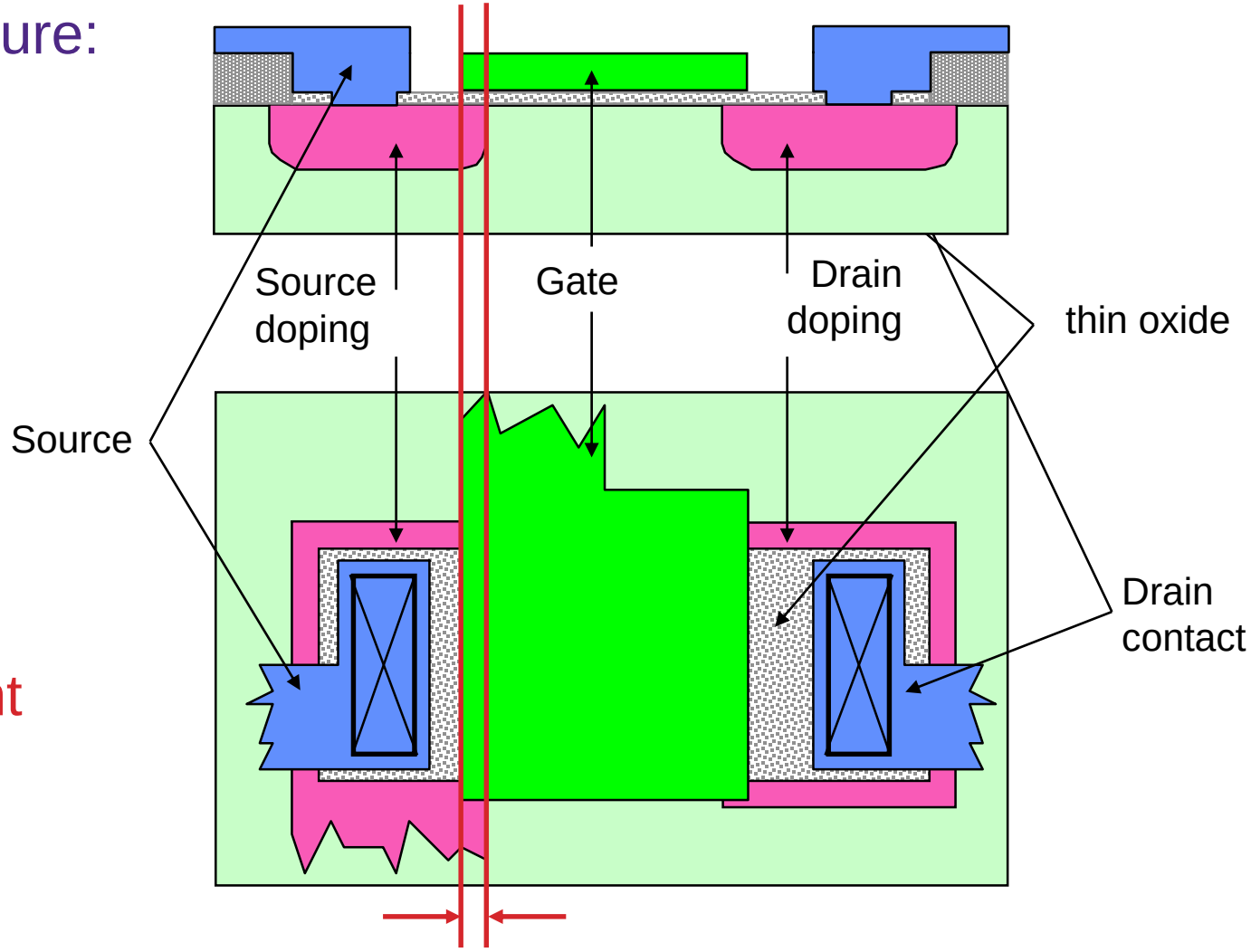
Problems:

- metal gate – large V_T
- requires accurate mask alignment

Poly-Si gate MOS transistor

In-depth structure:

Layout view:

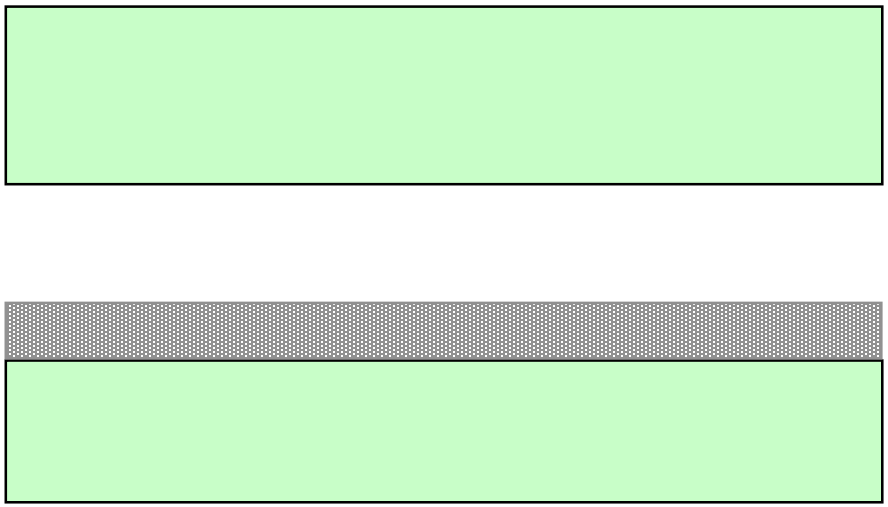


Advantages

- smaller V_T
- self alignment

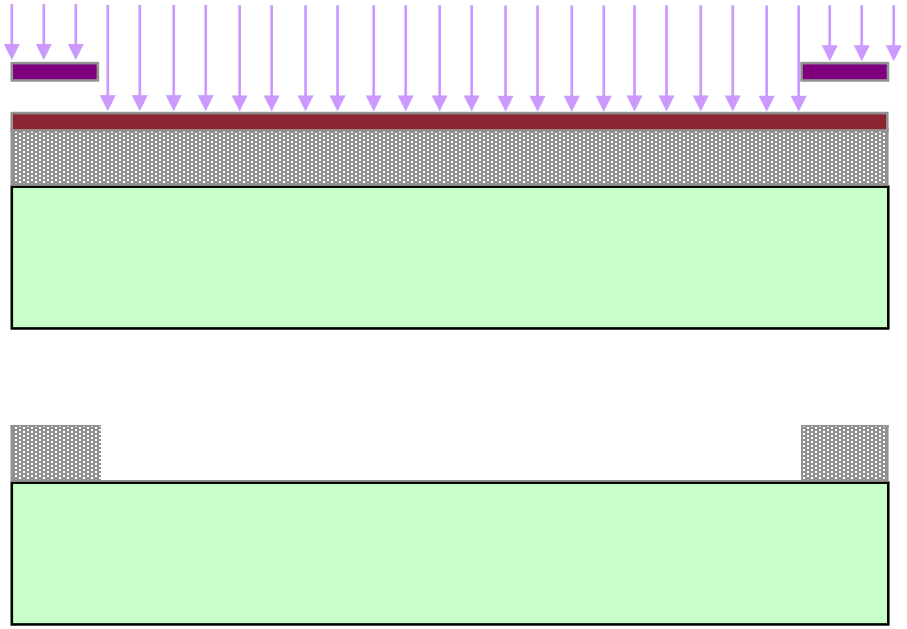
A poli-Si gate nMOS process

- Start with: p type substrate (Si wafer)
  - cleaing,
    - grow thick SiO_2 – this is called *field oxide*



The poli-Si gate nMOS process

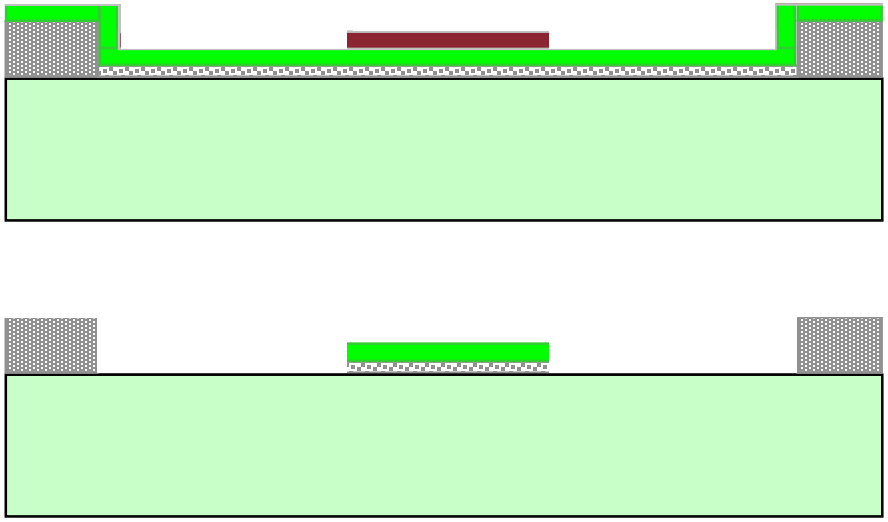
- Create the active zone with photolithography
  - coat with resist,
    - expose to UV light through a mask,
    - development, removal of exposed resists
    - etching of SiO_2 removal of the resist



M1: active zone

The poli-Si gate nMOS process

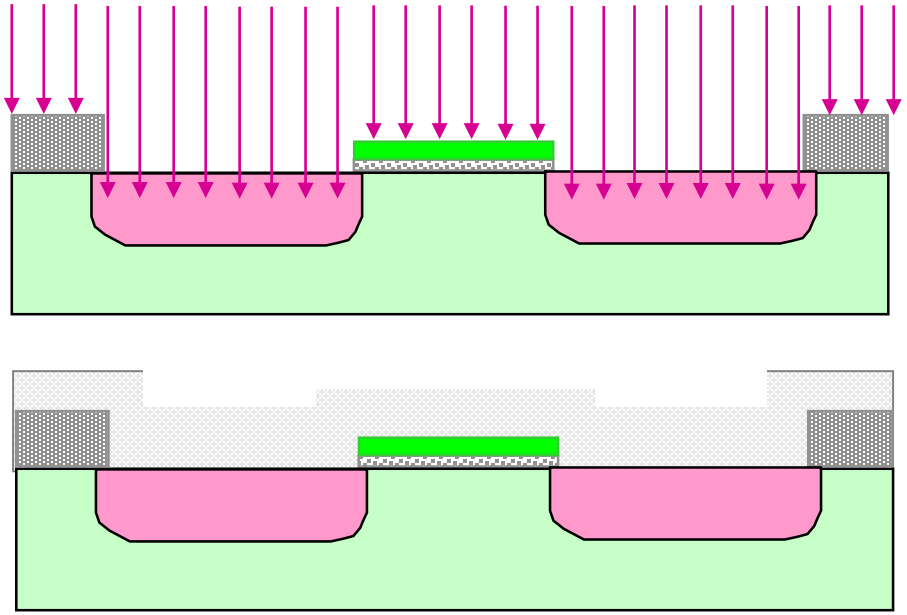
- Create the gate structure:
  - growth of thin oxide
  - deposit poly-Si
  - pattern poly-Si with photolithography (resist, exposure, develop)
  - etch poly-Si, etch thin oxide



M2: poly-Si pattern

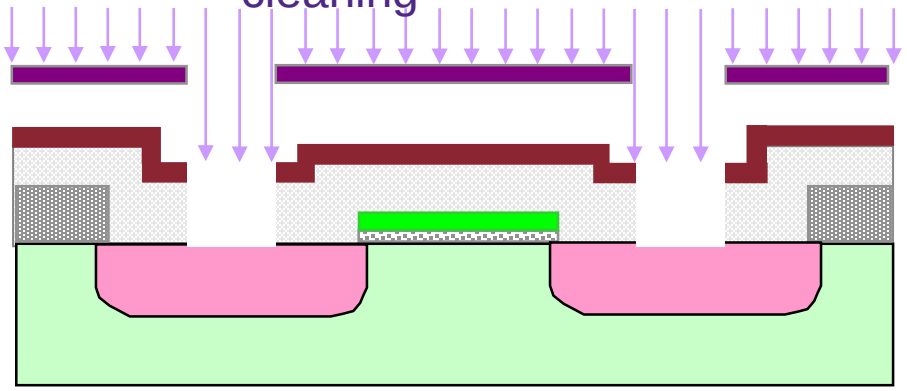
The poli-Si gate nMOS process

- S/D doping (implantation)
  - the exide (thin, thick) masks the dopants
  - this way the self-alignment of the gate is assured
- Passivation: deposit PSG



The poli-Si gate nMOS process

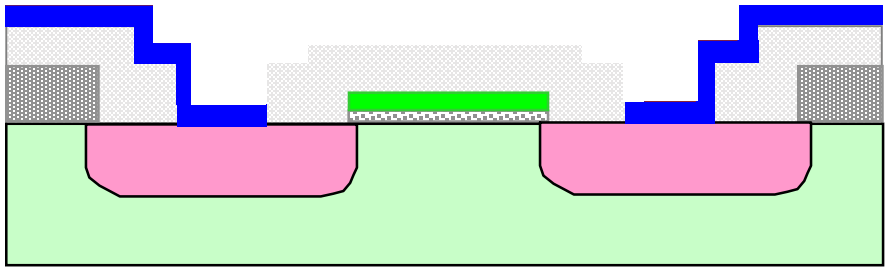
- Open contact windows through PSG
  - photolithography (resist, expose pattern, develop)
  - etching (copy the pattern)
  - cleaning



M3: contact window pattern

The poli-Si gate nMOS process

- Metallization
  - Deposit Al
  - photolithography, etching, cleaning

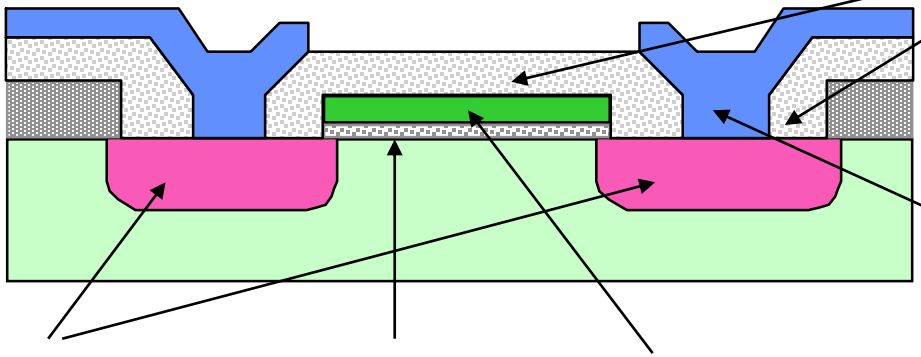


M4: metallization pattern

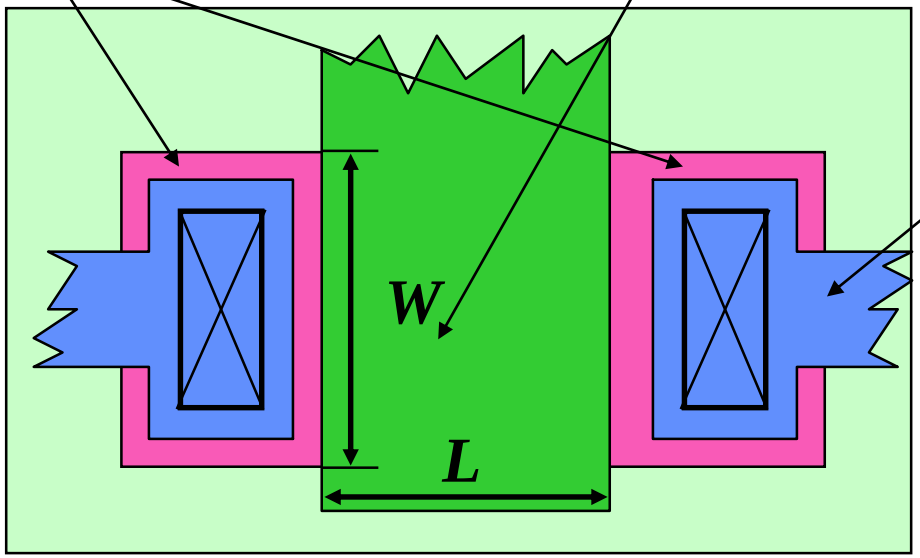
- The recepy of the process is given, the in-depth structure is determined by the sequence of the masks
- One needs to specify the shapes on the masks
  - ***The set of shapes on subsequent masks is called layout***

Poli-Si gate self-aligned device

Structure:



Layout:



Steps of the self-aligned poli-Si gate process

1) Open window for the active region **M**
   - photolitography, field oxide etching
2) Growth of thin oxide
3) Window for hidden contacts **M**
   - Contacts the poli-Si gate (yet to be deposited) with the active region (after doping).
3) Deposit poli-Si
4) Patterning of poli-Si **M**
5) Open window through the thin oxide (etching only)

Steps of the self-aligned poli-Si gate process

6) n+ doping:

   Form source and drain regions as well as wiring by diffusion lines. Through the hidden contact poli-Si gate will also be connected to diffused lines.

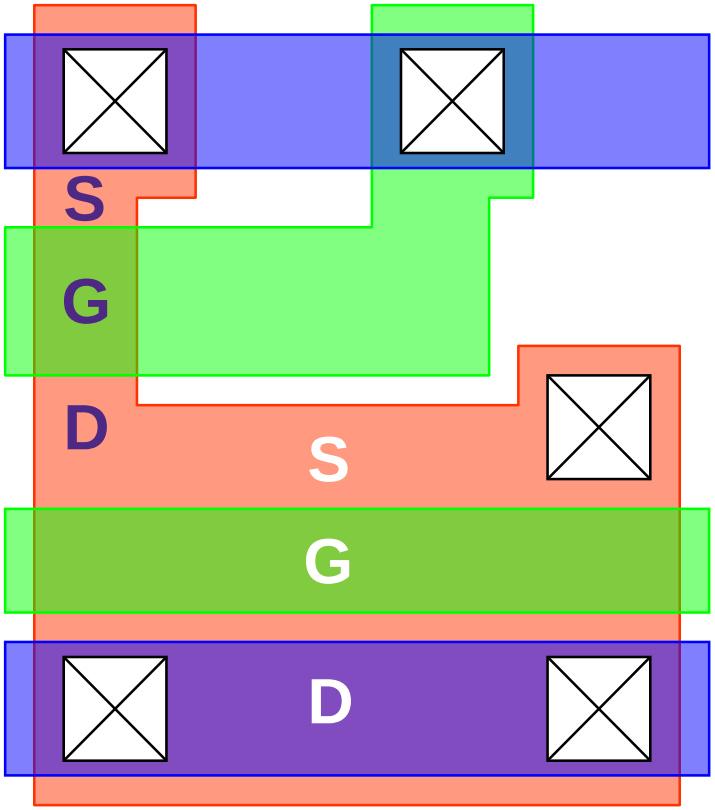
7) Deposit phosphor-silica glass (PSG) as insulator

8) Open contact windows through PSG-n **M**

9) Metallization

10) Patterning metallization layer **M**

Layout of a depletion mode inverter

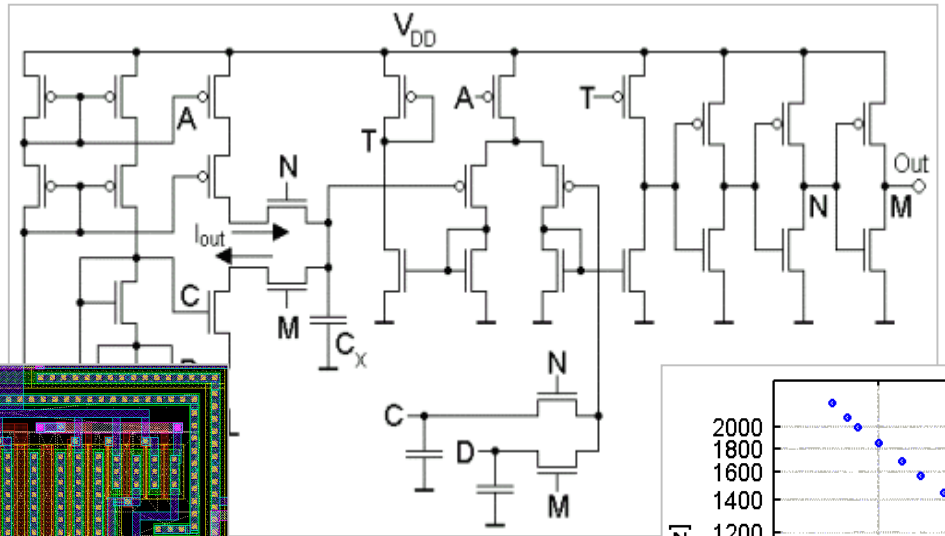


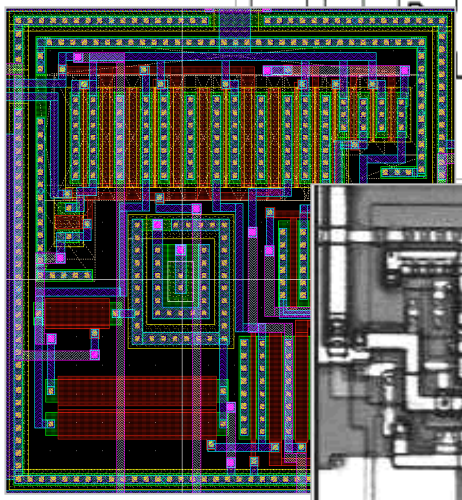
- Layout == set of 2D shapes on subsequent masks
- Masks are color coded:
  - active zone: red
  - poly-Si: green
  - contact windows: black
  - metal: blue
- Mask == layout layer

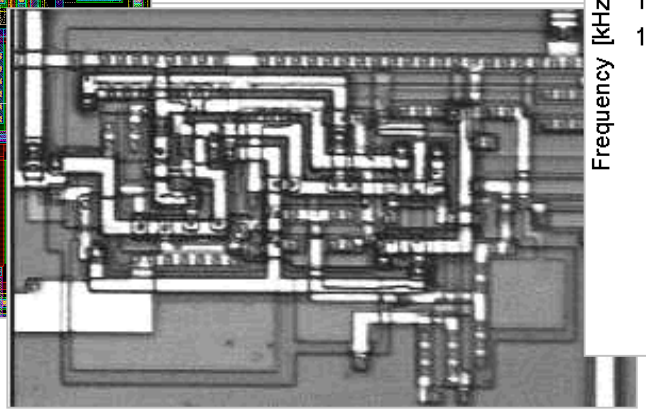
Where is a transistor? Channel between two doped regions:

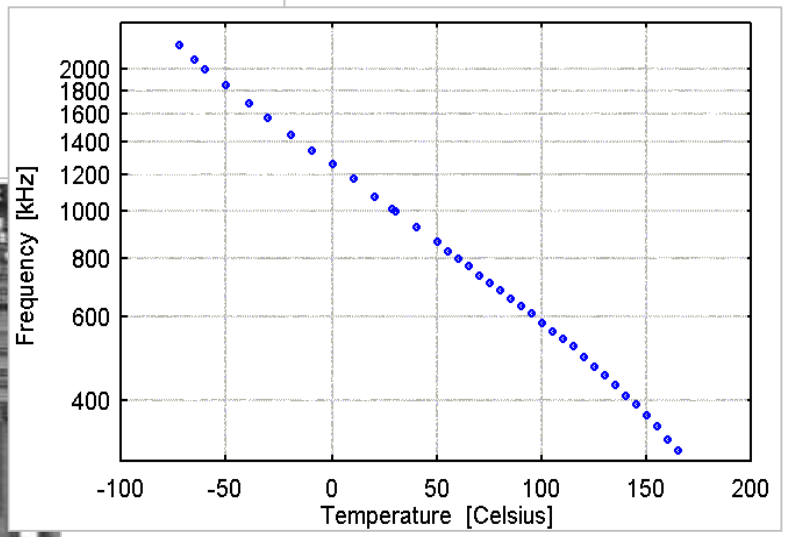
CHANNEL = ACTIVE AND POLY

Some more complex MOS circuits









n- & p-channel devices :

CMOS circuit, see later

Some more complex MOS circuits

Designed by CAD tools