



EET

Microelectronics, BSc course

Introduction

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Microelectronics BSc. Course

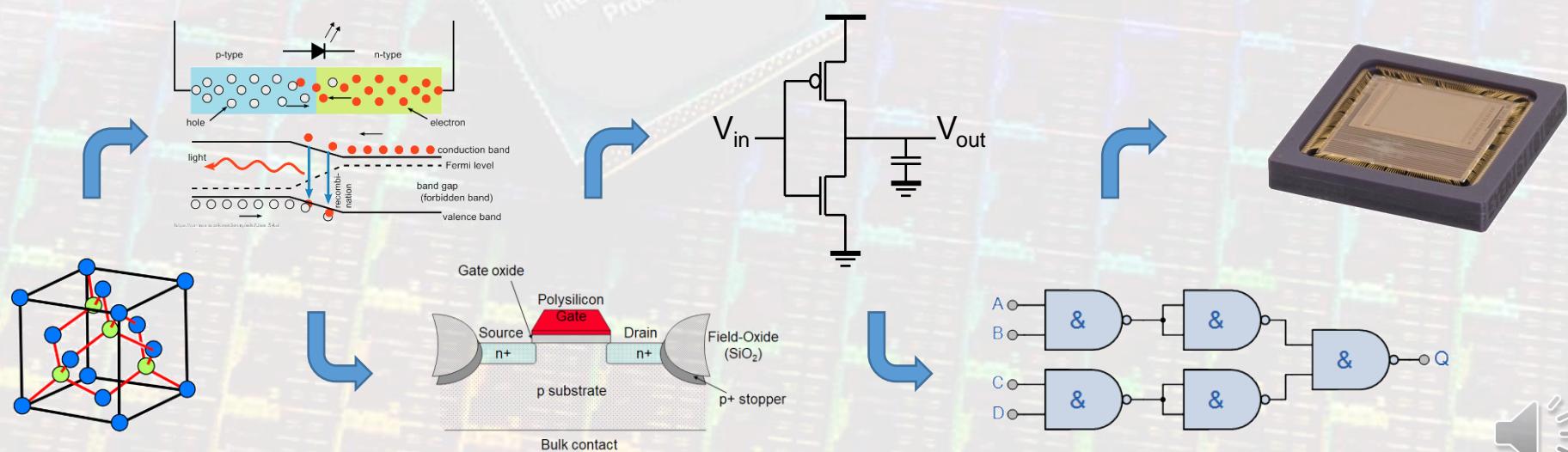
- ▶ Microelectronics usually means analog electronics design (mainly on chip level).
 - ▶ Analog electronics design in the BME curriculum: Electronics 1.
 - ▶ Microelectronics extends it with chip level considerations
 - ▶ A.S. Sedra, K.C. Smith, Microelectronic Circuits, Oxford Series in Electrical and Computer Engineering 6th Edition, ISBN-13: 9780199339136
- ▶ Related knowledge, skills
 - ▶ Semiconductor and quantum physics, solid-state physics, semiconductor manufacturing technology, Mixed-signal CAD design, simulation methodologies, packaging, modern VLSI circuits, etc.





Microelectronics BSc. Course

- ▶ New skills and knowledge, modern technologies, methodologies:
 - ▶ Operation, build-up, manufacturing of applied semiconductor devices (diode, transistor)
 - ▶ Logic gates and standard cells
 - ▶ Design methodology of modern ICs, VLSI circuits
 - ▶ MEMS and optoelectronic devices, etc.





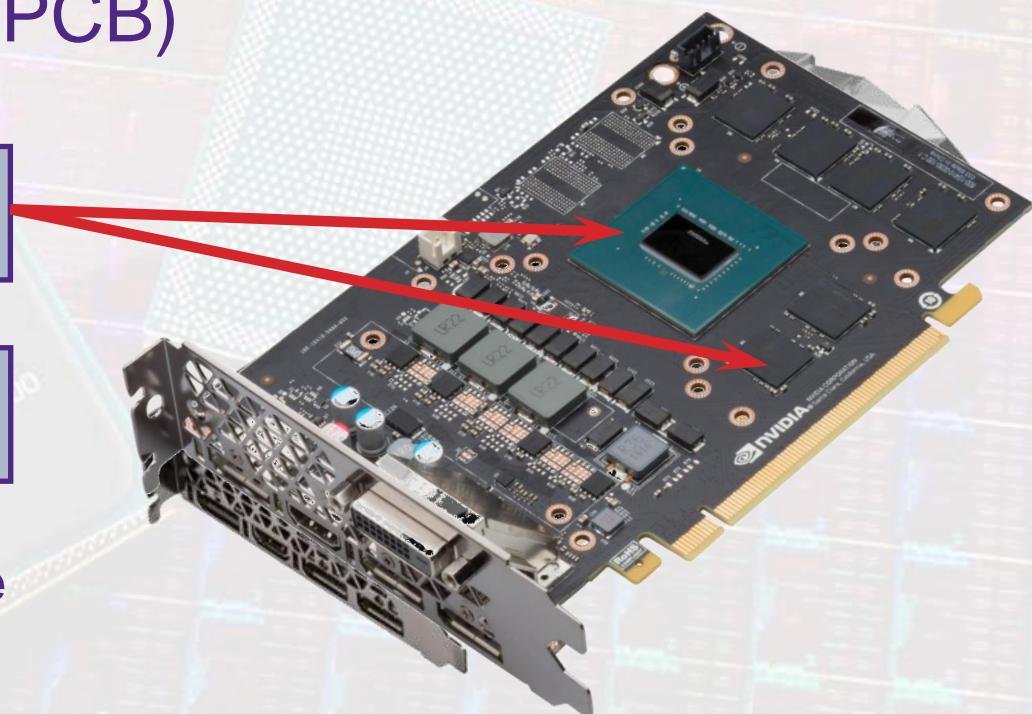
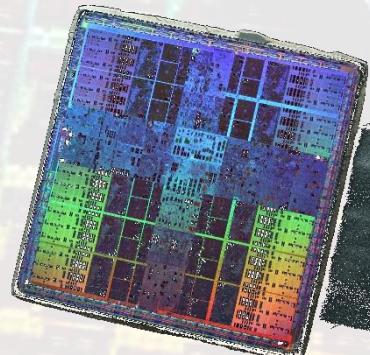
Basics

- ▶ Integrated circuits (IC-s) on a surface mounted printed circuit board (PCB)

We are interested in seeing
the inside of these

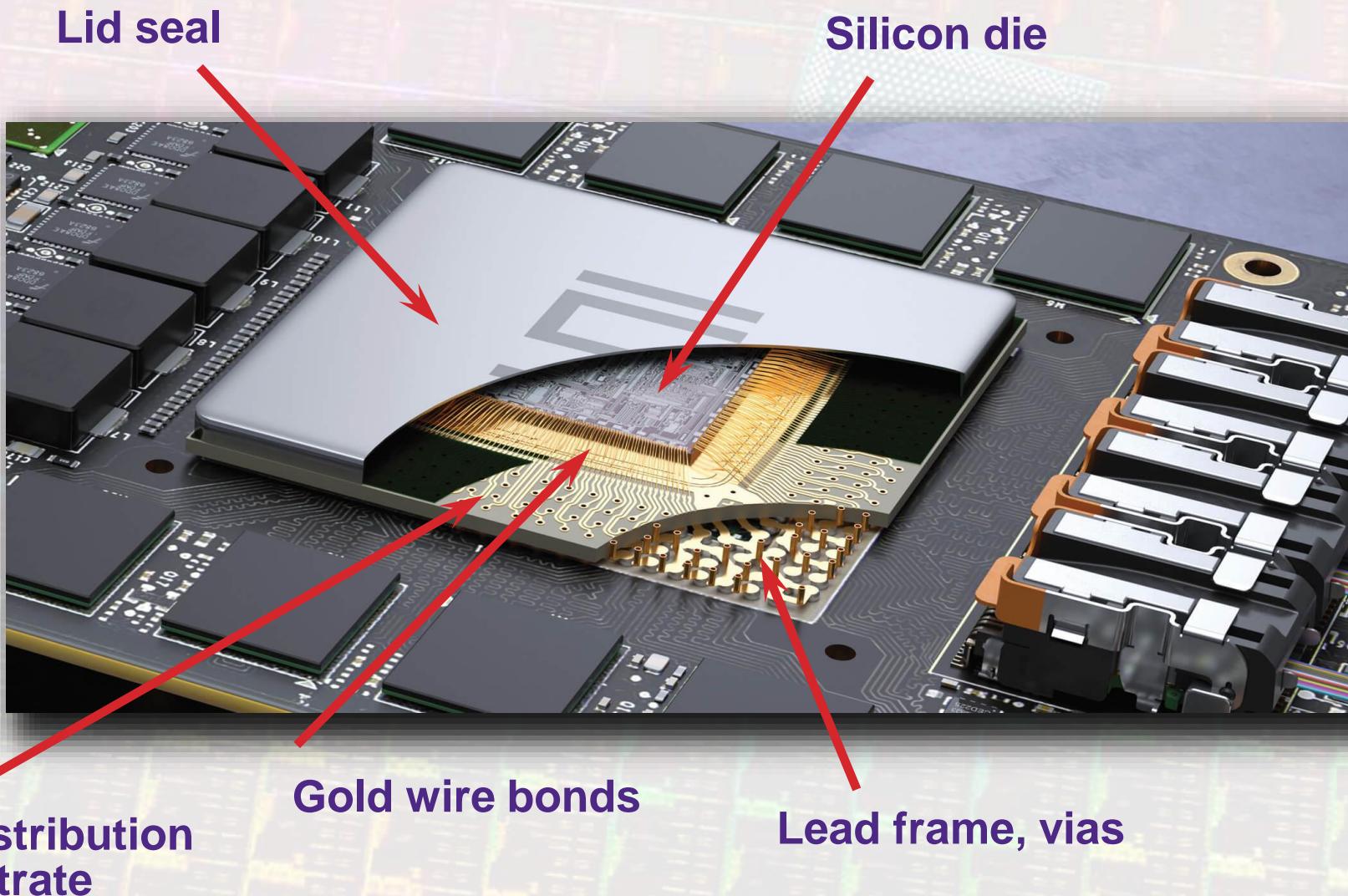
Let's have a look inside the
package!

There are silicon chips inside



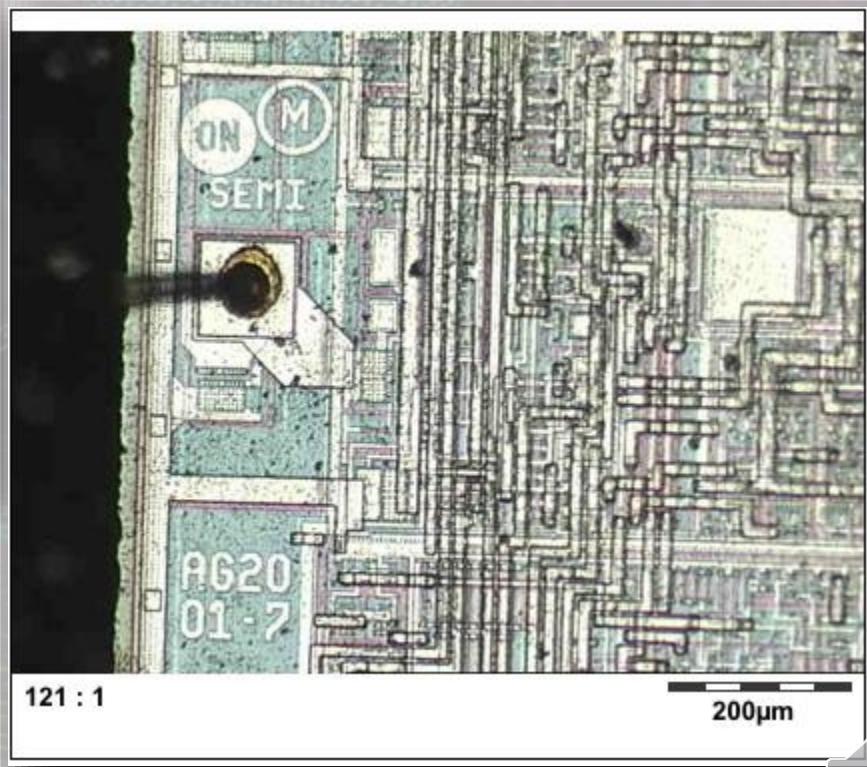
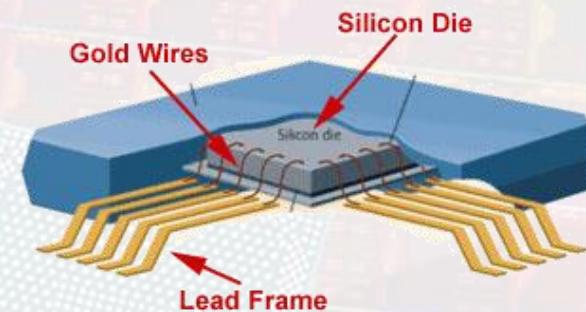
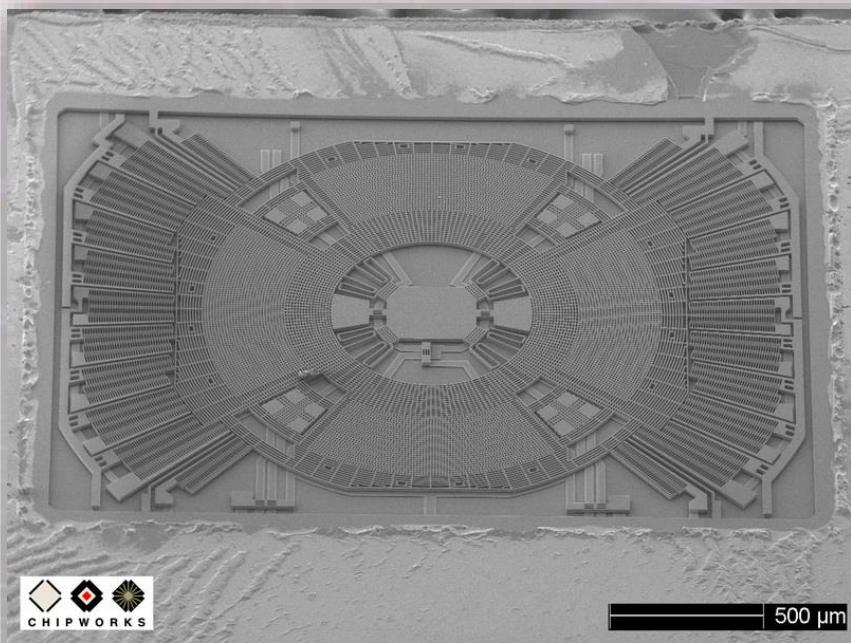


Inside the package





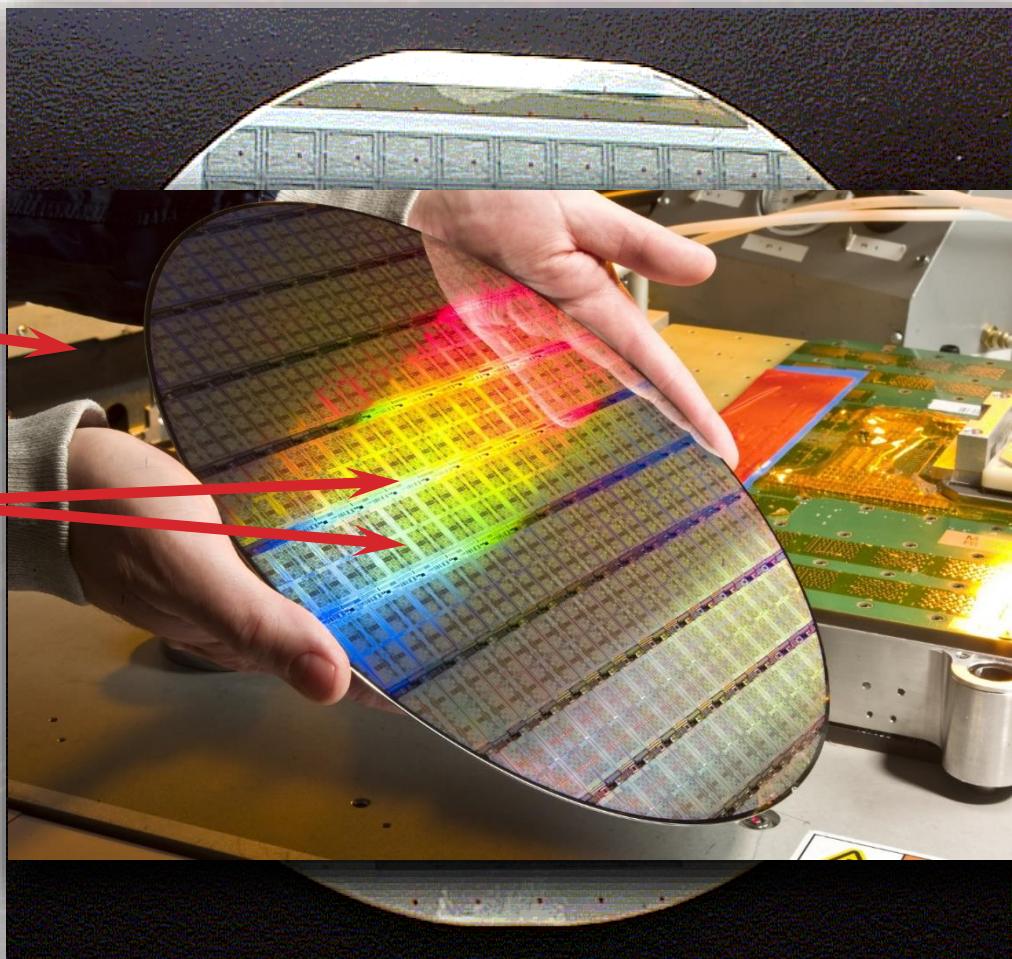
Inside the package





Basics

- Wafer, die or chip:
 - wafer made of perfect single Si crystal
- There are many identical dies (chips) on a wafer
- Wafer diameters: 15-20-25... cm or 4-6-8"
- 100...2000 dies/wafer, manufactured simultaneously





Si single crystal wafers





Si single crystal wafers

The screenshot shows a web browser window with the URL semi.org/en/wafer-size-transition-450-mm-5-misconceptions. The page features the SEMI logo and navigation links for About, Trending, Resources, Collaboration, and Events. A large, blurred background image of a city at night with streaks of light from traffic is visible. The main content is an article titled "Wafer-Size Transition to 450 mm? 5 Misconceptions". The text discusses common misconceptions about the transition to 450 mm wafers, mentioning Moore's Law, R&D costs, and the semiconductor industry's financial challenges.

Wafer-Size Transition to 450 mm? 5 Misconceptions

It seems that everyone in the industry "knows" that bigger wafers mean better productivity and more profits, and everyone "knows" that wafer size changes happen every 10 years, and everyone "knows" that bigger wafers are at least twice as productive as small wafers. However, many experts in the industry think that what "everyone knows" is not truly reality.

There is an industry-wide curiosity about the reality behind a wafer-size transition to 450 mm wafers. According to the ITRS, this transition should happen in 2012 to keep the industry on Moore's Law, and a few companies are pushing hard to make this happen.

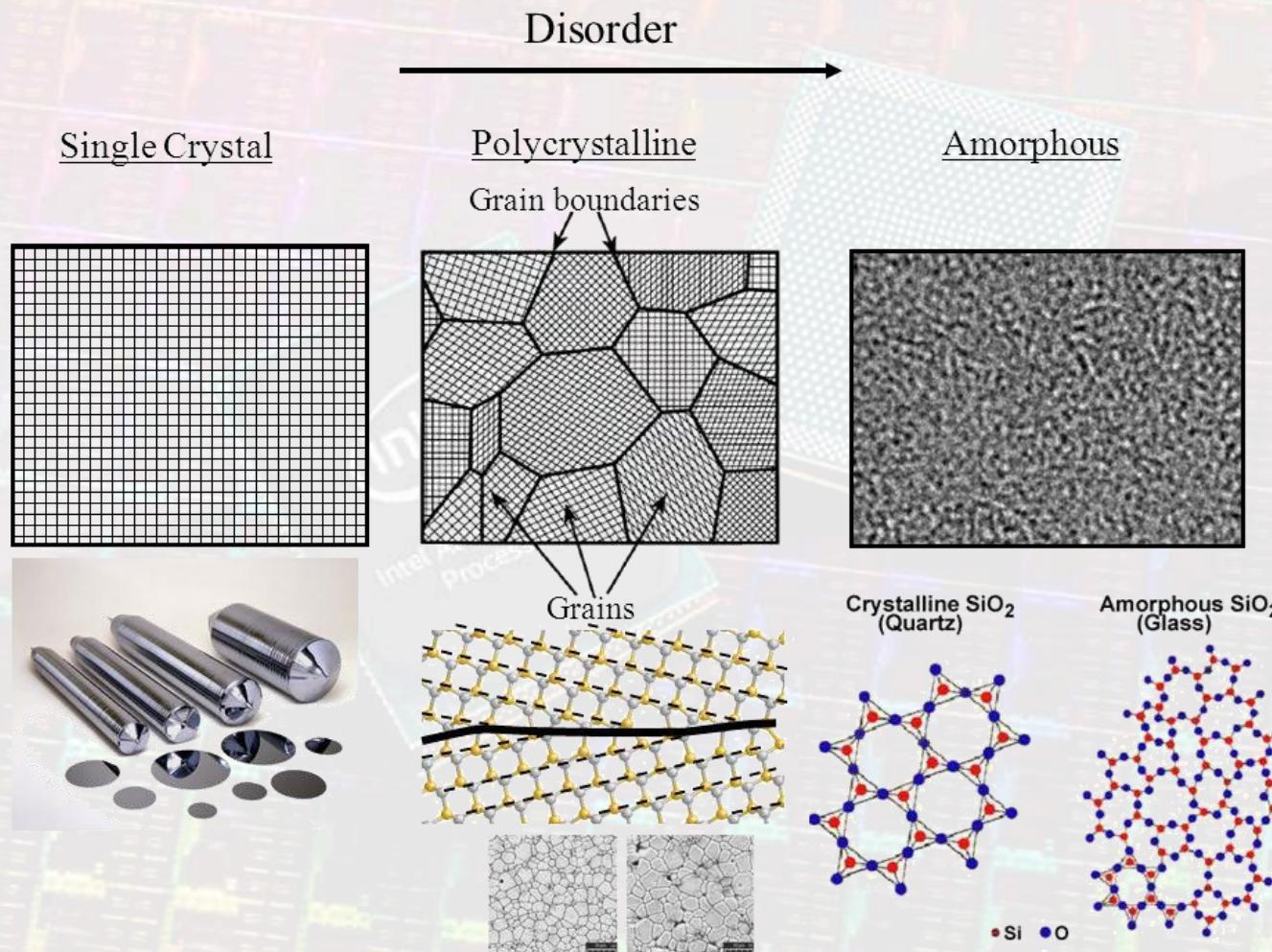
However, the fundamental assumptions that are driving the push for this transition are overstated. Moreover, limited research and development dollars available to tool and equipment suppliers means that investing R&D capital prudently is essential to survival of many companies in the semiconductor supply chain. A white paper released by SEMI in 2005 shows that semiconductor industry R&D dollars are becoming more constrained as advanced process R&D costs rise.

A transition to 450 mm wafers is an extremely expensive and risky proposition—estimates run to well over \$25 billion at the high end. The semiconductor industry simply cannot afford to make such an expensive investment based on future





Crystalline structures

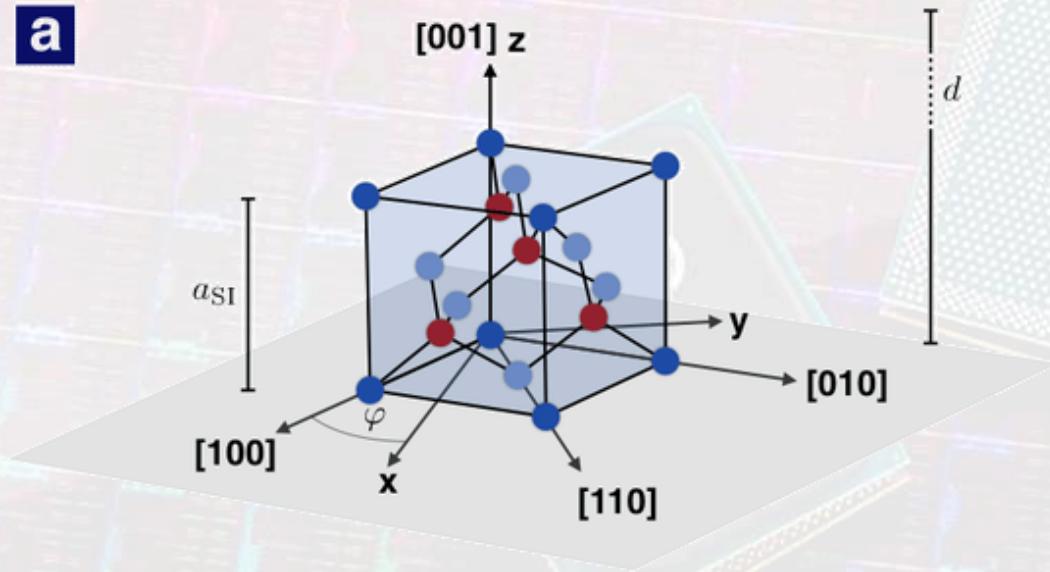
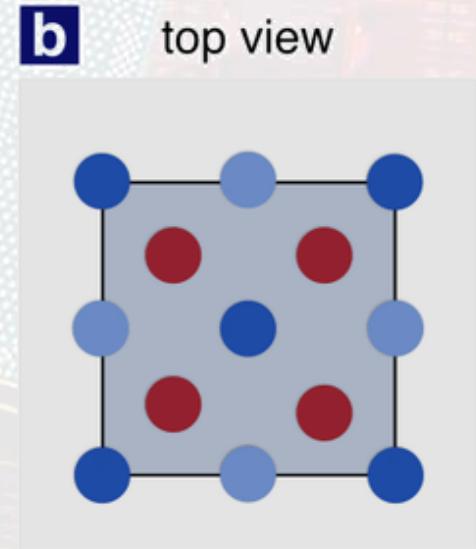


- Solidification & Crystalline Imperfections

Published by [Blanche Parsons](#)



Crystalline structures

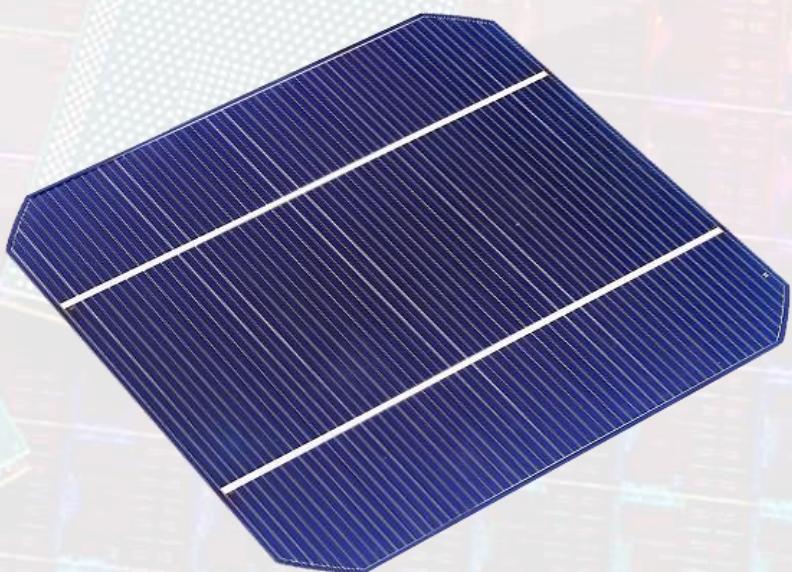
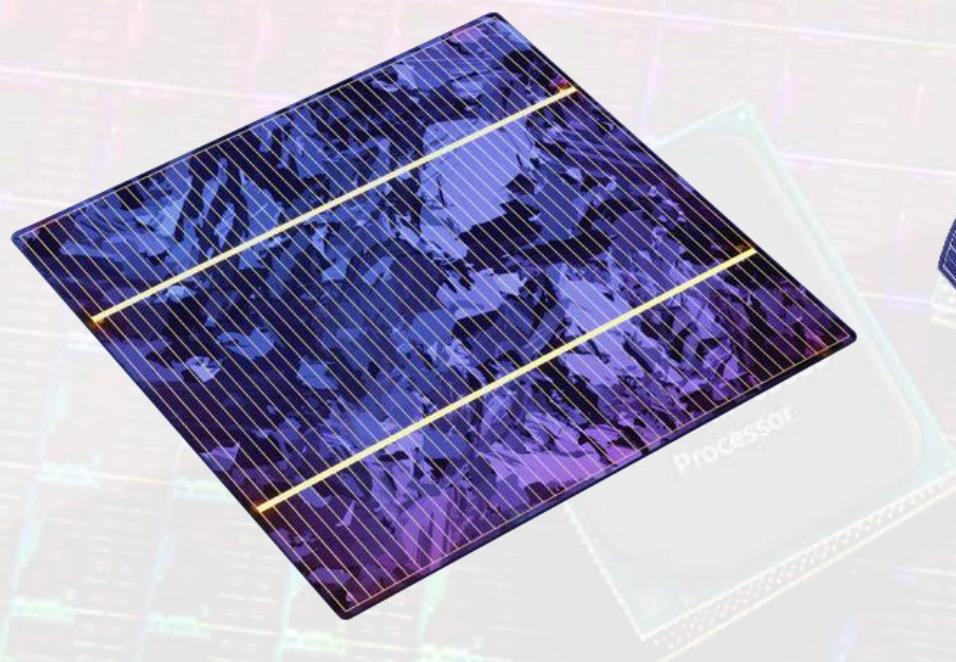
a**b**

- Brendel, Christian. (2019). Topologically Protected Transport of Phonons at the Nanoscale.





Results of crystallization

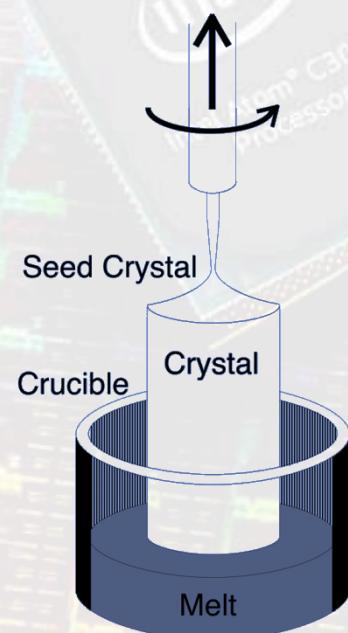
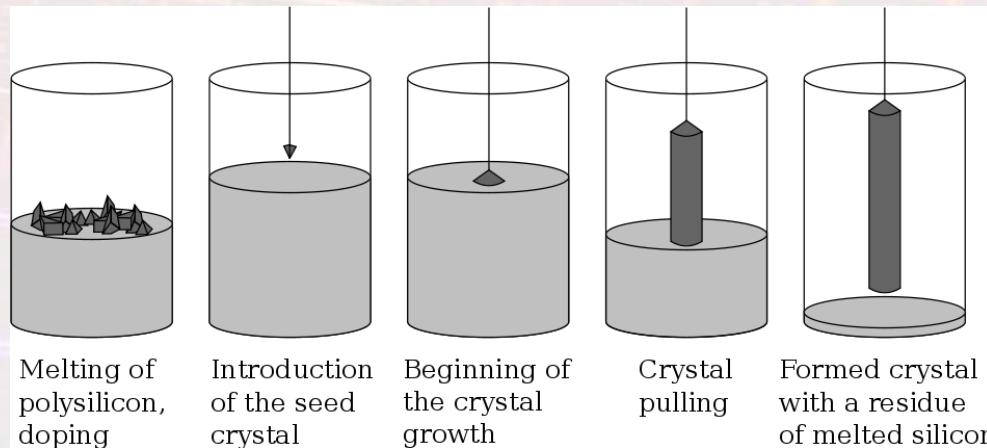


- Poly-Crystalline Solar Cell
- Mono-Crystalline Solar Cell



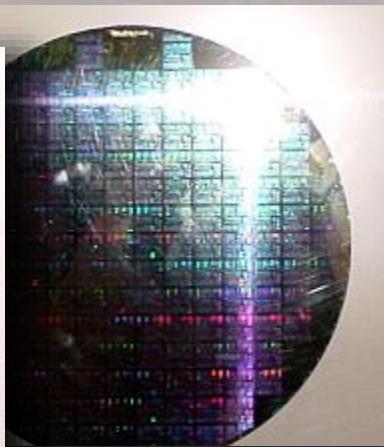


Manufacturing of single crystal wafers





Si single crystal, wafers (2007: 12")

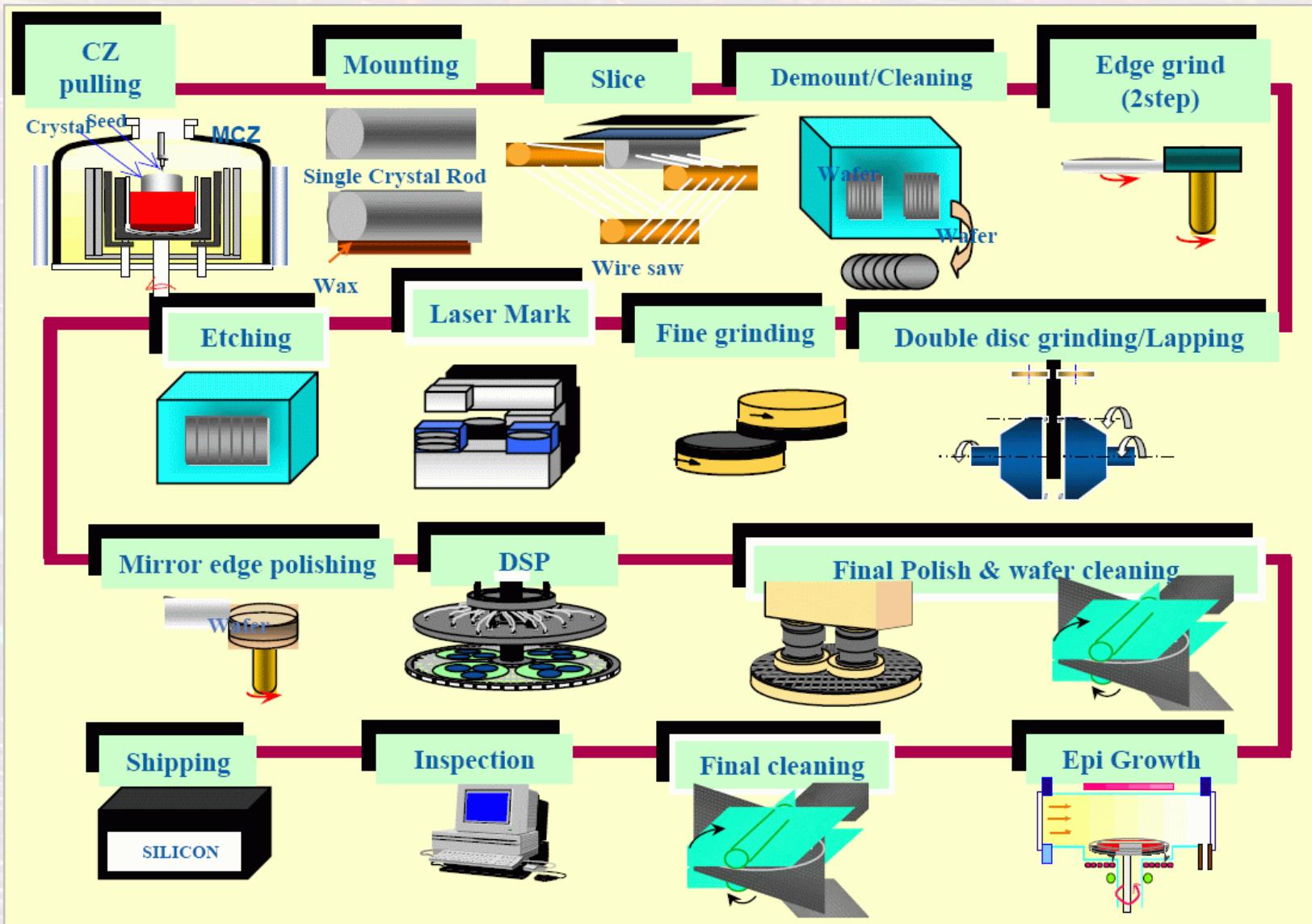


Finished Si wafer



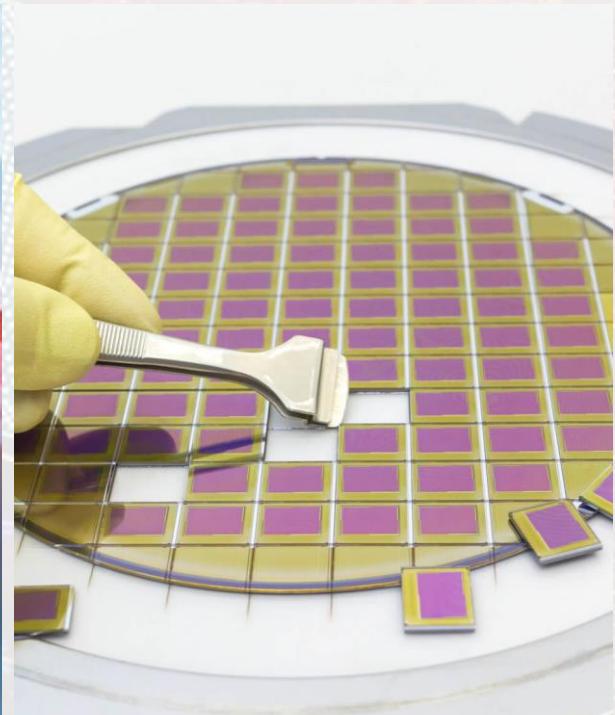
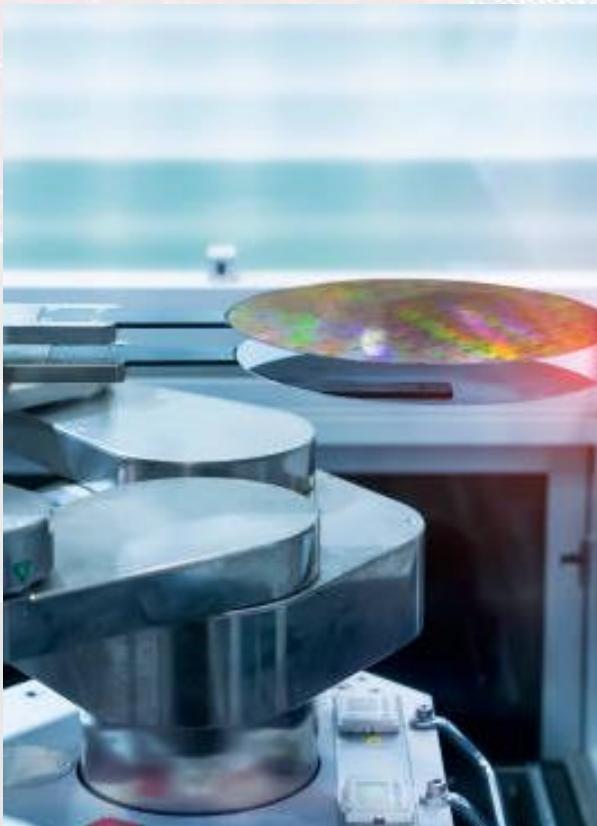


Manufacturing of wafers





Manufacturing of wafers





Basic processing principles

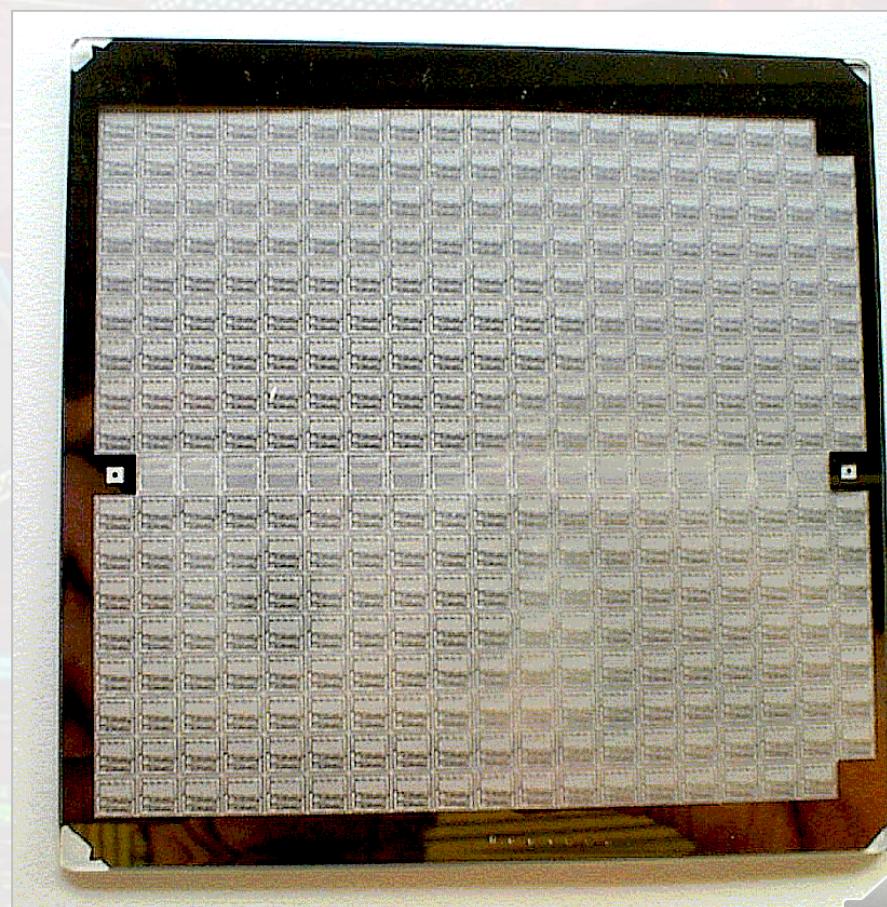
- **Layer growth or deposition:** new material layer is formed over the entire surface of the wafer
- **Patterning:** some patterns are formed in the deposited layer
 - deposition of a photo-sensitive lack (photoresist)
 - photographing the pattern onto the lack
 - developing the photoresist: pattern formed in the resist layer
 - transferring the pattern from the resist to the material layer underneath by some kind of **etching**
 - removal of the resist
- **In-depth deposition of external material:** ion implantation (formerly: diffusion)





Patterning

- The original pattern is on a so called photo-mask
 - made of chromium on glass substrate
 - many times larger than a chip
- Need for high level of accuracy:
 - 7nm over 30cm!
 - accuracy: $10^{-8}:1$
- Visible light:
 - $\lambda=0.3\text{-}0.6 \mu\text{m}$
 - deep UV needed! (193nm)
 - extreme UV (13.5nm)





Making tiny structures (patterning)

- Basic process: **photolithography**. Small features of a mask are photographed onto a lack called photo-resist



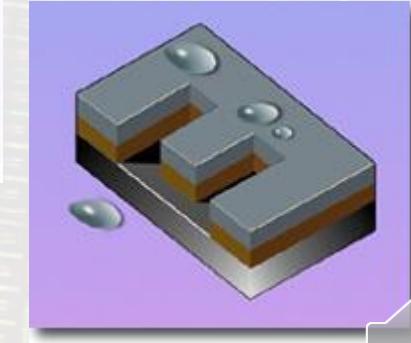
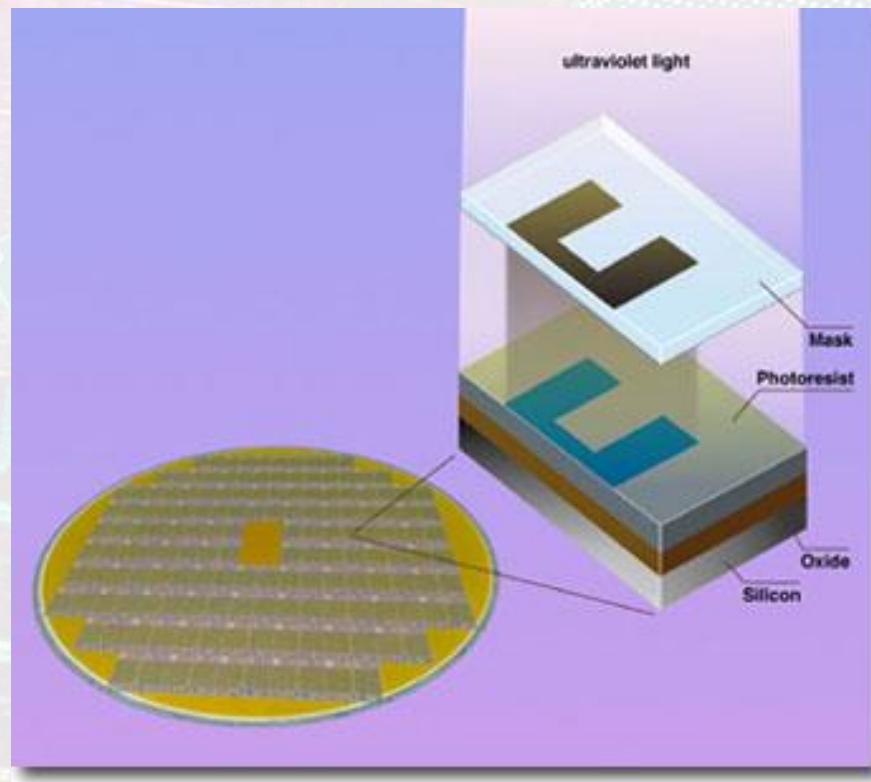
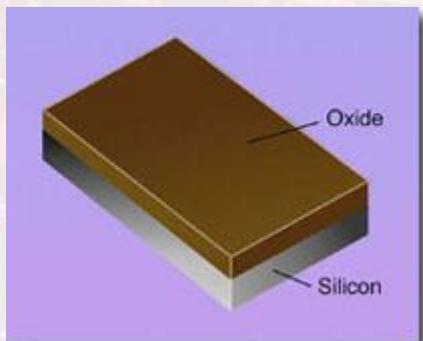
- ▶ UV light is used
- ▶ Resist is not sensitive to yellow

Semiconductor Technology Lab,
Microelectronics branch at DED



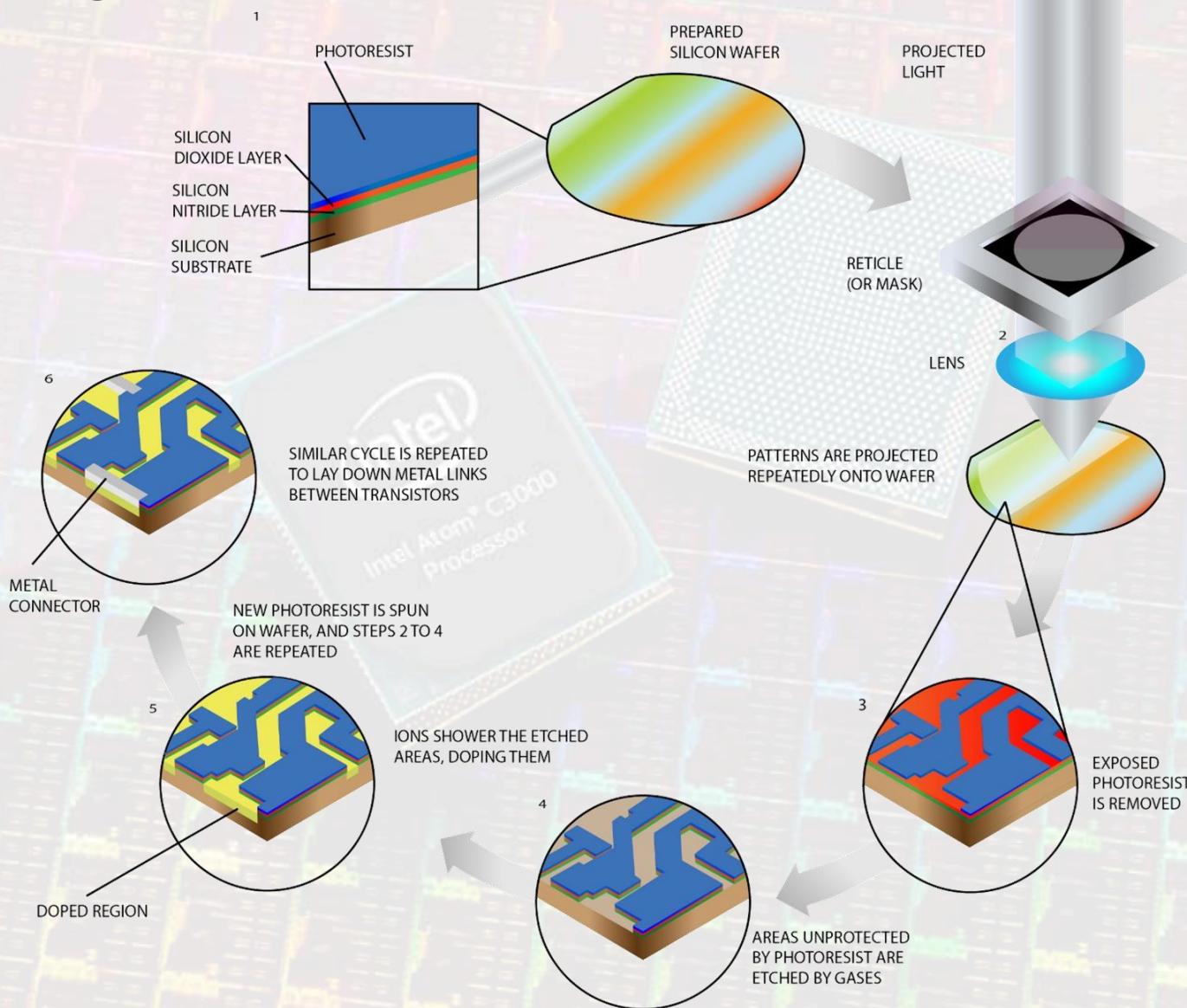


Patterning: photolithography





Patterning





Typical types of patterns on a chip

Metallization

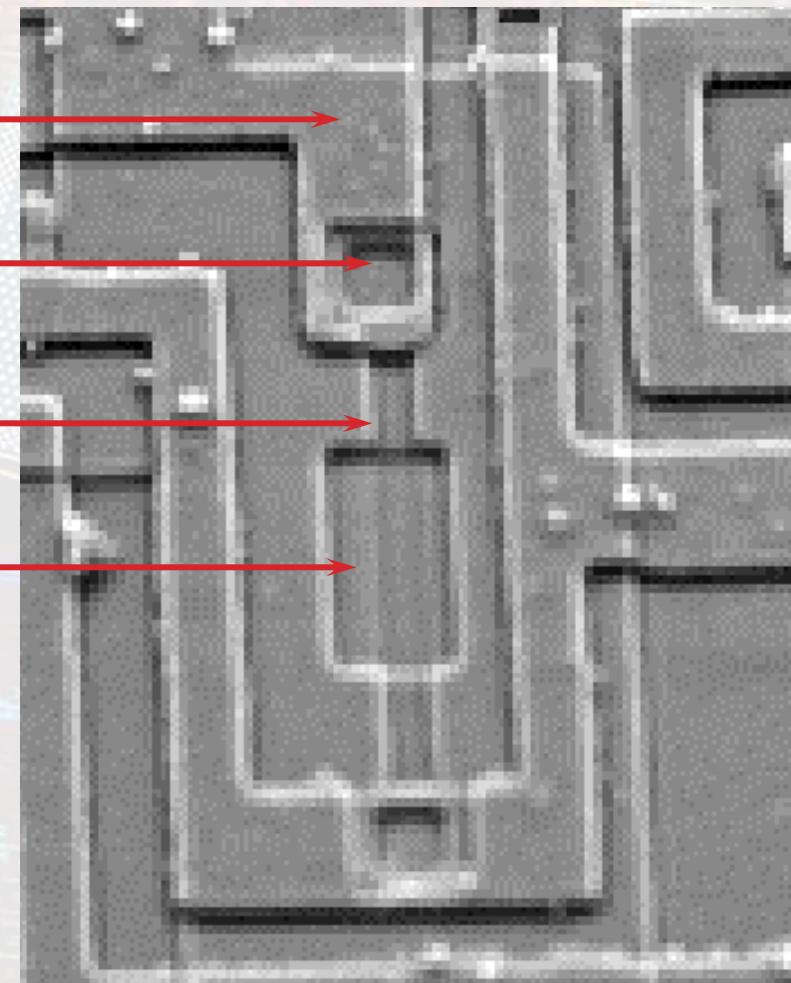
Contact window

P diffused (doped) region

N diffused (doped) region

One process: 15..25 masks

Problem: alignment of masks



SEM of a resistor in an analog IC

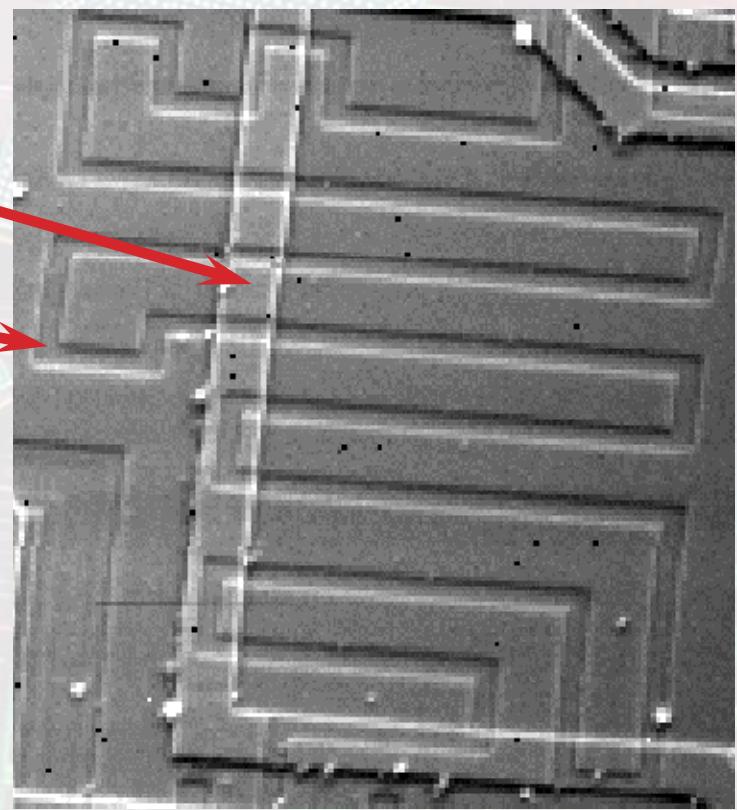




Basics

- **Minimal feature size (MFS)** – the smallest (thinnest) feature that you can create on the top of a silicon wafer (substrate)

Metallization line ("wire")
Doped region ("diffusion line")
MFS in the early days: 15-20 μm
MFS today: 7-10 nm or even less



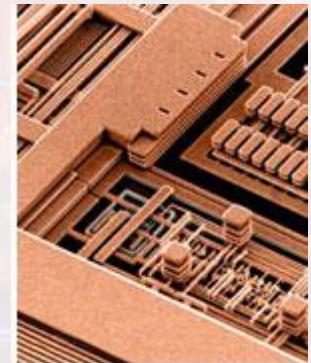
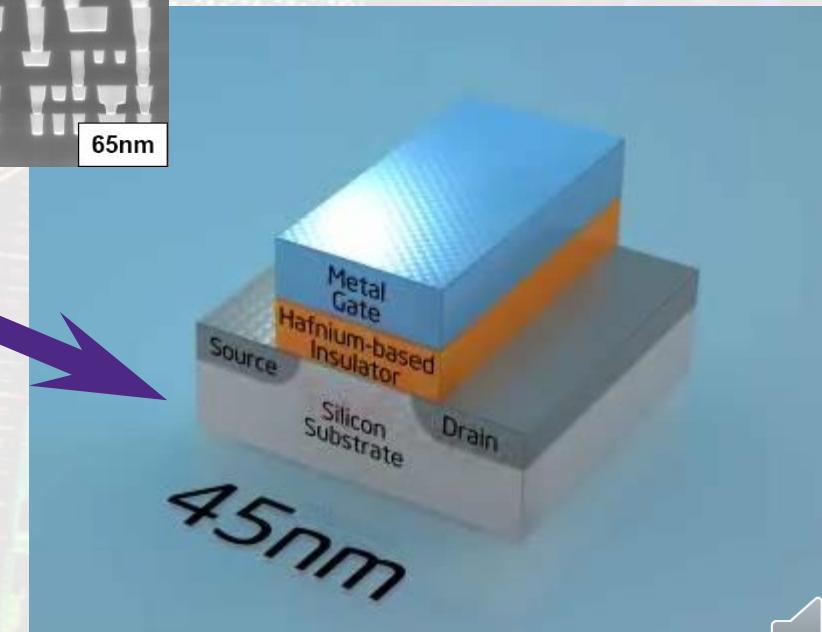
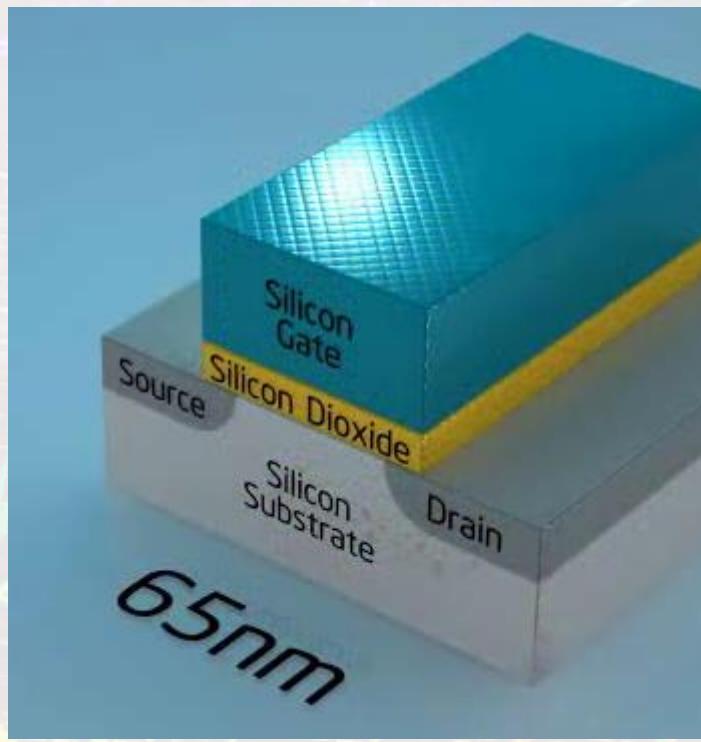
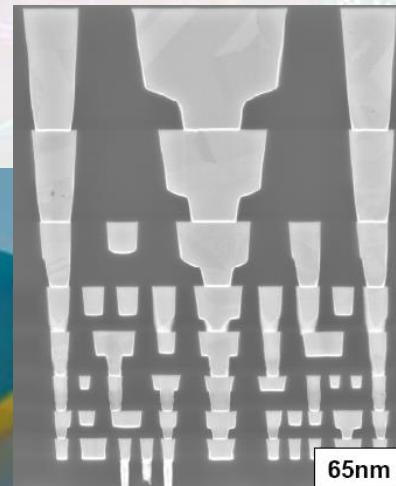
SEM microphotograph





Basics

- Minimal feature size (MFS) 2007/2008, Intel:



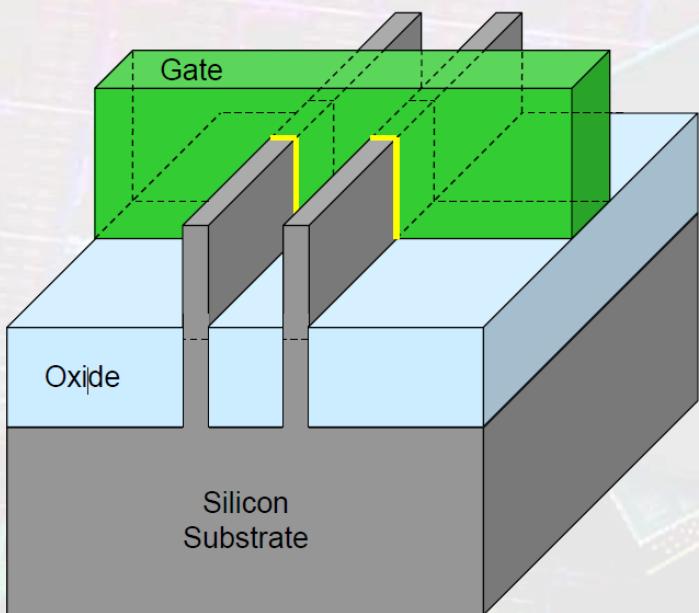
Many metal interconnects instead of polysilicon



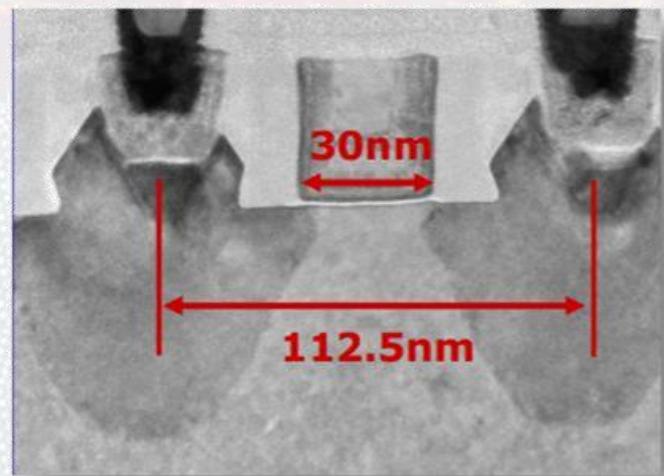


Basics

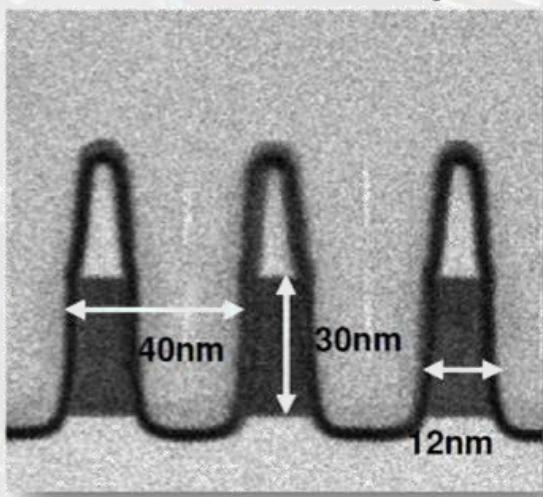
- **Minimal feature size (MFS)**
Intel 2012, 2014, 2018 (10nm)



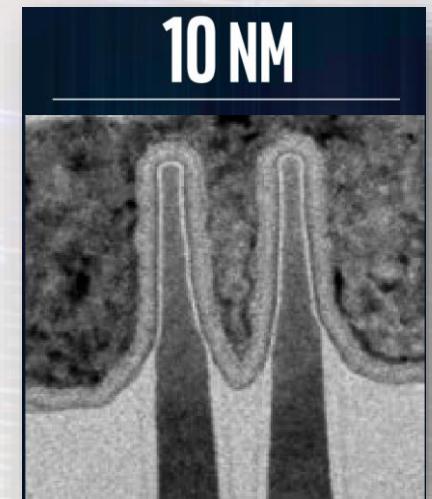
32nm Planar Example



22nm FinFET Example



10 NM

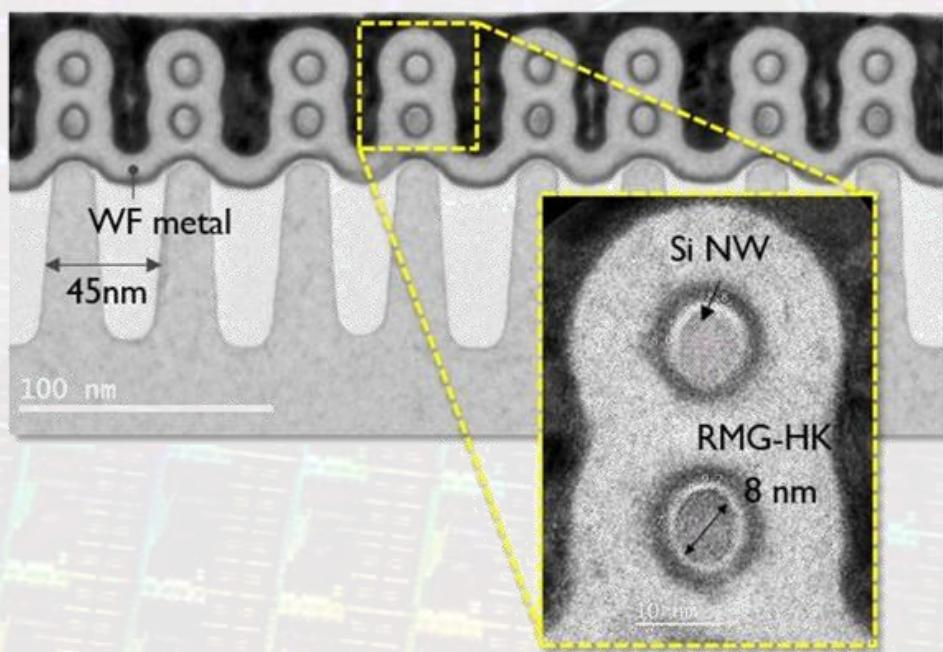




Basics

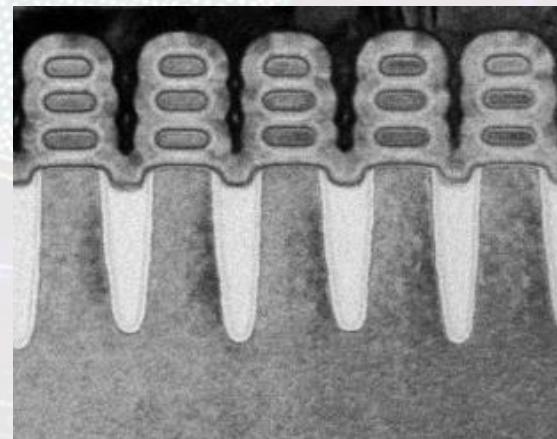
- **Minimal feature size (MFS)**

GAA IMEC demonstration
5nm (2017)



<https://semiengineering.com/going-to-gate-all-around-fets/>

GAA Samsung & IBM
5nm (2019)



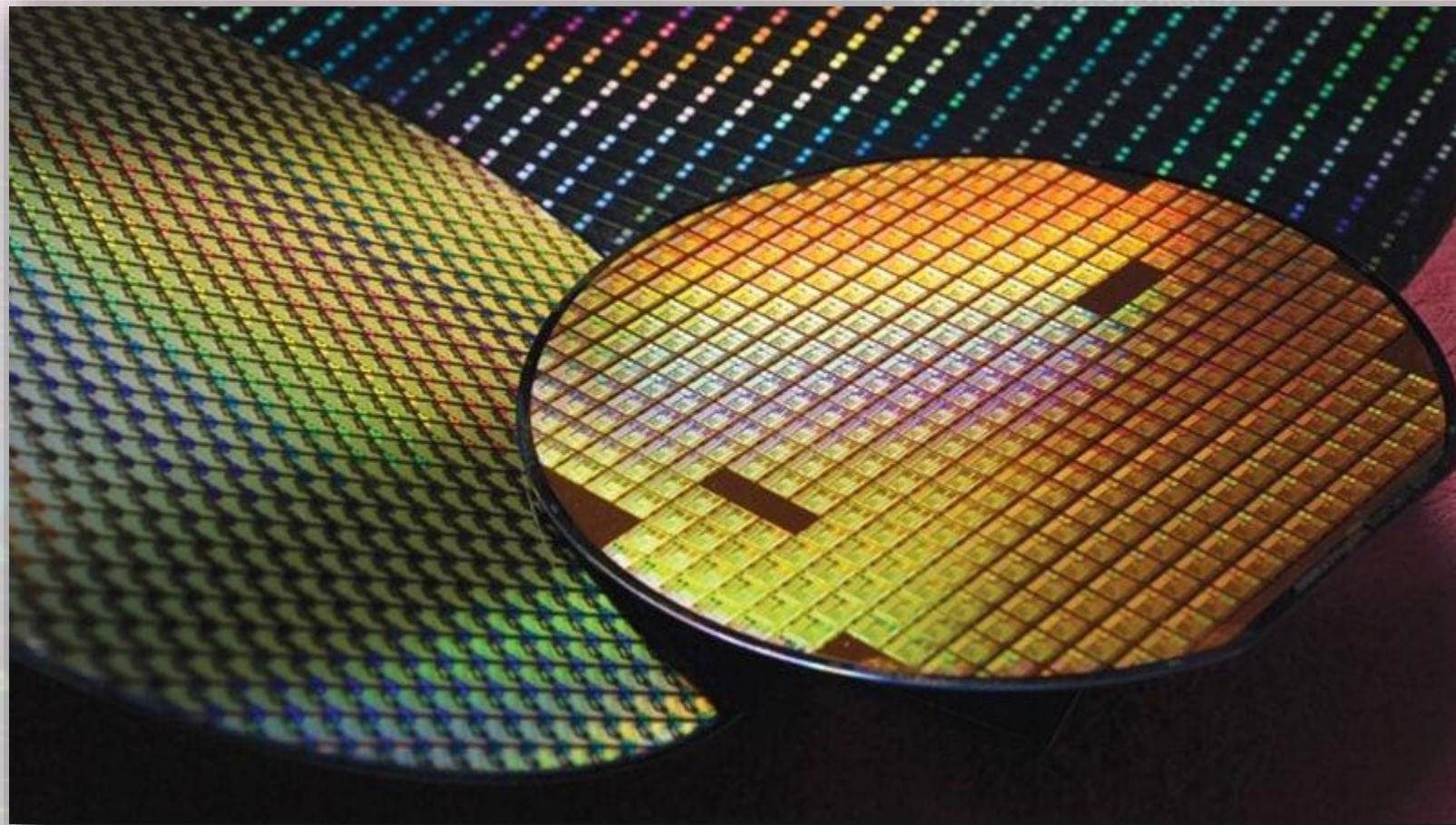
<https://www.eetimes.com/samsung-plans-3nm-gate-all-around-fets-in-2021/#>





Basics

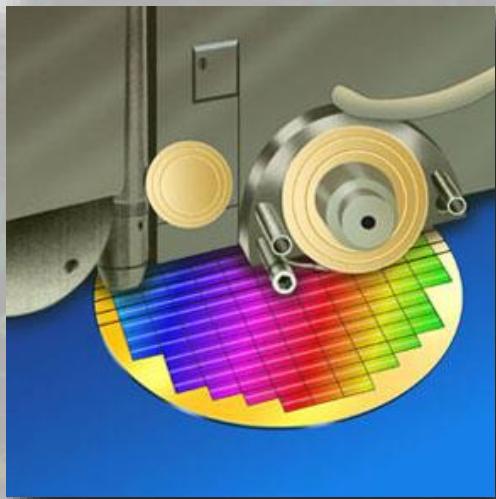
- Finished wafers before dicing



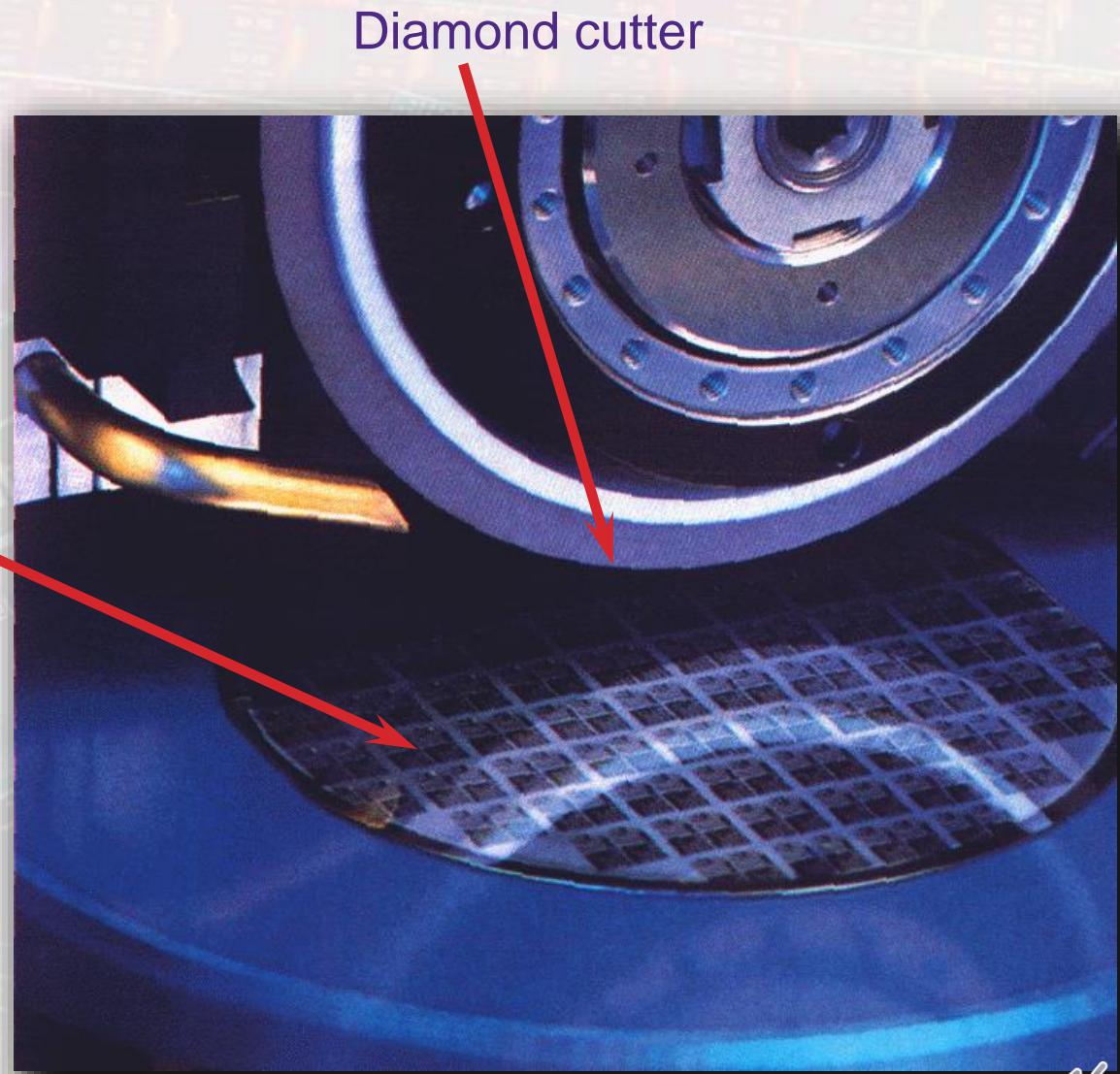


Basics

- Dicing of a wafer



A finished wafer with dice (chips) on top





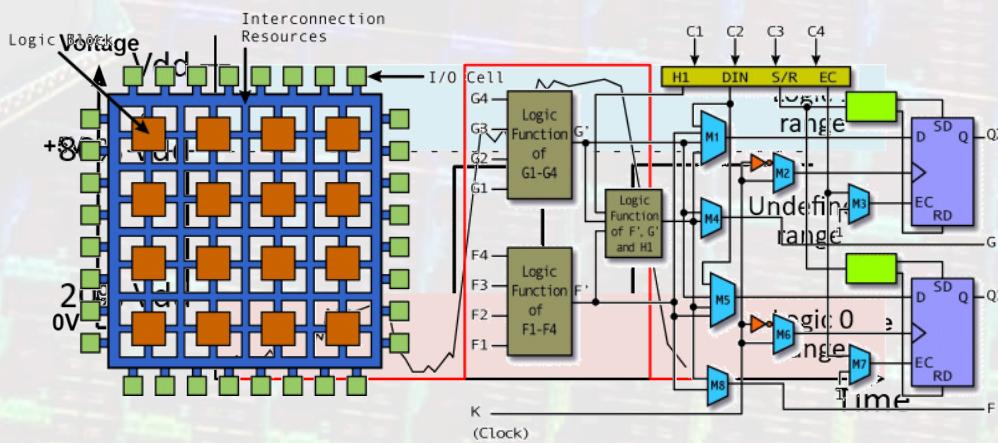
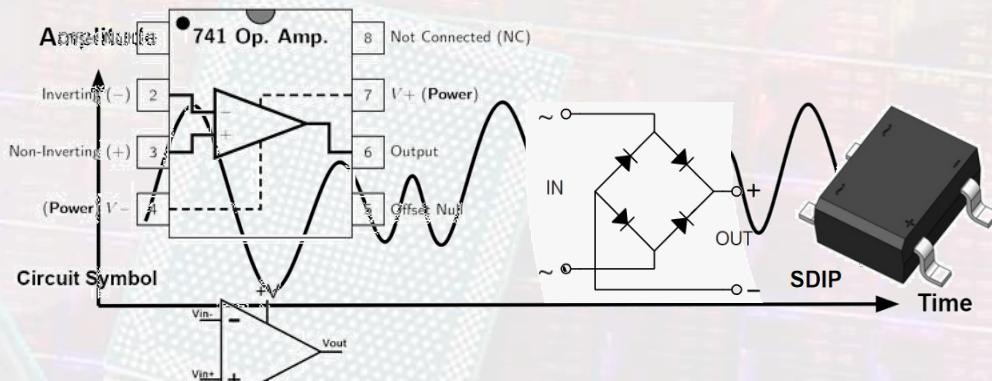
Basics

Analog integrated circuits

- Analog signal is time-varying and generally bound to a range and there is an infinite number of values within that continuous range.
- Operation amplifiers, converters, comparators

Digital integrated circuits

- A digital signal represents data as a sequence of discrete values
- It can only take on one value from a finite set of possible values at a given time.
- If distorted, it still can be read correctly
- CPUs, GPUs, microcontrollers, DSPs, FPGAs

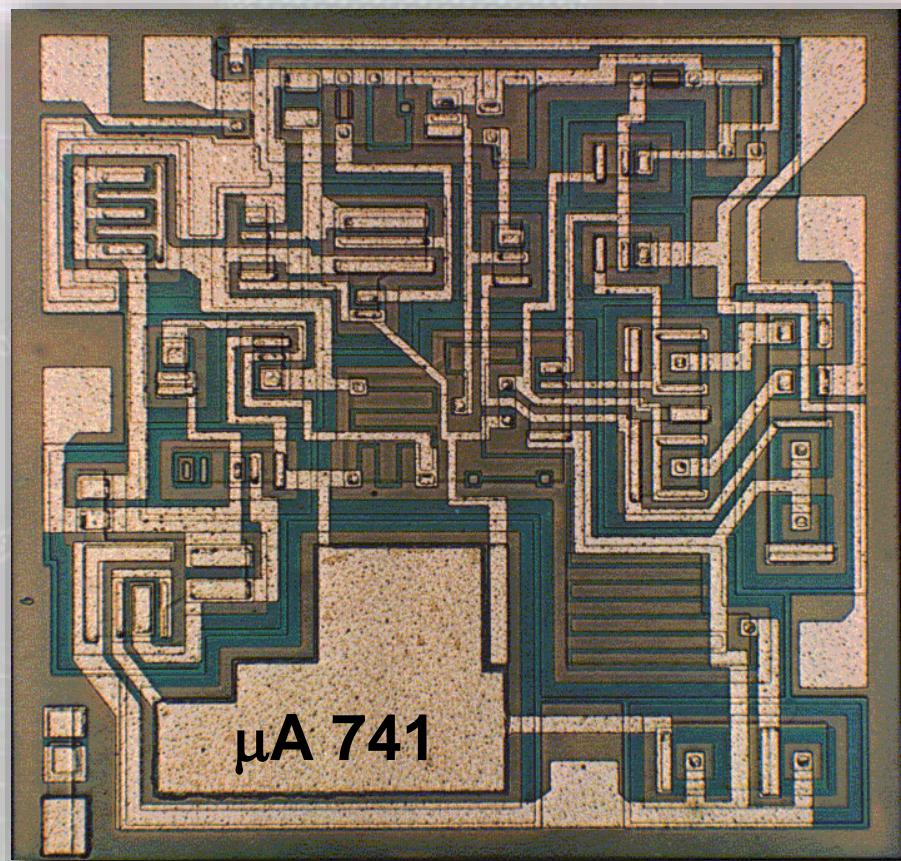
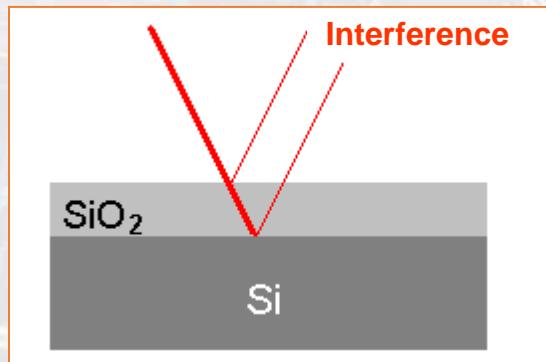




Basics

- A simple analog IC – microphotograph through an optical microscope

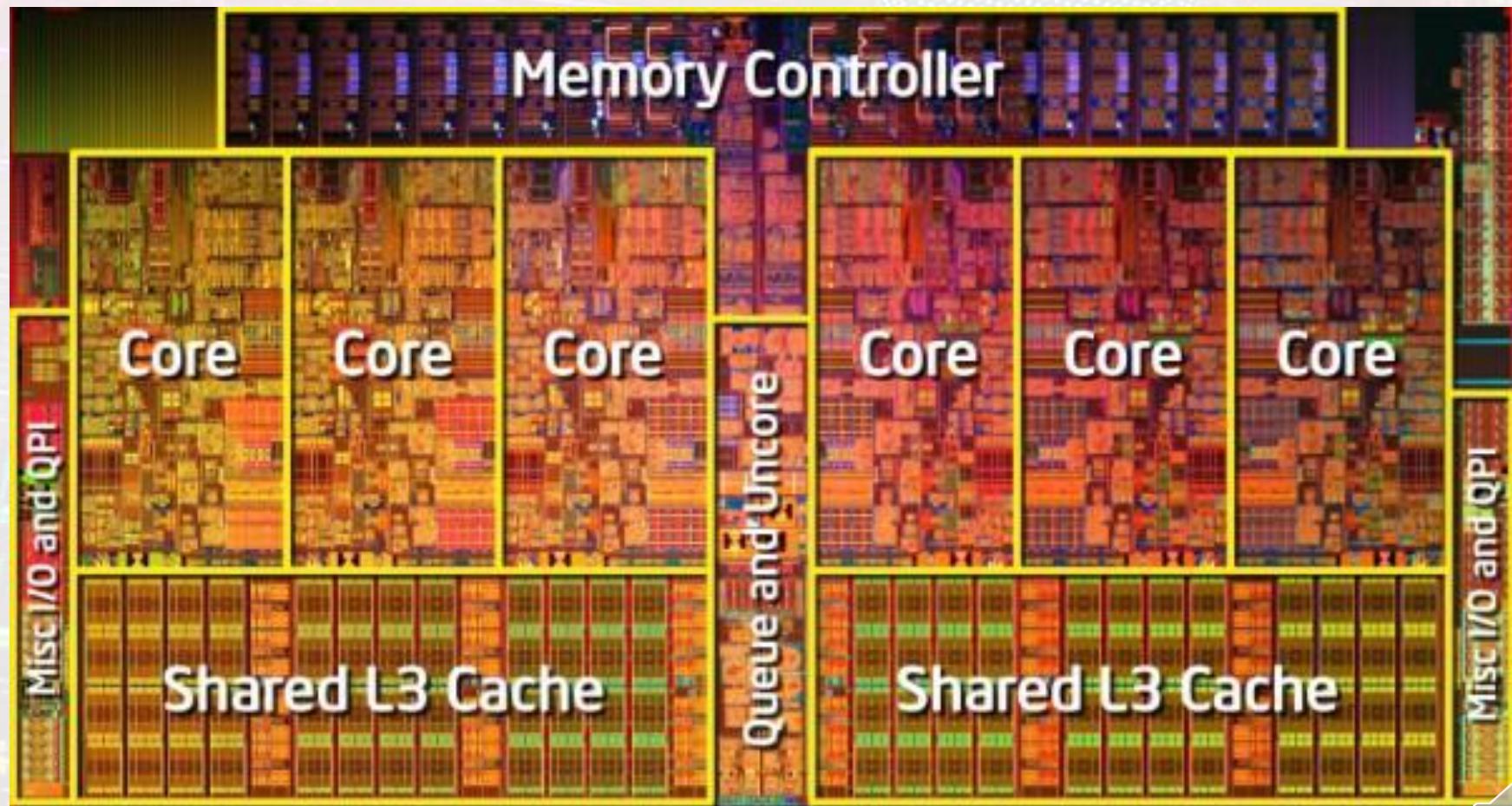
Features seem in different colors due to interference through SiO_2 layers of different thickness:





Basics

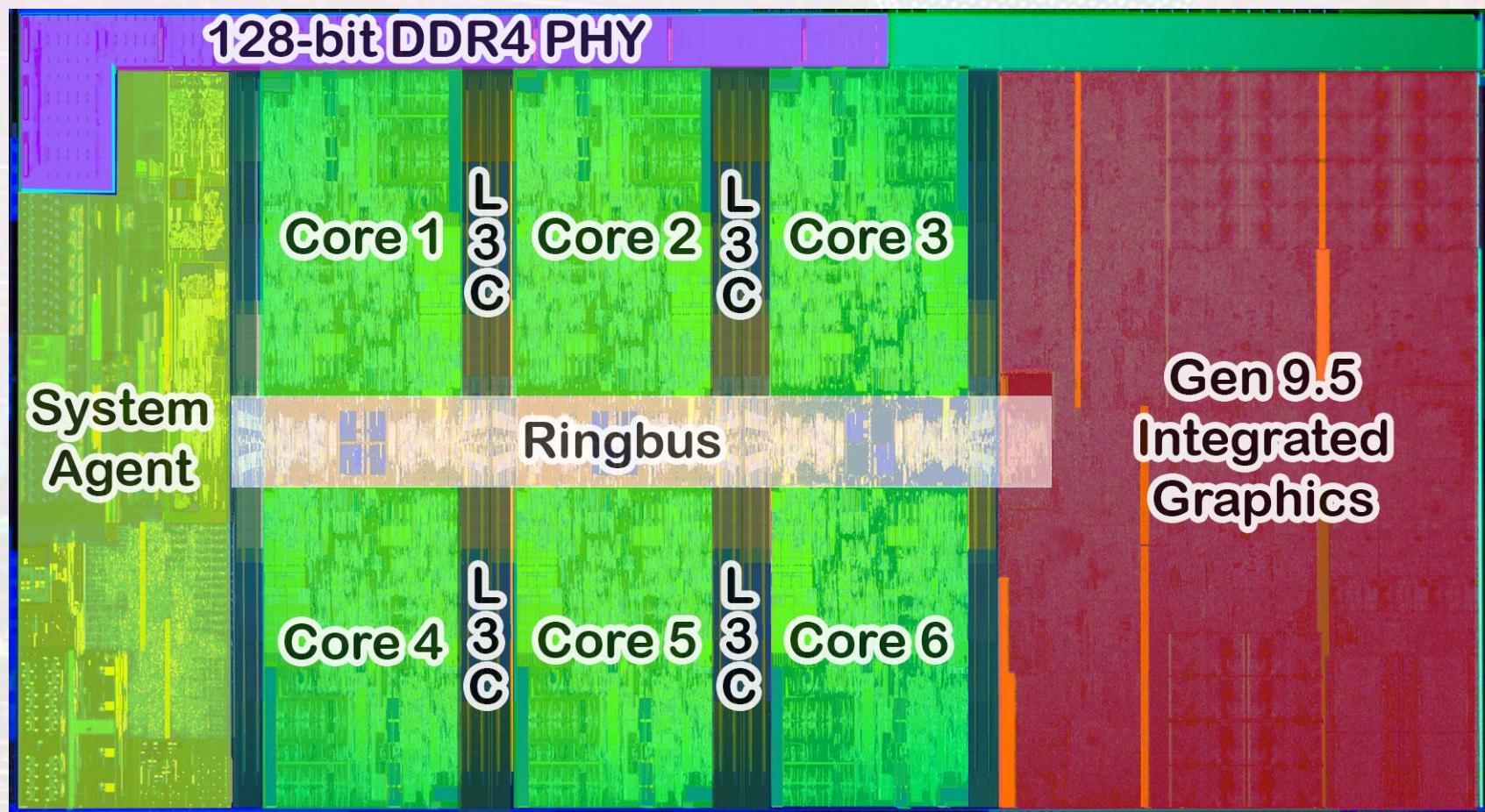
- Intel Xeon 5600, 434 mm²





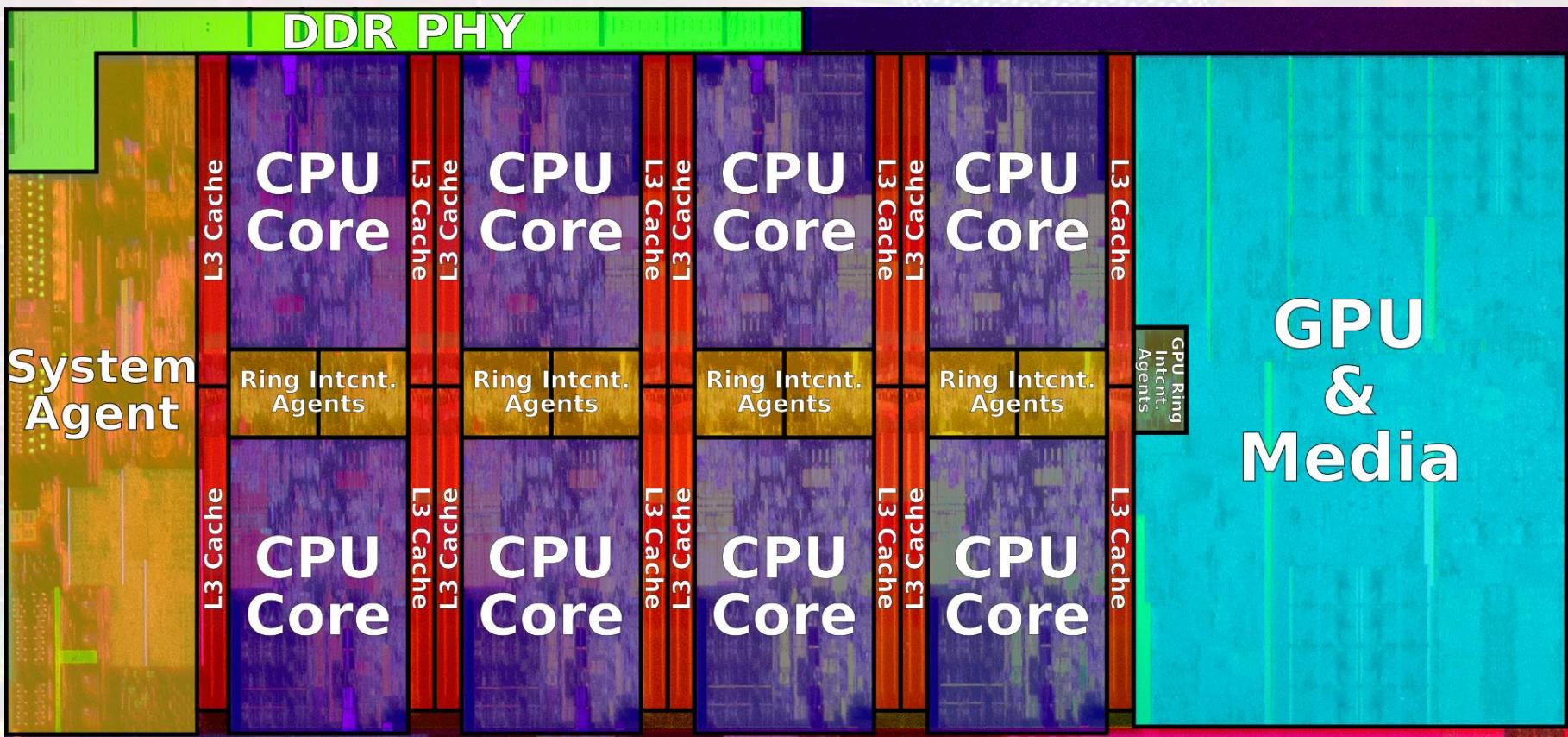
Basics

- Intel Core i5-8400, 150 mm²



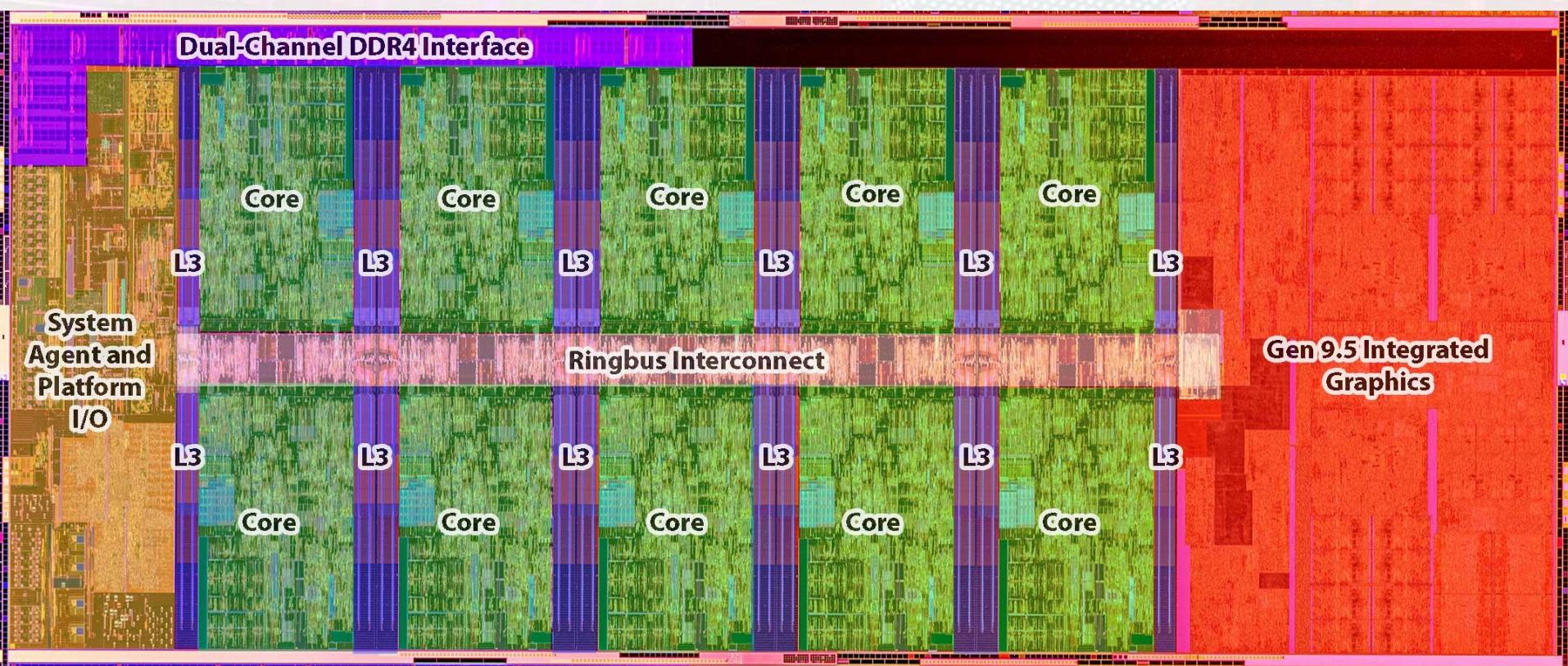
Basics

- Intel Core i9-9900K, ~177 mm² (unknown)



Basics

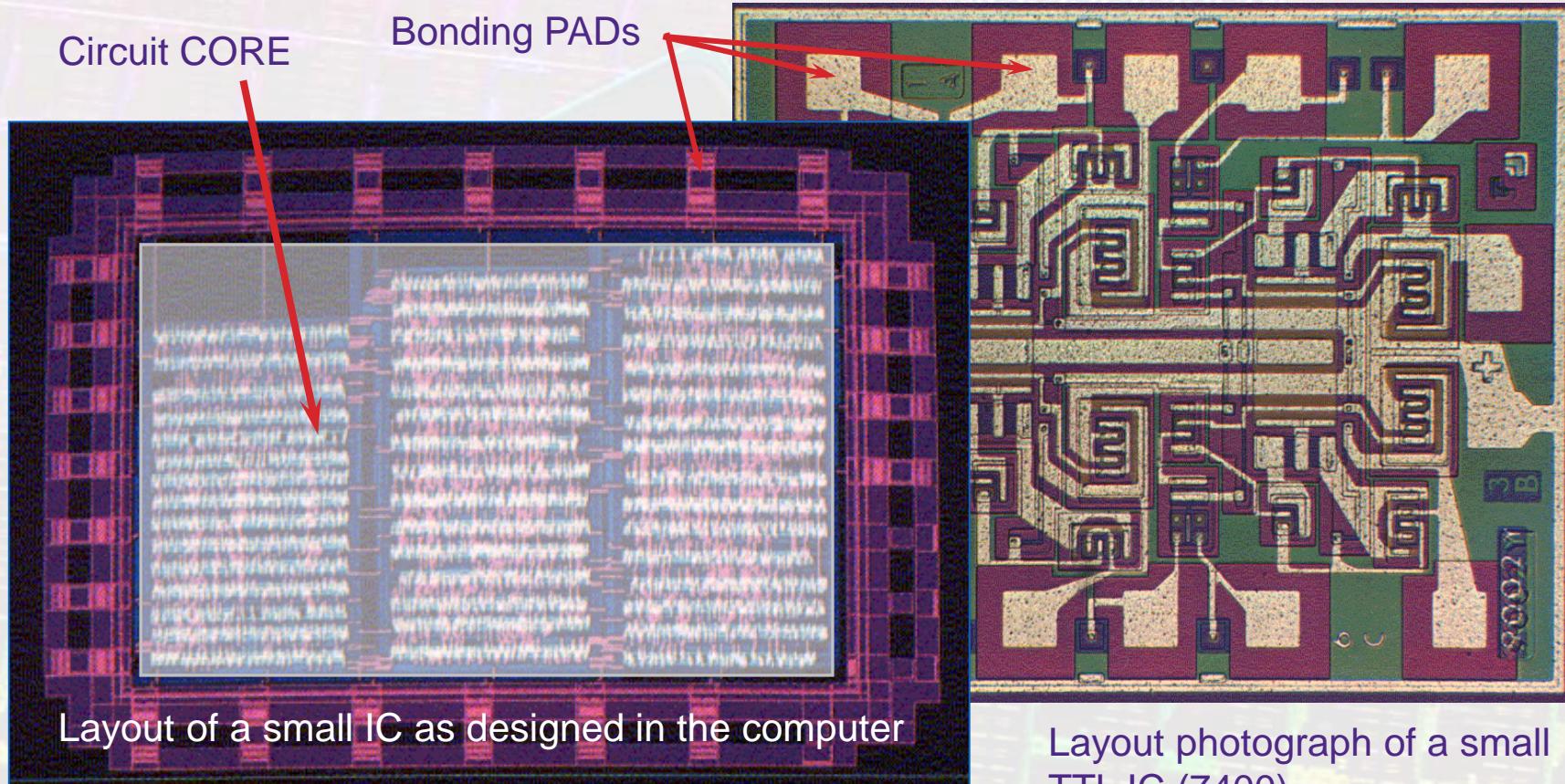
- Intel Core i9-10900K, ~198.4 mm²





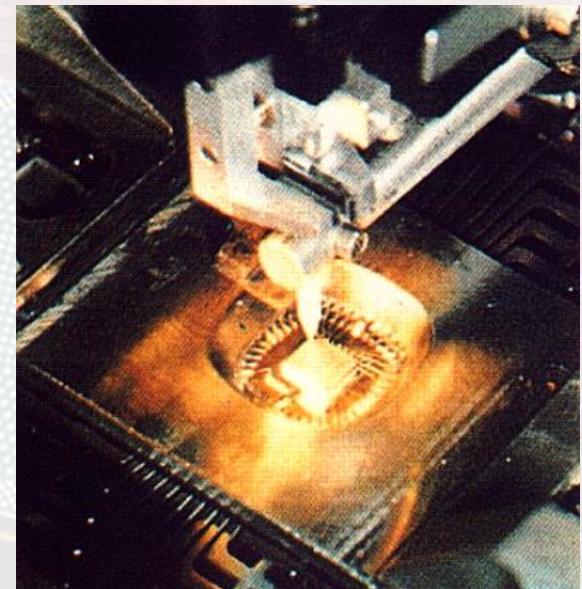
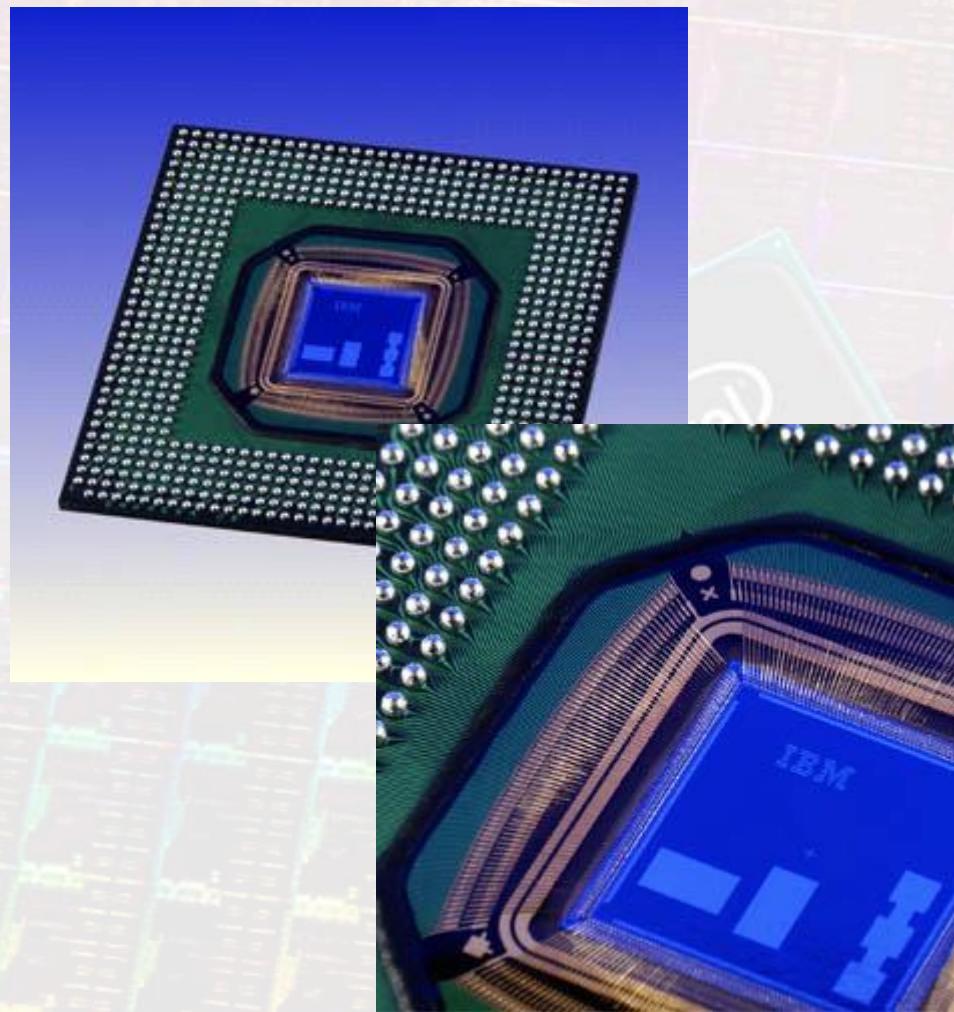
Basics

- **Layout:** collection of all features on all material layers (and in-depth doped ones) which form the IC





Packaging: a great challenge today



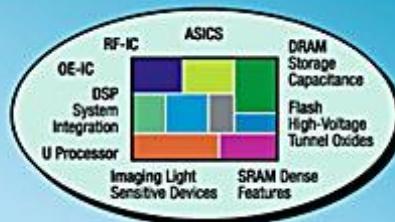
Many connections – fine *pitch*

- *high frequency properties*
- *thermal properties*

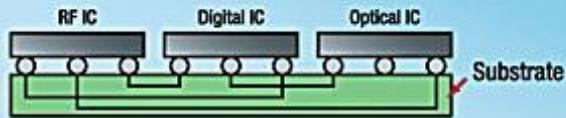


Modern packaging – 3D integration

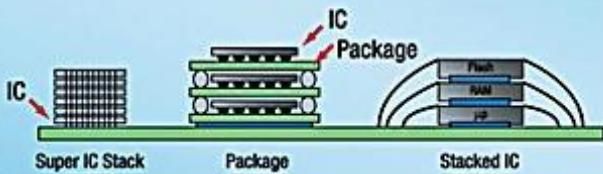
SOC
Complete system on one chip



MCM
(Multi-Chip Module)
Interconnected components

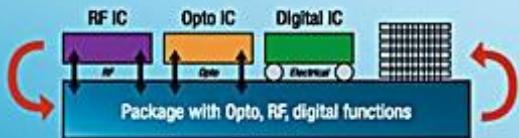


SIP
Stacked chip/package
for reduced form factors



SOP

- Optimizes functions between ICs and package
- Miniaturizes systems



ASIC

DRAM

Si interposer

50µm pitch

Microbump

Top Chip

Cu Wired

Bottom Chip

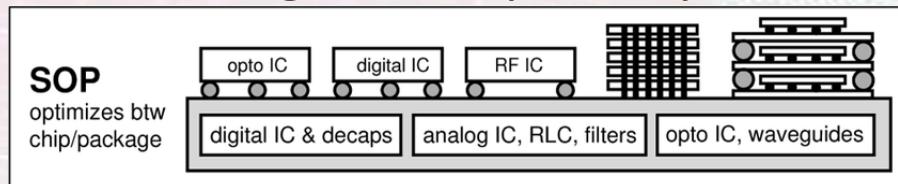
Substrate



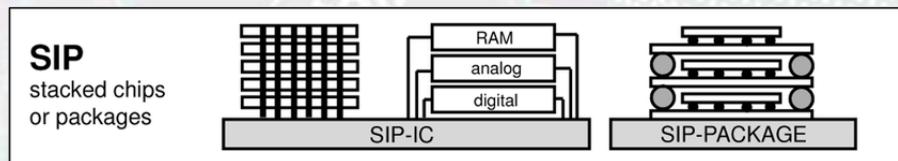


Packaging – one of the big challenges

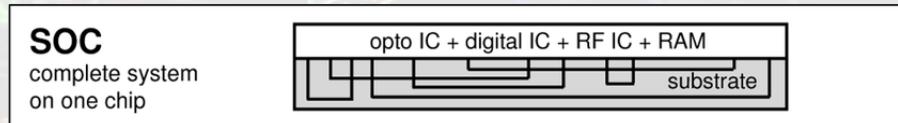
- SoP - System on Package - Complete system integration



- SiP - System in Package - is a number of integrated circuits enclosed in a single module (package)



- SoC - System on Chip - integrates all components of a computer or other electronic system into a single chip.



- LoC - is a device that integrates one or several laboratory functions





The silicon fab

- Cleanroom
- Some process steps





The cleanroom



Tiny structures are created on the surface of the wafers: high level of cleanliness is required!

Special suit – like for astronauts

Special room: **cleanroom**; much cleaner than the operation room of a hospital



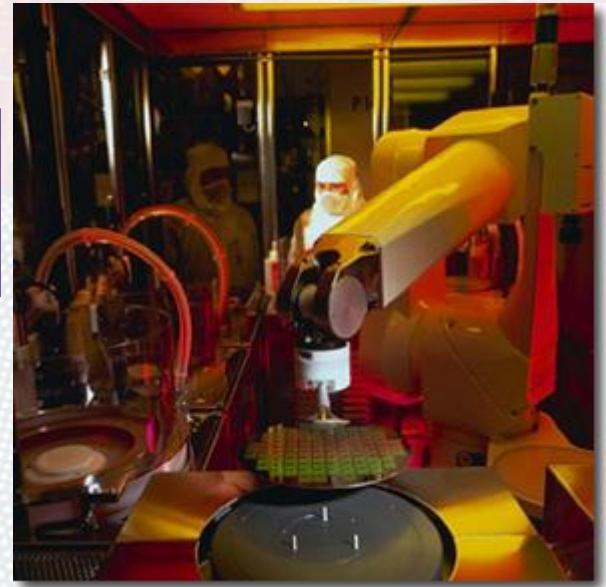


The cleanroom

Tiny structures are created on the surface of the wafers: high level of cleanliness is required!



EET cleanroom



IBM

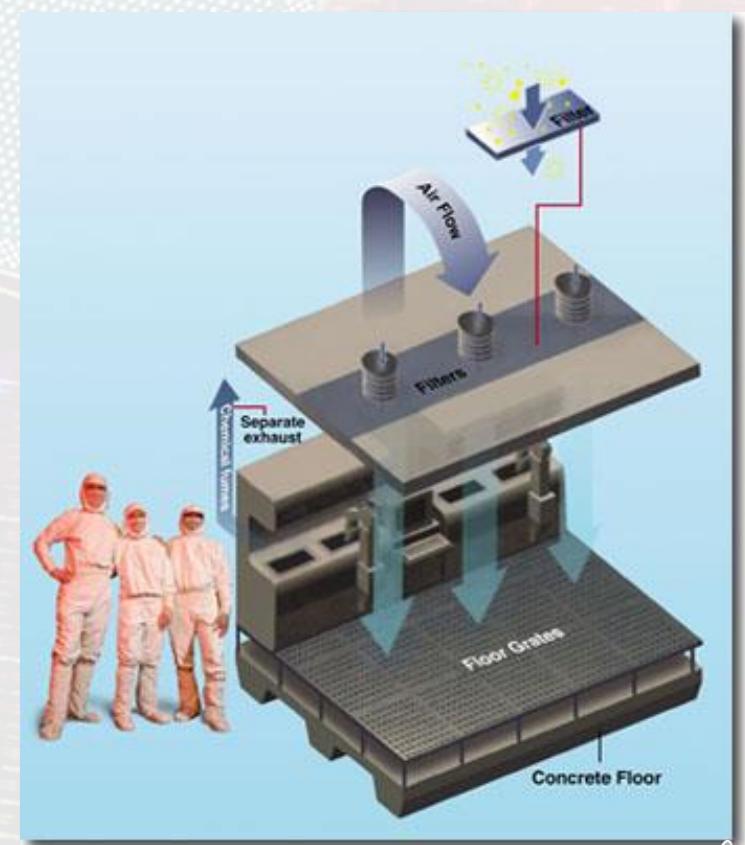
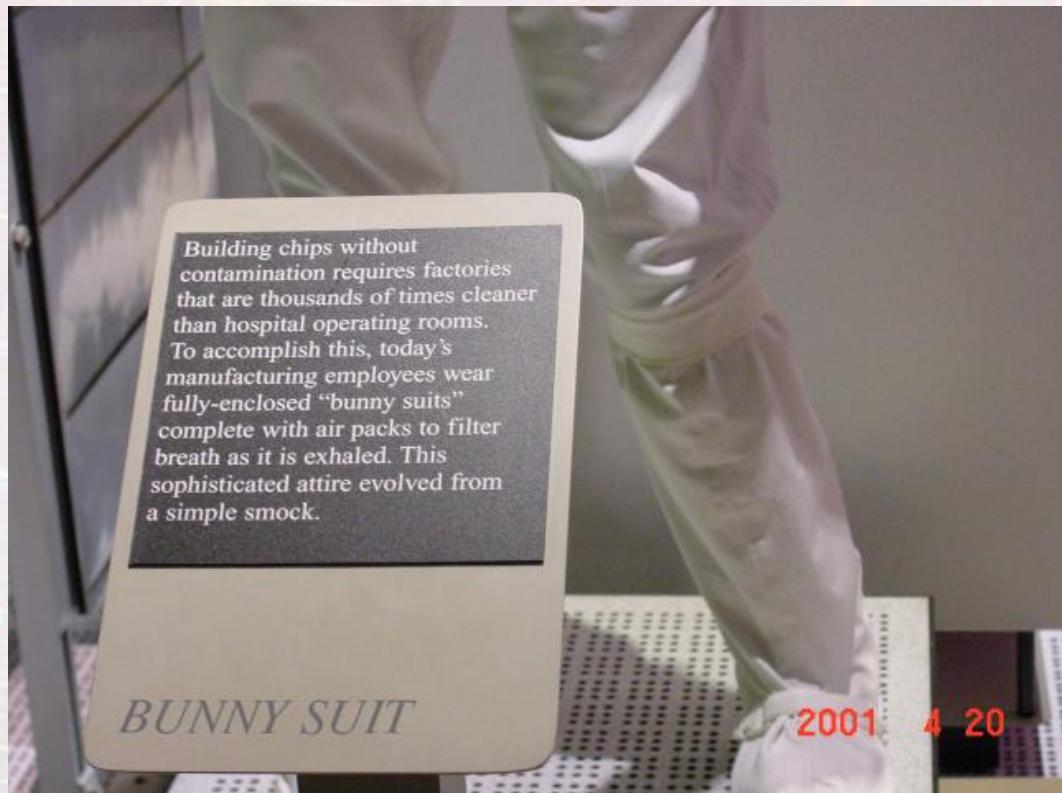


Intel Museum





The cleanroom





The cleanroom



Suiting Up

This is a typical sequence of steps that everybody who plans to enter a fab must follow:

1. Store personal items.
2. Discard any gum, candy, etc.
3. Remove any makeup with clean room soap and water.
4. Take a drink of water to wash away throat particles.
5. Cover any facial hair with a surgical mask or beard/mustache cover.
6. Put on a lint-free head cover.
7. Clean shoes with shoe cleaners.
8. Place shoe covers over street footwear.
9. Enter an air shower designed to blow off loose particles.
10. Exit air shower and enter shoe change room.
11. Clean any small, pre-approved items to be taken inside.
12. Pick up booties.
13. Sit on "dirty" side of bench.
14. Put on one bootie.
15. Swing booted foot to "clean" side of bench.
16. Put on other bootie on "dirty" side.
17. Swing booted foot to "clean" side.
18. Enter main gowning room.
19. Set aside badge, pager, and any other items to be taken inside.
20. Put on nylon gowning gloves.
21. Obtain bunny suit and belt from hanger.
22. Put on bunny suit without letting it touch the floor.
23. Put on belt.
24. Tuck bunny suit pant legs into booties.
25. Fasten snaps at top of booties.
26. Attach filter unit to belt.
27. Attach battery pack to belt.
28. Plug filter unit into battery pack.
29. Obtain helmet, safety glasses.





Cleanroom at the DED

- New semiconductor lab @ Building Q



*Semiconductor Technology
Laboratory,*

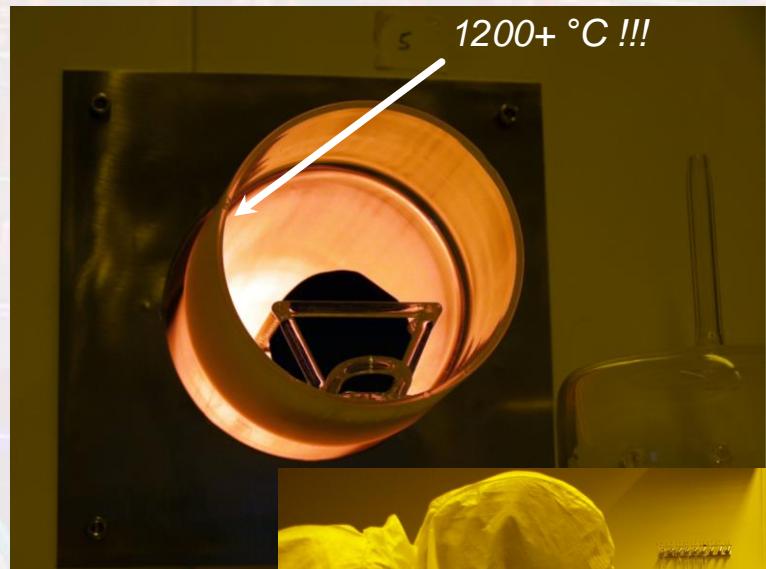
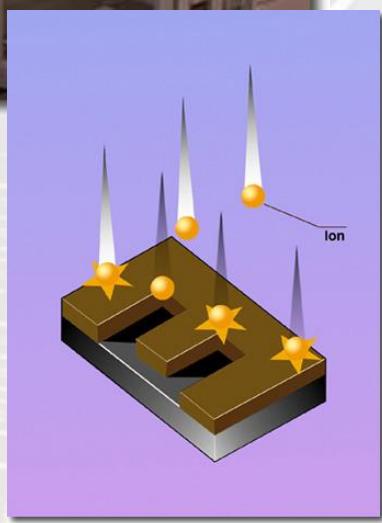
*Smart System Integration
MSc minor spec.*

Solar cells manufacturing





Ion-implanter, diffusion furnace



Semiconductor Technology Lab,
Microelectronics branch at DED

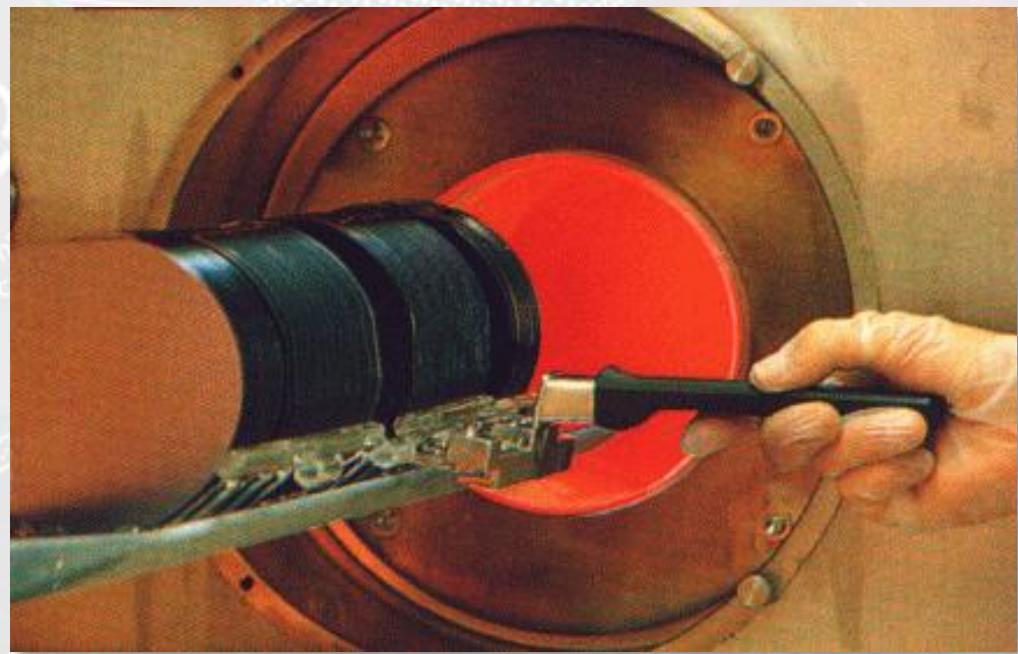




A batch

- Si wafers are processed in so called batches
- 40..100 wafers/batch, 10 000 – 50 000 chips/batch
- **Batch fabrication**

Inserting a batch into a diffusion furnace





Wafer sizes

- Today at around 30cm in diameter (8") or even 12"





An Intel *fab*





Intel fab sites - 2022

Fab name	City	Production start year	Process (wafer, node)
D1B	USA, Oregon, Hillsboro	1996	300mm, Development
RB1	USA, Oregon, Hillsboro	2001	300mm, Development
D1C	USA, Oregon, Hillsboro	2001	300mm, Development
RP1	USA, Oregon, Hillsboro	2001	300mm, Research
D1D	USA, Oregon, Hillsboro	2003	300mm, Development
D1X	USA, Oregon, Hillsboro	2013	300mm, Development
Fab 11X	USA, New Mexico, Rio Rancho	1995 upgrade 2020/2021 with 22/14	300mm, 45nm/32nm, Packaging
Fab 12	USA, Arizona, Chandler	2006	300mm, 22nm/14nm/10nm
Fab 22	USA, Arizona, Chandler	2002	300mm, 22nm/14nm/10nm
Fab 24	Ireland, Leixlip	2006	300mm, 14nm ^[2]
Fab 28a	Israel, Kiryat Gat	1996	300mm, 22nm
Fab 28	Israel, Kiryat Gat	2008	300mm, 22nm/10nm ^{[3][4]}
Fab 32	USA, Arizona, Chandler	2007	300mm, 22nm/14nm/10nm
Fab 42	USA, Arizona, Chandler	2020	300mm, 10nm/7nm (2024)
SC2	USA, California, Santa Clara		Reticle/Masks , Intel Mask Operations ^[8]





Intel fab sites - 2022

Fab name	City	Production start year	Process (wafer, node)
Fab 52	USA, Arizona, Chandler	(2024) ^[6]	300mm, 7nm
Fab 62	USA, Arizona, Chandler	(2024) ^[7]	300mm, 7nm
Fab 34	Ireland, Leixlip	2023	300mm, 7nm ^[5]
	Malaysia, Kedah, Kulim	(2024)	300mm, Packaging ^[9]





Intel fabs 2006-2008

- 65nm fabs, ~2006



- 45nm: "Fab32", 2007-



An Intel manufacturing technician uses a scanner to start the very first 45nm production lot of 300mm wafers inside of Fab 32, Intel's first high-volume 45nm chip factory in Chandler, Ariz.



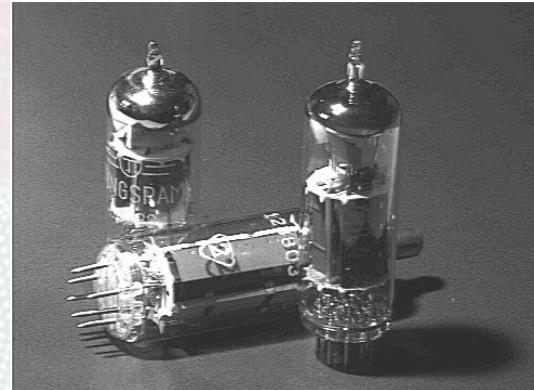
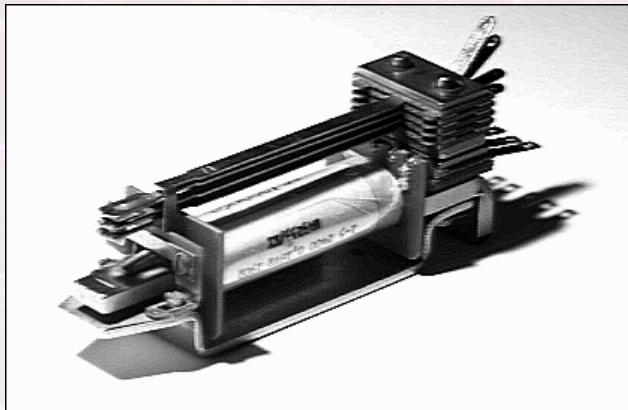


History, trends

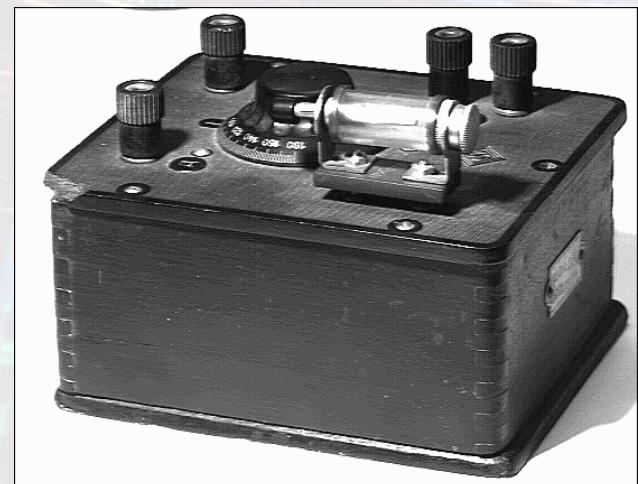
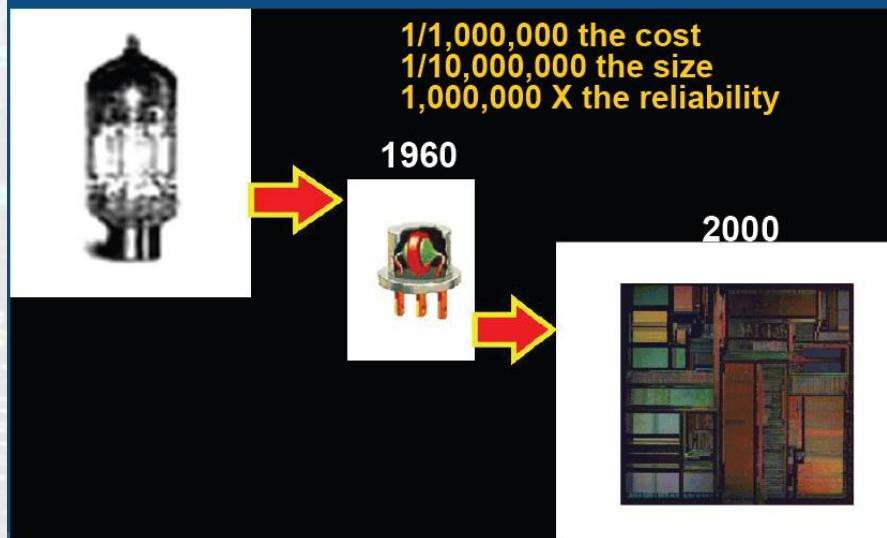


Roots

1837 Morse, telegraph



1920



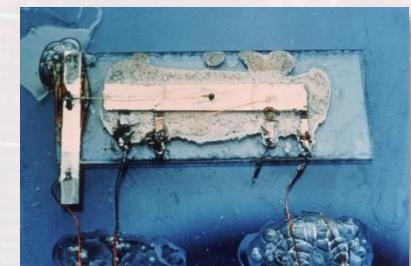
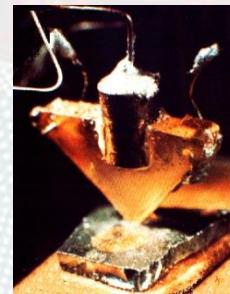
~1920 radio receiver



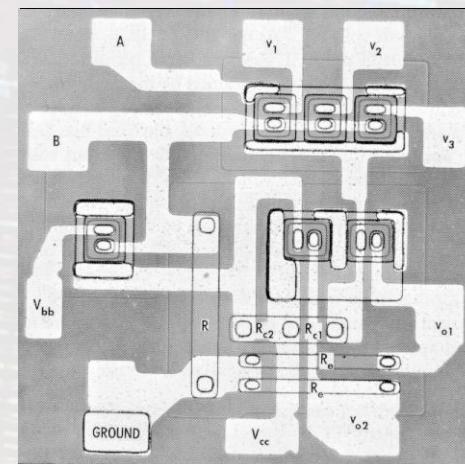
Microelectronics: fastest growing industry

Revolution of the transistors

- Transistor – Bardeen (Bell Labs), 1947
- Bipolar transistor – Schockley, 1949
- The 1st bipolar logic gate – Harris, 1956
- The 1st monolithic IC – Jack Kilby, 1959
- The 1st commercial IC with logic gates – Fairchild, 1960
- TTL – 1962..1990-ies
- ECL – 1974..1980-ies



You can make an IC of such a "complexity" in the cleanroom of the Department





Microelectronics: fastest growing industry

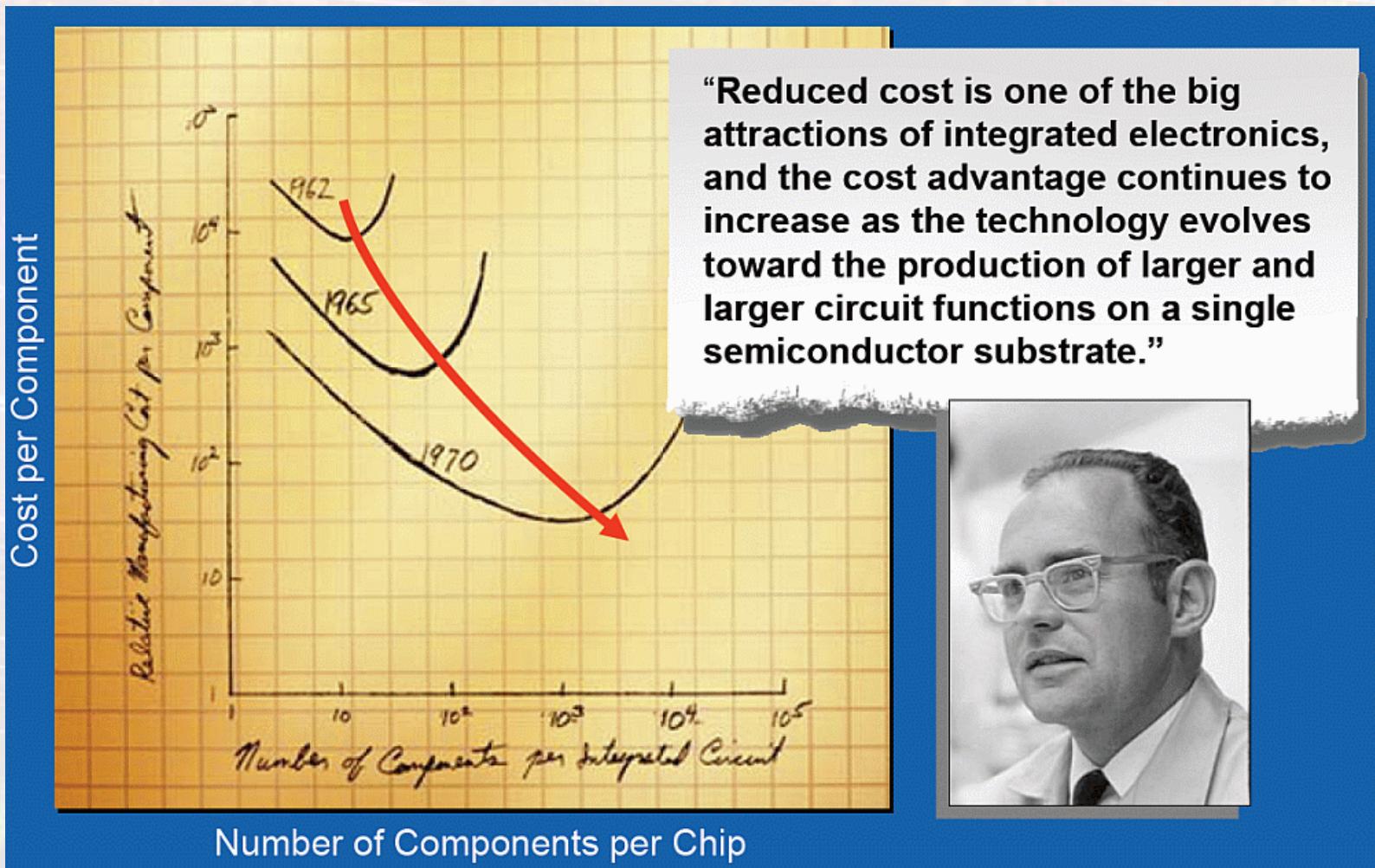
Development of the MOSFETs:

- MOSFET transistor – Lilienfeld (Canada, 1925) and Heil (England, 1935)
- CMOS – 1960s, stack due to manufacturing problems
- pMOS processes in the 1960s
- nMOS processes in the 1970s (4004, 8080)
- CMOS processes from the 1980s – preferred MOSFET process due to low power consumption
- Nowadays e.g.:
 - BiCMOS, GaAs, SiGe – for very high frequency circuits
 - SOI, Cu metallization, *low-K* dielectrics





Gordon Moore, 1965:





Microelectronics: fastest growing industry

Moore's law

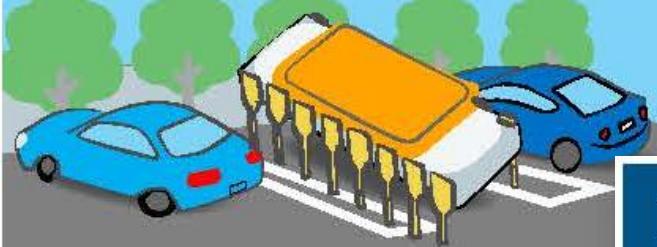
- In 1965 Gordon Moore predicted that in every 14..18 months the number of transistors integrated in a chip will double (exponential growth)
- This prediction is valid even today.
- The 1 million transistors/chip threshold was reached in the 1980s
 - 2300 transistors, 1 MHz clock frequency (Intel 4040) - 1971
 - 16 million transistors (UltraSPARC III)
 - 42 million transistors, 2 GHz clock frequency (Intel P4) - 2001
 - 140 million transistors, (HP PA-8500) – 1998
 - ~3 billion transistors, (i7-9900K) - 2018
- *More than Moore*: further increase of integration density, e.g. 3D stacking of chips (RAM-s, pen drives)





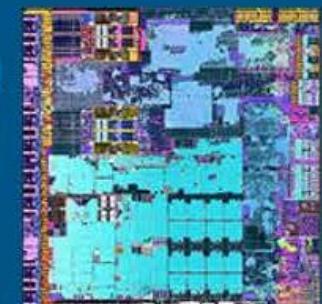
Moore's law

IF AN INTEL-BASED ANDROID** PHONE WERE BUILT USING 1971 TECHNOLOGY, THE PHONE'S MICROPROCESSOR ALONE WOULD BE THE SIZE OF A PARKING SPACE.



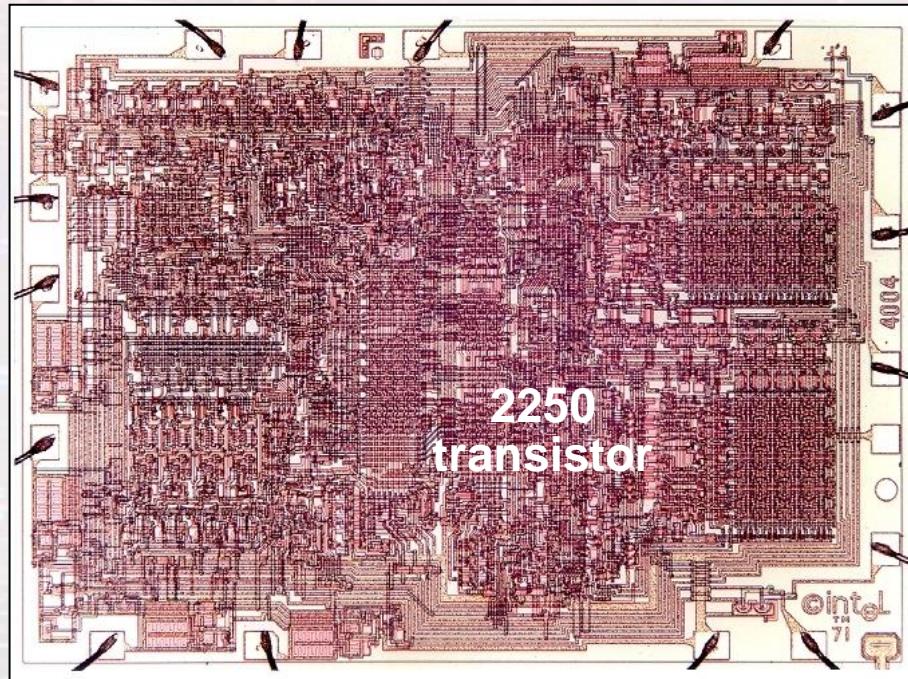
- ▶ Result of 50 years of progress presented through a modern CPU and a processor of a modern smart phone

COMPARED TO INTEL'S FIRST MICROPROCESSOR, THE INTEL® 4004, TODAY'S 14NM PROCESSORS DELIVER 3,500 TIMES THE PERFORMANCE, AT 90,000 TIMES THE EFFICIENCY AND AT 1/ 60,000TH THE COST.





Microelectronics: fastest growing industry



1971 -Intel 4040

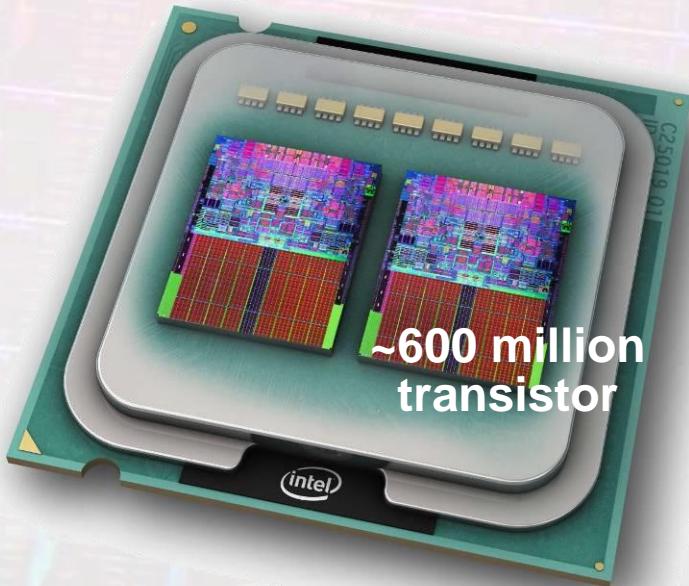


2002 - Intel Pentium IV

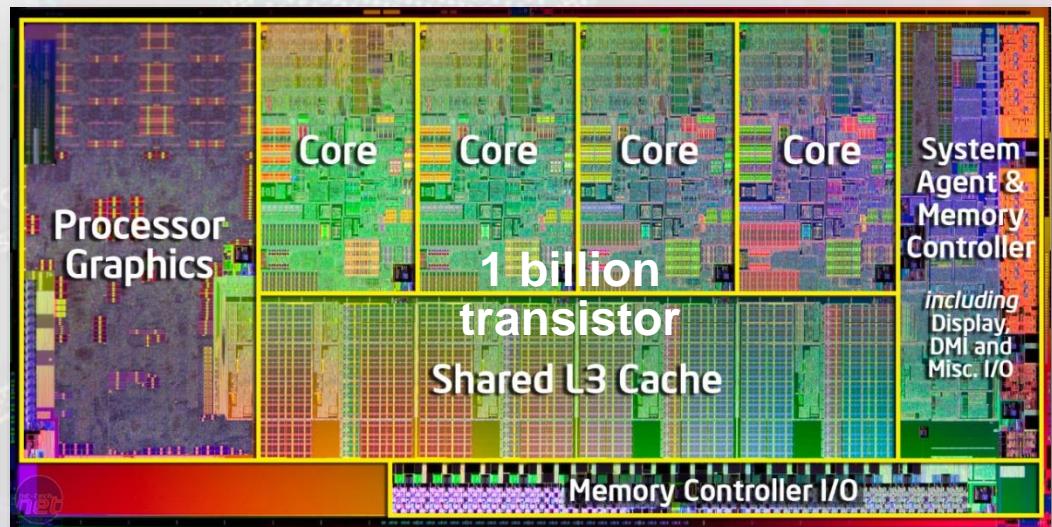




Microelectronics: fastest growing industry



2007 - Intel Core2 EE



2012 - Core i7





Microelectronics: fastest growing industry

Moore's Law: circa 2008

Intel® Atom™ - dual-core

47 Millions Transistors
45nm node
Hi-k Metal Gate
193 dry Litho

Rice – single grain

In 2014, on 14nm technology, the above chip would be 1/8 the size
- Much smaller than the grain of rice!





Prognosis: roadmap

The screenshot shows a web browser window for the International Technology Roadmap for Semiconductors (ITRS) at itrs2.net. The page features a navigation bar with links to HOME, ITRS NEWS, ITRS REPORTS, ITRS SCHEDULE, ITRS MODELS AND PAPERS, and IRC/FOCUS TEAMS/ITWG INFORMATION. The main content area displays the ITRS 2.0 logo, followed by a section titled "ITRS SPONSORS" listing five industry associations:

- ESIA** European Semiconductor Industry Association
- JEITA** Japan Electronics and Information Technology Industries Association
- KSIA KOREA SEMICONDUCTOR INDUSTRY ASSOCIATION** Korean Semiconductor Industry Association
- SIA SEMICONDUCTOR INDUSTRY ASSOCIATION** Semiconductor Industry Association
- TSIA** Taiwan Semiconductor Industry Association





Recent – company webpages

2016-17 CCG Mobile Product Roadmap

Schedule represents front-end of [RTS](#)

BDW = Broadwell	BSW = Braswell
SKL = Skylake	APL = Apollo Lake
KBL = Kaby Lake	GLK = Gemini Lake
CNL = Cannon Lake	CHT = Cherry Trail
CFL = Coffee Lake	

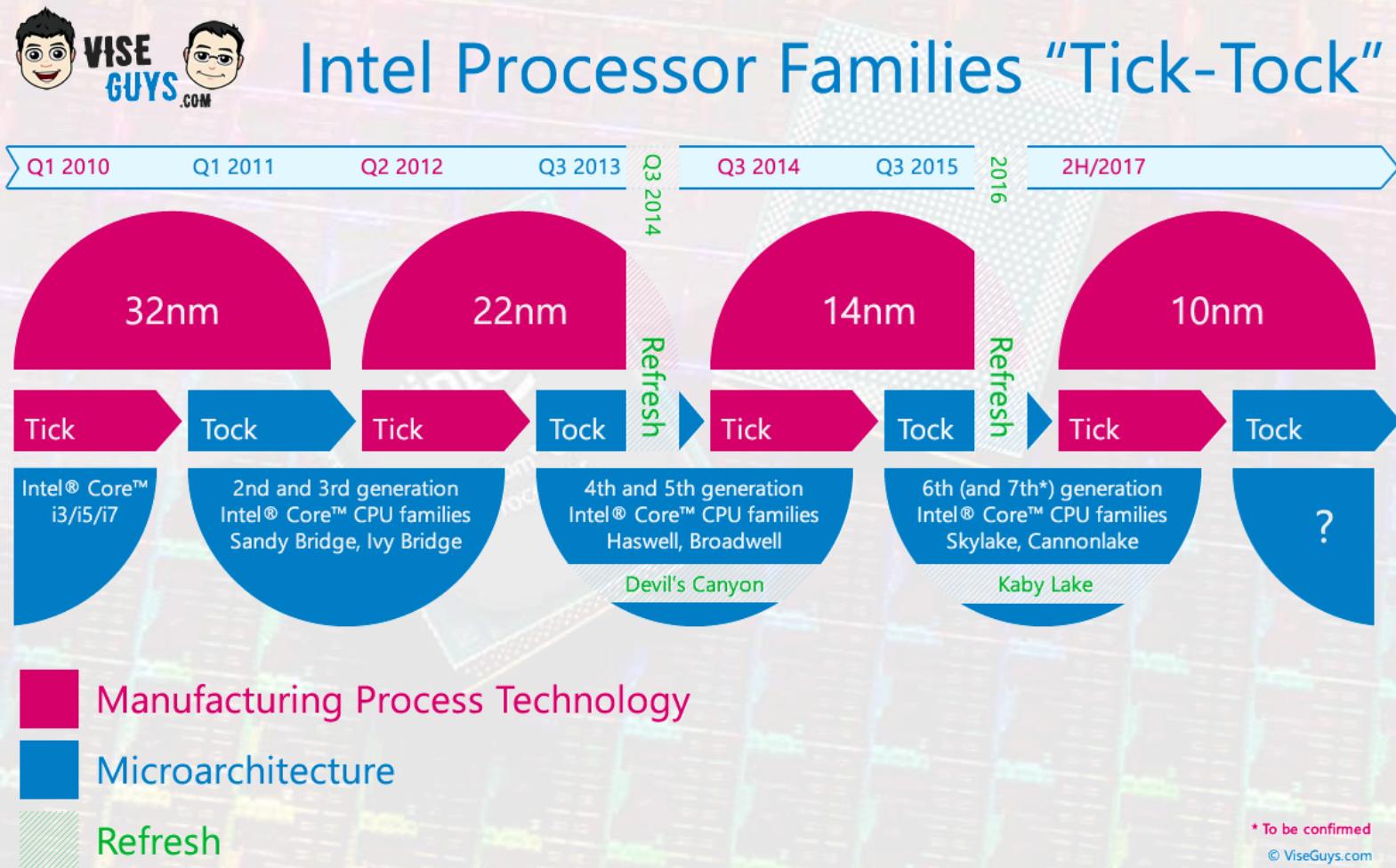


	Q2'16	Q3'16	Q4'16	Q1'17	Q2'17	Q3'17	Q4'17	Q1'18	Q2'18
H Processor	Skylake 45W, 2-chip BGA								QC GT4e 6C GT2 CFL 45W
	Skylake 45W, 2-chip BGA	QC GT2		Kaby Lake 45W, 2-chip BGA				QC GT2	
U Processor	Skylake 15W/28W, SoC BGA		GT3e	Kaby Lake 15W/28W, SoC BGA			GT3e	CFL 15W/28W	QC GT3e
	Skylake 15W SOC BGA GT2			Kaby Lake 15W, SoC BGA			GT2	CNL 15W, SoC BGA	GT2
Y Processor	Skylake 4.5W, SoC BGA	GT2		Kaby Lake 4.5W, SoC BGA			GT2	CNL 5.2W, SoC BGA	GT2
N Processor	BSW 4W/6W, SoC BGA	QC	Apollo Lake 4W/6W, SoC BGA			QC	GLK 4W/6W,Soc BGA		QC



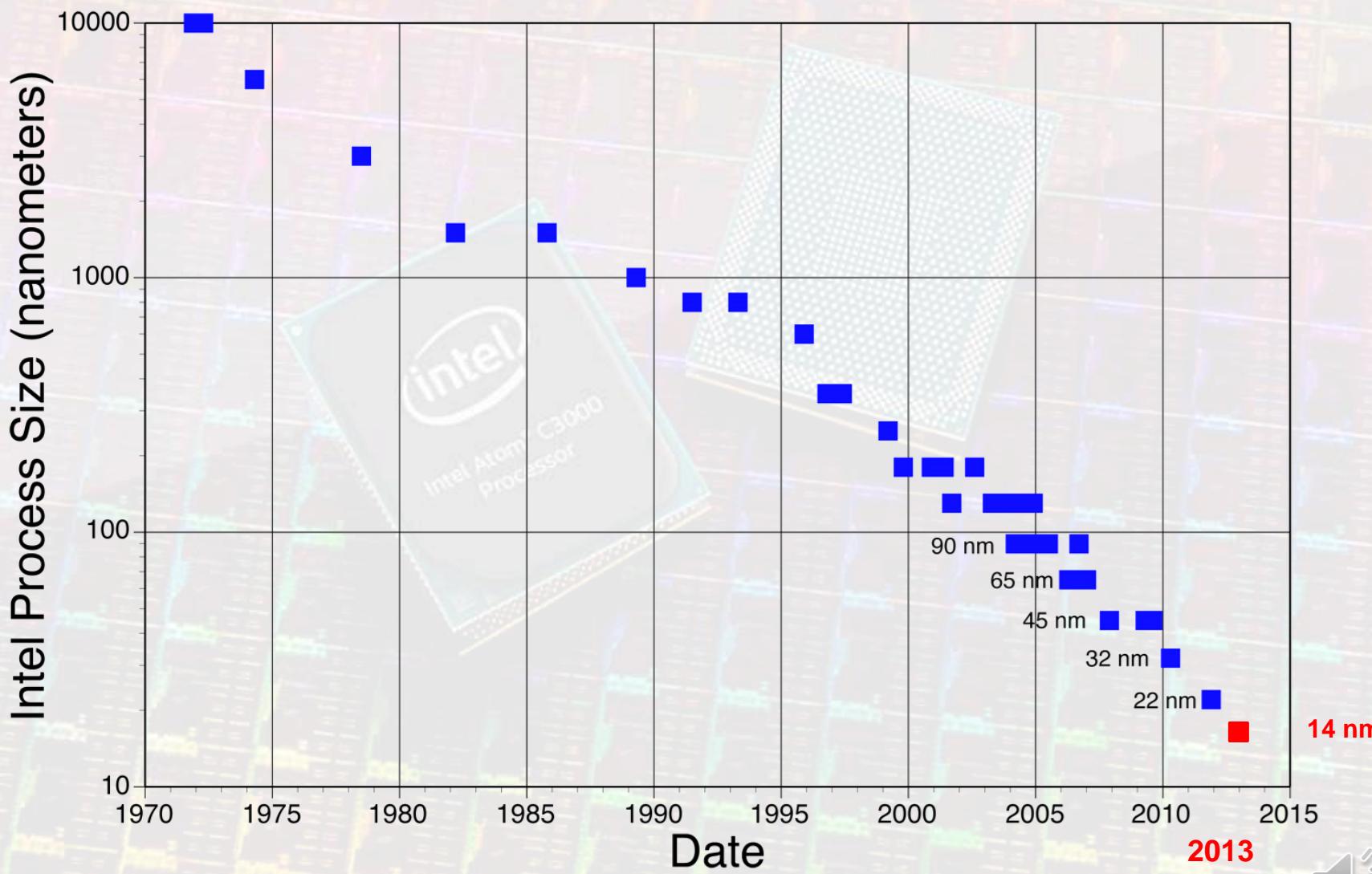


Recent – company webpages



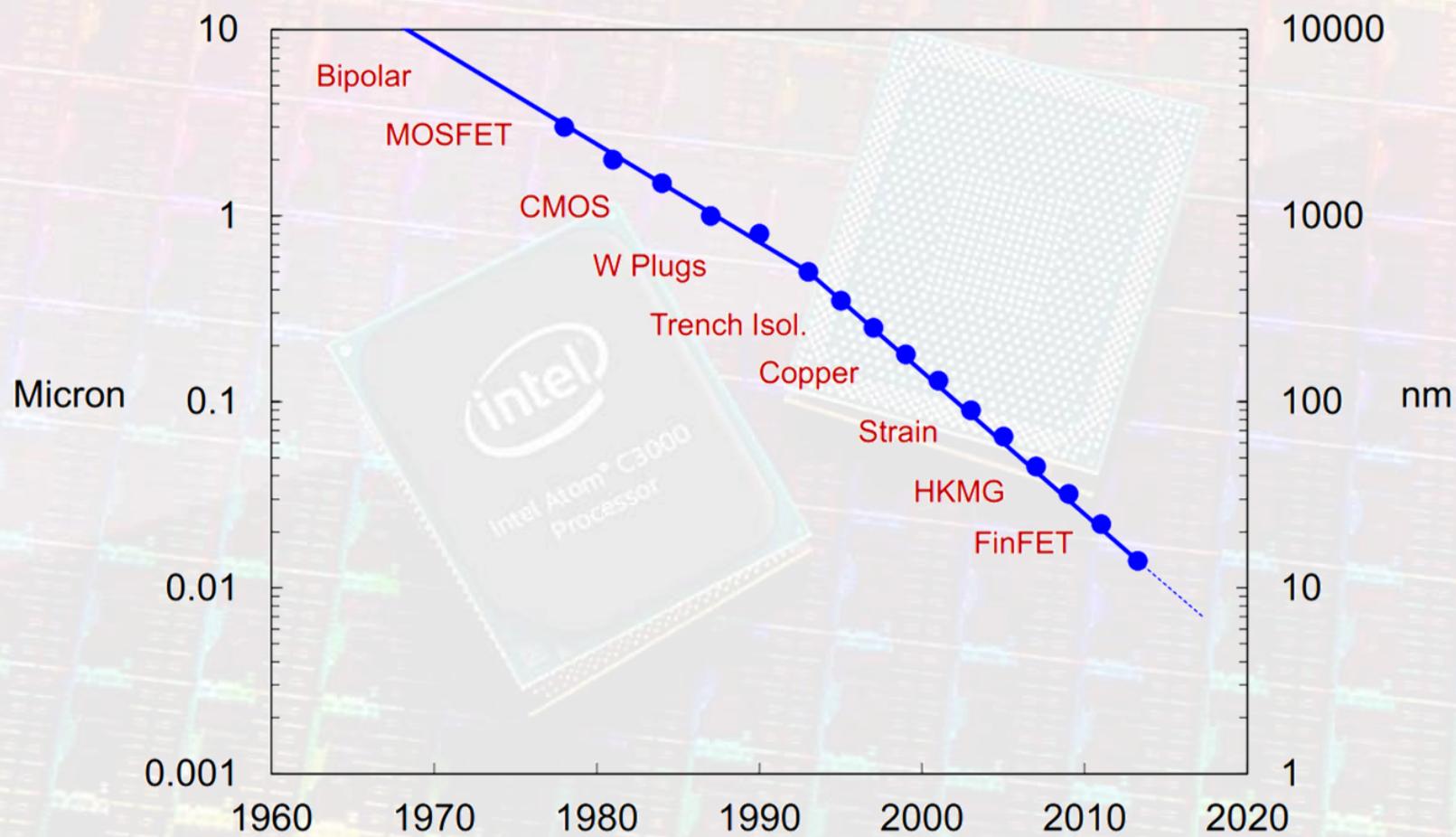


Minimal feature size – trend (Intel)





Minimal feature size – trend (Intel)



Process/device innovation has always been an indispensable part of scaling





Toplist of processors in 2015

Intel HEDT Flagship Processors (Gen vs Gen Specifications Comparison):

Intel HEDT Family	Gulftown	Sandy Bridge-E	Ivy Bridge-E	Haswell-E	Broadwell-E	Skylake-E
Process Node	32nm	32nm	22nm	22nm	14nm	14nm
Flagship SKU	Core i7-980X	Core i7-3960X	Core i7-4960X	Core i7-5960X	Core i7-6950X	Core i7-7970X (TBA)
Max Cores/Threads	6/12	6/12	6/12	8/16	10/20	TBD
Clock Speeds	3.33/3.60 GHz	3.30/3.90 GHz	3.60/4.00 GHz	3.00/3.50 GHz	3.00 GHz / TBD	TBD
Max Cache	12 MB L3	15 MB L3	15 MB L3	20 MB L3	25 MB L3	TBD
Max PCI-Express Lanes	32 Gen2	40 Gen2	40 Gen3	40 Gen3	TBD	TBD
Chipset Compatibility	X58 Chipset	X79 Chipset	X79 Chipset	X99 Chipset	X99 Chipset	New HEDT Chipset (TBA)
Socket Compatibility	LGA 1366	LGA 2011	LGA 2011	LGA 2011-3	LGA 2011-3	New HEDT Socket (TBA)
Memory Compatibility	DDR3-1066	DDR3-1600	DDR3-1866	DDR4-2133	DDR4-2400	DDR4-2400+
Max TDP	130W	130W	130W	140W	TDP	TBD
Launch	Q1 2010	Q4 2011	Q3 2013	Q3 2014	1H 2016	2017
Launch Price	\$999 US	\$999 US	\$999 US	\$999 US	~\$999 US	TBD

Main features:

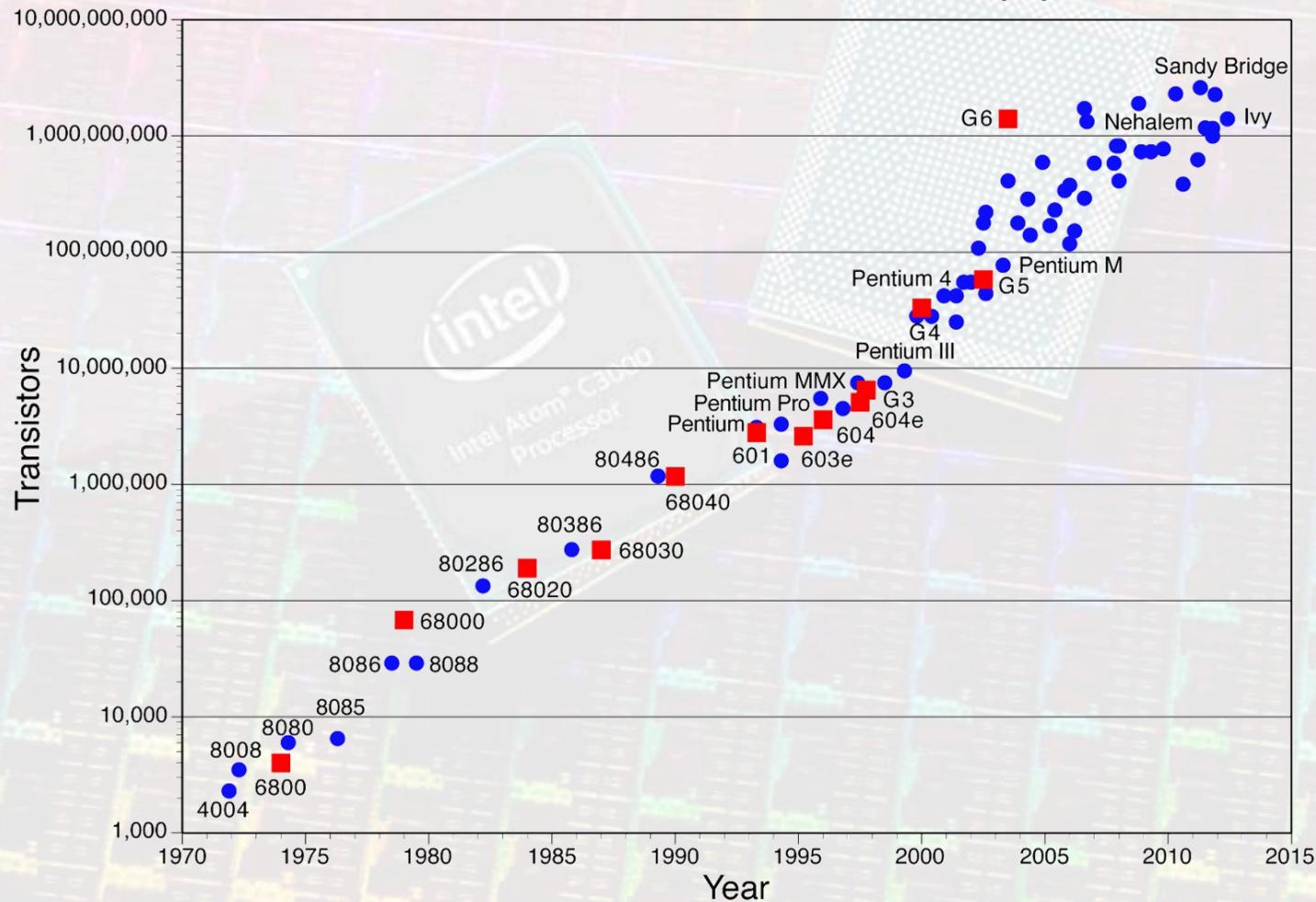
- clock frequency,
- CACHE size, organization
- packaging
- die size,
- number of transistors
- power consumption





A Moore's law for processors

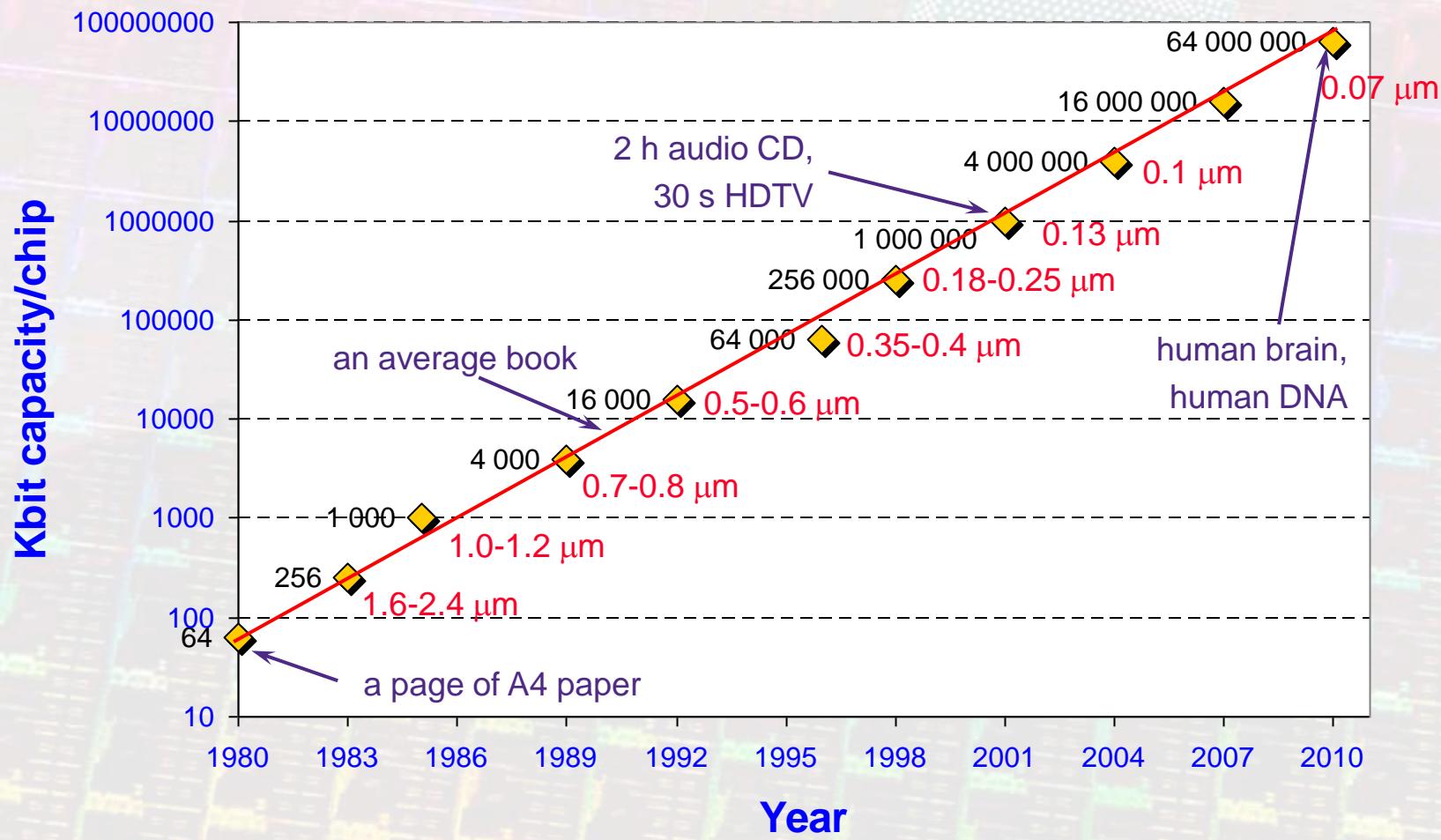
- Number of transistors doubles in almost every year





Development of DRAMs

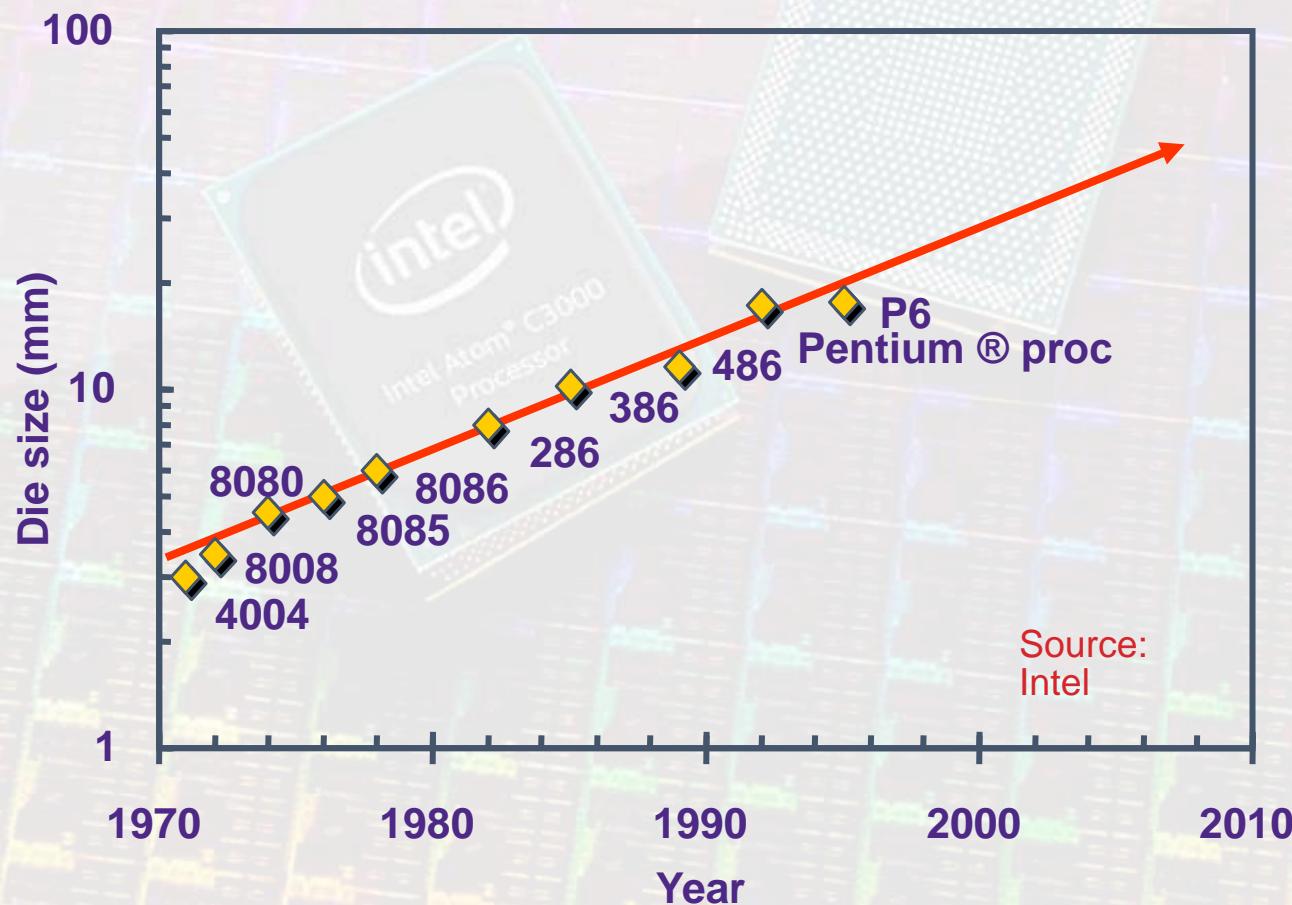
- 4-times growth in every 3 years





Increase of the *die size*

- 2-fold growth in 10 years – 7% annual growth, corresponds to Moore's law

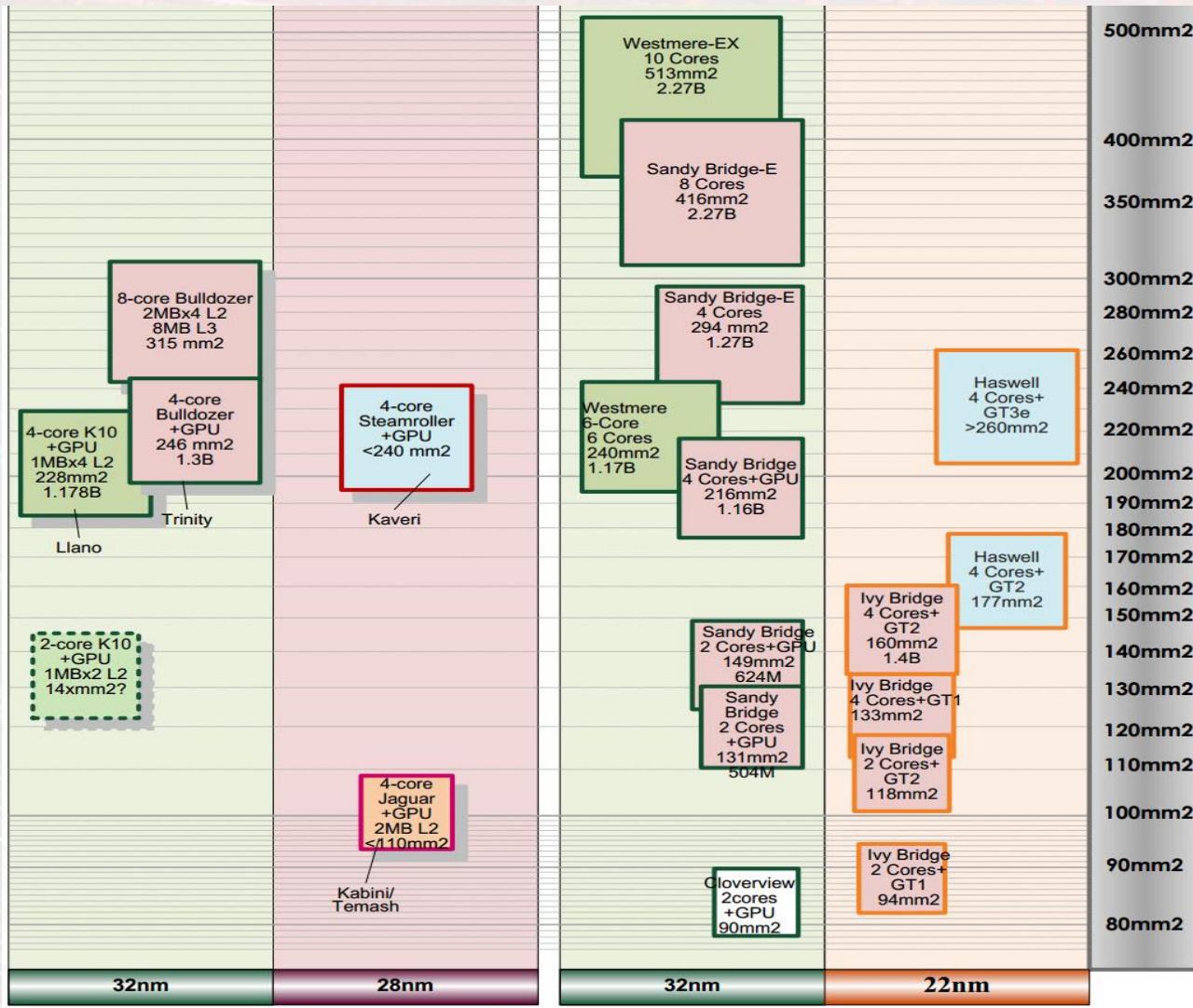


Source:
Intel





Increase of the *die size*

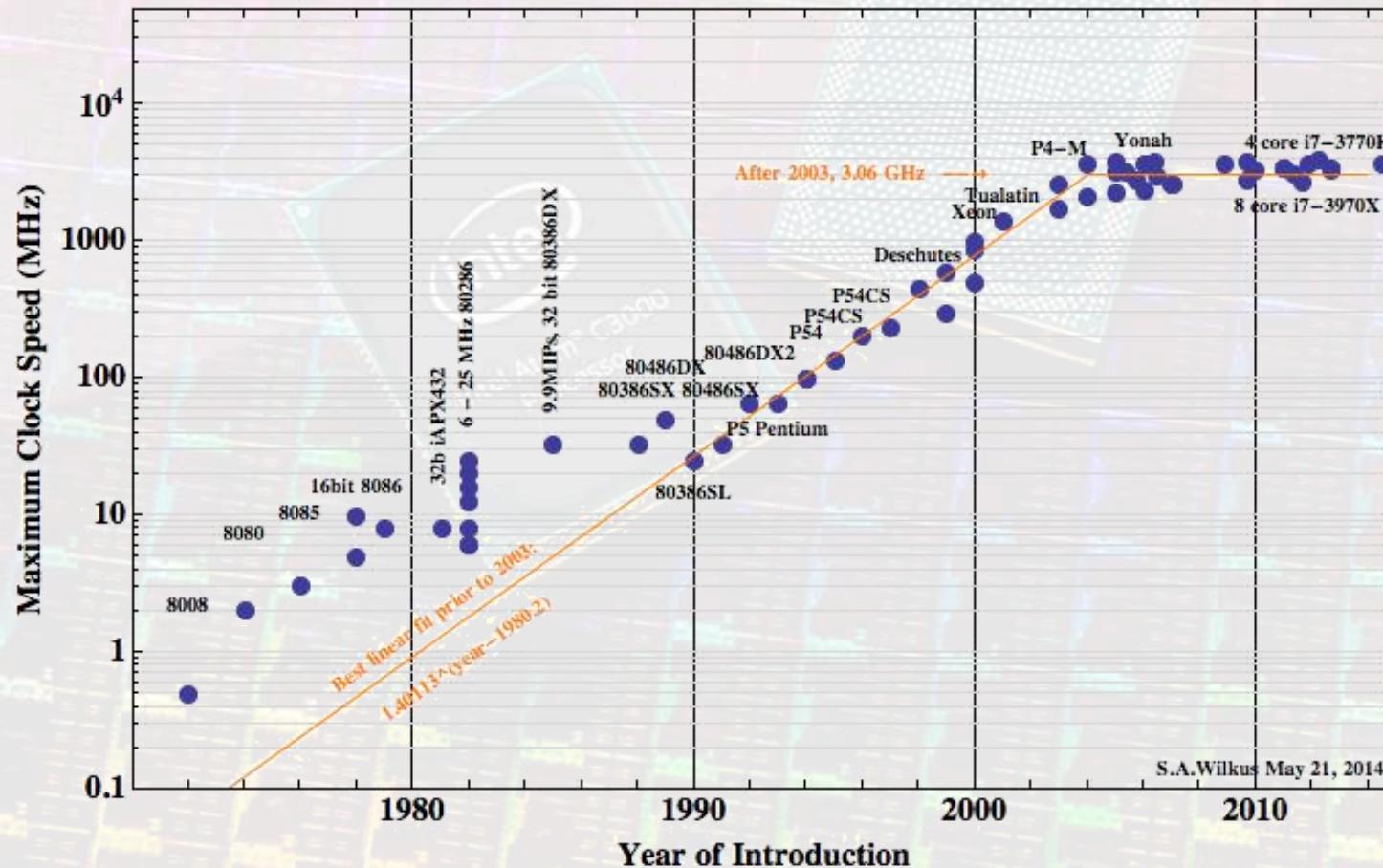




Clock frequency trend

2× every 2 years

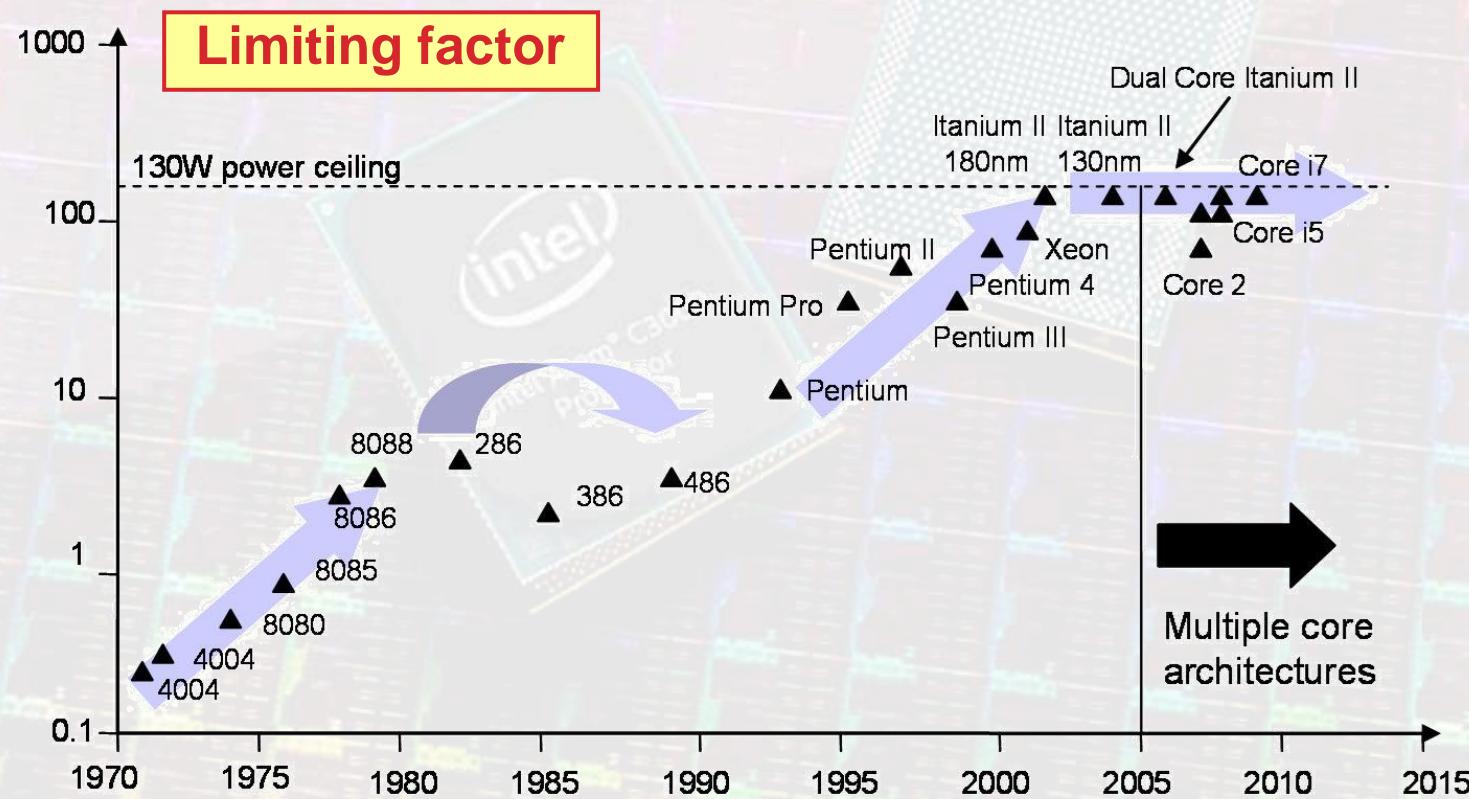
μProcessor Clock Speed Trends





Power consumption trend

- Continuous increase in case of processors



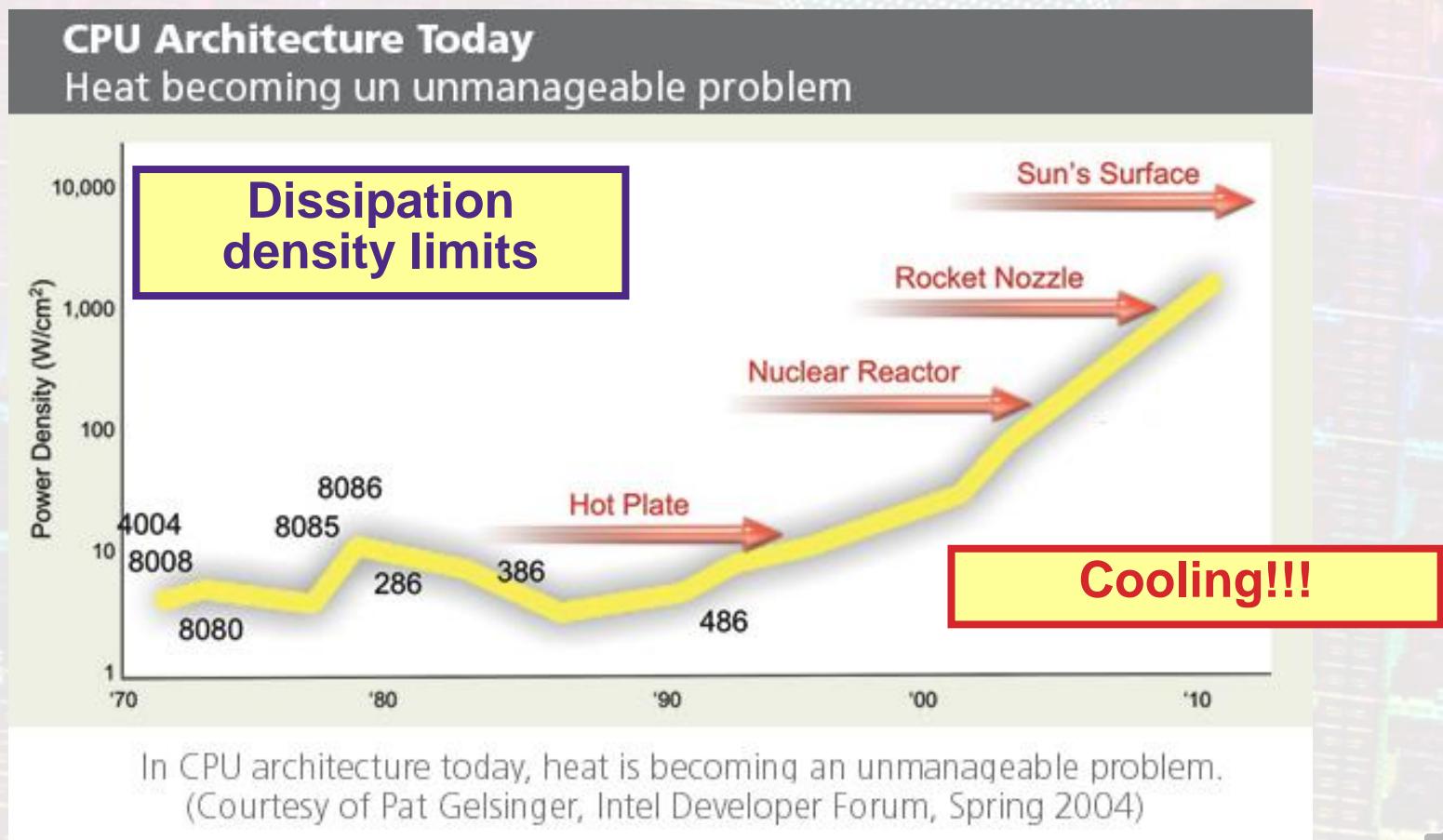
Adapted from ARC 2010 presentation by Dr. Ram Krishnamurthy, Intel Research





Increase in dissipation density

- Power consumption growth faster than the die size





More than Moore integration ITRS

