

File | C:/Users/rasi... Not syncing

netlist 537 2/6

FPGA Design Flow

```

graph LR
    1[1. Specifications] --> 2[2. RTL Coding]
    2 --> 3[3. Standard Cell]
    3 --> 4[4. Pre-Layout Timing Analysis]
    4 --> 5[5. Automatic Placement and Routing]
    5 --> 6[6. Post-Layout Timing Analysis]
    6 --> 7[7. Logic Verification]
    
    2 -- "Pass Simulation?" --> 3
    4 -- "Timing Analysis Pass?" --> 5
    6 -- "Timing Analysis Pass?" --> 7
    
    2 -- "VHDL Coding" --> 2
    2 -- "Simulation" --> 3
    3 -- "Timing Constraints" --> 4
    4 -- "Placement and routing" --> 5
    5 -- "Timing Analysis" --> 6
    6 -- "Verification" --> 7
  
```

- HDL Coding**
 - HDL provide the possibility to implement system with high abstraction levels (Hides complicated implementation details).
 - Designer more concerned about the design functionality than the detailed circuit design.
- Simulation**
 - For verifying the design functionality (Tool: ModelSim - Mentor Graphics).
- Synthesis**
 - Analysing the HDL code and converts it into optimized logic gates (**Netlist**).
 - Synthesis is an important tool to improve designers' productivity.
 - Input: HDL code, the technology library and constraint file.
 - As an output, it will produce the **Netlist** and timing file (*.sdf).
 - Synthesis tools for FPGA are: Quartus II (Altera) and ISE (Xilinx).

Ref: Dr. Mahdi Shabany / Sharif University of technology
 Department of Electron Devices - Ali Kareem Abdulrazzaq
 Microelectronics – Digital Design, Lesson 1 21

Digital System Design - Introduction

FPGA Design Flow

```

graph LR
    1[1. Specifications] --> 2[2. RTL Coding]
    2 --> 3[3. Standard Cell]
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    4 -- "Placement and routing" --> 5
    5 -- "Timing Analysis" --> 6
    6 -- "Verification" --> 7
  
```

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Flag question

What stops the execution of a process?

Select one:

a. The "wait" statement.

b. Either using "wait" statement or no further changes in the values of the sensitivity list.

c. The process is sequentially executed and will not stop executing.

d. No further changes in the values of its sensitivity list.

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ►

Quiz navigation

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Finish attempt ...

8:27 AM

FPGA Design Flow

```

graph LR
    1[1. Specifications] --> 2[2. RTL Coding]
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    2 -- "Simulation" --> 2
    
    2 -- "Pass Simulation?" --> 3
    3 -- "Yes" --> 4
    3 -- "No" --> 2
    
    4 -- "Timing Constraints" --> 4
    4 -- "Synthesis" --> 5
    4 -- "Timing Analysis Pass?" --> 5
    
    5 -- "Placement and routing" --> 5
    5 -- "Timing Analysis" --> 6
    5 -- "Timing Analysis Pass?" --> 6
    
    6 -- "Timing Analysis" --> 6
    6 -- "Verification" --> 7
    6 -- "Timing Analysis Pass?" --> 7
  
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1. HDL Coding

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Microelectronics – Digital Design, Lesson 1 21

Digital System Design - Introduction

FPGA Design Flow

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graph LR
    1[1. Specifications] --> 2[2. RTL Coding]
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    5 -- "Timing Analysis" --> 6
    5 -- "Timing Analysis Pass?" --> 6
    
    6 -- "Timing Analysis" --> 6
    6 -- "Verification" --> 7
    6 -- "Timing Analysis Pass?" --> 7
  
```

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Question 28
Not yet answered
Marked out of 1.00
 Flag question

What does the following VHDL statement mean when it appears alone in a line ($B \leq A$)?

Select one:

a. Not correct VHDL statement

b. The value of A will be assigned to B

c. The value of B should be smaller or equal than A

d. The value of B will be assigned to A

[Clear my choice](#)

[Next page](#)

◀ Midterm retake - calculation, essay

FPGA Design Flow

1. HDL Coding
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 Microelectronics – Digital Design, Lesson 1 21

Digital System Design - Introduction

FPGA Design Flow

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English (en)

Question 27
 Not yet answered
 Marked out of 1.00
[Flag question](#)

What we call the process of automatically converting the RTL code to netlist

Answer: **Synthesis**

Next page

◀ Midterm retake - calculation, essay

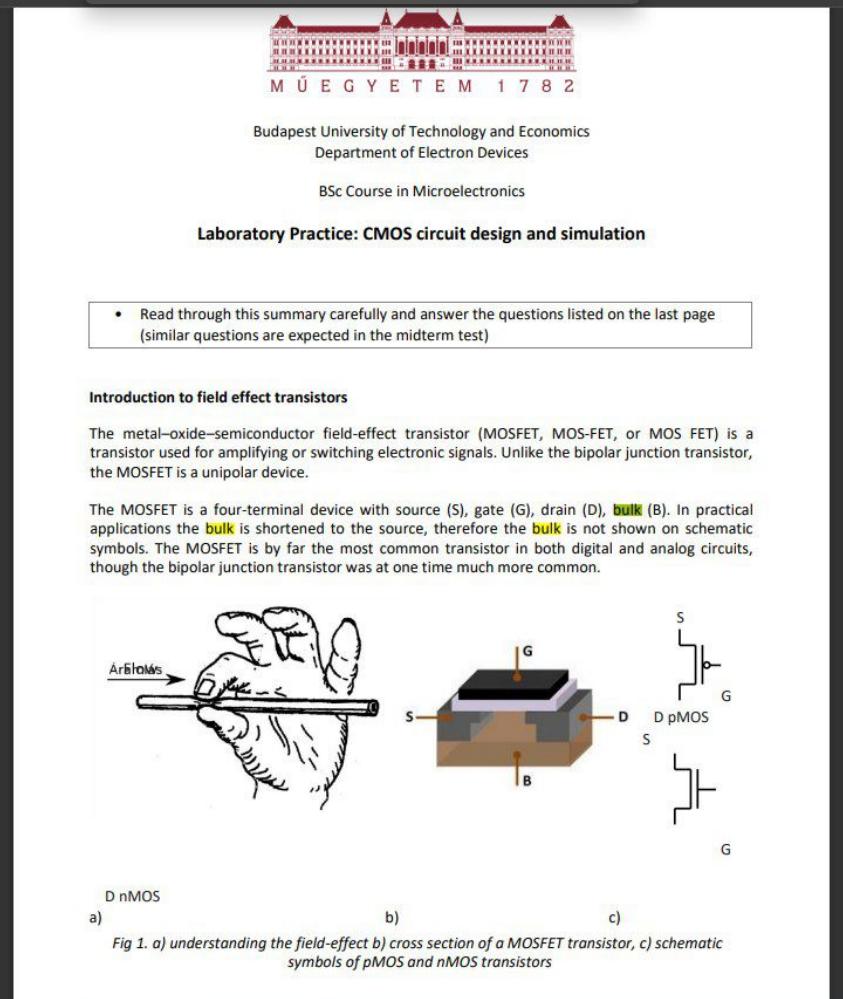
Jump to...

Exam - calculation, essay, VHDL, schematic ▶

Quiz navigation

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8:27 AM



Question 26

Not yet answered

Marked out of 1.00

 Flag question

During the we replace a capacitor with an open circuit and an inductor with a short circuit.

a. AC analysis

b. Noise analysis

c. DC analysis

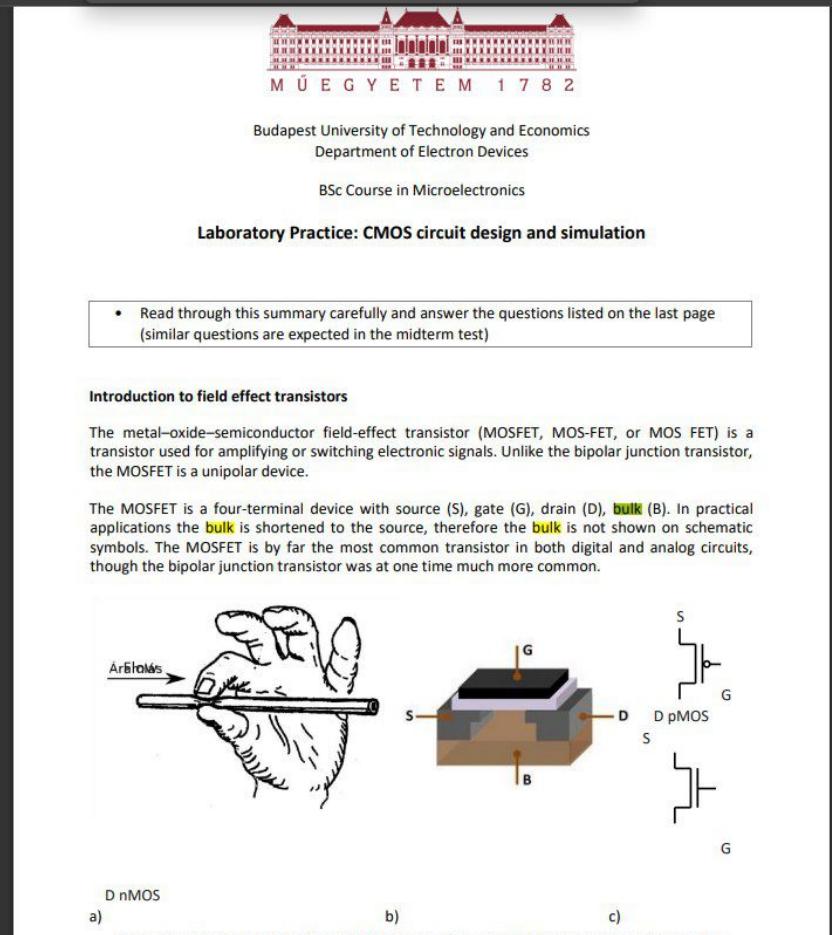
d. DC transfer curve analysis

[Clear my choice](#)

[Next page](#)

 [Midterm retake - calculation, essay](#)

 [Exam - calculation, essay, VHDL, schematic ►](#)



- Read through this summary carefully and answer the questions listed on the last page (similar questions are expected in the midterm test)

Introduction to field effect transistors

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a transistor used for amplifying or switching electronic signals. Unlike the bipolar junction transistor, the MOSFET is a unipolar device.

The MOSFET is a four-terminal device with source (S), gate (G), drain (D), **bulk** (B). In practical applications the **bulk** is shortened to the source, therefore the **bulk** is not shown on schematic symbols. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common.

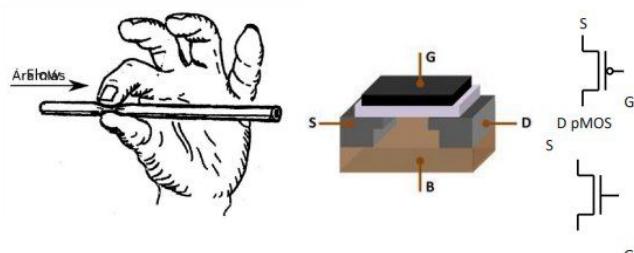


Fig 1. a) understanding the field-effect b) cross section of a MOSFET transistor, c) schematic symbols of pMOS and nMOS transistors

In order to have unique transistors or circuit elements, specified by the manufacturer, we must apply an ... directive with the library path.

a. .INCLUDE
 b. .TTRAN
 c. .MEAS
 d. .MODEL

[Clear my choice](#)

[Next page](#)

[◀ Midterm retake - calculation, essay](#)

[Exam - calculation, essay, VHDL, schematic ▶](#)

bulk 8/12 Not syncing



Budapest University of Technology and Economics
Department of Electron Devices
BSc Course in Microelectronics

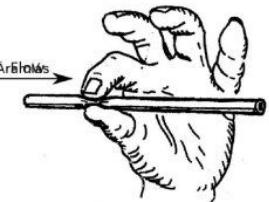
Laboratory Practice: CMOS circuit design and simulation

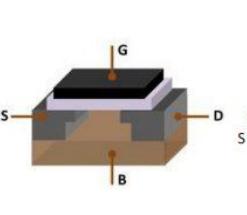
- Read through this summary carefully and answer the questions listed on the last page (similar questions are expected in the midterm test)

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The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a transistor used for amplifying or switching electronic signals. Unlike the bipolar junction transistor, the MOSFET is a unipolar device.

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a) 

b) 

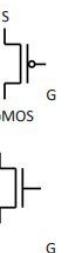
c) 

Fig 1. a) understanding the field-effect b) cross section of a MOSFET transistor, c) schematic symbols of pMOS and nMOS transistors

Not syncing

https://edu.v... English (en)

Question 24
Not yet answered
Marked out of 1.00
Flag question

In statement '.TRAN 1ns 1000NS UIC .OP 40ns' the operating point is calculated at t=...

a. 41 ns.
 b. 40 ns.
 c. 1 ns.
 d. 1000 ns.

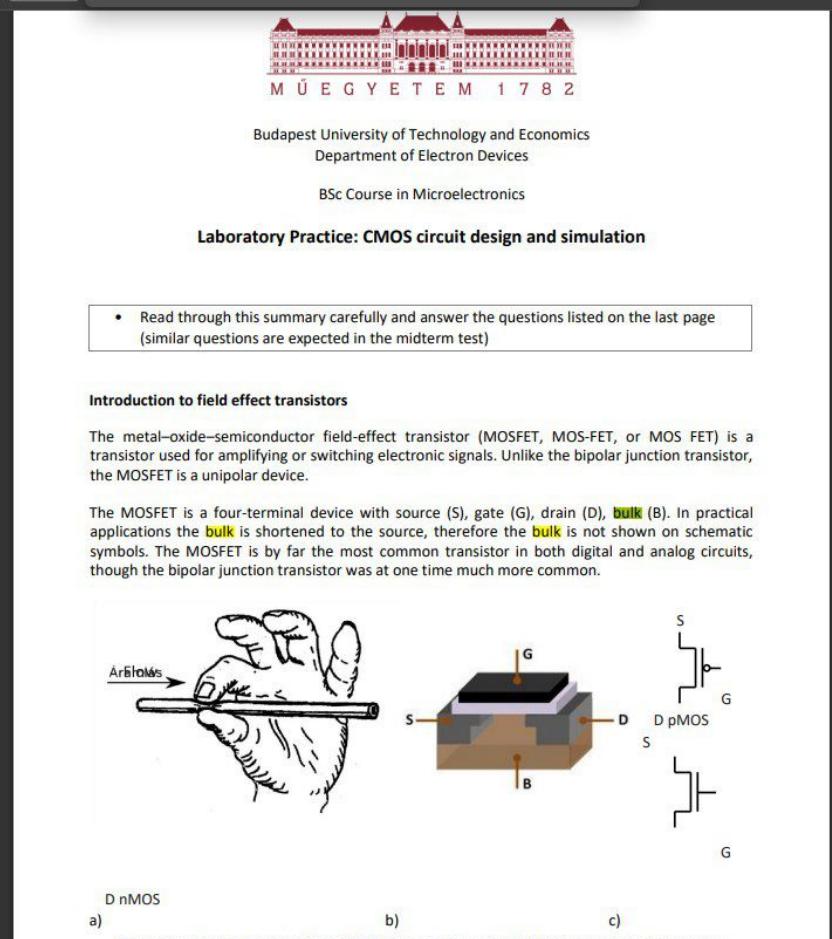
Clear my choice

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶



D nMOS

10

3

Fig 1. a) understanding the field-effect b) cross section of a MOSFET transistor, c) schematic symbols of pMOS and nMOS transistors.

→ ⌂ ⌂ https://edu.v... 🔍 ⭐ ⓘ Not syncing

Flag question

When simulating a CMOS circuitry, it must be ensured that the bulk node of a PMOS is connected to the ...

- a. Drain.
- b. Supply voltage.
- c. GND.
- d. Source.

[Clear my choice](#)

[Next page](#)

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ►

Quiz navigation

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---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----

43



Not syncing

42

Microelectronics 04.02.2019

Introduction

Intel fab sites

Fab name	City	Production start year	Process (Wafer, node)
D1X	Hillsboro, Oregon, United States	2013	300 mm, 14/10/7nm
D1D	Hillsboro, Oregon, USA	2003	300 mm, 14/10/7nm
D1C	Hillsboro, Oregon, USA	2001	300 mm, 22/14/10 nm
Fab 12	Chandler, Arizona, USA	1996	300 mm, 65 nm
Fab 32	Chandler, Arizona, USA	2007	300 mm, 14/10 nm
Fab 42	Chandler, Arizona, USA	2020	300 mm, 10/7 nm
Fab 11	Rio Rancho, New Mexico, USA	1993 (Closed)	200 mm, 45/32 nm
Fab 11X	Rio Rancho, New Mexico, USA	1995 upgrade 2020/2021 with 22/14	300 mm, 45/32 nm
Fab 17	Hudson, Massachusetts, USA	1998 (Closed)	200 mm, 130 nm
Fab 24	Leixlip, Ireland	2006	300 mm, 14 nm
Fab 28	Kiryat Gat, Israel	2008	300 mm, 22/10 nm
Fab 68	Dalian, Liaoning, China	2010	300 mm, 65 nm 3D NAND, 3DXPoint

Microelectronics 04.02.2019

43

Not syncing

Flag question

The dicing saw has an air-bearing design, which is needed because:

- a. the vibration of the environment need to be damped.
- b. the temperature is too high.
- c. otherwise the dust particles may contaminate the equipment.
- d. RPM is too high.
- e. the wafer is positioned using vacuum.

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶

Quiz navigation

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

8:23 AM

392 thca

1/7

Because of the temperature gradient heat current of P develops (remember, how the charge carrier concentration gradient causes electric current!).

$$R_{th} = \frac{\Delta T}{P} = \frac{L}{\lambda A} [K/W] \quad (4)$$

where $L[m]$ is the length and $A[m^2]$ is the cross-sectional surface of the brick.

Obviously the temperature of a body cannot change immediately, because the body itself should be filled of heat. The ability of a body to store heat is the heat capacitance. To rise up the temperature of the body by ΔT , a sum of W energy is requested:

$$C_{th} = \frac{W}{\Delta T} = c_v \cdot A \cdot L \quad (5)$$

where $c_v[W/(m^3 * T)]$ is the volumic heat capacity.

The thermal time constant is analogous the time constant of an R-C circuit as follows:

$$\tau_{th} = R_{th} C_{th} \quad (6)$$

The heat which is generated within the chip structure should be transferred to the ambient otherwise the temperature of the chip rises above the safe operation area. It depends on two factors:

- How the heat can be transferred from the chip (or more precisely, the place where the heat is generated: the p-n junction) to the chip package (or case): R_{thjc} (read: thermal resistance junction to case).
- How the heat can be transferred towards from the case to the ambient (it depends on the size of the heatsink, convective heat transfer etc.): R_{thea} (read: thermal resistance case to ambient)

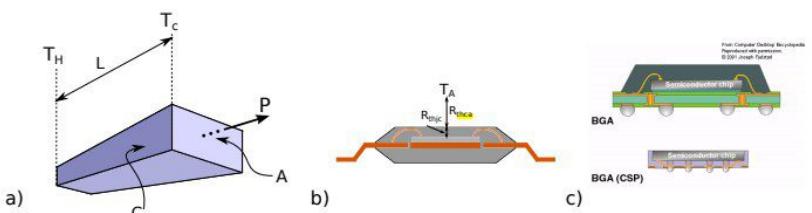


Figure 1: a) Understanding thermal resistance b) DIP package cross section and R_{thjc} , R_{thea} values c) modern BGA and BGA flip chip cross sections

R_{thjc} and R_{thea} are shown on the device's datasheets. Let's consider a device dissipating $100mW$ in DIP package, having $R_{thjc} = 37K/W$ and $R_{thea} = 70K/W$. What will be the junction temperature, if the ambient temperature is $25^\circ C$?

$$T_j = T_{amb} + P(R_{thjc} + R_{thea}) = 25 + 10.7 = 35.7^\circ C \quad (7)$$

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English (en)

Question 20

Not yet answered

Marked out of 1.00

Flag question

What does the value of R_{thca} thermal resistance show?

- a. The thermal resistance between the active (dissipating) zone and the inner edge of the top of the package.
- b. The thermal resistance between the active (dissipating) zone and the ambient.
- c. The thermal resistance between the top of the package and the ambient.
- d. The thermal resistance between the active (dissipating) zone and the PCB board.

[Clear my choice](#)

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[◀ Midterm retake - calculation, essay](#)

[Jump to...](#)

Exam - calculation, essay, VHDL, schematic ▶



lumenous flux si

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Результатов: примерно 1 900 000 (0,53 сек.)

Показаны результаты по запросу **luminous flux si**Искать вместо этого [lumenous flux si](#)[https://en.wikipedia.org › wiki › Перевести эту страницу](https://en.wikipedia.org/wiki/Luminous_flux)

Luminous flux - Wikipedia

The **SI unit of luminous flux** is the lumen (lm). Until 19 May 2019, one lumen was defined as the luminous flux of light produced by a light source that emits one ...

[Units](#) · [Context](#) · [Relationship to...](#)[https://en.wikipedia.org › wiki › Перевести эту страницу](https://en.wikipedia.org/wiki/SI_unit_of_luminous_intensity)

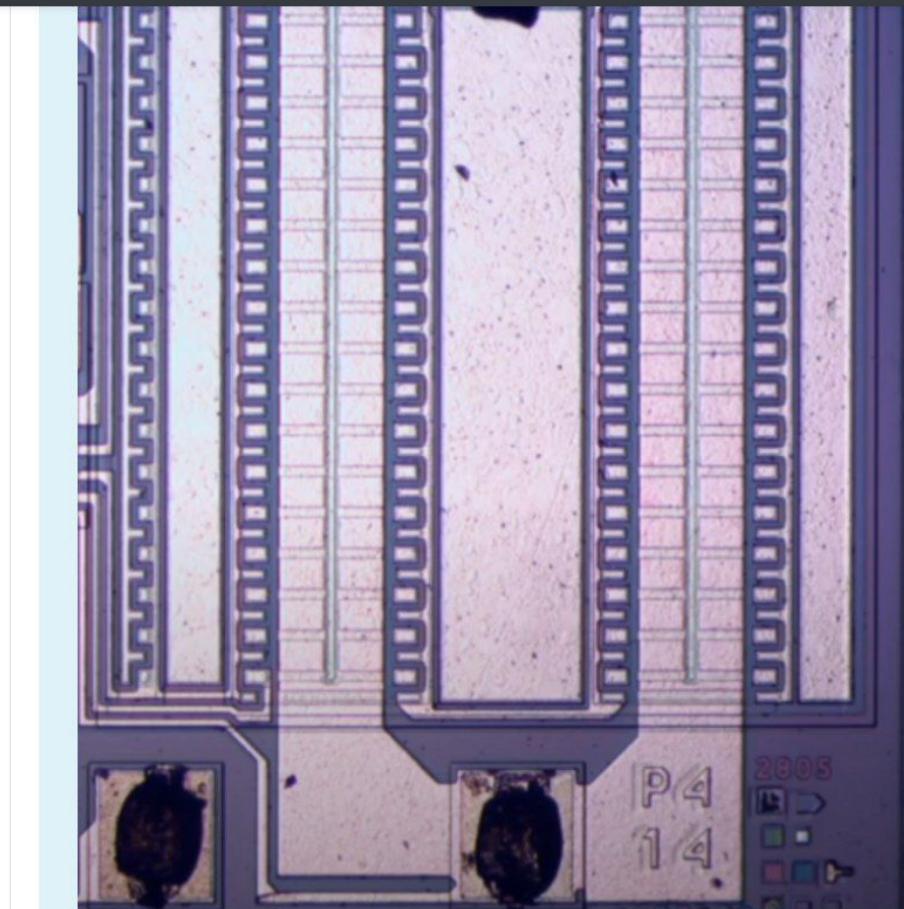
SI unit of luminous intensity - - Wikipedia

In photometry, **luminous intensity** is a measure of the wavelength-weighted power emitted per unit solid angle by a light source in a particular direction per unit solid angle, based on ...

[Relationship to other...](#) · [Units](#) · [Usage](#)[https://www.sciencedirect.com › ... › Перевести эту страницу](https://www.sciencedirect.com/)

Luminous Flux - an overview | ScienceDirect Topics

The **SI unit of luminous flux** is the lumen (lm). One lumen is defined as the luminous flux of light produced by a light source that emits 1 cd of **luminous intensity** over a solid angle of 1 steradian.



Select one or more:

-
- a. diode



lumenous flux si

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Результатов: примерно 1 900 000 (0,53 сек.)

Показаны результаты по запросу **luminous flux si**Искать вместо этого [lumenous flux si](#)[https://en.wikipedia.org › wiki › Перевести эту страницу](https://en.wikipedia.org/wiki/Luminous_flux)

Luminous flux - Wikipedia

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[Units](#) · [Context](#) · [Relationship to...](#)[https://en.wikipedia.org › wiki › Перевести эту страницу](https://en.wikipedia.org/wiki/SI_unit_of_luminous_intensity)

SI unit of luminous intensity - - Wikipedia

In photometry, **luminous intensity** is a measure of the wavelength-weight light source in a particular direction per unit solid angle, based on ...

[Relationship to other...](#) · [Units](#) · [Usage](#)[https://www.sciencedirect.com › ... › Перевести эту страницу](https://www.sciencedirect.com/)

Luminous Flux - an overview | ScienceDirect Topics

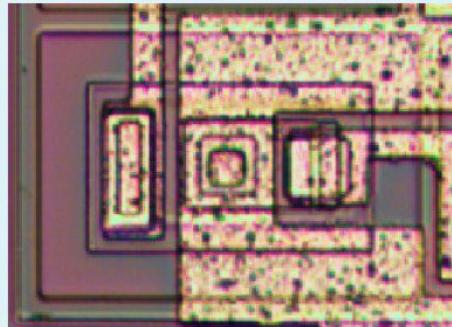
The **SI** unit of **luminous flux** is the lumen (lm). One lumen is defined as the light produced by a light source that emits 1 cd of **luminous intensity** over

Not syncing

English (en)

[Flag question](#)

What type of electronic component can you see on the image?



Select one or more:

- a. resistor
- b. transistor
- c. capacitor
- d. diode

[Next page](#)[◀ Midterm retake - calculation, essay](#)[Jump to](#)

lumenous flux si

[Все](#) [Картинки](#) [Карты](#) [Видео](#) [Новости](#)

Результатов: примерно 1 900 000 (0,53 сек.)

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Luminous flux - Wikipedia

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[Units](#) · [Context](#) · [Relationship to...](#)https://en.wikipedia.org/wiki/SI_unit_of_luminous_intensity

SI unit of luminous intensity - - Wikipedia

In photometry, **luminous intensity** is a measure of the wavelength-weight light source in a particular direction per unit solid angle, based on ...

[Relationship to other...](#) · [Units](#) · [Usage](#)<https://www.sciencedirect.com/science/topics/luminous-flux-an-overview>

Luminous Flux - an overview | ScienceDirect Topics

The **SI** unit of **luminous flux** is the lumen (lm). One lumen is defined as the light produced by a light source that emits 1 cd of **luminous intensity** over

Question 17

Not yet answered

Marked out of 1.00

[Flag question](#)

What is the wavelength of photolithography in the labs of DED?

 a. 465 nm b. 1 μm c. 13.5 nm d. 50 nm e. 0.1 μm[Clear my choice](#)[Next page](#)[◀ Midterm retake - calculation, essay](#)[Jump to...](#)[Exam - calculation, essay, VHDL, schematic ▶](#)

Not syncing

led efficiency and temperature

Все Картинки Новости Видео Покупки Ещё Настройки Инструменты

результатов: примерно 382 000 000 (0,70 сек.)

оказаны результаты по запросу led efficiency and **temperature**
скажи вместо этого led efficiency and temperatre

Light Emitting Diode (**LED**) has the advantages over the traditional lamps in the future. ... When operation **temperature** increases from 327 K to 380 K, the light **efficiency** of LED decreases 20%. The **temperature** rising, the radiation at the potential well decreases, so as to decrease the luminous **efficiency**.

<https://www.researchgate.net> › ... › Materials Science › LED

Effect of temperature and current on LED luminous efficiency

О выделенных описаниях Оставить отзыв

Похожие запросы

What is the effect of temperature on LED output?

How hot is too hot for LED?

In what factors does the efficiency of LED depend?

Not syncing

Flag question

The efficiency of an LED decreases as the temperature of the PN junction decreases.

Next page

◀ Midterm retake - calculation, essay

Jump to... Exam - calculation, essay, VHDL, schematic ▶

Quiz navigation

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
19 20 21 22 23 24 25 26 27 28 29 30

Finish attempt ...

Time left 0:11:31

Not syncing

265 p channel 1/5 ⌂ ⌃ ⌁ ⌂ ...

The MOSFETs

Field effect transistors 3

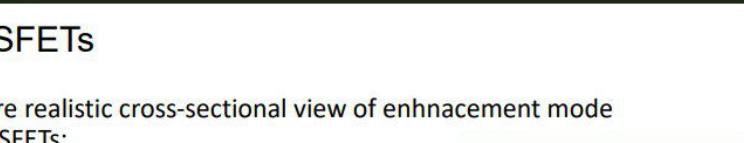
- Symbols:

The diagram illustrates various symbols for MOSFETs and their operating modes:

- JFET:** A symbol showing a single terminal between Gate (G) and Source (S), with Drain (D) at the top.
- MOSFET (n channel):** A symbol showing a single terminal between Gate (G) and Source (S), with Drain (D) at the top. The text "n channel" is written below it.
- MOSFET (p channel enhancement mode):** A symbol showing a single terminal between Gate (G) and Source (S), with Drain (D) at the top. The text "p channel enhancement mode" is highlighted in yellow.
- MOSFET (p channel depletion mode):** A symbol showing a single terminal between Gate (G) and Source (S), with Drain (D) at the top. The text "p channel depletion mode" is highlighted in yellow.
- MOSFET (depletion mode):** A symbol showing two terminals between Gate (G) and Source (S), with Drain (D) at the top. The text "depletion mode" is written below it.
- MOSFET (n channel enhancement mode):** A symbol showing two terminals between Gate (G) and Source (S), with Drain (D) at the top. The text "n channel enhancement mode" is written below it.

a.) b.) c.)

- More realistic cross-sectional view of enhancement mode MOSFETs:



The diagram illustrates a cross-section of an enhancement mode MOSFET. It features a red 'Polysilicon Gate' on top of a yellow 'Gate Oxide'. Below the gate is a green 'N+' 'Source / Drain Regions' layer. The entire structure is embedded in a blue 'P-Type' substrate. On either side of the central channel, there are yellow 'Field Oxide' regions. Labels point to the 'Gate oxide', 'Polysilicon Gate', 'N+ Source / Drain Regions', 'P-Type', and 'Field Oxide'.

- Schematically, when the transistor is opened, it can be substituted by a short. When the transistor is closed, it can be substituted by an open.

Digital circuits are commonly built of using both pMOS and nMOS transistors. This type of digital circuits is called CMOS (means complementary MOS). A CMOS circuitry consists a pMOS circuit block connected to the power supply (V_{dd}) and an nMOS circuit block connected to the ground (V_{ss}). Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

CMOS inverter

The simplest digital circuit is the inverter. An inverter has an input and an output. The output is always the opposite value of the input. The figure above describes the way of operation. When the input is '1' (gate voltages are e.g. 5 V) the pMOS closes and the nMOS opens, therefore the output is shorted to the ground. The output voltage equals to the ground potential, the digital value is '0'. If the input is '0' (gate voltages are 0 V) the pMOS opens and the nMOS closes. The output is shorted to the power supply, therefore the output voltage refers to '1' (e.g. 5 V).

IN	OUT
A	NOT A
1	0
0	1

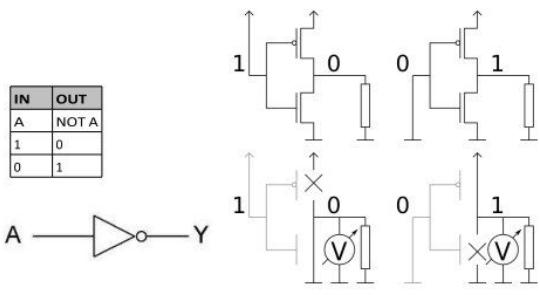


Fig 2. The inverter operation

Questions

1. What MOSFET stands for? What is the difference between nMOS and pMOS? How the terminals are called?

Question 12

Not yet answered

Marked out of 1.00

 Flag question

When both nMOS and pMOS transistors of a CMOS logic gates are ON, the output is:

Select one:

- a. 0 or ground or LOW state.
 - b. 1 or Vdd or HIGH state.
 - c. cannot be identified due to mutual conduction.
 - d. None of the above

[Next page](#)

► Midterm retake - calculation, essay

Jump to

Exam - calculation, essay, VHDL, schematic ►

Quiz navigation

368 consumption 11/17 ⌂ ⌃ ⌁ ⌂ ⌃ ...

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CMOS

Power consumption of CMOS inv.:

- Mutual conduction ("short power"):**
 - During a certain period of the rise of the input signal both transistors are "on" if $V_{Th} < U_{IN} < V_{DD} - V_{Tp}$ this is called mutual conduction

$$I_{MAX} = K(V_{DD}/2 - V_T)^2$$

- charge flowing through: $\Delta Q = b t_{up} I_{MAX}$, where t_{up} is the time while current is flowing, b is a constant depending on the signal shape.
 $b \approx 0.1-0.2$

$$P = f \Delta Q V_{DD} = f V_{DD} b t_{up} K (V_{DD}/2 - V_T)^2$$

$$P \sim f V_{DD}^3$$

Microelectronics 27-04-2020 19

CMOS

Power consumption of CMOS inv.:

- Charge pumping:**
 - At switching the C_L load capacitance is charged to VDD through the p-channel device when the output changes to 1, later, when switching the output to 0, it is discharged towards GND through the n-channel device.

Question 11
Not yet answered
Marked out of 1.00
[Flag question](#)

Regarding the power consumption of CMOS circuitry, it is known that _____.
Select one:

a. the consumption regarding the mutual conduction is proportional to the frequency and the third power of the supply voltage

b. its static consumption is significant

c. the consumption regarding the charge pumping is proportional to the square of the frequency and the supply voltage

d. its dynamic consumption is insignificant

[Clear my choice](#)

[Next page](#)

◀ Midterm retake - calculation, essay

Jump to...

The MOSFETs

Field effect transistors 3

- Symbols:

The diagram illustrates several FET symbols and their operating modes:

- JFET:** Shows two symbols for an n-channel JFET, with the drain (D) at the top and source (S) at the bottom.
- MOSFET:** Shows three symbols for p-channel enhancement mode MOSFETs, with drain (D) at the top. The middle symbol is highlighted with a yellow box.
- MOSFET:** Shows two symbols for p-channel depletion mode MOSFETs, with drain (D) at the top. The middle symbol is highlighted with a yellow box.
- MOSFET:** Shows two symbols for n-channel enhancement mode MOSFETs, with drain (D) at the top. The middle symbol is highlighted with a yellow box.
- a.)** Shows the symbols from the first four rows.
- b.)** Shows the symbols from the second row of each column.
- c.)** Shows the symbols from the third row of each column.

- More realistic cross-sectional view of enhancement mode MOSFETs:

The diagram illustrates a cross-section of an enhancement mode MOSFET. It features a red 'Polysilicon Gate' positioned above a green 'Gate Oxide'. Below the gate, there are two blue 'Source / Drain Regions' situated on a dark blue 'P-Type' substrate. The entire structure is surrounded by a light blue 'Field Oxide'. Labels point to the 'Gate oxide', 'Polysilicon Gate', 'Source / Drain Regions', and 'Field Oxide'.

Question 11

Not yet answered

Marked out of 1.00

 Flag question

Regarding the power consumption of CMOS circuitry, it is known that

Select one:

- a. the consumption regarding the mutual conduction is proportional to the frequency and the third power of the supply voltage
 - b. its static consumption is significant
 - c. the consumption regarding the charge pumping is proportional to the square of the frequency and the supply voltage
 - d. its dynamic consumption is insignificant

► Midterm retake - calculation, essay

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265 p channel 1/5

The MOSFETs

Field effect transistors 3

- Symbols:

The diagram shows several symbols for MOSFETs and JFETs, with labels indicating channel type and mode:

- JFET:** n channel symbol (G, S, D terminals) and p channel symbol (G, S, D terminals).
- MOSFET:** n channel enhancement mode (G, S, D terminals), p channel enhancement mode (G, S, D terminals), n channel depletion mode (G, S, D terminals), and p channel depletion mode (G, S, D terminals).
- Cross-sections:** A vertical cross-section of a MOSFET with labels: Gate Oxide, Polysilicon Gate, Field Oxide, N_D, GATE, N_D, P-Type, Source / Drain Regions, and Field Oxide.

a.) b.) c.)

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Flag question

It is a(n)...

Select one:

- a. n channel JFET
- b. n channel depletion mode MOSFET
- c. p channel JFET
- d. p channel enhancement mode MOSFET

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶

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reverse region 1/3 ...

Operation of PN junctions

Main features

The graph shows Current [mA] on the y-axis (0 to 100) and Voltage [V] on the x-axis (-3 to 1). A curve starts at approximately (-1.5, 0), remains near zero until about -0.7V, then rises sharply to about (0.7, 100). A vertical dashed line marks $V_F \approx 0.7 \text{ V}$.

Reverse region: $I \sim 10^{-12} \text{ A/mm}^2$ (Si, T=300 K)

Forward region: $I \sim \exp(V/V_T)$

Rectifies

The characteristic: $I = f(V)$

Microelectronics 26-02-2018 6

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English (en) ...

Question 7
Not yet answered
Marked out of 1.00
Flag question

Which region/mode does n channel enhancement MOSFET operate if gate-source voltage is 1.2 V, drain-source voltage is 0.9 V, threshold voltage is 0.4 V?

Select one:

a. forward mode
 b. triode region
 c. reverse mode
 d. saturation region

Clear my choice

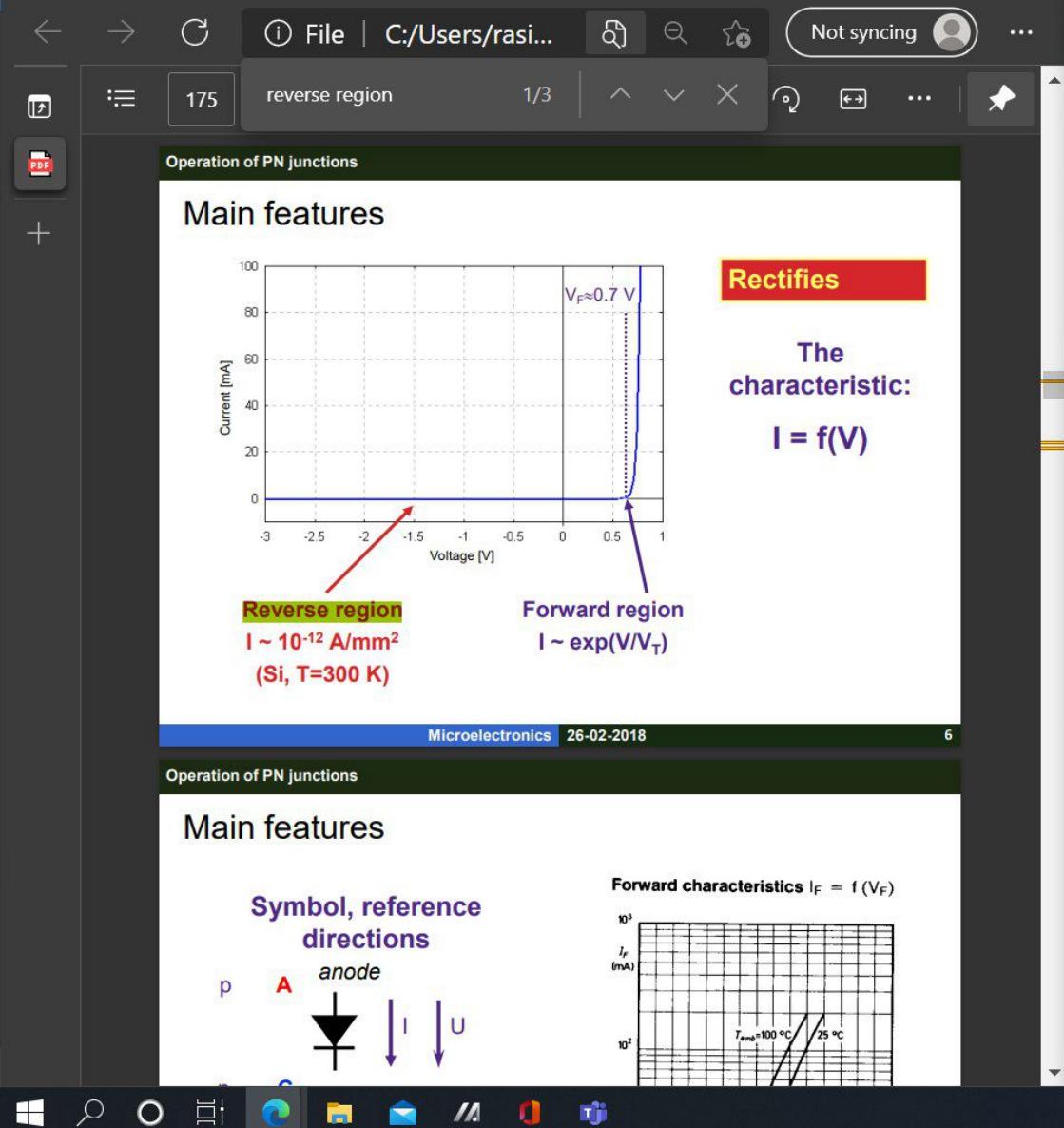
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◀ Midterm retake - calculation, essay

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Exam - calculation, essay, VHDL, schematic ▶

8:08 AM



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Question 7
Not yet answered
Marked out of 1.00
Flag question

Which region/mode does n channel enhancement MOSFET operate if gate-source voltage is 1.2 V, drain-source voltage is 0.9 V, threshold voltage is 0.4 V?

Select one:

- a. forward mode
- b. triode region
- c. reverse mode
- d. saturation region

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◀ Midterm retake - calculation, essay

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Exam - test questions (page 5 of 5) +

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Finish attempt ...

Time left 0:25:31

Question 5
Not yet answered
Marked out of 1.00
[Flag question](#)

The increasing dissipation in a chip gives strong limitations

Select one:

a. memory usage

b. the clock frequency

c. die size

d. number of transistors per chip

[Clear my choice](#)

[Next page](#)

◀ Midterm
retake -

Exam -
calculation

The slide contains two main figures:

Graph of CPU Clock Speeds (MHz) vs. Year:

Year	Clock Speed (MHz)
1971	0.75
1972	1.0
1973	1.75
1974	2.0
1975	2.5
1976	3.0
1977	4.0
1978	5.0
1979	6.0
1980	7.5
1981	8.0
1982	10.0
1983	12.5
1984	15.0
1985	17.5
1986	20.0
1987	22.5
1988	25.0
1989	27.5
1990	30.0
1991	32.5
1992	35.0
1993	37.5
1994	40.0
1995	42.5
1996	45.0
1997	47.5
1998	50.0
1999	52.5
2000	55.0
2001	57.5
2002	60.0
2003	62.5
2004	65.0
2005	67.5
2006	70.0
2007	72.5
2008	75.0
2009	77.5
2010	80.0
2011	82.5
2012	85.0
2013	87.5
2014	90.0
2015	92.5
2016	95.0
2017	97.5
2018	100.0

Heat becoming unmanageable problem:

Dissipation density limits

Power Density (W/cm²)

Hot Plate, Nuclear Reactor, Rocket Nozzle, Sun's Surface

Cooling!!!

Exam - test questions (page 6 of 10) +

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Finish attempt ...

Time left 0:24:56

Question 6

Not yet answered

Marked out of 1.00

Flag question

In case of acceptor doping:

Select one:

- a. specific dopants can be As, P, Sb
- b. electrons become the majority charge carriers
- c. semiconductors become n-type
- d. the Fermi level shifts closer to the valance band

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◀ Midterm

Exam -

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Finish attempt ...
Time left 0:23:31

Question 8
Not yet answered
Marked out of 1.00

With the vapor deposition in semiconductors
Select one:

- a. dopants move in the substrate as a consequence of concentration gradient
- b. metal layer is deposited in the top of mask layer
- c. the substrate surface is bombed with accelerated dopants
- d. a new atomic thin layer is formed on the top of the substrate

Mi Course BMEI autom Advan

vapor deposition 0/0

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Narrow base structure

- The thickness of p region is smaller than the diffusion length → only a part of the e-s recombination
- No difference in the (current) conduction!
- Electric field moves the holes from the contact to the PN junction
 - Small part of the forward voltage is dropped here*

Microelectronics 26-02-2018

Operation of PN junctions

Reverse operation of the diode

- Effect of reverse (negative) U**
 - Potential step increases so as the electric field in the space charge region
 - Current balance disrupted: drift current became dominant, e- drift from the p to the n region
- Drift of the minority carriers on both sides towards the other region!**
- e- concentration decreases in the p region near the junction

Exam - test questions (page 9 of 10) +

← → C 🔍 edu.vik.bme.hu/mod/quiz/attemp... Q ☆ G 📁 🌐 🗑 📰 📈 📜 📧

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Finish attempt ...

Time left 0:22:48

Question 9
Not yet answered
Marked out of 1.00
Flag question

How does the reverse mode operation of the pn junction react to temperature increase?

Select one:

- a. the reverse current decreases by ~7-10%/K
- b. the reverse voltage decreases by ~7-10%/K
- c. the reverse characteristics are temperature independent
- d. the reverse voltage increases by ~2mV/K

Next page

◀ Midterm retake - calculation, essay

Jump to... ▾

Exam - calculation, essay, VHDL, schematic ►

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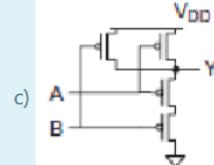
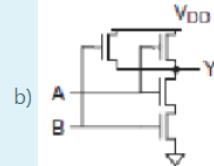
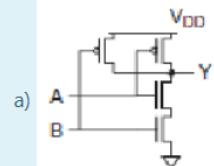
Question 12

Not yet answered

Marked out of 1.00

Flag question

The CMOS logic circuit for NAND gate is:



d) None of the above.

Select one:

a. Two nMOS in series connection and two pMOS in parallel connection

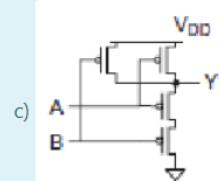
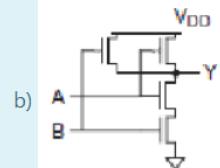


19 20 21 22 23 24

25 26 27 28 29 30

Finish attempt ...

Time left 0:20:29



d) None of the above.

Select one:

- a. Two nMOS in series connection and two pMOS in parallel connection.
- b. Two nMOS in series connection and two other nMOS in parallel connection.
- c. Two pMOS in series connection and two other pMOS in parallel connection.
- d. None of the above.

Exam - test questions (page 13 of 13)

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Finish attempt ...

Time left 0:19:15

Question 13 Not yet answered Marked out of 1.00 Flag question

A ring oscillator contains _____. Select one:

- a. odd number of latches.
- b. even number of latches.
- c. even number of inverters.
- d. odd number of inverters.

Next page

Midterm retake - calculation, essay

Jump to... Exam - calculation, essay, VHDL, schematic

Course BMEV autom Advan

reverse mode operation 1/1

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Operation of PN junctions

Diode characteristics

- Forward and reverse mode operation
- Ideal characteristic
- Secondary effects

Microelectronics 26-02-2018

Operation of PN junctions

Forward operation of the diode

Exam - test questions (page 18 of 20)

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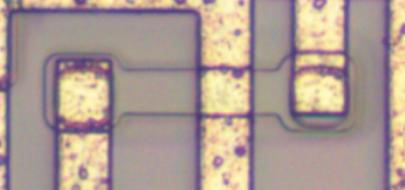
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Finish attempt ...

Question 18 Not yet answered Marked out of 1.00 Flag question

What type of electronic component can you see on the image?



Select one or more:

- a. capacitor
- b. resistor
- c. transistor
- d. diode

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MECART CLEANROOMS

Techniques can be used, according to the quantity and size of particles per cubic meters of air. The primary authority in the US and Canada is the ISO classification system ISO 14644-1.

This ISO standard includes these clean room classes : ISO 1, ISO 2, ISO 3, ISO 4, ISO 5, ISO 6, ISO 7, ISO 8 and ISO 9. ISO 1 is the "cleanest" class and ISO 9 is the "dirtiest" class. Even if it's classified as the "dirtiest" class, the ISO 9 clean room environment is cleaner than a regular room.

The most common ISO clean room classes are ISO 7 and ISO 8. The Federal Standard 209 (FS 209E) equivalent for these ISO classes are Class 10,000 and Class 100 000.

The old Federal Standard 209E (FS 209E) includes these clean room classes : Class 100,000; Class 10,000; Class 1,000; Class 100; Class 10; Class 1. This standard was replaced in 1999 by ISO-14644-1. It was withdrawn in 2001, but it is still widely used.

Clean rooms must also follow industry-specific and regional standards. For

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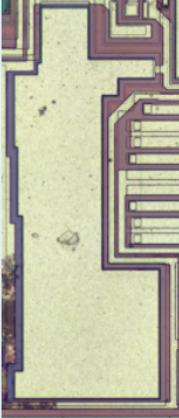
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Finish attempt ... Time left 0:15:21

Question 19 Not yet answered Marked out of 1.00 Flag question

What type of electronic component can you see on the image?



Select one or more:

- a. diode
- b. resistor
- c. transistor
- d. capacitor

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MECART CLEANROOMS

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Finish attempt ...

Time left 0:14:25

Question 20
Not yet answered
Marked out of 1.00
Flag question

What does the value of R_{thjc} thermal resistance show?

- a. The thermal resistance between the active (dissipating) zone and the ambient.
- b. The thermal resistance between the active (dissipating) zone and the inner edge of the top of the package.
- c. The thermal resistance between the active (dissipating) zone and the PCB board.
- d. The thermal resistance between the top and the bottom of the case.

Clear my choice

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Micro Cours BME auto

Файл | C:/Users/Пользователь CMOS inverter 1/13 Список для чтения

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Characteristics of inverters, rudiments

- Noise immunity:
 - Same U_{out} corresponds to a wide U_{in} range
 - There are 3 regions in the characteristic
 - On the L and H sides the characteristic is flat, i.e. any voltage change in the input has negligible effect on the output.

L and H regions

transfer characteristic of an ideal and a realistic inverter

Microelectronics 26-03-2021

MOS inverters

Characteristics of inverters, rudiments

- Signal regeneration
 - depends on the slope of the middle region

Exam - test questions (page 21 of 21)

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Question 21 Not yet answered Marked out of 1.00 Flag question

What is the unit of thermal resistance?

- a. K/W
- b. K-W/s
- c. W·s/K
- d. W/K

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Midterm retake - calculation, essay

Jump to... Exam - calculation, essay, VHDL, schematic

CMOS inverter 1/13 Список для чтения

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Characteristics of inverters, rudiments

- Noise immunity:
 - Same U_{out} corresponds to a wide U_{in} range
 - There are 3 regions in the characteristic
 - On the L and H sides the characteristic is flat, i.e. any voltage change in the input has negligible effect on the output.

U_{out}

"1"

"0"

U_{in}

L and H regions

transfer characteristic of an ideal and a realistic inverter

Microelectronics 26-03-2021 17

MOS inverters

Characteristics of inverters, rudiments

- Signal regeneration
 - depends on the slope of the middle region

U_1 U_2 U_3 U_{out}

10:45 28.05.2021 ENG 2

Exam - test questions (page 23 of 23) +

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Finish attempt ...

Time left 0:12:24

Question 23 Not yet answered Marked out of 1.00

Flag question

A sequence of nonlinear operating points calculated while sweeping the input load(s) or a circuit parameter is called...

a. Noise analysis.

b. DC analysis.

c. DC transfer curve analysis.

d. AC analysis.

Next page

Midterm retake - calculation

Jump to... Exam - calculation, essay, VHDL

Micro Cours BME cutter

google.com/search?q=cutter+pla... 🔍 ⚡ Сервисы Авиабилеты Яндекс Список для чтения

cutter plane dicing

Bce Картинки Видео Покупки Новости Ещё Настройки Инстр...

Результатов: примерно 547 000 (0,59 сек.)

Картинки по запросу cutter plane dicing



Пожаловаться на картинки

Показать все →

https://en.wikipedia.org/wiki/Wafer_dicing Перевести эту страницу

Wafer dicing - Wikipedia

Cross sectional micrograph of cleavage plane after stealth dicing a Si wafer of 150 µm thickness, compare Ref. Dicing of silicon wafers may also be performed by a ...

Похожие запросы

Exam - test questions (page 24 of 24) + Microe Course BMEV A seq Q1 X

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Finish attempt ...

Time left 0:11:26

Question 24 Not yet answered Marked out of 1.00

Flag question

The statement used to store an estimate of DC operating point during transient analysis is the...

a. .TTRAN
b. .OP
c. .TRAN
d. .OPT

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◀ Midterm retake - calculation

Jump to... ↴

Exam - calculation, essay, VHDL

brainly.in/question/8861091 🔍 ⭐ 📁 🗑 🗑 🗑 🗑

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BRAINLY Search...

Answer

anushakul Helping Hand • 1 answer

noise analysis

applied ac bias

the gate output is connected either power or ground

vdd+2vtn

reduced by eight

douwdek0 and 3 more users found this answer helpful

THANKS 2 ★★★★★ 1.0 (1 vote)

are u sure about these answers

10:48 ENG 28.05.2021 2

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Question 25 Not yet answered Marked out of 1.00 Flag question

The statement which bypass initial DC operating point analysis is the...

a. .TRAN
 b. .OP
 c. .TTRAN
 d. .OPT

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Midterm retake - calculation, essay

Jump to... Exam - calculation, essay, VHDL, schematic

CMOS inverter 1/13 Microelect... 341 / 584 56% 10:49 28.05.2021

Characteristics of inverters, rudiments

- Noise immunity:
 - Same U_{out} corresponds to a wide U_{in} range
 - There are 3 regions in the characteristic
 - On the L and H sides the characteristic is flat, i.e. any voltage change in the input has negligible effect on the output.

U_{out}

"1" "0"

U_{in}

L and H regions

transfer characteristic of an ideal and a realistic inverter

Microelectronics 26-03-2021 17

MOS inverters

Characteristics of inverters, rudiments

- Signal regeneration
 - depends on the slope of the middle region

U_1 U_2 U_3

10:49 28.05.2021 2

Exam - test questions (page 26) + ▾

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Finish attempt ...

Time left **0:10:57**

Question 26
Not yet answered
Marked out of 1.00
[Flag question](#)

In order to have unique transistors or circuit elements, specified by the manufacturer, we must apply an ... directive with the library path.

a. .MODEL
 b. .MEAS
 c. .TTRAN
 d. .INCLUDE

Next page

[◀ Midterm retake - calculation](#) [Jump to...](#) [▶ Exam - calculation, essay VHDL](#)

Characteristics of inverters, rudiments

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MOS inverters

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Finish attempt ...

Time left 0:10:48

Question 26

Not yet answered

Marked out of 1.00

Flag question

In order to have unique transistors or circuit elements, specified by the manufacturer, we must apply an ... directive with the library path.

a. .MODEL

b. .MEAS

c. .TTRAN

d. .INCLUDE

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Midterm retake - calculation

Jump to...

Exam - calculation, essay, VHDL

Mi Course BMEV A seq Q1. In

CMOS inverter 1/13

Microelect... 341 / 584 56%

Characteristics of inverters, rudiments

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U_{out}

"1"

"0"

U_{in}

L and H regions

transfer characteristic of an ideal and a realistic inverter

Microelectronics 26-03-2021

17

MOS inverters

Characteristics of inverters, rudiments

- Signal regeneration
 - depends on the slope of the middle region

U_{out}

1 2 1 3 ...

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Finish attempt ...

Time left 0:10:09

Question 27

Not yet answered

Marked out of 1.00

Flag question

What is the scope of a variable (VHDL'87)?

Select one:

- a. Process.
- b. Variables are not allowed in VHDL'87.
- c. Different architectures which are connected to the same entity.
- d. Architecture.

Next page

Midterm retake - calculation, essay, VHDL, schematic

Jump to...

Exam - calculation, essay, VHDL, schematic

Mi Course BMEVI A seq In order

CMOS inverter

Microelect... 341 / 584

Characteristics of inverters, rudiments

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MOS inverters

Characteristics of inverters, rudiments

Signal regeneration

- depends on the slope of the middle region

U₁ U₂ U₃ ...

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Finish attempt ...
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Question 28
Not yet answered
Marked out of 1.00
Flag question

Which VHDL unit contains sequential statements?
Answer:

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Midterm retake - calculation, essay

Exam - calculation, essay, VHDL, schematic ▶

Mi Course BMEV A seq In order

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Список для чтения

Architecture 2/33

Microelect... 547 / 584

library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

library work;
use work.DataTypes_pkg.all;

Department of Electron Devices - Ali Kareem Abdulrazzaq

Digital System Design - Introduction

VHDL Structural Elements

A VHDL design consist of three fundamental design units:

2. Entity Declaration

- port name: used to identify pin(s) and providing the ability to connect it to the design unit or other designs units.
- mode: give the direction of the port. It can be in, out, or inout, as will be discussed later
- data type: define the data type of the port which can be bit, integer, std_logic, and many other types.

entity entity_name is
port (

10:50
ENG
28.05.2021
2

Started on Friday, 28 May 2021, 10:53 AM**State** Finished**Completed on** Friday, 28 May 2021, 11:49 AM**Time taken** 56 mins 49 secs**Grade** Not yet graded**Question 1**

Complete

Mark 2.00 out of 2.00

If the doping levels of an abrupt Si diode are

$$N_d = 10^{19}/\text{cm}^3$$

$$N_a = 10^{15}/\text{cm}^3$$

Calculate the diffusion potential at room temperature!

Answer: 0.838

Question 2

Complete

Mark 4.00 out of 4.00

If the doping levels of an abrupt Si diode are

$$N_d = 10^{17}/\text{cm}^3$$

$$N_a = 10^{15}/\text{cm}^3$$

and

$$\epsilon_r = 11.8$$

$$\epsilon_0 = 8.85419e-12 \text{ F/m}$$

$$U = 0$$

Calculate the width of the depletion layers on the less doped side (**um**)!

Answer: 0.969

Question 3

Complete

Mark 4.00 out of 4.00

Calculate the saturation current (**mA**) of a p channel enhancement MOSFET if

- gate-source voltage is -1.2 V
- threshold voltage is -0.3 V
- channel width 0.5 μm
- channel length 0.35 μm
- electron mobility 500 $\text{cm}^2/(\text{V}\cdot\text{s})$
- oxide relative permittivity 3.84
- vacuum permittivity 8.85419E-12 F/m
- oxide thickness 15 nm

Assume that the MOSFET is in saturation!

Answer: 0.065

Question **4**

Complete

Marked out of 10.00

Describe the steps of photolithography. Explain a number of modern photolithography methods!

Steps:

1. Cleaning. The wafers are cleaned from contaminations on the surface.
2. Thermal annealing. The wafer is heated to evaporate humidity from the surface.
3. Adhesion enhancement. By applying chemicals to enhance the adhesion of the photoresist to the wafer.
4. Photoresist coating. The wafer is covered with photoresist by spin coating. There are 2 types: positive and negative photoresists.
5. Soft bake. For evaporating of the excess solvents from the photoresist.
6. Mask alignment and exposure. The mask is aligned properly to the substrate. The photoresist is exposed to UV light that causes a chemical change in it.
7. Development. Portions of the photoresist are dissolved by a chemical developer. If it is a positive resist then the exposed resist is dissolved and the unexposed area remains on the wafer. For the negative resist, it is another way around.
8. Hard bake. The developed photoresist is hardened and stabilized.

Modern photolithography methods:

1. Immersion lithography: the air gap between the final lens and the wafer surface with a liquid medium. It requires multiple patterning due to the resolution limit.
2. Electron-Beam Direct-Write Lithography: the focused beam of electrons draw shapes on a surface covered with electron-sensitive film.
3. Extreme Ultraviolet (EUV) lithography: uses a range of extreme ultraviolet wavelengths.

Question 5

Complete

Marked out of 10.00

Draw the state diagram of a VHDL design that takes d as a serial bit stream input and outputs a logic '1' whenever the sequence "010" occurs.

 [exam.jpg](#)[◀ Exam - test questions](#)

Jump to...

Basic semiconductor physics ►