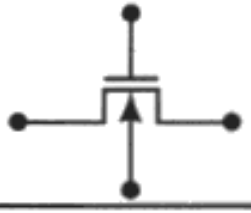
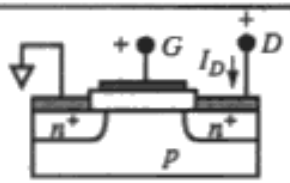
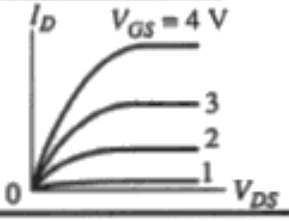
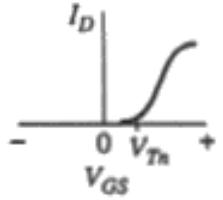
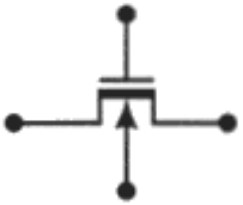
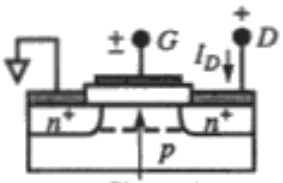
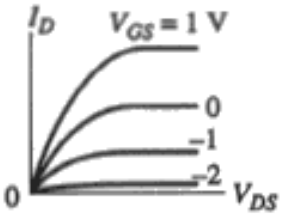
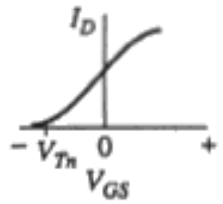
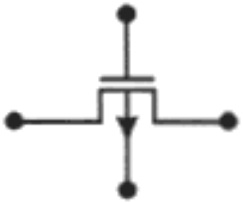
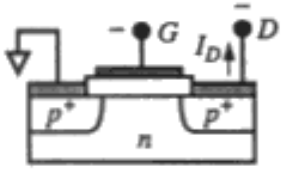
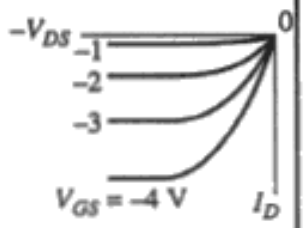
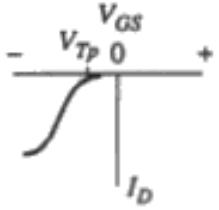
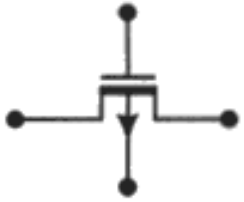
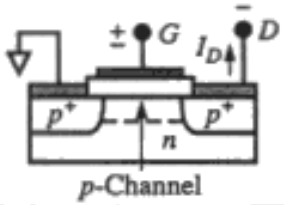
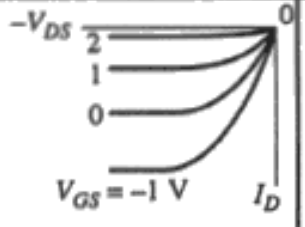
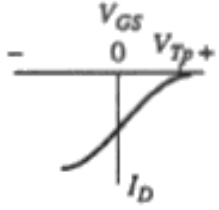
Budapest University of Technology and Economics
Department of Electron Devices

Microelectronics, BSc course

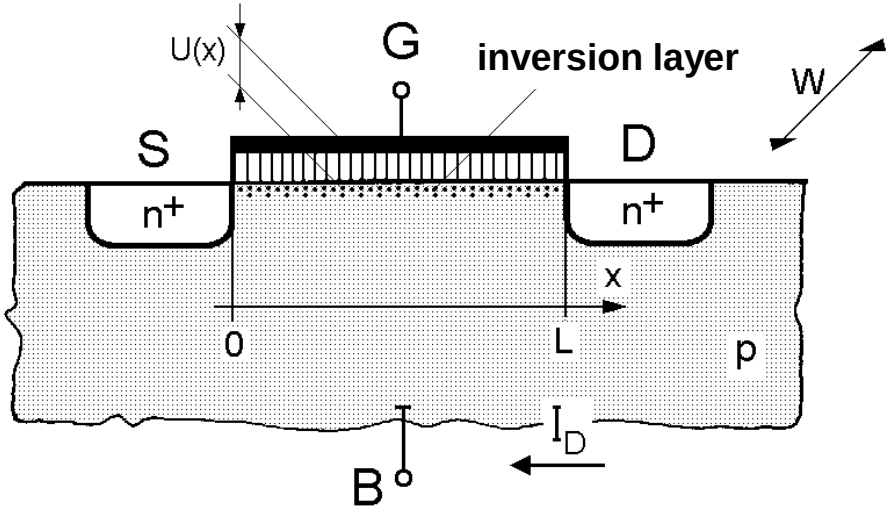
nMOS/CMOS Logic Gates

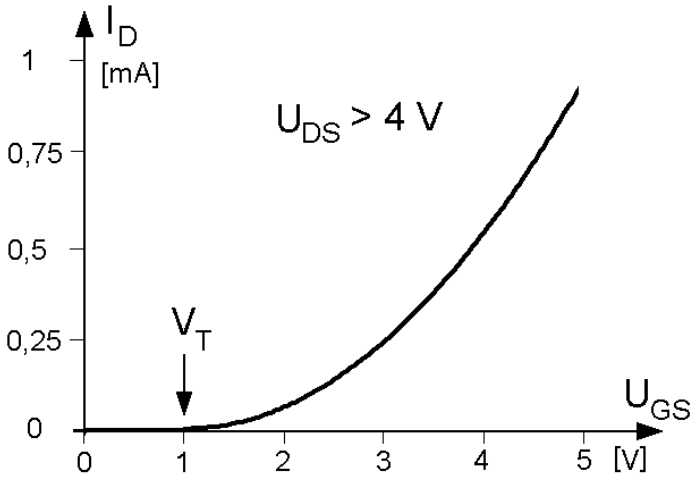
Overview of MOSFET types

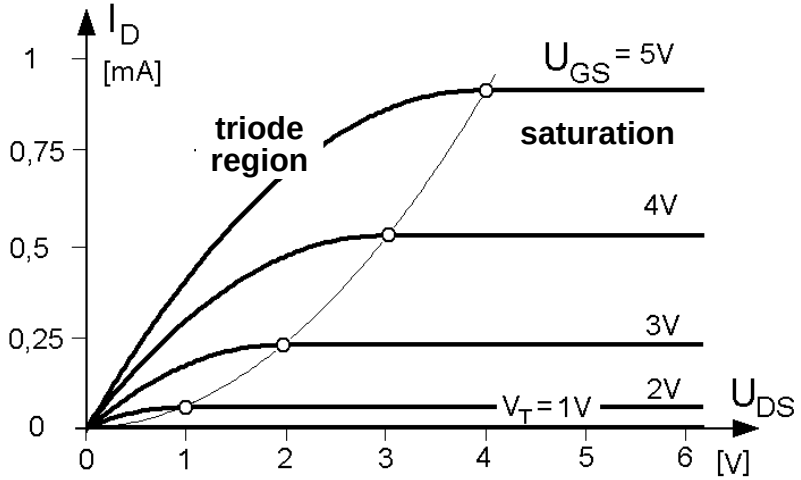
Type	Circuit Symbol	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)				
n-Channel Depletion (Normally On)				
p-Channel Enhancement (Normally Off)				
p-Channel Depletion (Normally On)				

Char. of enhancement mode n type MOSFETs

Now we calculate with this!

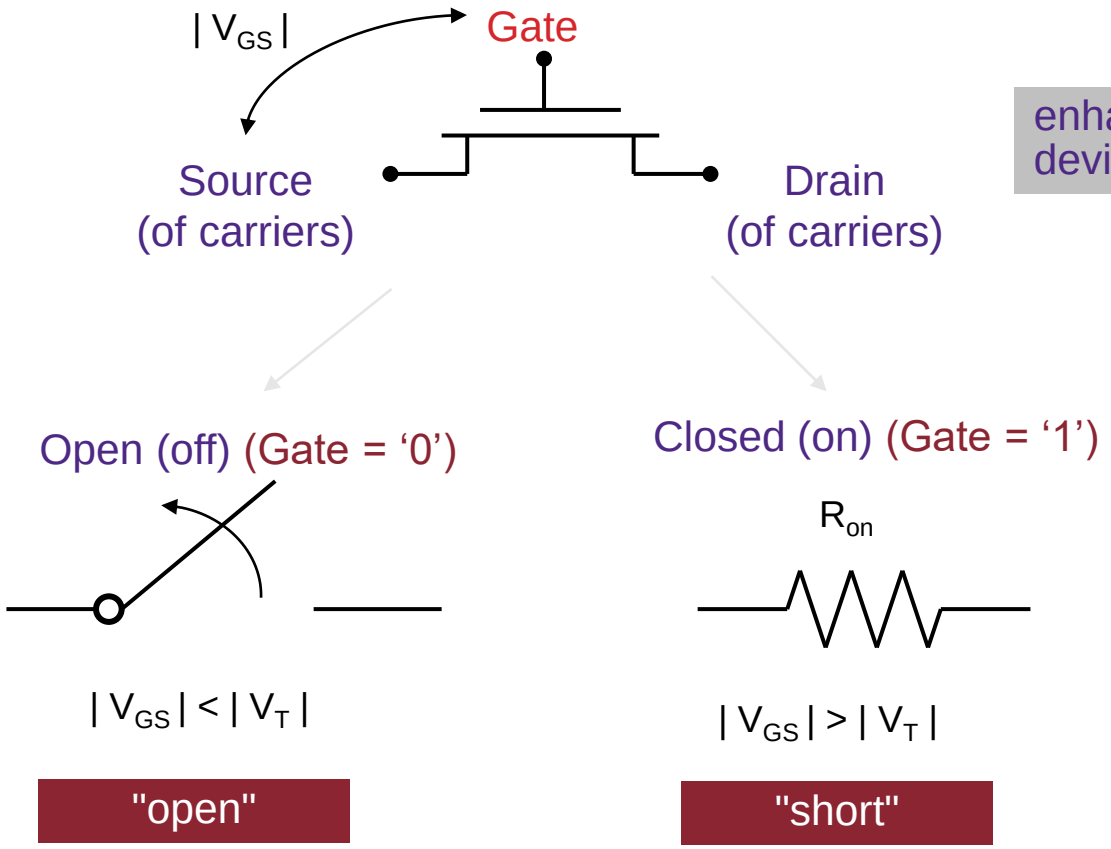






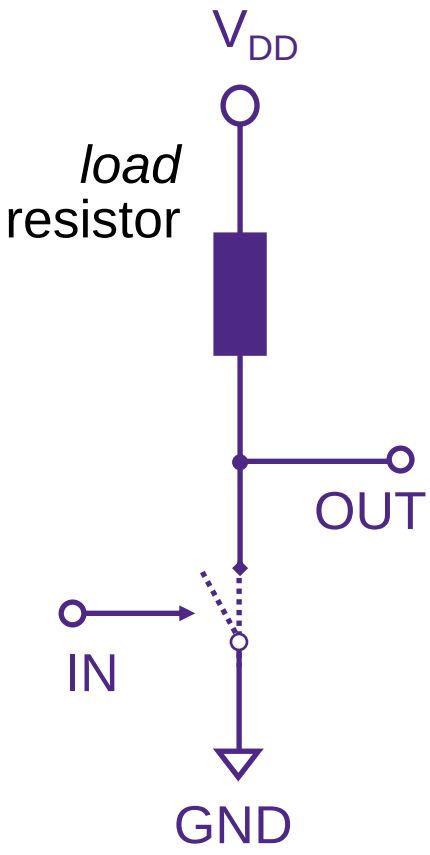
Simple model of MSOFETs

- The simplest (logic) model:
  - no conduction (off) / conduction (on)



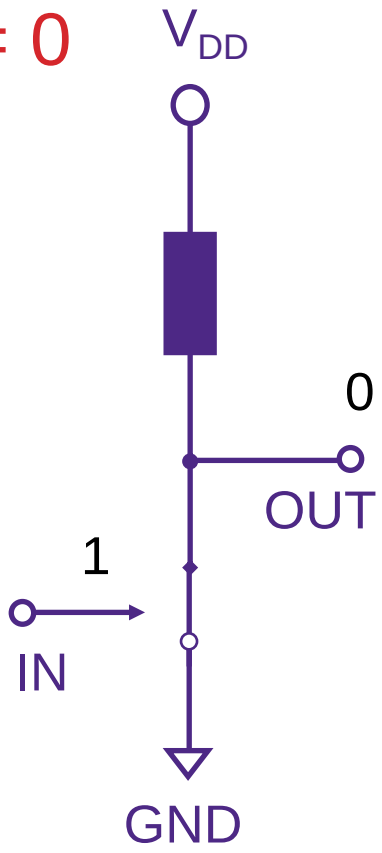
Let's construct an inverter!

- Resistor at supply voltage (V_{DD})
- Other end connected to ground (GND) through a switch
- Switch controlled by a logic signal:
  - 1 (V_{DD} level) – "short"
  - 0 (GND level) – "open"
- The output is the common node of the switch and the resistor

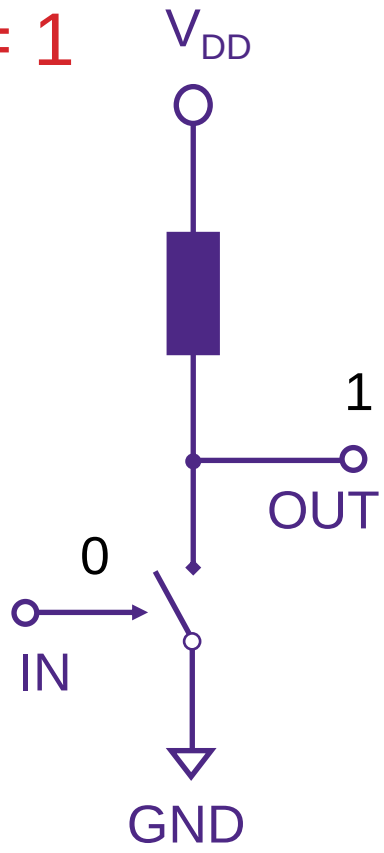


Let's construct an inverter!

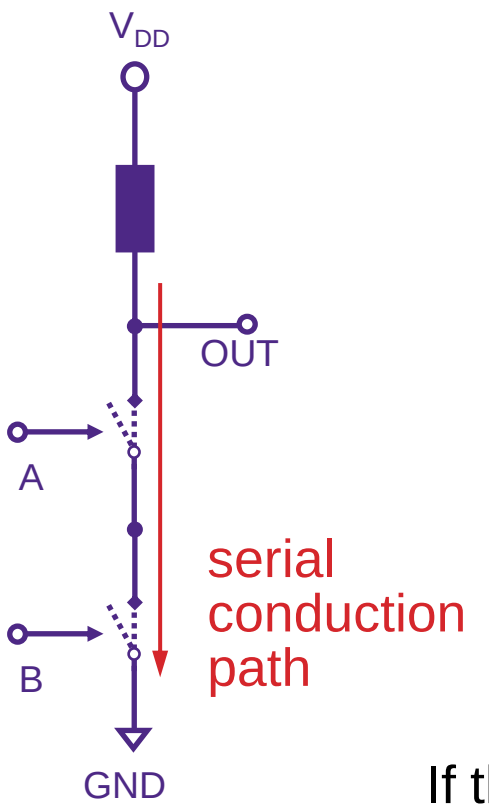
- IN = 1
  - switch "on"
  - output connected to GND
  - OUT = 0



- IN = 0
  - switch "off"
  - output floating at V_{DD}
  - OUT = 1



Two switches in series: NAND gate

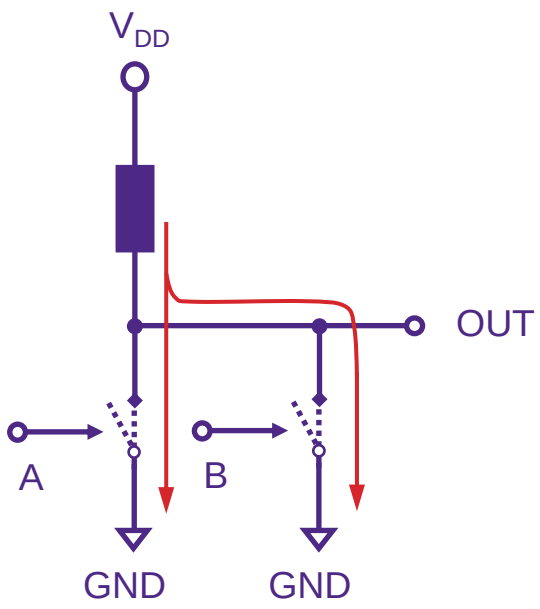


- If A and B equal to 1, then OUT=0
- This is the
  NOT (A AND B) function,
  i.e. NAND

In practice with max. 3..4 inputs.

If there are *parallel* conductions paths then we get the *NOR function*

The scheme of the NOR gate:



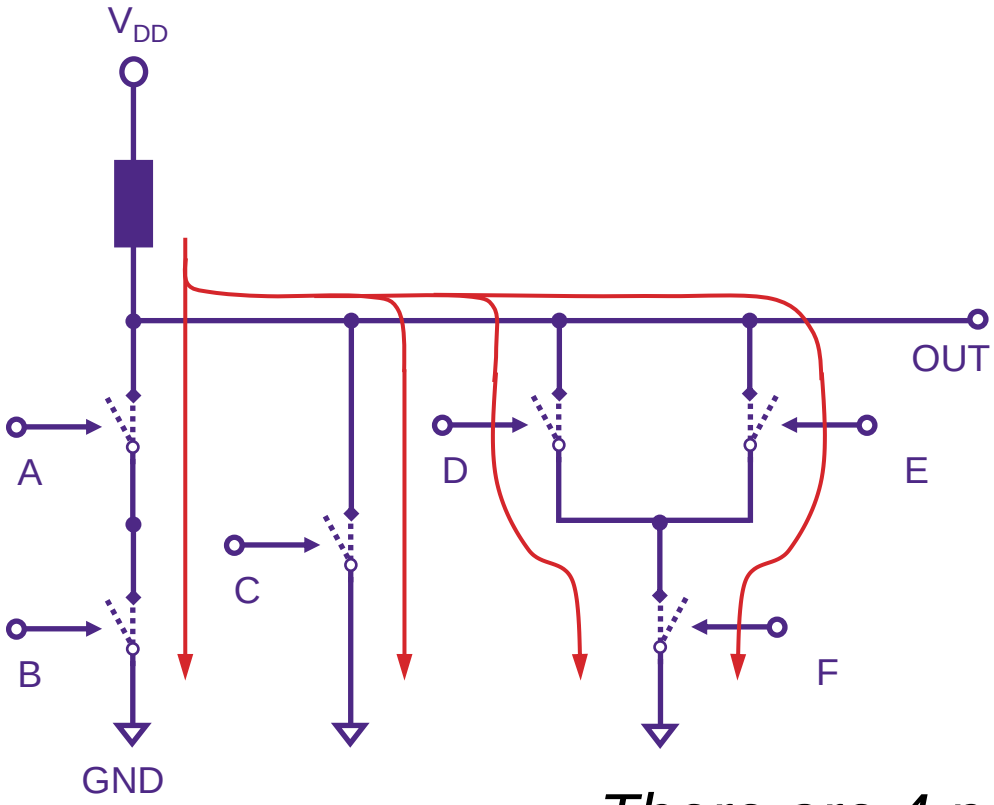
PARALLEL
conduction path

- If A or B equals to 1, then OUT=0
- This is the
  NOT (A OR B) function,
  i.e. NOR

Complex conduction paths == option for complex logic gates

Complex logic gates

- Serial paths connected in parallel

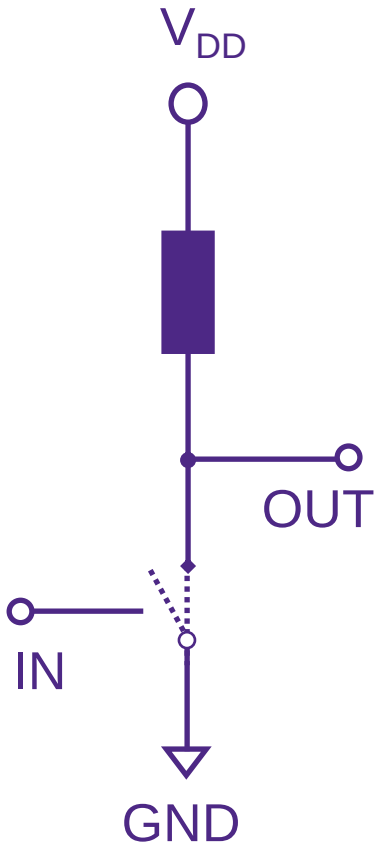


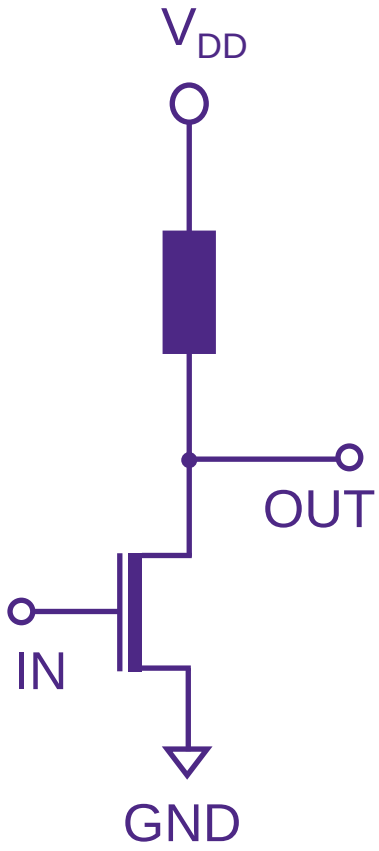
$$Out = \overline{AB + C + (D + E)F}$$

There are 4 paths

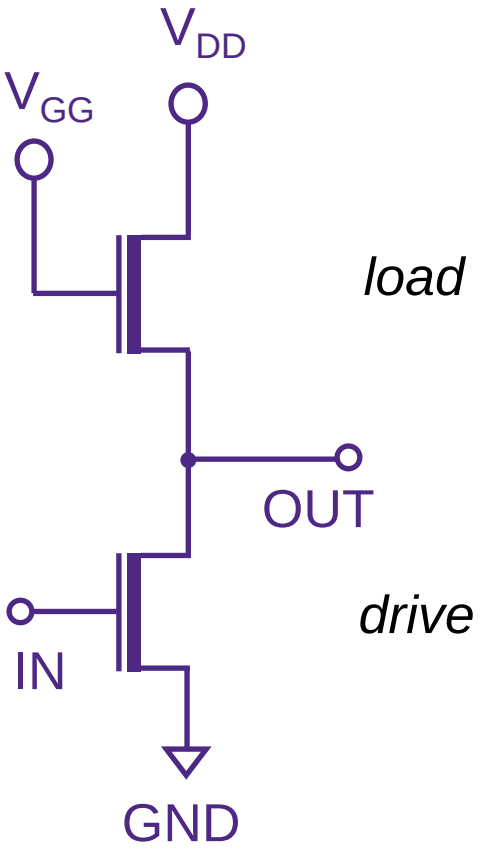
Inverter realizations

Switch = n channel MOSFET: *normally OFF device*



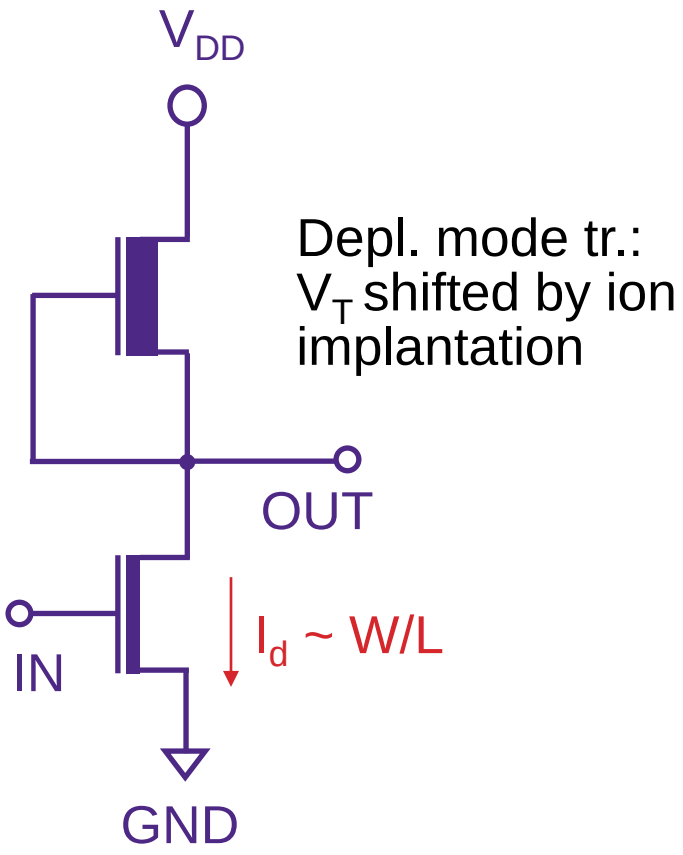


Load resistor: another transistor, e.g. in triode region



Needs another supply – **not OK**

nMOS technique – very simple

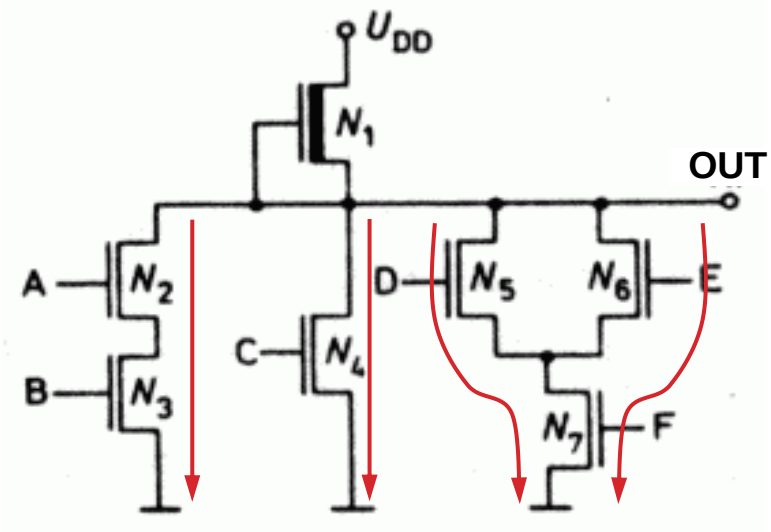


- Simple process, outdated, many disadvantages
  - static consumption if OUT=0
  - if OUT = 0, it will not be a pure GND level
  - asymmetrical transfer characteristic (see later)

- In both cases the *load* resistor is replaced by a MOSFET but this transistor was not provided with an active control
  - *This is the passive load inverter*

Complex gates (in nMOS)

- Serial conduction paths in parallel, e.g.:



There are 4 paths

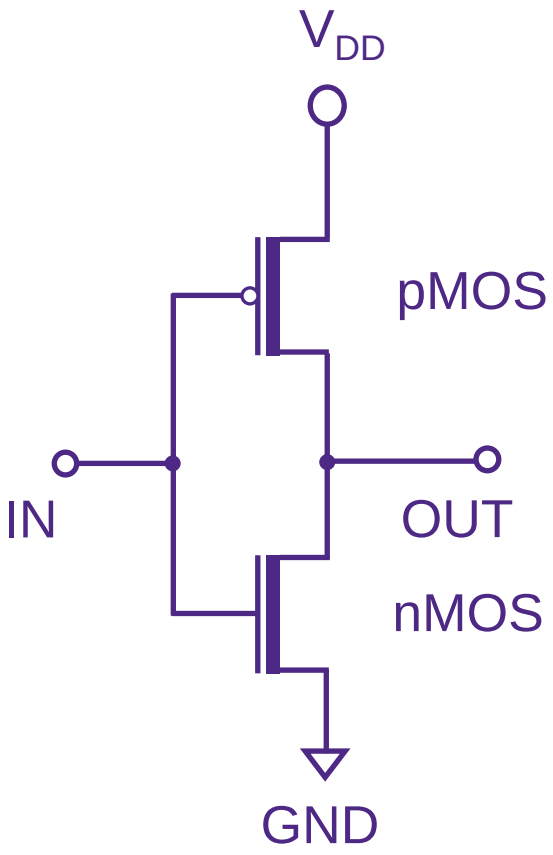
$$OUT = \overline{AB + C + (D + E)F}$$

The CMOS technique

- The name comes from: **C**omplementary **MOS**
- Idea: the load also should be provided with active control
  - **if** the nMOS *driver* (switching) transistor conducts, **then** the *load* transistor must be an "open" circuit
  - **if** the nMOS *driver* (switching) transistor is an "open circuit", **then** the *load* must be conducting

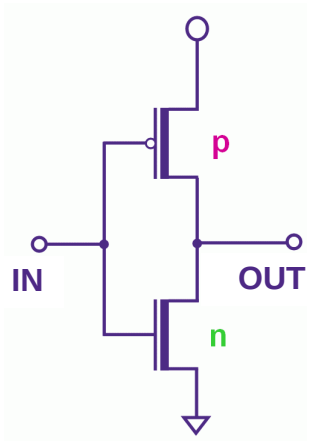
- This needs such a *normally OFF device* which needs "opposite" control signals than the nMOS transistors
  - Such device is an enhancement mode pMOS transistor

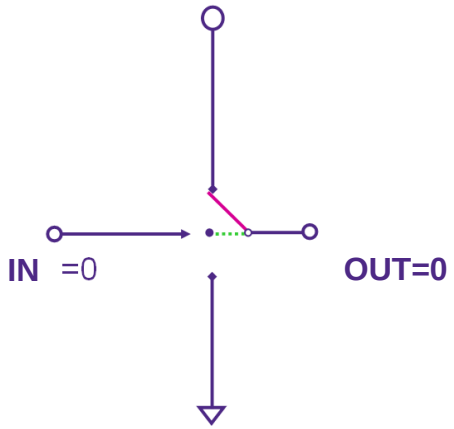
The CMOS inverter



- An n and a p type enhancement mode device
- Active load inverter: the two transitors have the same common control

In steady state only one device is "on", the other is "off".



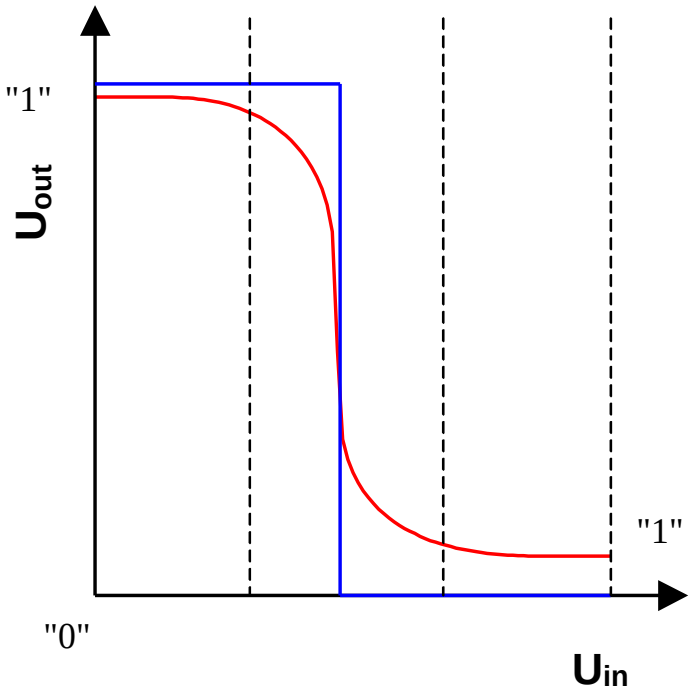


Characteristics of inverters, rudiments

- Transfer characteristic:
  - output voltage vs. input voltage

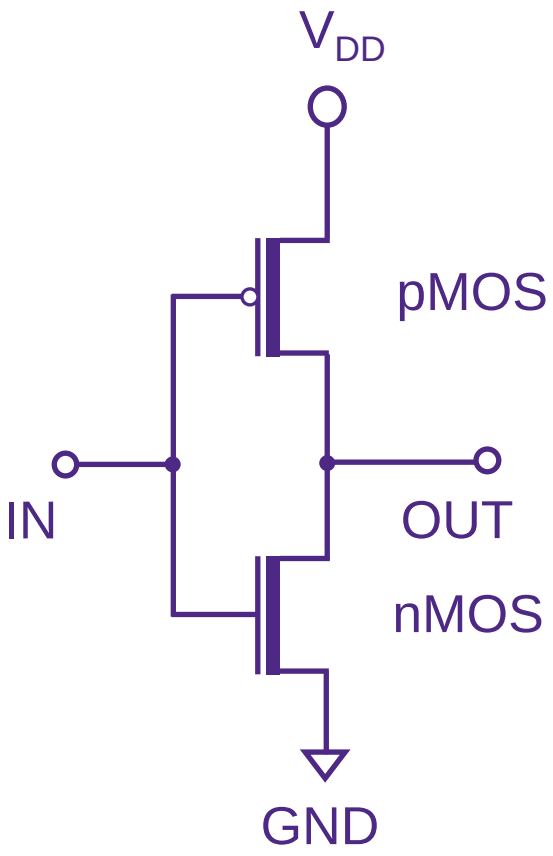
$$U_{out} = f(U_{in})$$

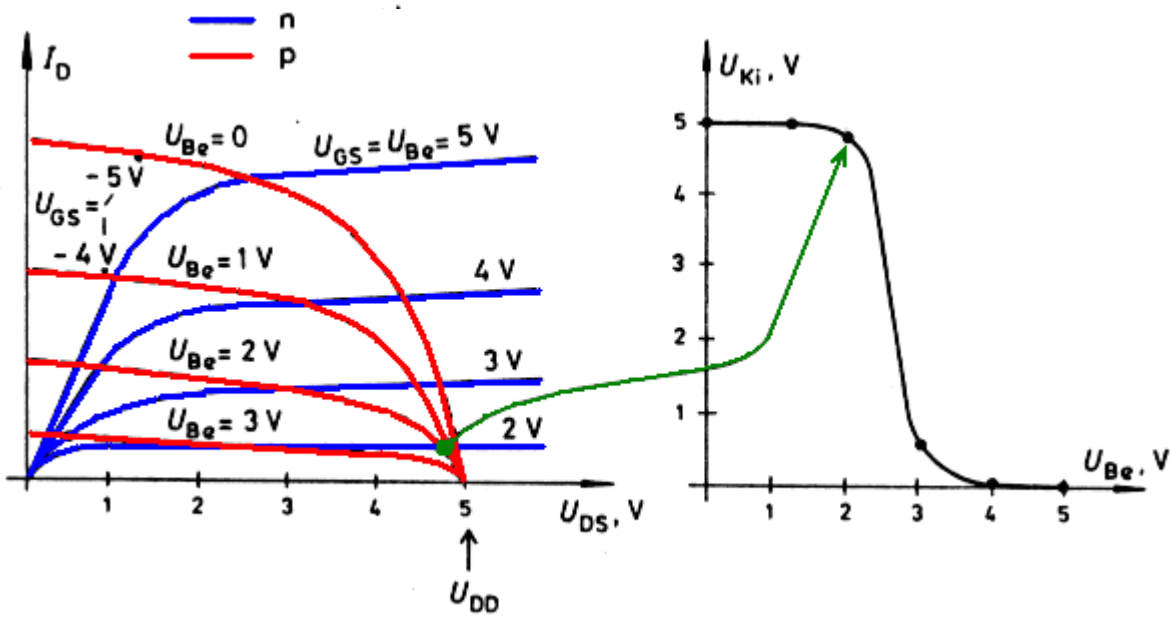
The output signal is the inverted version of the logic value of the input signal



transfer characteristic of an ideal and a realistic inverter

Xfer char. of a CMOS inverter

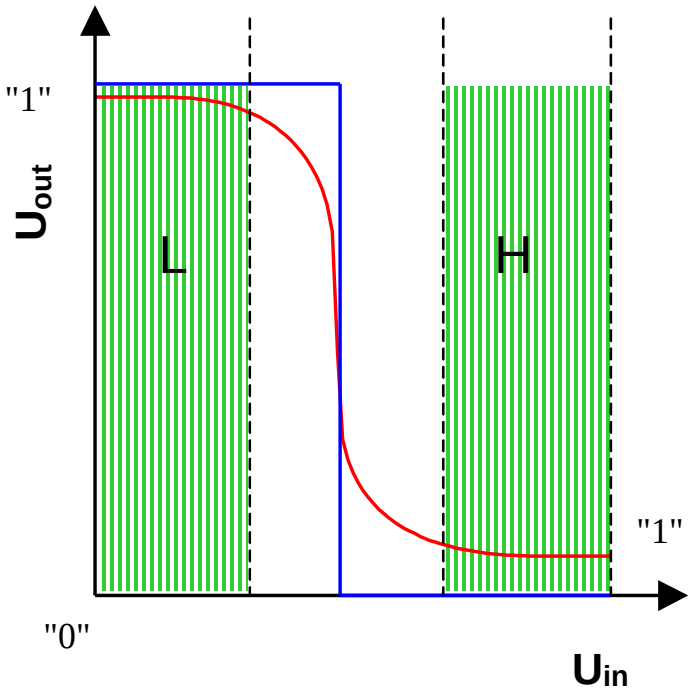




$U_{IN}=U_{GSn}$ $U_{OUT}=U_{DSn}$

Characteristics of inverters, rudiments

- Noise immunity:
  - Same U_{out} corresponds to a wide U_{in} range
  - There are 3 regions in the charactersitic
  - On the L and H sides the characteristc is flat, i.e. any voltage change in the input has negligible effect on the output.



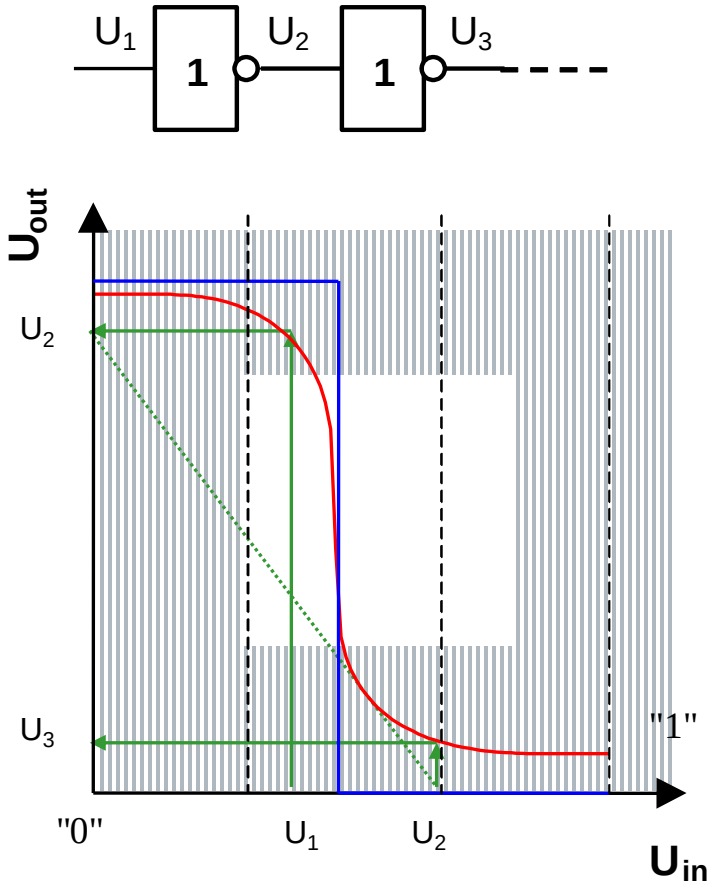
transfer characteristic of an ideal and a realistic inverter

L and H regions

Characteristics of inverters, rudiments

- Signal regeneration
  - depends on the slope of the middle region

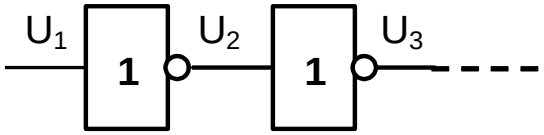
U_1 is a "bad" logic 0 signal. Output U_2 of the first inverter is already close to an acceptable logic 1 level. output voltage U_3 at the second inverter is already a "good" logic 0 level.



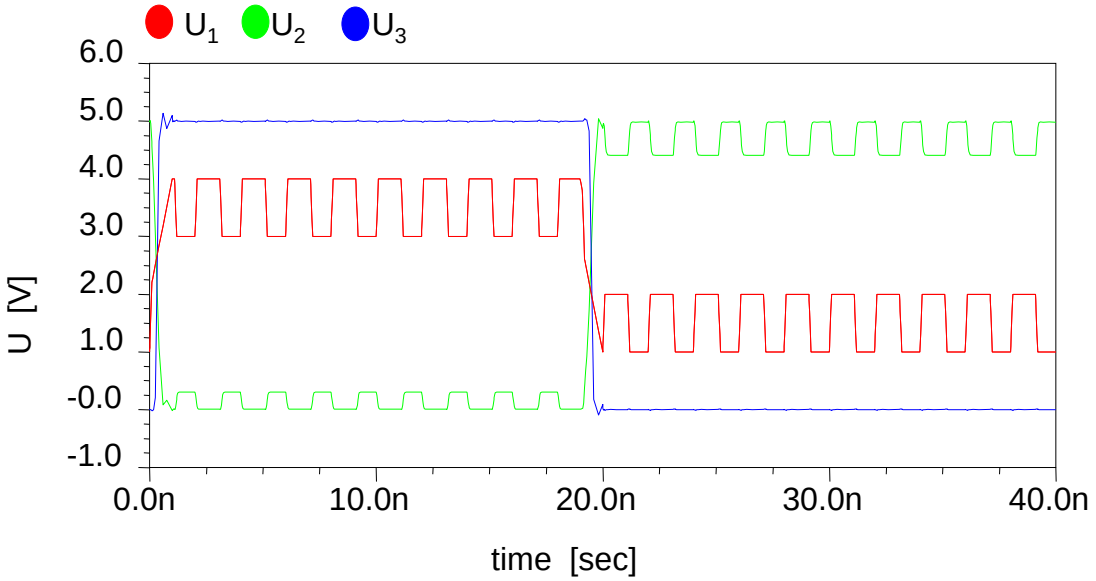
transfer characteristic of an ideal and a realistic inverter

Characteristics of inverters, rudiments

- Signal regeneration



U_L=0V, U_H=5V



(SPICE simulation)

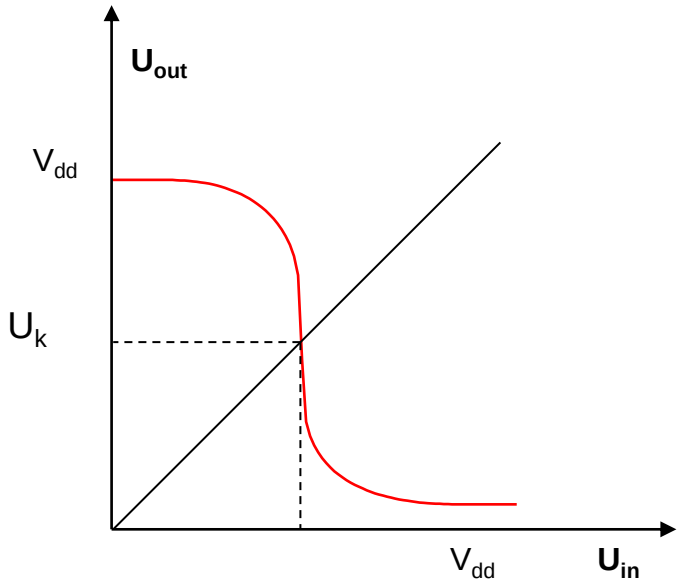
In case of U_3 both the voltage level and the signal form are visibly regenerated!

Characteristics of inverters, rudiments

- Inverter logic threshold voltage

The level, under which the signals will be converted into logical 0 and above which the signals will be converted by the inverter chain into logical 1

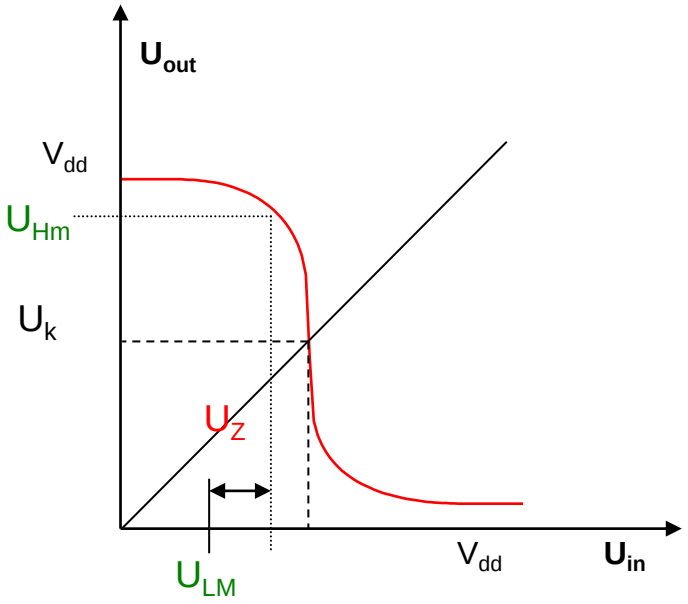
Intersection of the $U_{in}=U_{out}$ line and the x-fer characteristic



Characteristics of inverters, rudiments

- Logic level ranges

The voltage range of the logic 0 and 1 values within which the circuit works safely in the respective logic level



Example: 74HC00,
V_{dd}=3V,
U_{LM}=0.9V
U_{Hm}=2.1V

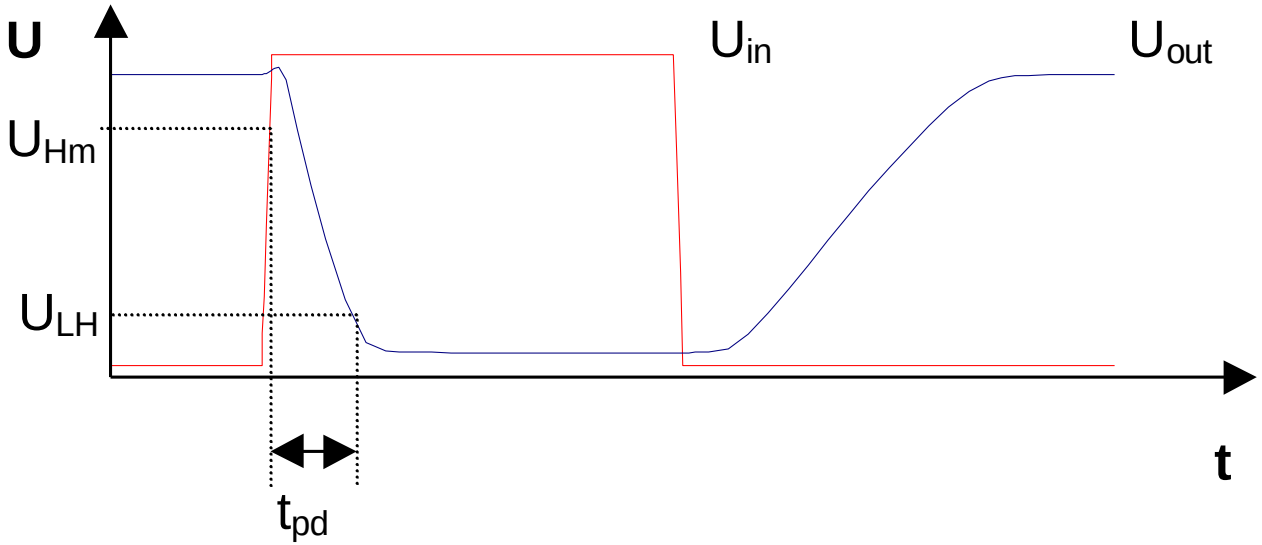
Important voltage values

U_{LM}, max. of logic 0

U_{Hm}, min. op logic 1

Characteristics of inverters, rudiments

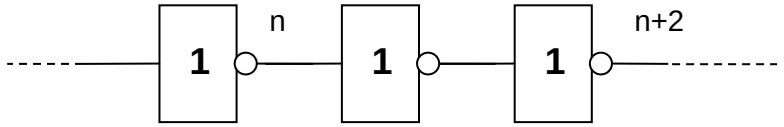
- Propagation delay



t_{pd} is difficult to define, and may be different for switching on and off (e.g. nMOS inverters)

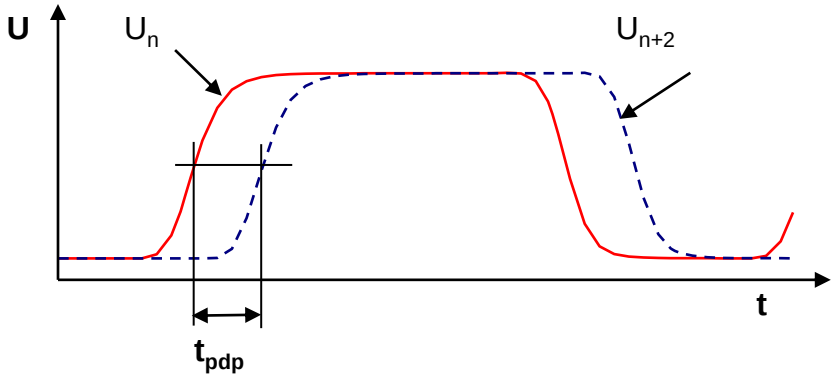
Characteristics of inverters, rudiments

- Inverter pair delay



A long chain of uniform inverters is assumed. After a certain number of inverters the signal form will be determined by the inverter properties only.

After propagating through 2 inverters the signal will be the same, the delay will be $\mathbf{t_{pdp}}$ – *the inverter* ***pair propagation delay***

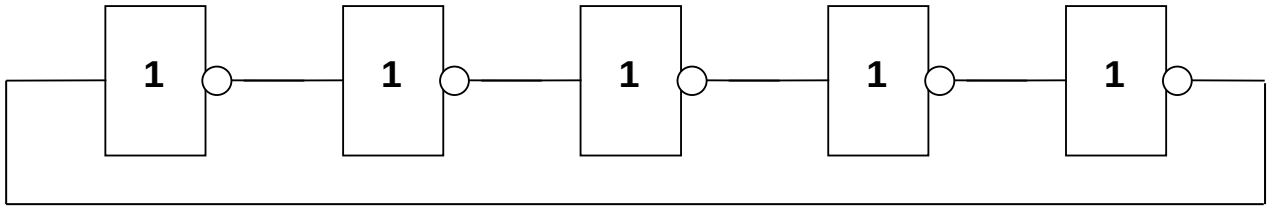


Characteristics of inverters, rudiments

- Measuring the inverter pair delay

THE RING OSCILLATOR

Odd number of inverters connected in a chain, no stable state $\Rightarrow$ oscillation



$$T=n \cdot t_{pd}$$

Characteristics of inverters, rudiments

- Power-delay product ($P\tau$)
  - **low power** and **small delay** refer to good quality,
  - their product is a **figure of merit** for the quality of a circuit family.
  - the physical meaning: the minimal energy, needed to work on 1 bit of information.