

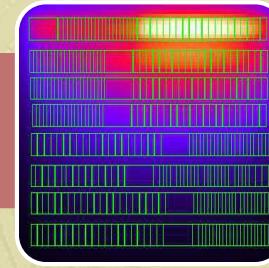
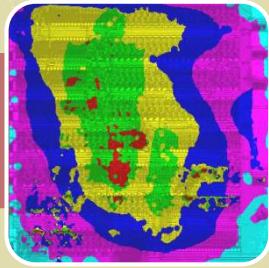
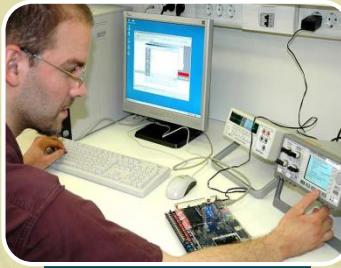
Budapest University of  
Technology and  
Economics



# Microelectronics, BSc course

Manufacturing technology

Department of Electron Devices



# The process: manufacturing technology

Overview of the steps and equipment



# Production of polysilicon

20% of the Earth's crust is made up by silica glass ( $\text{SiO}_2$ ) or silicat

From silica glass Si with 2...3% impurity can be produced in arc furnace:



Reacted with hydrochloric acid gas, trichlorosilane with boiling point of  $32^\circ\text{C}$



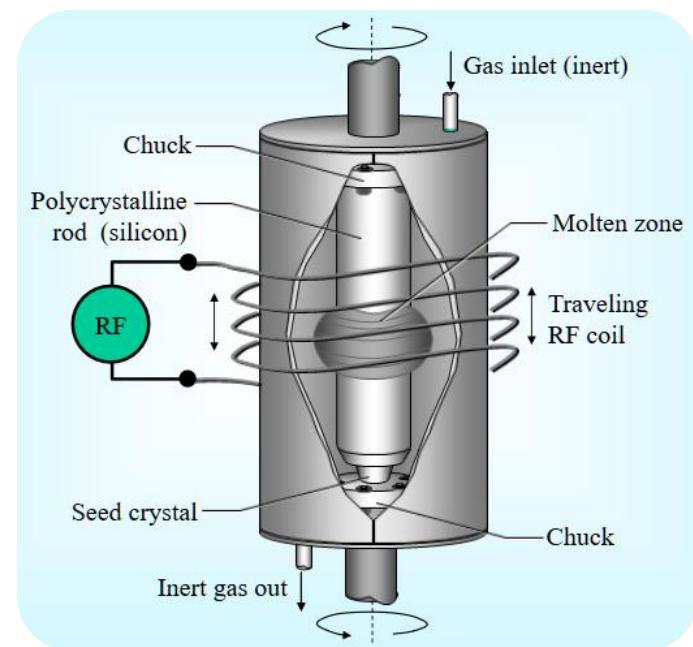
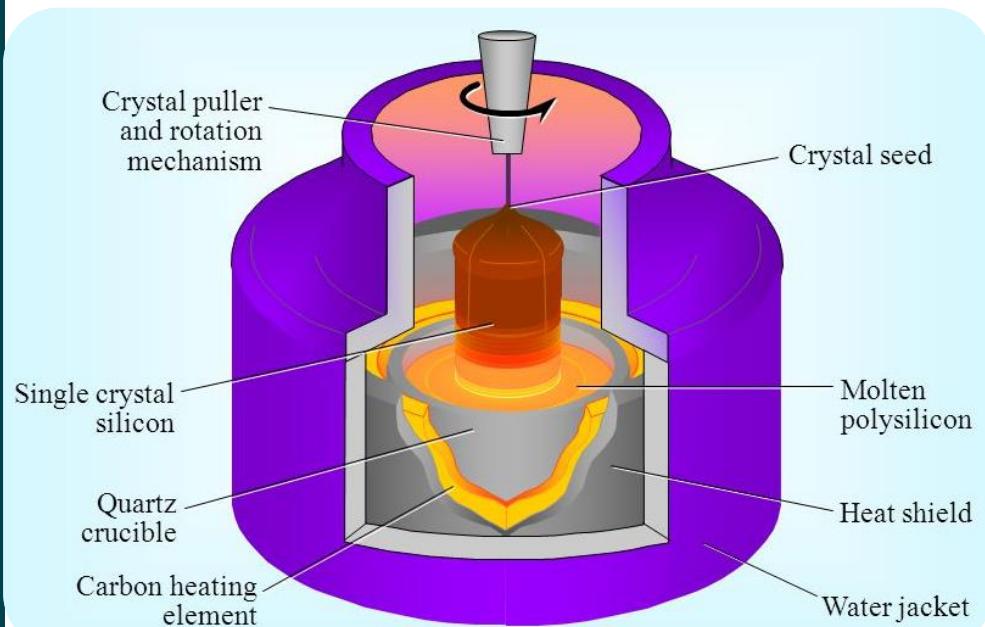
Impurity concentration can be decreased below  $10^{13} \text{ db/cm}^3$

Poly Si (rod) manufacture:



# Creating single crystal rods

Czochralsky (CZ) or FloatingZone (FZ) procedure



# Properties of the silicon

14 atomic number in the periodic table

Melting point at 1415°C

Diamond crystal (face centered cubic)

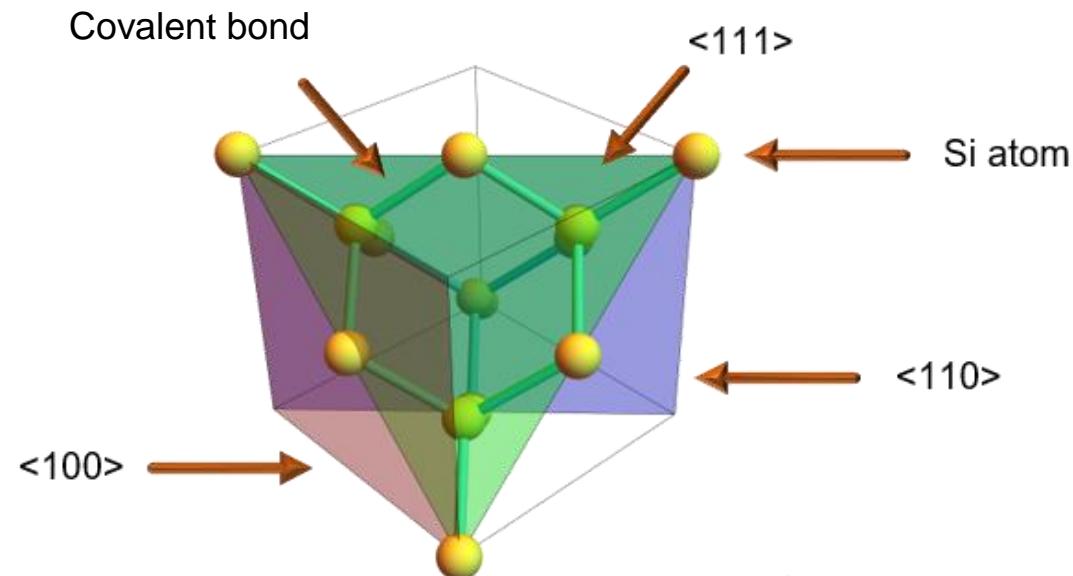
Good heat conductance property  $\alpha = 156 \frac{W}{mK}$

Excellent mechanical properties

High degree of hardness

High tensile stress

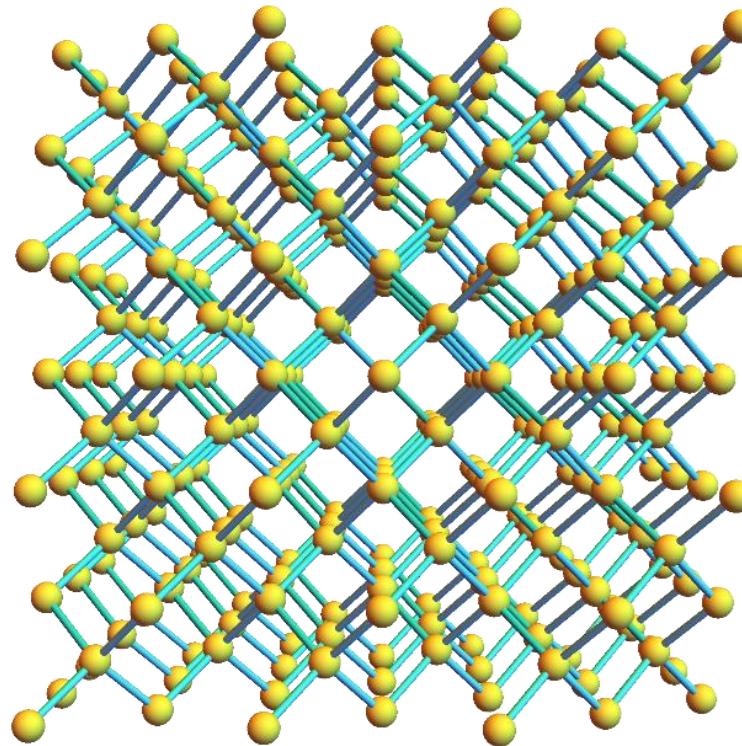
But rigid



# Properties of the silicon

Different orientation (*viewing the structure from different views*) different usage

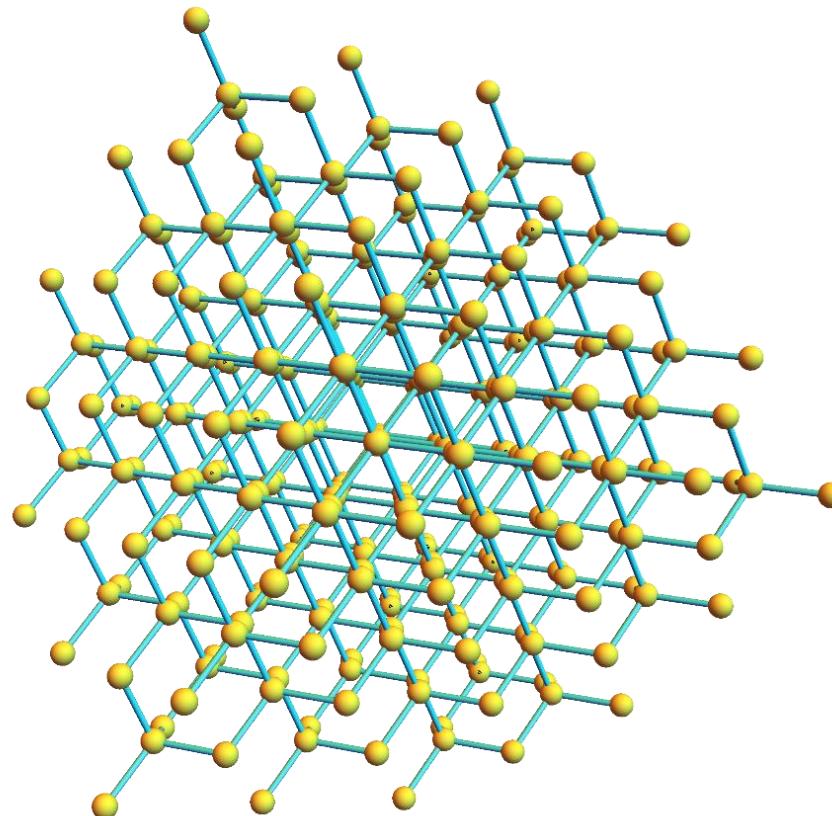
CMOS circuits: substrate with  $<100>$  orientation



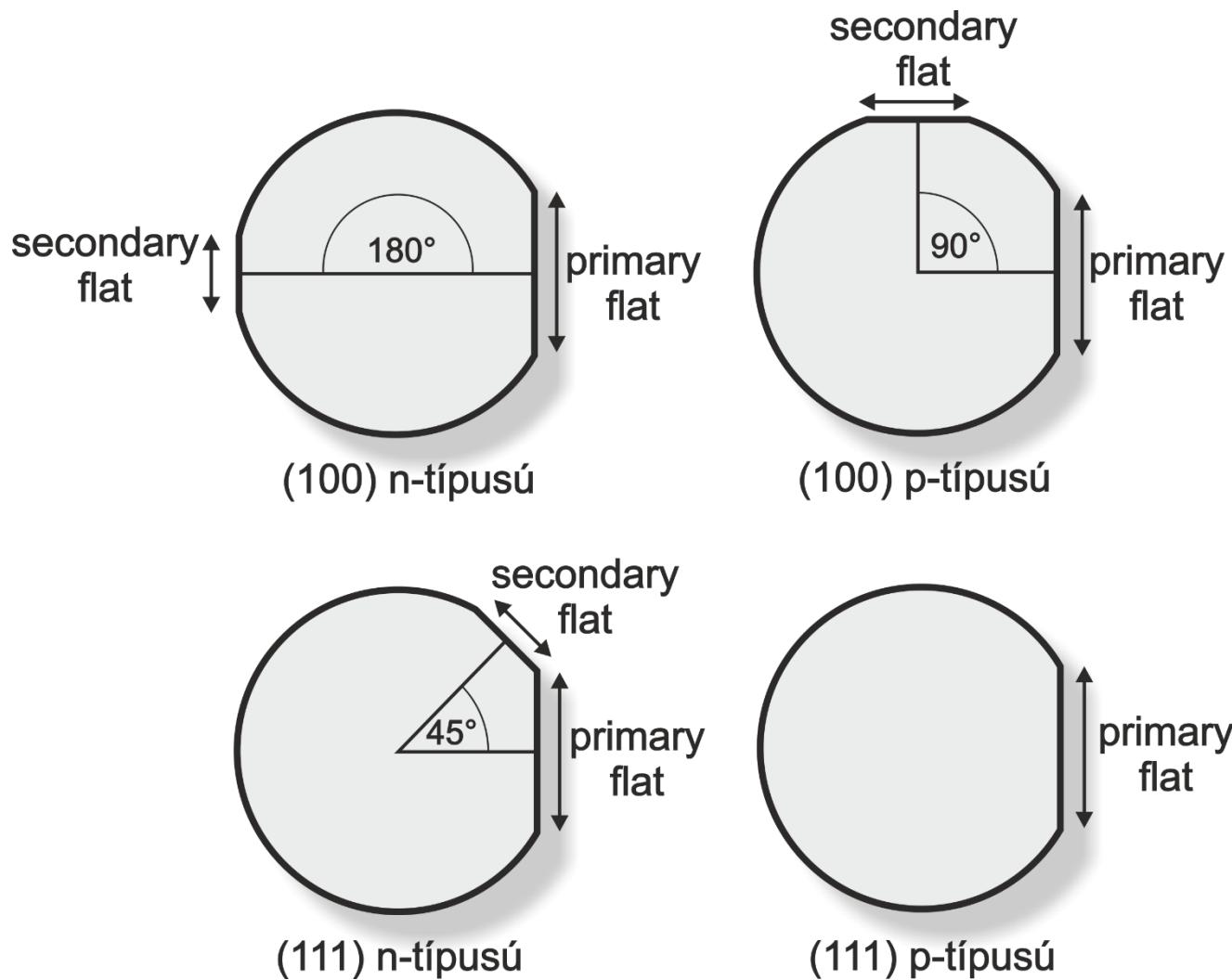
# Properties of the silicon

Different orientation (*viewing the structure from different views*) different usage

Bipolar circuits: substrate with  $<111>$  orientation

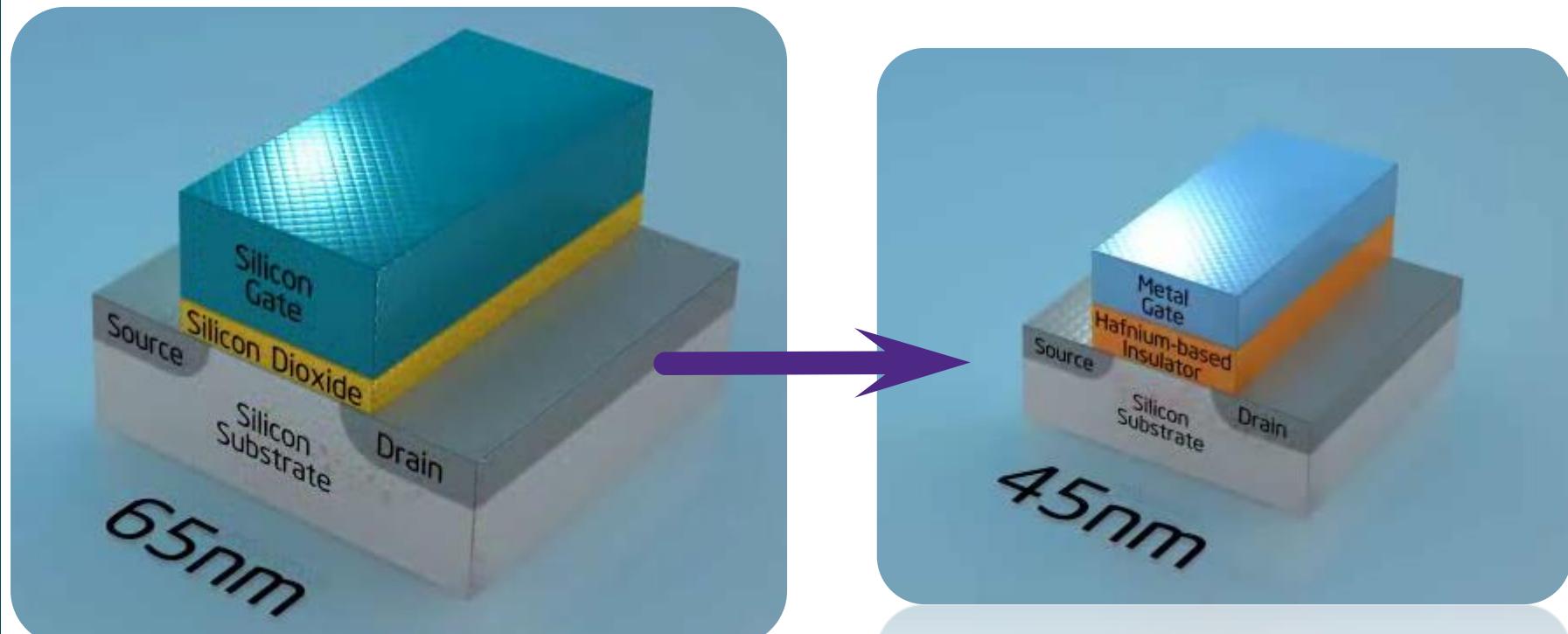


# Substrate orientations



# Devices to manufacture - MOSFETs

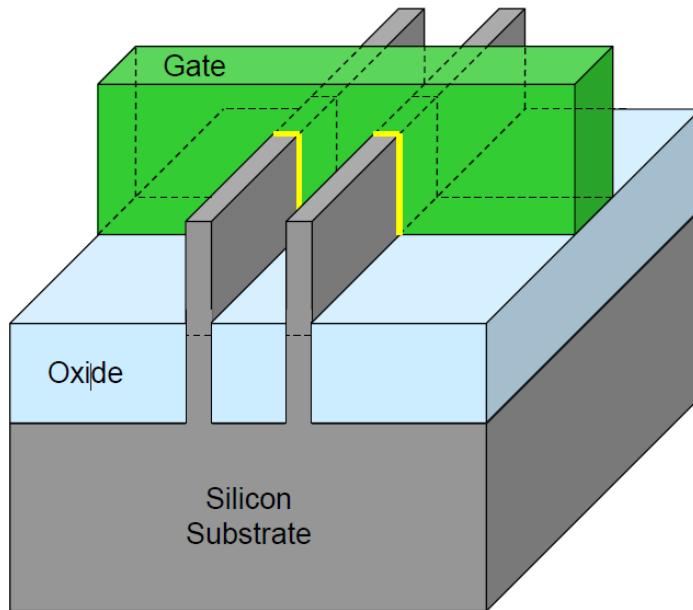
Minimal Feature Size (MFS) 2007/2008, Intel



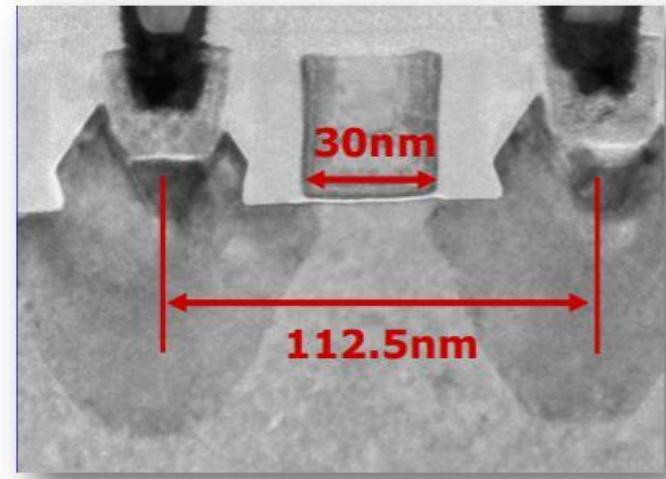
# Devices to manufacture - FinFETs

Minimal feature size (MFS)

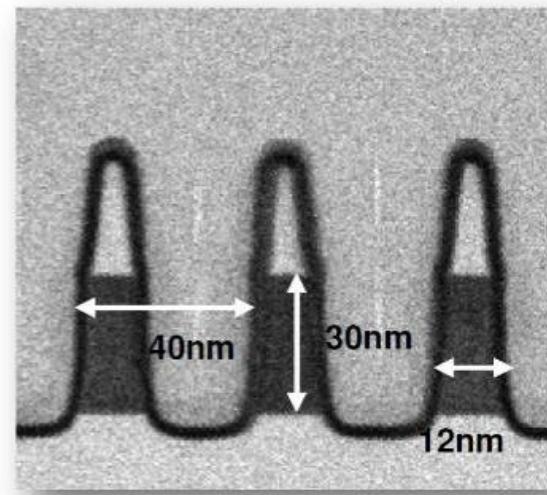
Intel 2012, 2014, 2018 (10nm)



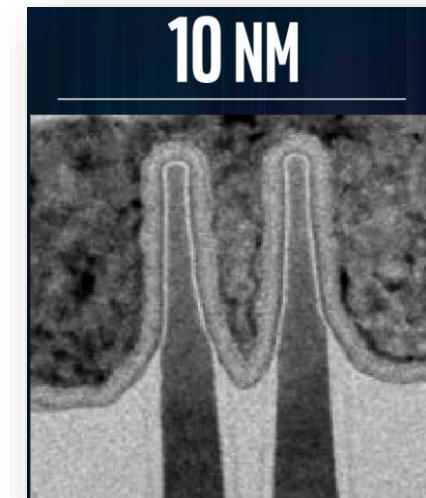
32nm Planar Example



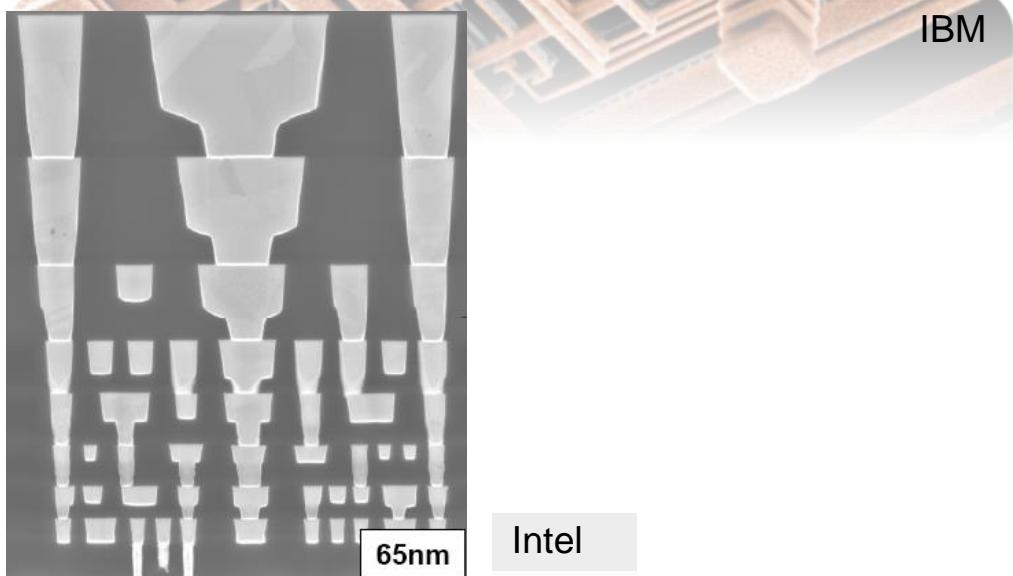
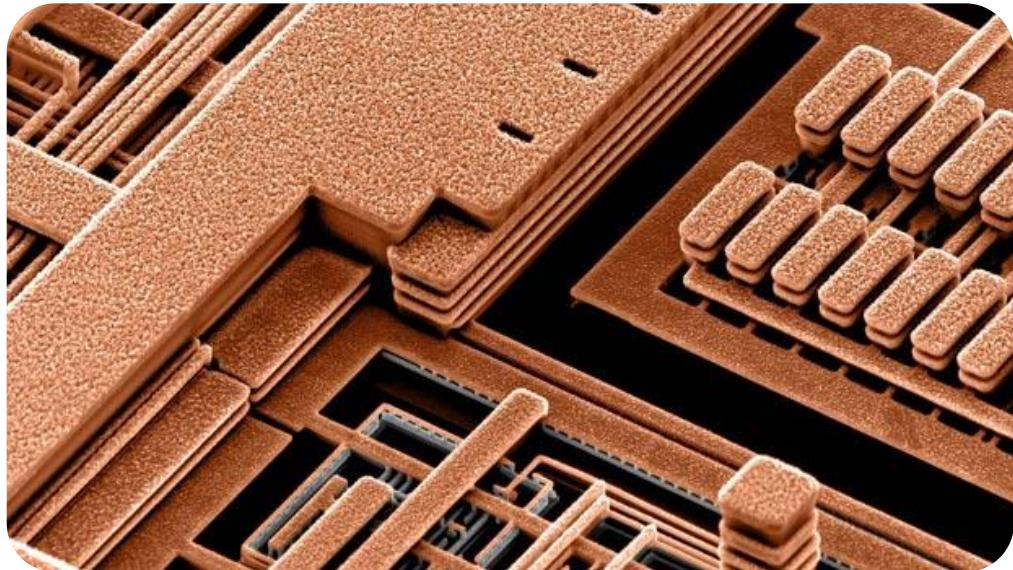
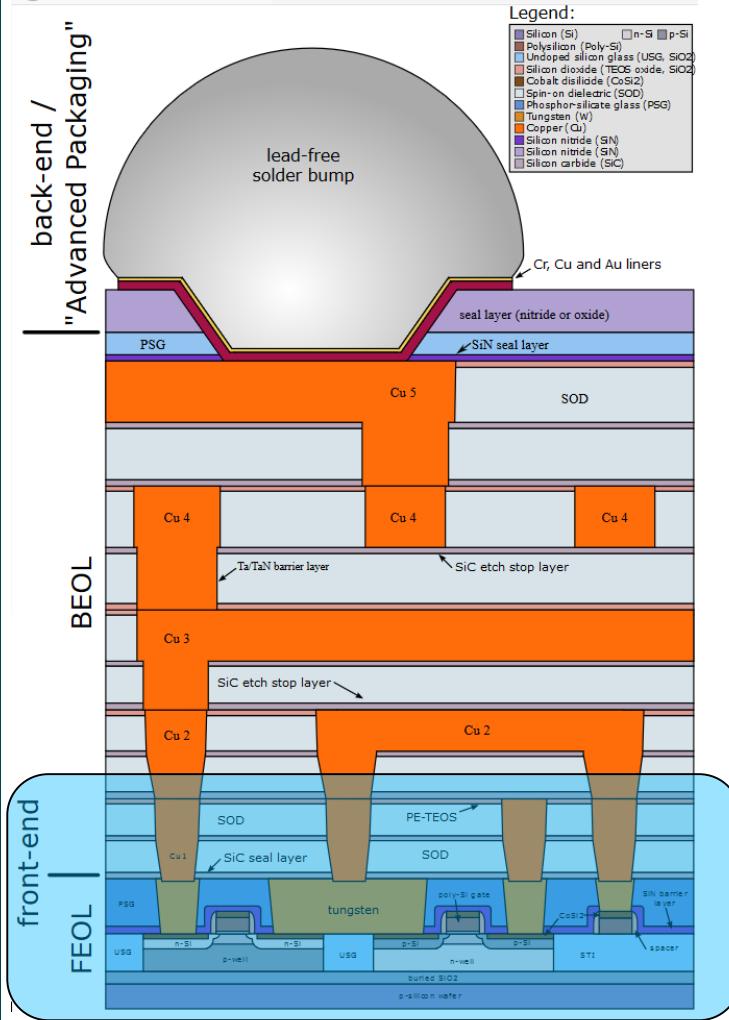
22nm FinFET Example



10 NM



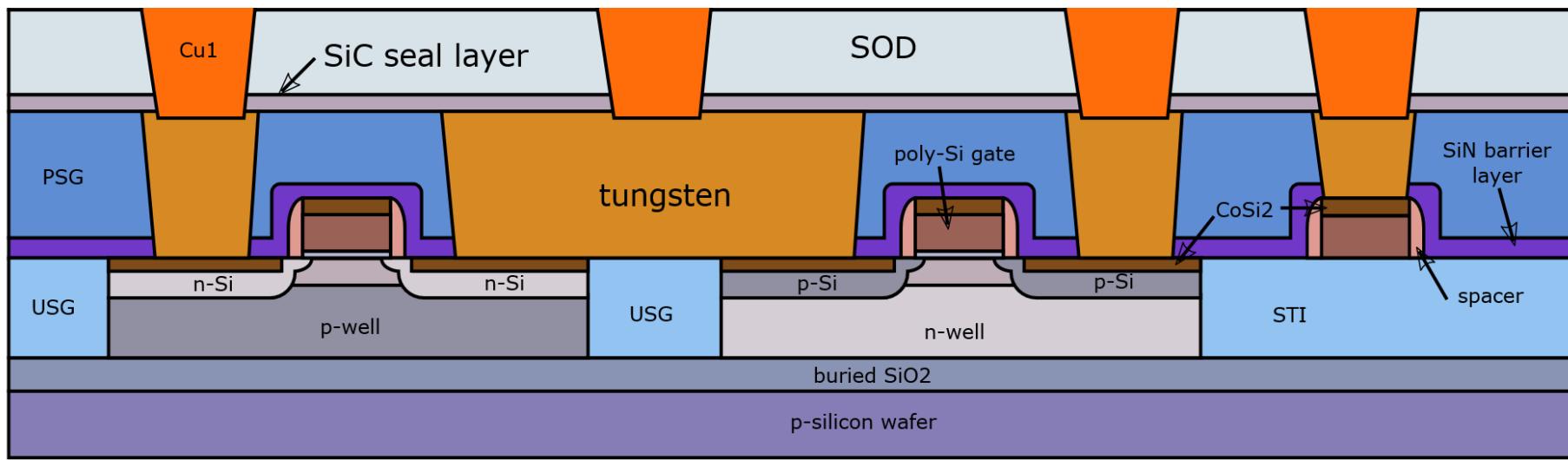
# Devices to manufacture - Metalization



65nm

Intel

# Devices to manufacture - Metalization



# Basic processing principles

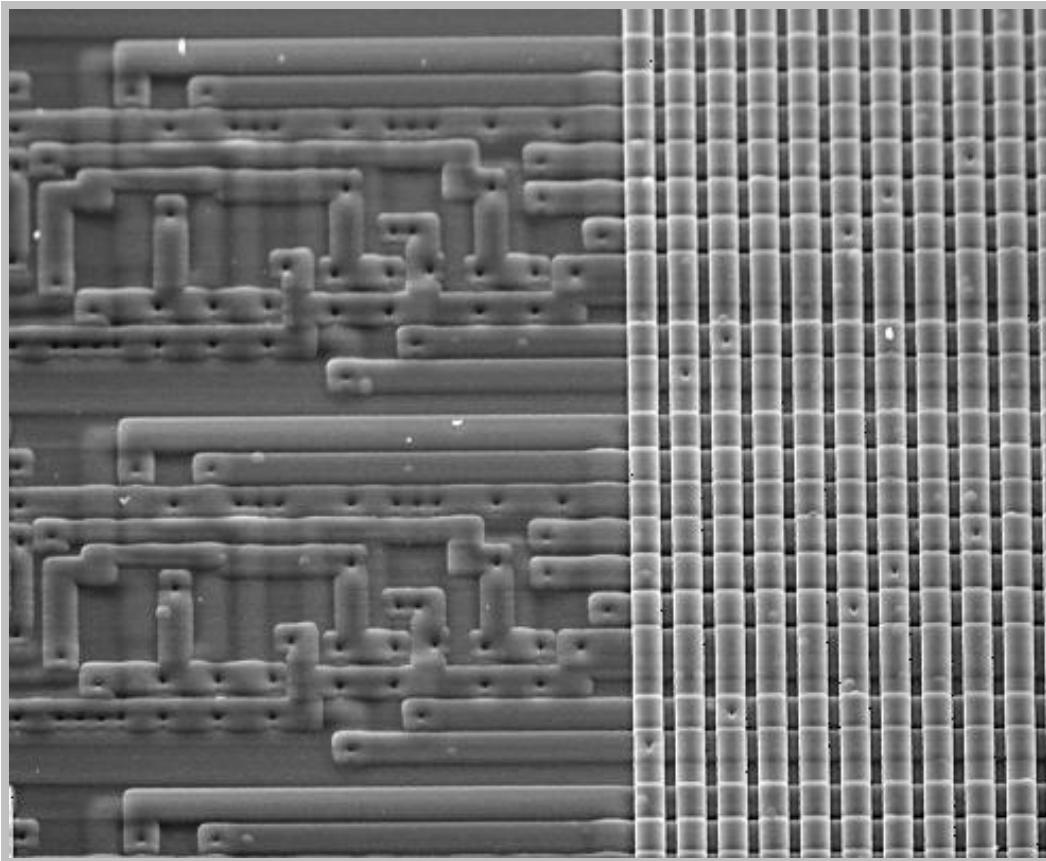
**Layer growth or deposition:** new material layer is formed over the entire surface of the wafer

**In-depth deposition of external material:** diffusion, ion implantation

**Patterning:** some patterns are formed in the deposited layer

- deposition of a photo-sensitive lack (**photoresist**)
- photographing the pattern onto the lack
- developing the photoresist: pattern formed in the resist layer
- transferring the pattern from the resist to the material layer underneath by some kind of **etching**
- removal of the resist

# Monolithic IC-s



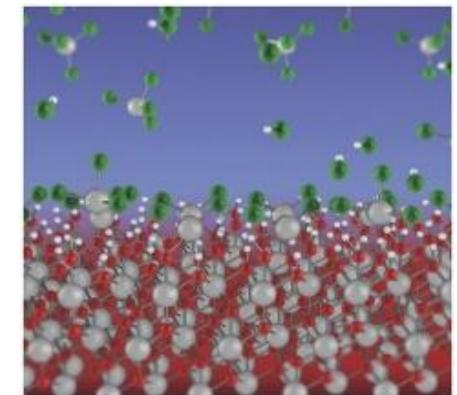
Mono lit = single stone

- In-depth structure
  - *Layer growth, deposition*
- Surface structure
  - *Patterning*

**MFS – the major property of a process**

$15 \mu\text{m} \rightarrow 7 \text{ nm}$

# Layer growth or deposition



# In-depth structure

Layer growth / deposition:

Growth of epitaxial layer (continue the Si-lattice but doped)

today e.g.: IBE – ion-beam epitaxy: atomic layers are grown

LPE: *liquid phase epitaxy*

VPE: *vapor phase epitaxy*

CVD: *chemical vapor deposition* – continuous carrier gas ( $H_2$ ) flow

MBE – *molecular-beam epitaxy*: atomic layers are grown in  $10^{-8}$  Pa vacuum  
(examination of quantum effects, possible way to create quantum devices)

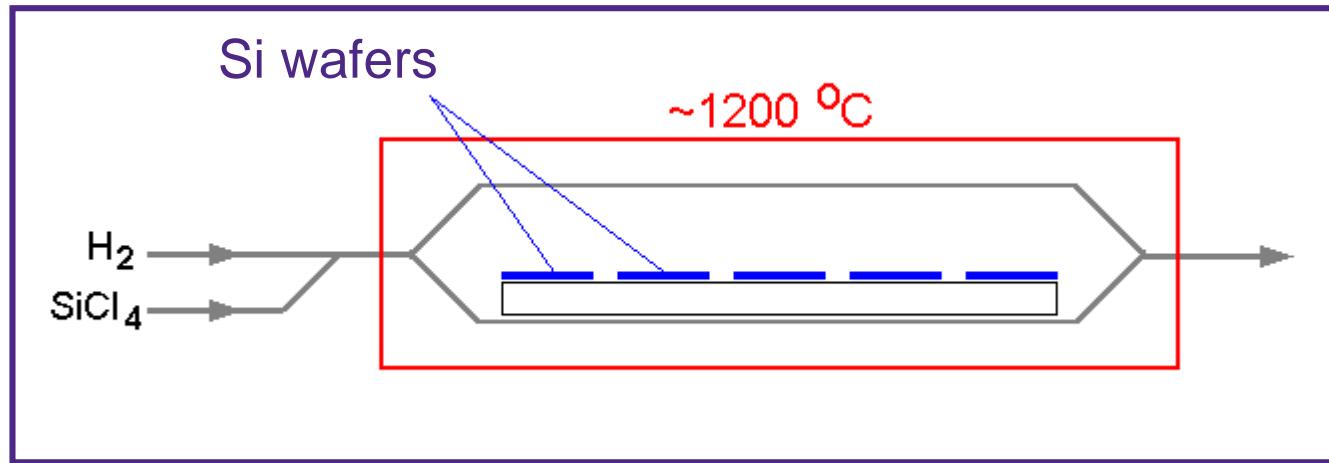
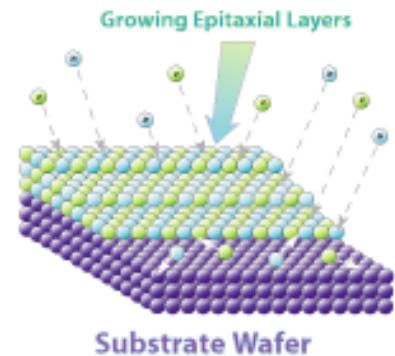
Oxidation (deposit/grow  $SiO_2$ )

Evaporation (e.g. deposit metal such as Al)

Sputtering

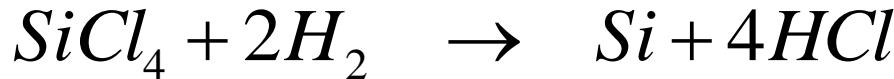
# Growth of epitaxial layers

The classical epitaxial growth  
either from gas or from liquid phase



The crystalline structure of the Si wafer is perfectly continued by the layer grown

$\sim 1200 \text{ }^{\circ}\text{C}$



# Growth of epitaxial layers

Depending on the  $\text{SiCl}_4/\text{H}_2$  ratio

- Growth of a single crystalline layer
- Growth of poly-crystalline silicon – called poly-Si
- Etching off Si
- Doping!



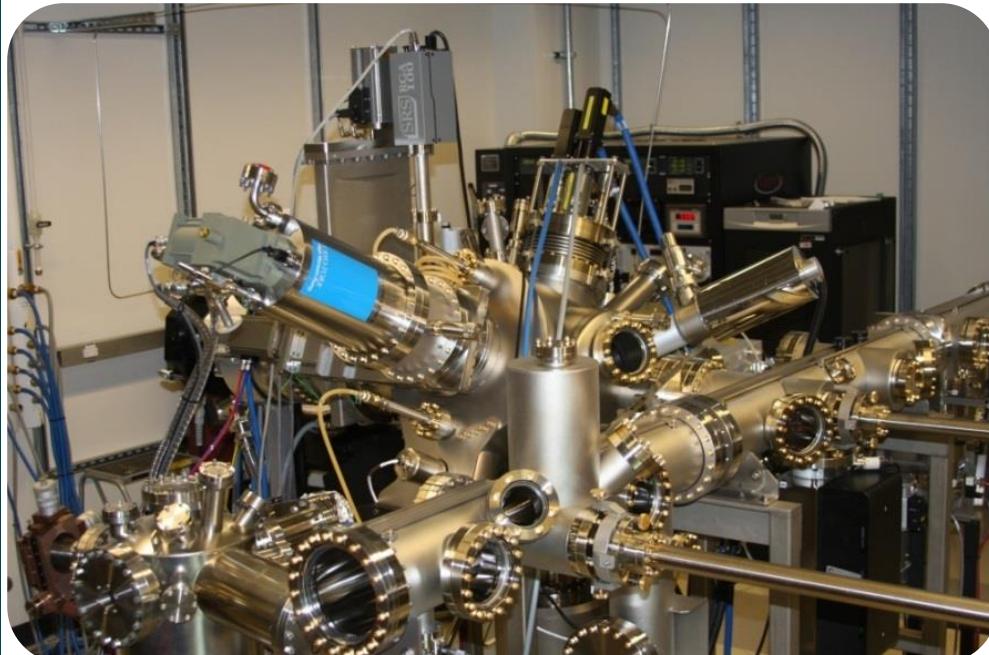
# Growth of epitaxial layers

Molecular-beam epitaxy:

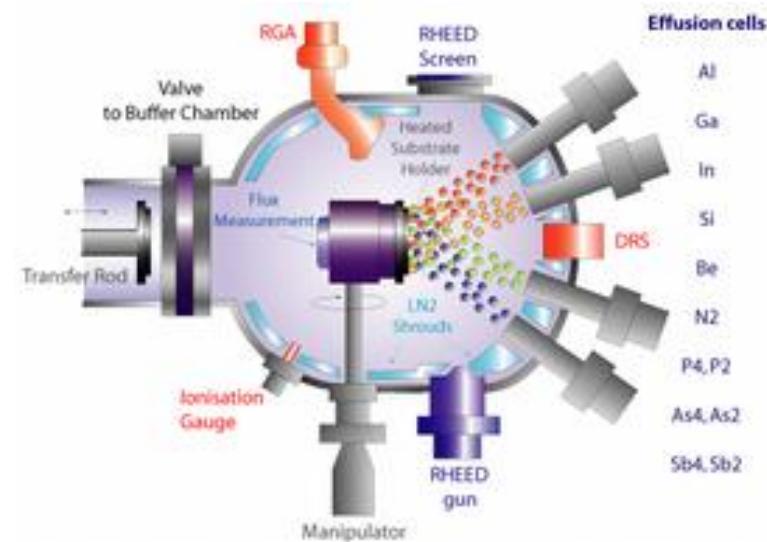
Multi-layer, varying composition, compound semiconductors

Quantum devices

Cc. 100 nm/h grow speed



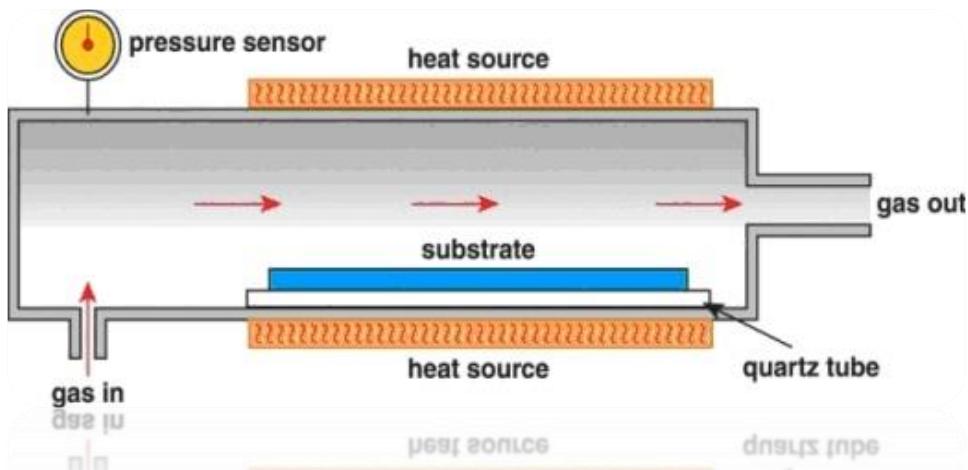
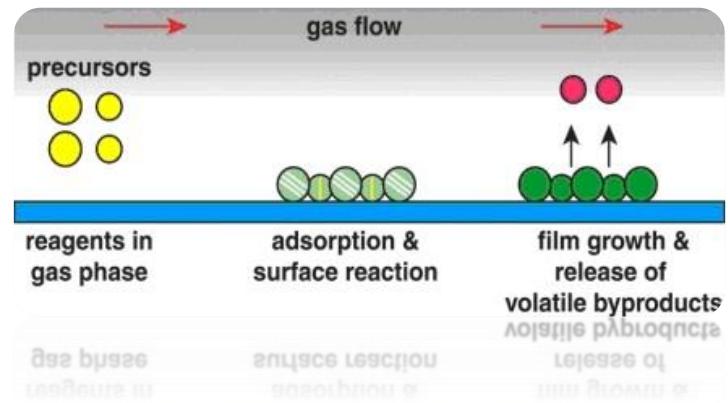
***MBE: molecular beam epitaxy***



# Growth of oxide layers

- ▶ Thermal oxidation (900-1200 °C)
- ▶ Chemical Vapor Deposition (CVD)

$$d_{SiO_2} \sim \sqrt{t}$$

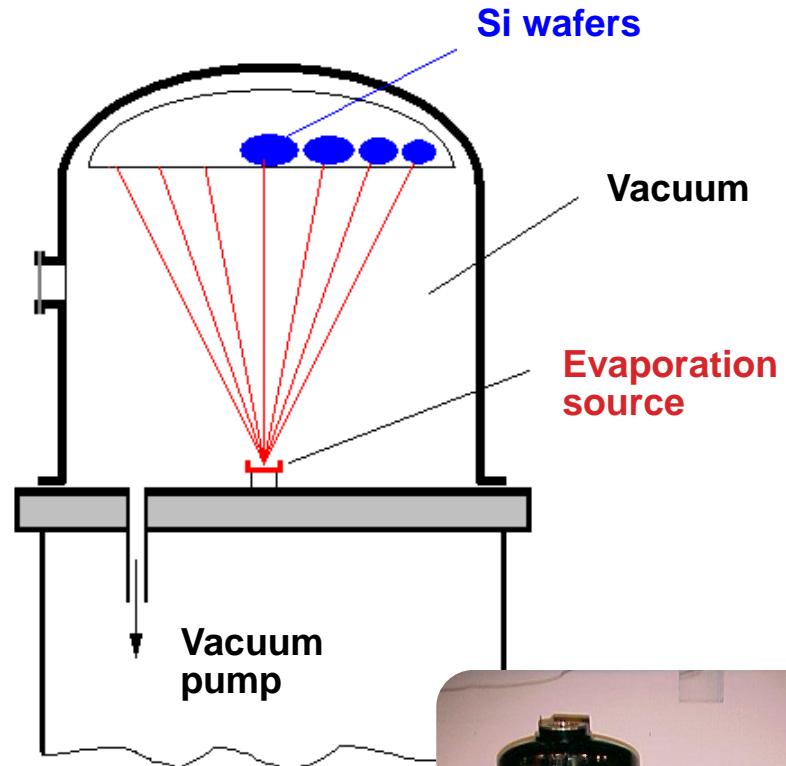


# Vapor deposition

Free mean path > size of the chamber

## Metallization

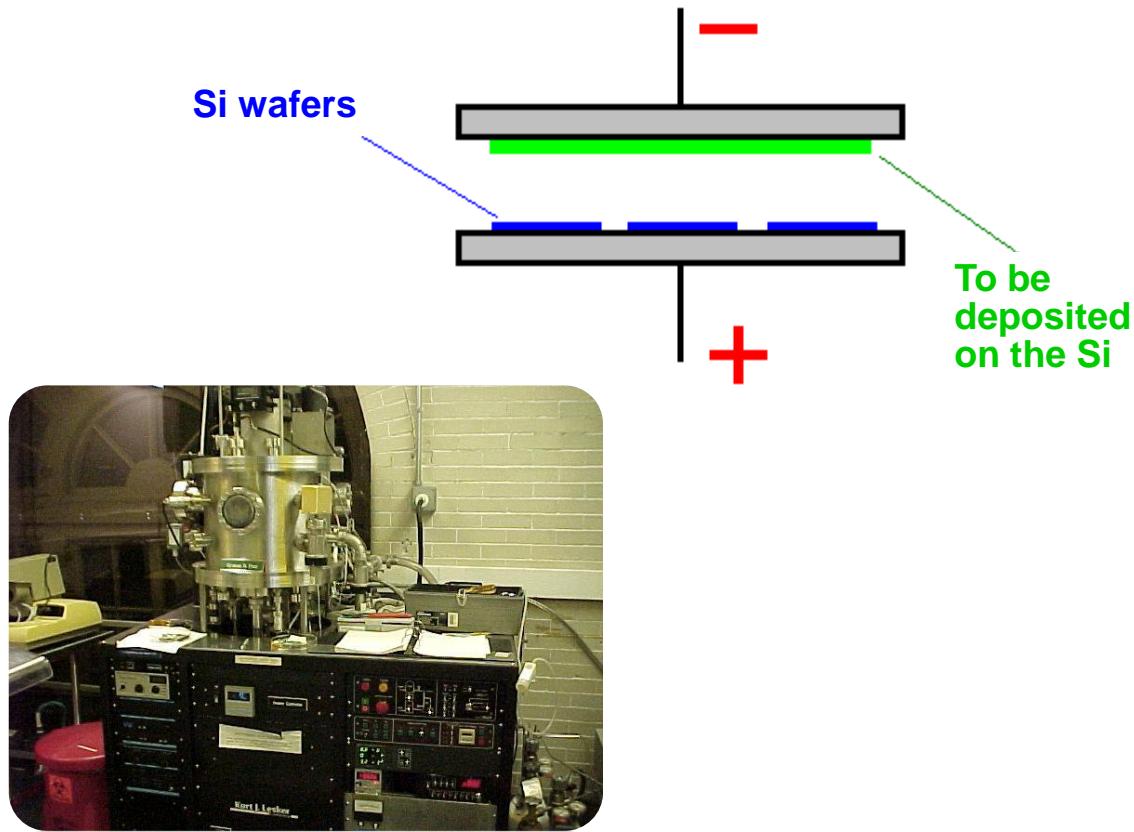
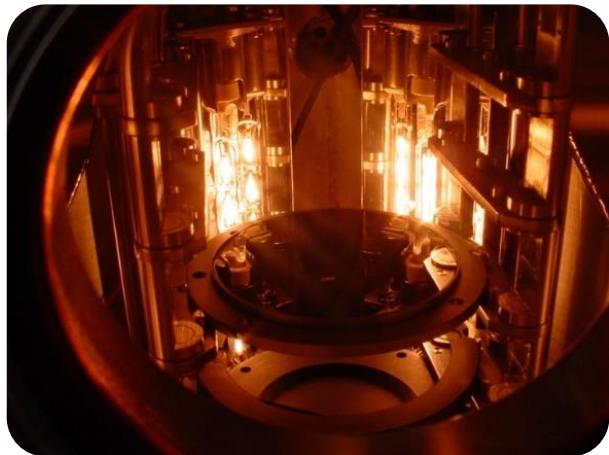
~0.1-0.5 µm



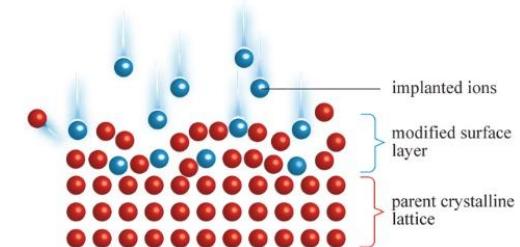
# Sputtering

Gas discharge is used to carry the material to be deposited from a cathode (e.g. Ar atmosphere)

Using high frequency **dielectrics** can also be sputtered

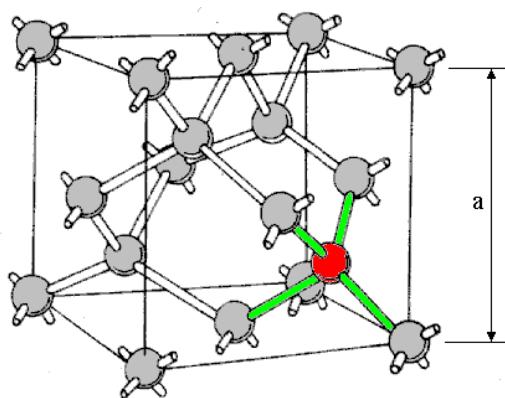


# In-depth deposition of external material

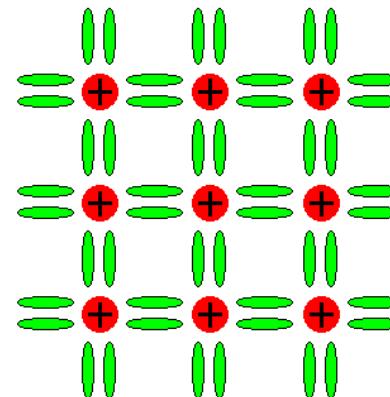


# In-depth structure

Deposition of dopants (foreign atoms) in the silicon crystal to modify its properties



Simplified view in 2D

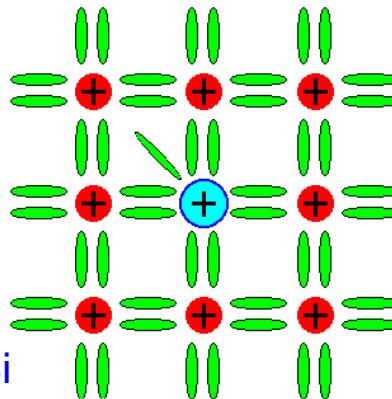


Diamond lattice in 3D

Dopant from  
column V  
(Phosphorus):

extra electron  
**DONOR**

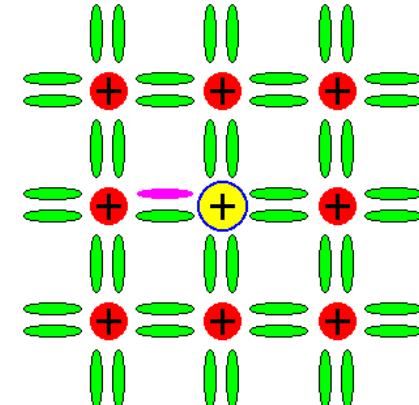
n-type Si



Dopant from  
column III  
(Boron):

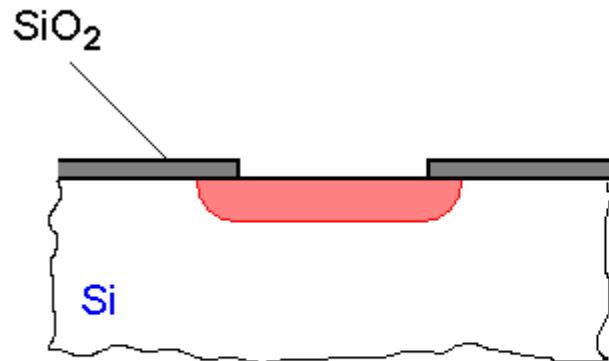
1 less electron  
**ACCEPTOR**

p-type Si

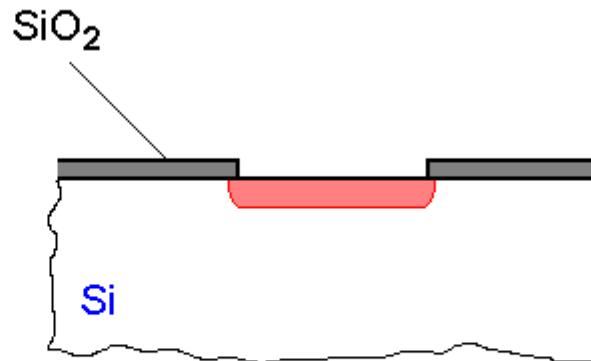


# How to select where to dope?

$\text{SiO}_2$  is an excellent mask against the flux of dopants

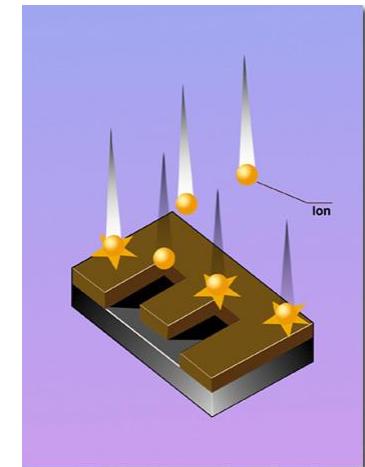


**Diffusion**  
**deep profile**



**Ion implantation**  
**shallow profile**

Masked by a  $\text{SiO}_2$  pattern



# In-depth structure

## Deposition of dopants by diffusion

Dopants diffuse in the high temperature Si-lattice

The energy of the Si atoms helps the dopants move

Movement mechanisms:

interstitial movement: movement by changing place with a Si atom

movement along crystalline defects

In-depth distribution of dopants is determined by Fick's laws:

$$J = -D \frac{\partial c}{\partial x} \quad D = D(T) \quad !$$

$$\frac{\partial c}{\partial t} = - \frac{\partial J}{\partial x}$$

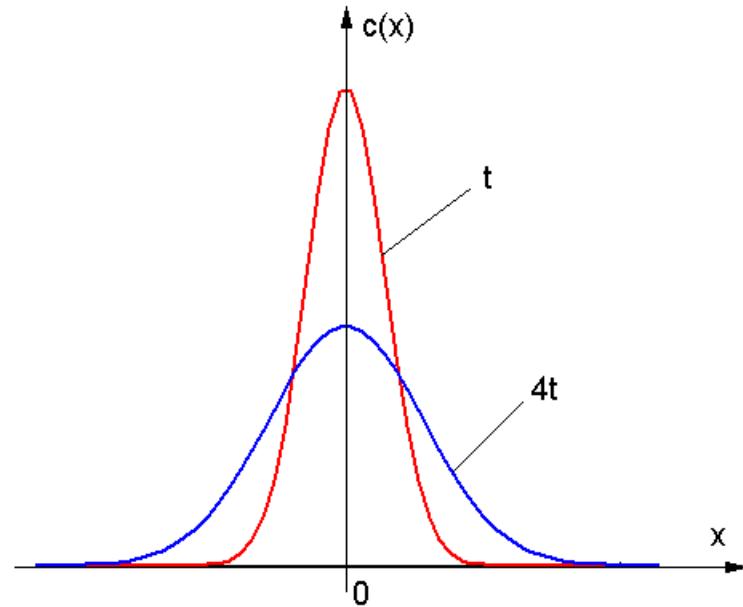
$$\boxed{\frac{\partial c}{\partial t} = D \frac{\partial^2 c}{\partial x^2}}$$

# Diffusion

The solution is:

$$c(x,0) = M_0 \cdot \delta(x)$$

$$c(x,t) = \frac{M_0}{\sqrt{4\pi Dt}} \exp\left(-x^2 / 4Dt\right)$$

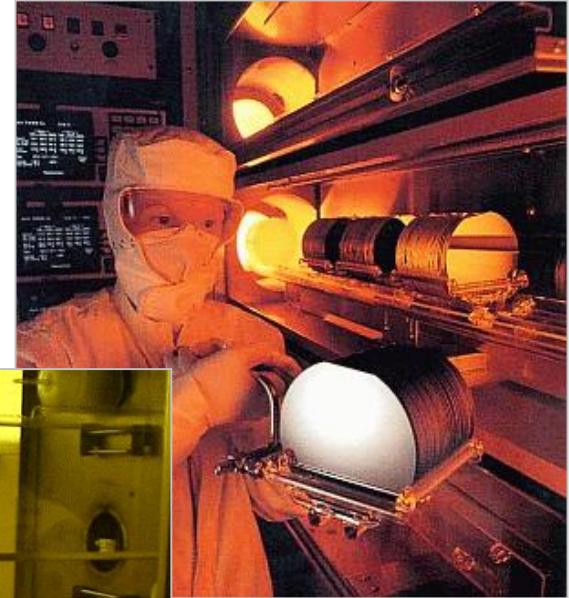


Two steps

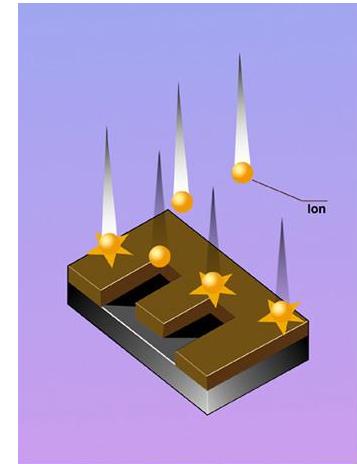
- initial deposition / pre-diffusion (e.g. 1100°C, 3 hours)
- drive-in (e.g. 1240°C, 1 hours)

# Diffusion

## The diffusion furnace



Masked by a  $\text{SiO}_2$  pattern



# Industry scale diffusion furnace

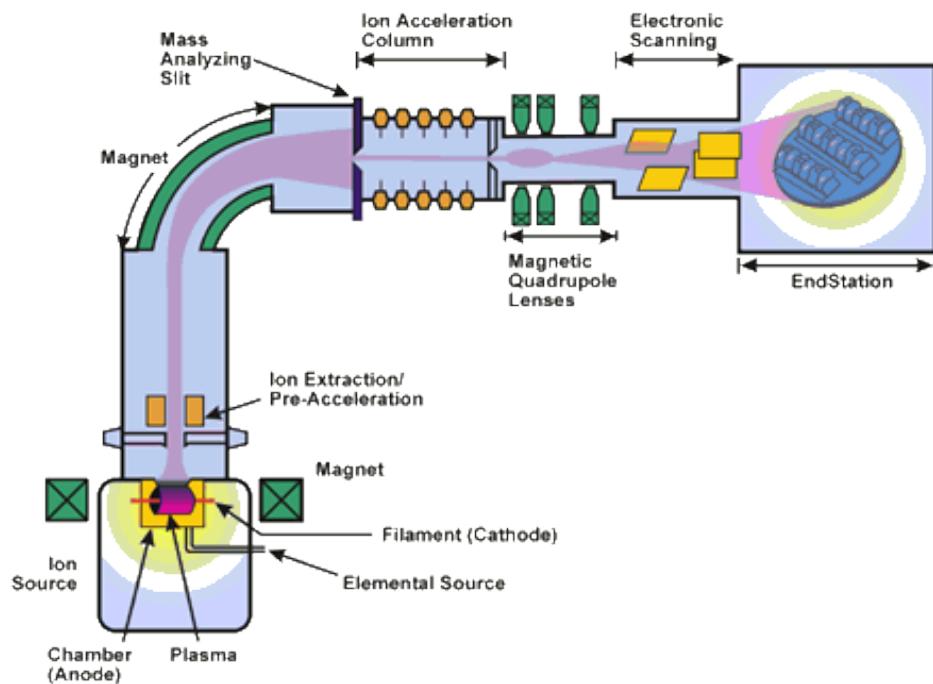


# Ion implantation

## Procedure:

1. Doping atoms are inserted into the ion source then they are ionized
2. Ions are accelerated by the electrical field
3. The surface of the wafer is bombarded to get the ions into the wafer

Ions fired upon the targeted Si wafer chosen from an ion beam with a mass spectrometer



# Ion implantation

From an ion beam one selects the ions that target the Si and penetrate the lattice

Initial distribution of deposited dopants depends on the energy and the dose of the ion beam

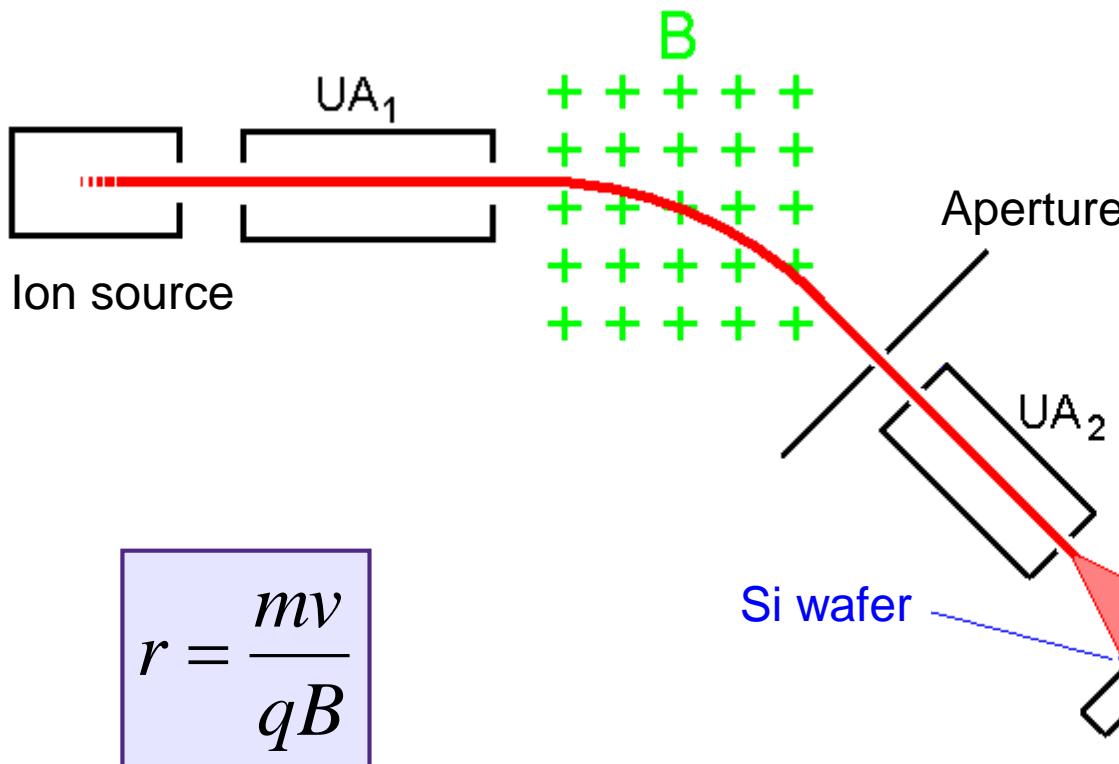
Thermal treatment follows the implantation

restore the Si-lattice

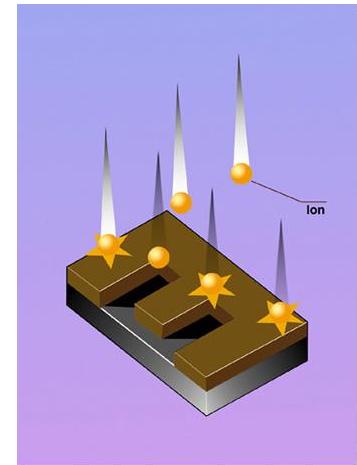
drive-in the dopants (form final doping profile)

~100 kV voltage is used

# Ion implantation



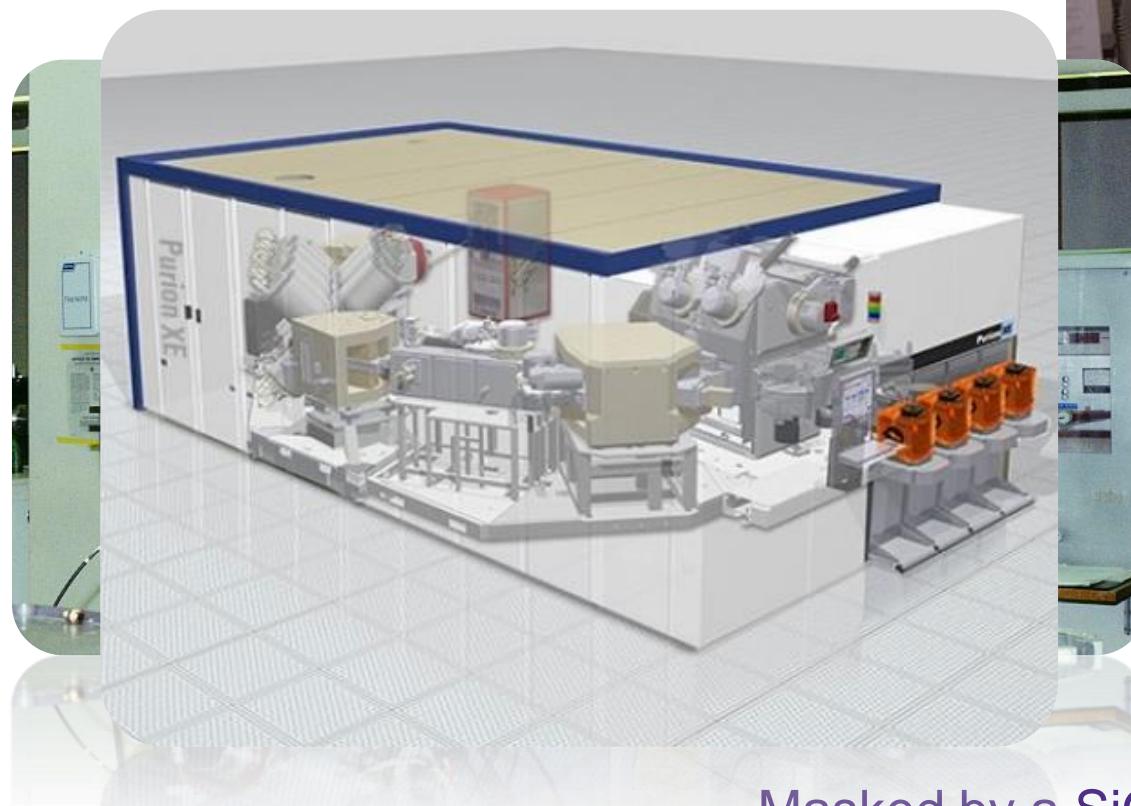
Masked by a  $\text{SiO}_2$  pattern



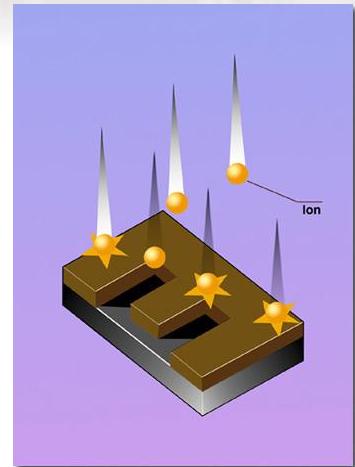
# Ion implantation

It is a **low temperature** process.

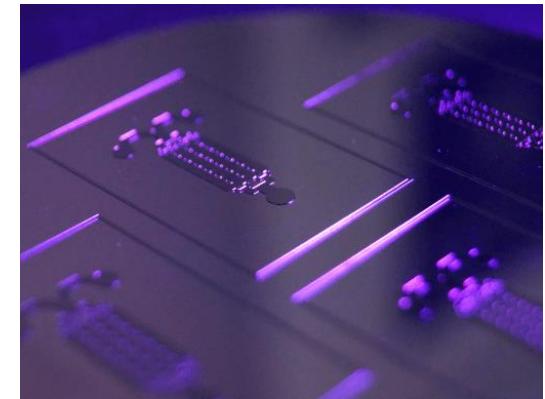
**Advantage:** existing profiles are less effected



Masked by a  $\text{SiO}_2$  pattern



# Patterning



# Window opening

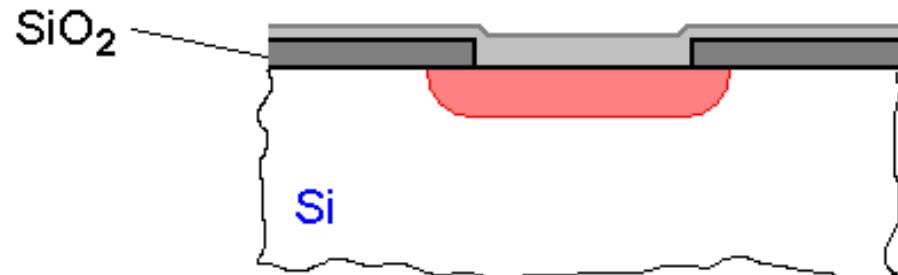
With photolithography – always the first step of any patterning

Problem of oxide steps: step coverage

Alignment problems: wafer-mask, mask-mask

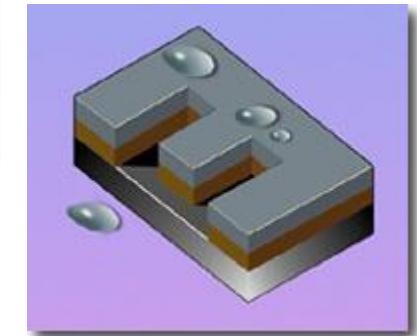
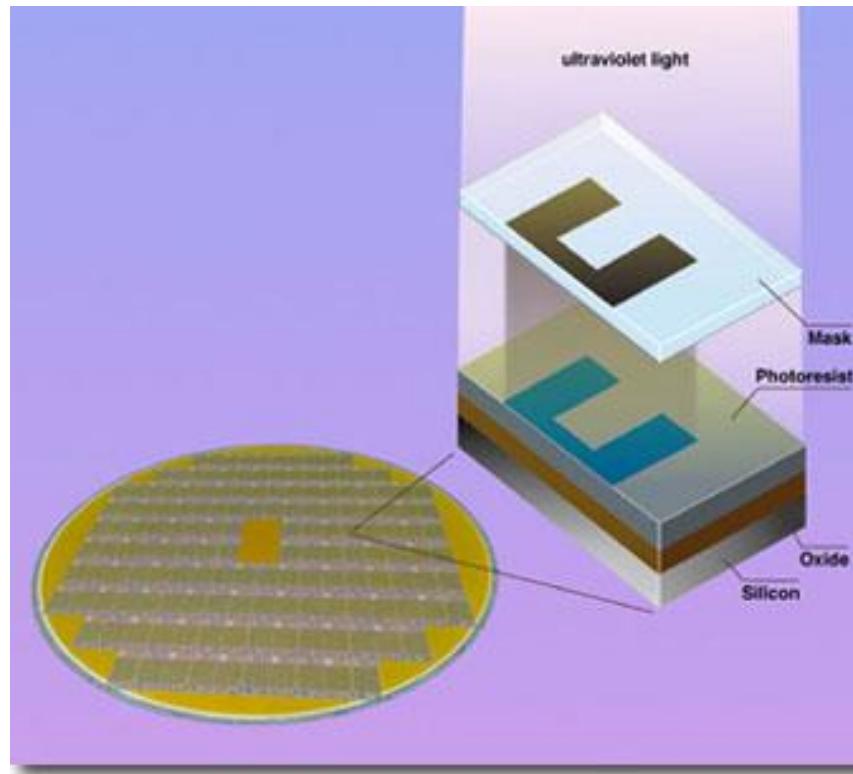
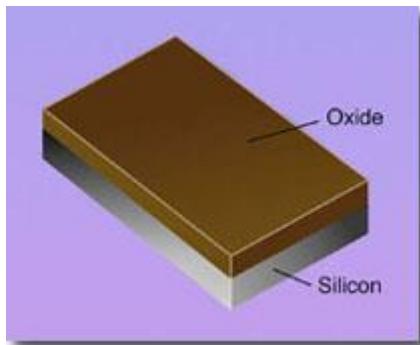
Diffraction

Standing wave effect



Window opening on the  
oxide with  
photolithography

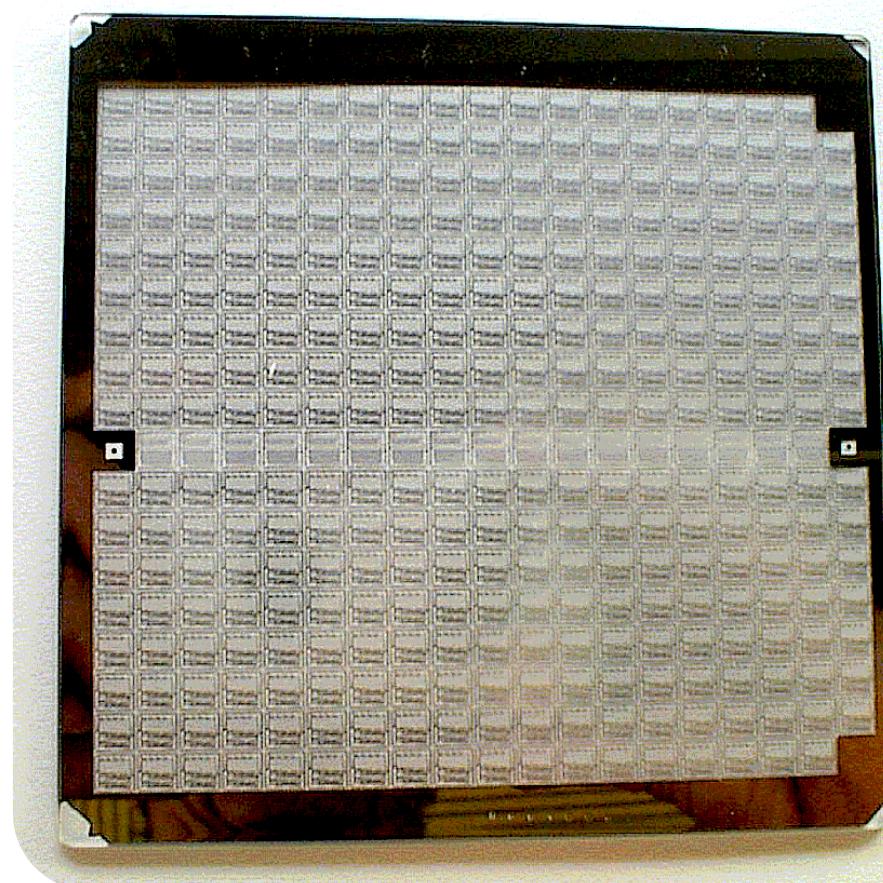
# Patterning: photolithography



# Patterning

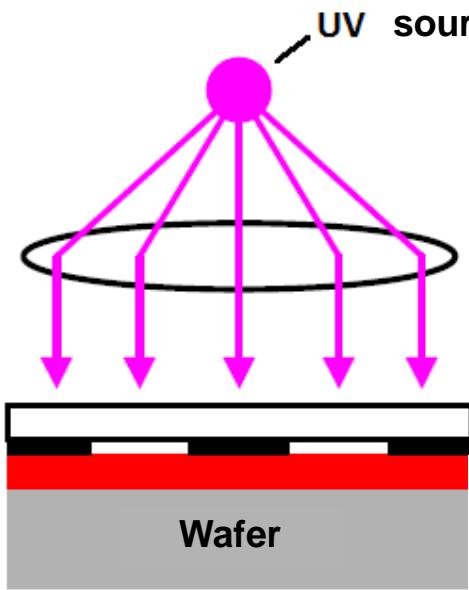
The original pattern is on a so called photo-mask

- made of chromium on glass substrate
  - many times larger than a chip
- Need for high level of accuracy:
- $0.03\mu\text{m}$  over 30cm!
  - $10^{-7}$
- Visible light:
- $\lambda=0.3\text{-}0.6 \mu\text{m}$
  - deep UV needed!

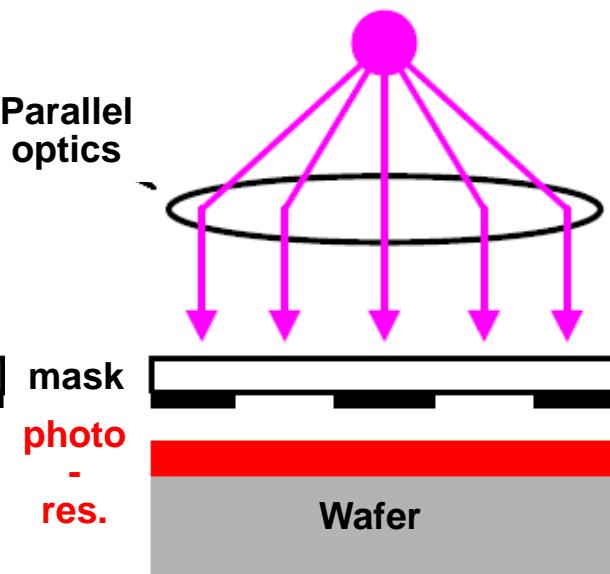


# Mask alignment

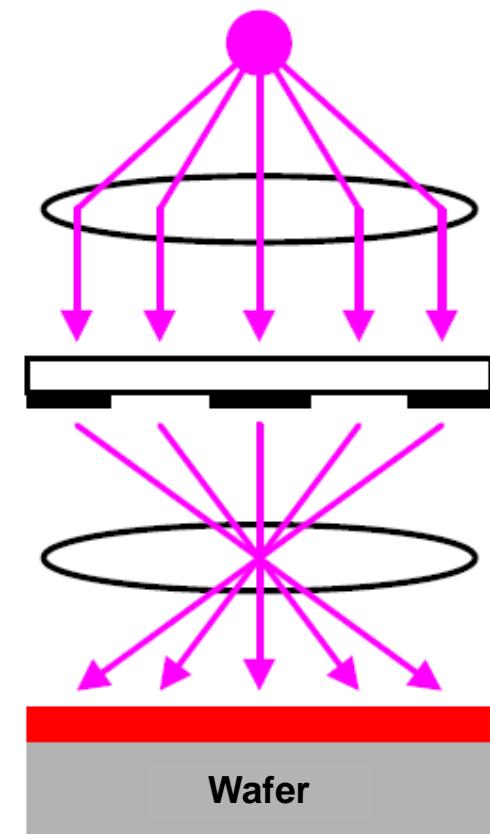
CONTACT



PROXIMITY



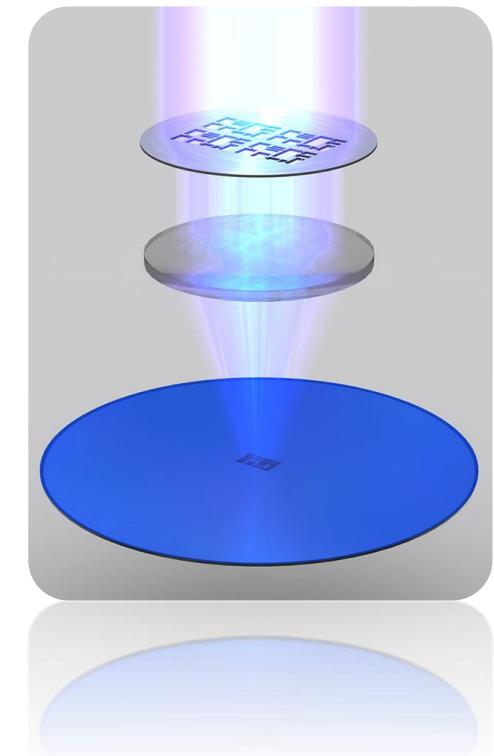
PROJECTION



# Patterning: photolithography

## Major steps:

- ▶ Thermal annealing (evaporation of the absorbed humidity)
- ▶ Adhesion enhancement (chemical procedure)
- ▶ **Photoresist** coating
- ▶ Drying (evaporation of the solvents from the photoresist) – soft bake
- ▶ Mask allignment and exposure
- ▶ Development
- ▶ Hard bake (curing the photoresist, further improvement of adhesion)



# Photoresist

- ▶ 1..2um thickness (10um if it needs to be resistant)
- ▶ Polymer + photoactive component + solvent
- ▶ Solvent determines the viscosity of the mixture
  - Important at the spinning
- ▶ Negative or positive resist: If the photoactive component makes the polymer **easier** or **harder** to desolve during the exposition, then we call the photoresist **positive** or **negative**



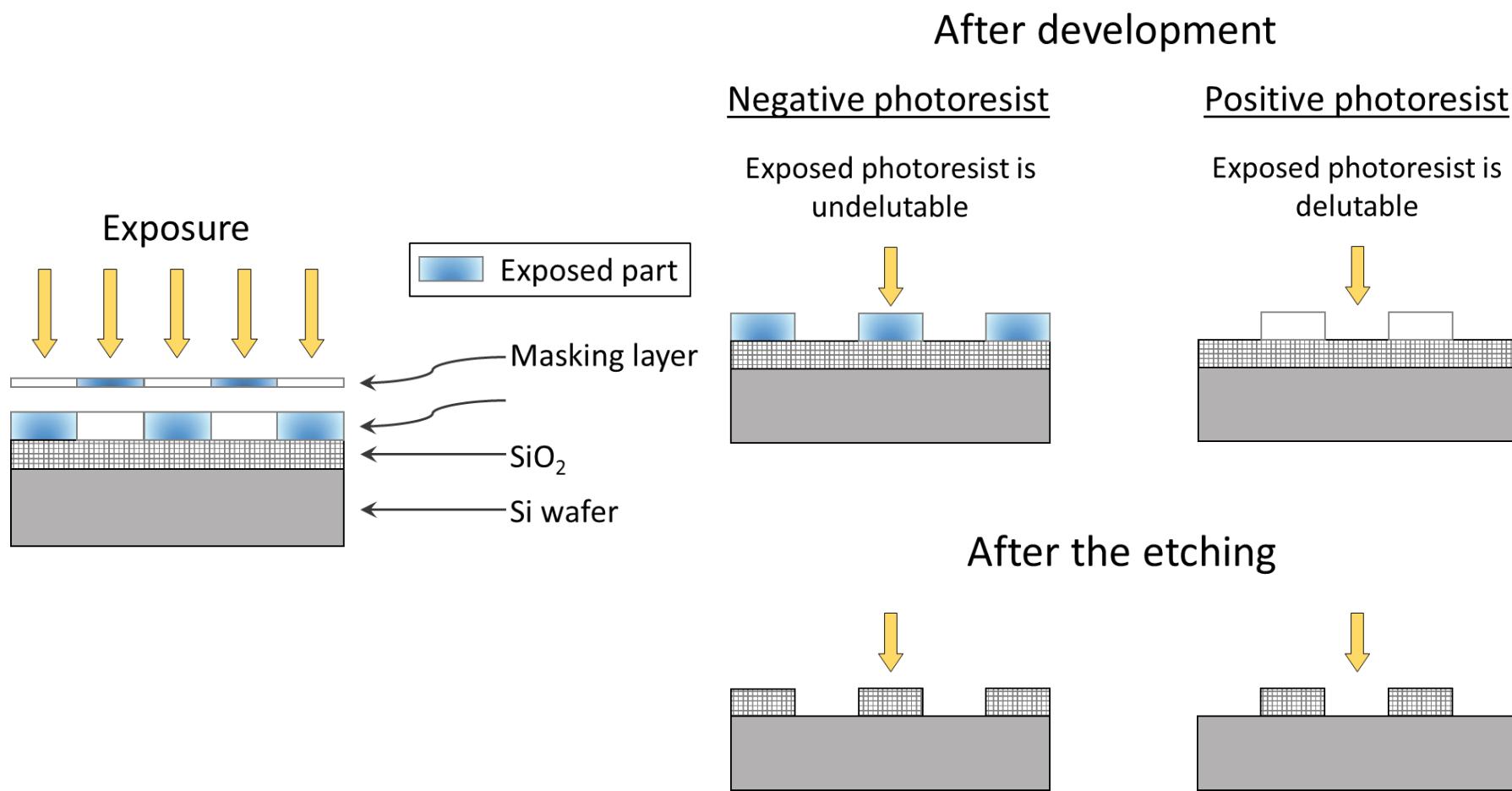
# Photoresist

## Properties:

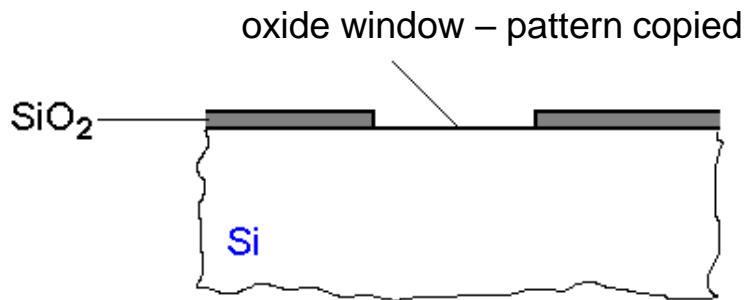
- spectral sensitivity,
- viscosity,
- lightsensitivity (relation of the absorbed photons and the transformed molecules)
- contrast (difference in dissolution velocity between the exposed and the shaded areas)
- resolution



# Photolithography



# The photolithography



E.g. metallization pattern:

1. deposit metal over the entire surface
2. coat with resist
3. UV photography through mask, develop
4. etch off unnecessary metal
5. remove resist

# Modern photolithography

MFS=7nm  
(2019)

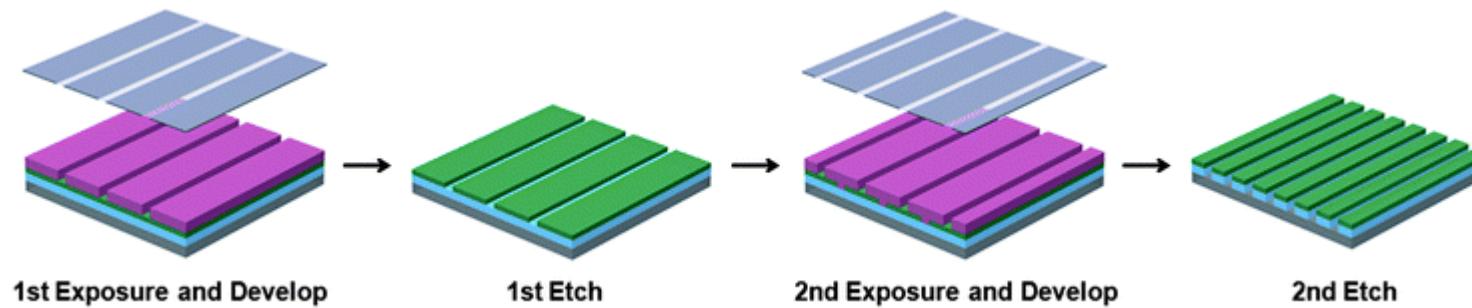
How to go below 193nm resolution?

## ► Immersion lithography

Liquid, usually purified multiple times, distilled water (NA increase)

## ► Multiple patterning

Exposure repeated several times



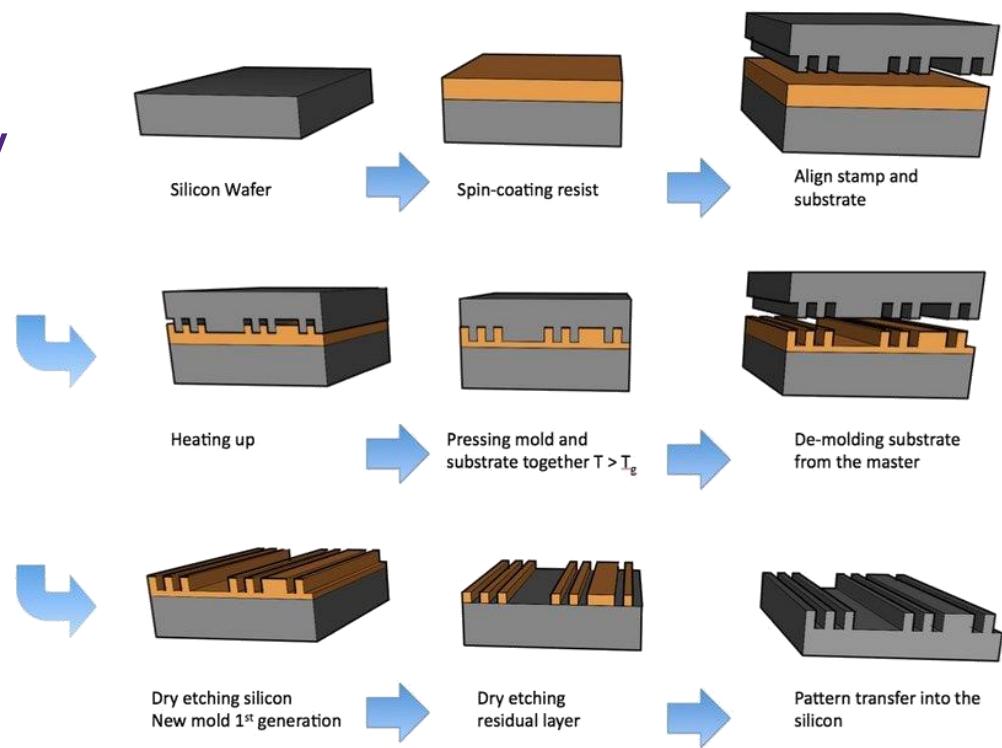
# Modern photolithography

MFS=7nm  
(2019)

How to go below 193nm resolution?

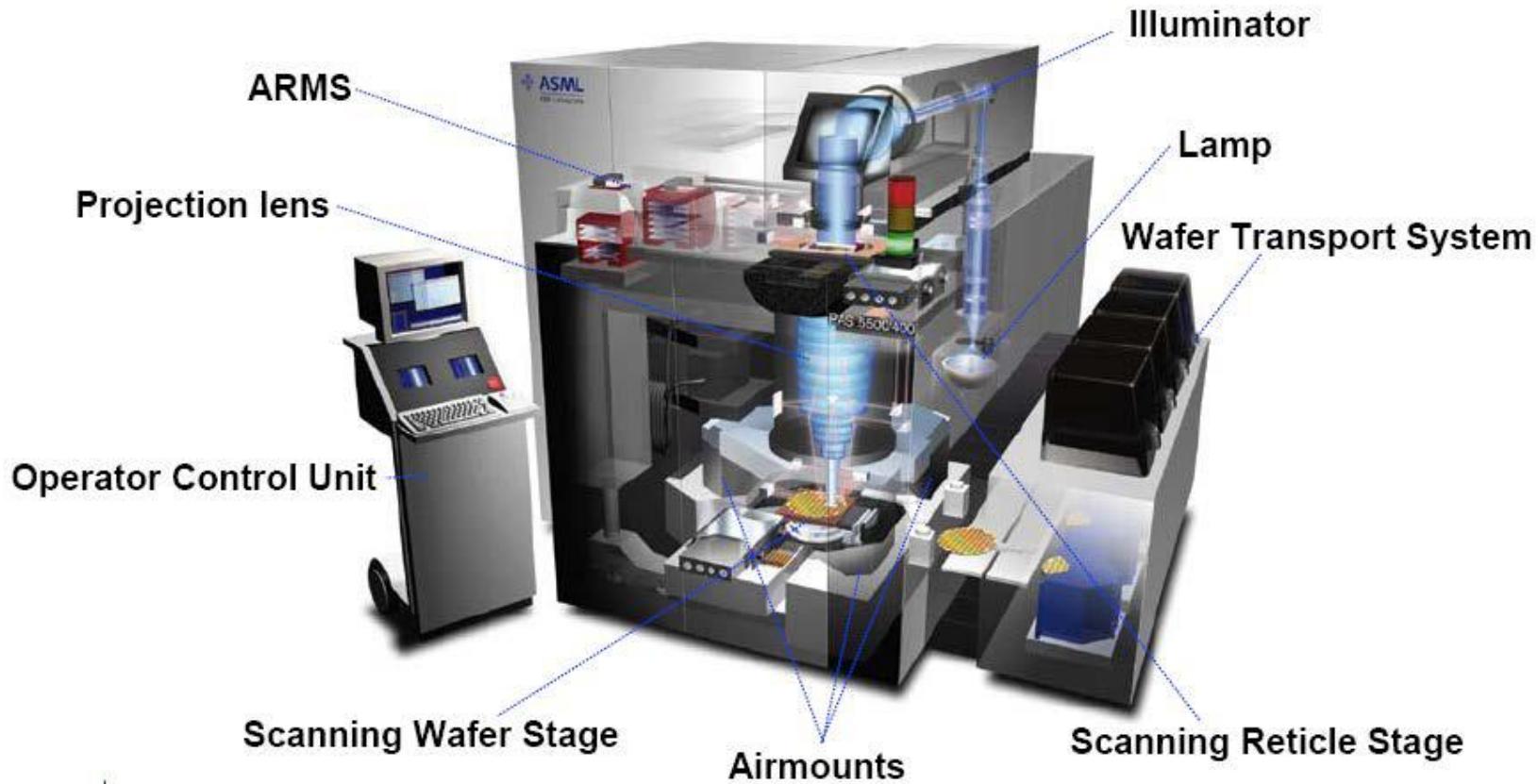
- ▶ Electron-Beam Direct-Write Lithography
  - resolution below 10nm but not on the whole wafer at the same time!
  - Slow!

- ▶ Nanoimprint lithography
  - contact lithography, printing template pressed and dried into a soft polymer (act as a „photoresist”)



# Modern photolithography

## Extreme Ultraviolet (EUV) lithography



ASML TWINSCAN NXE:3300B

# Intel making of a chip

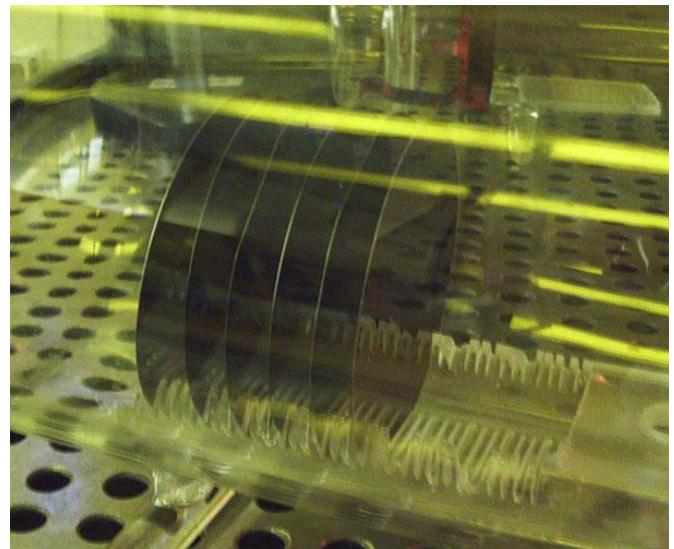


# A simple pMOS process

Process at our cleanroom facility

The process steps

# Steps of a simple pMOS process



## Wafer cleaning

# Steps of a simple pMOS process



## Growth of thick SiO<sub>2</sub> (field oxide)

# Steps of a simple MOS process



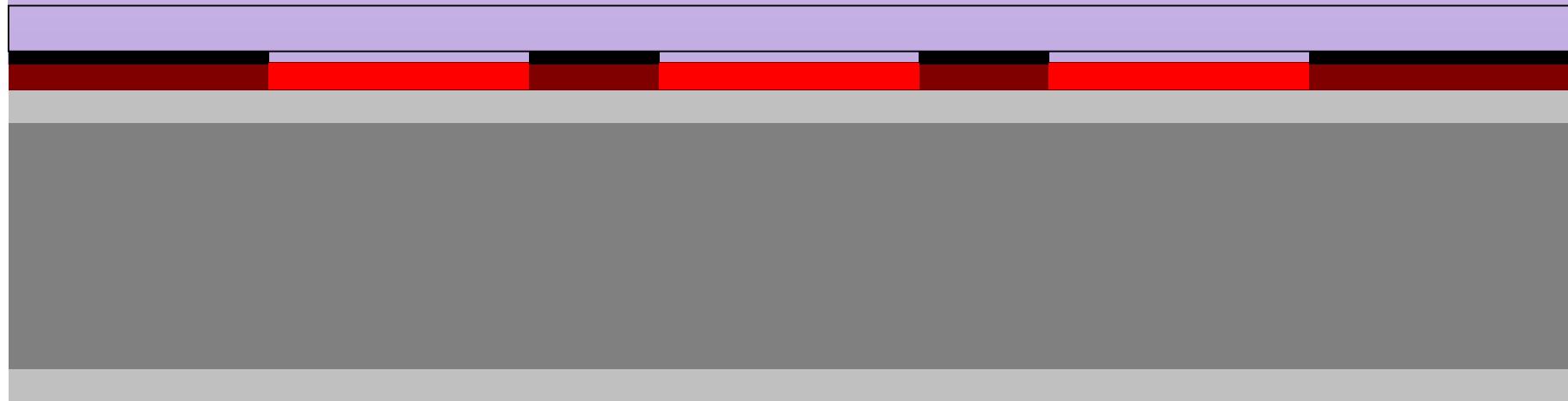
## Photolithography: spin-coating with resist

# Steps of a simple pMOS process



## Photolithography: mask alignment

# Steps of a simple pMOS process



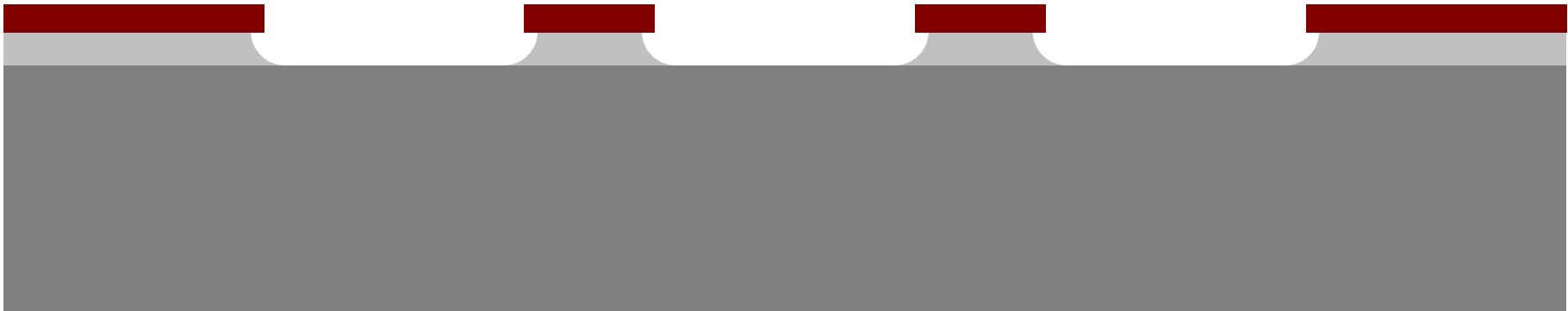
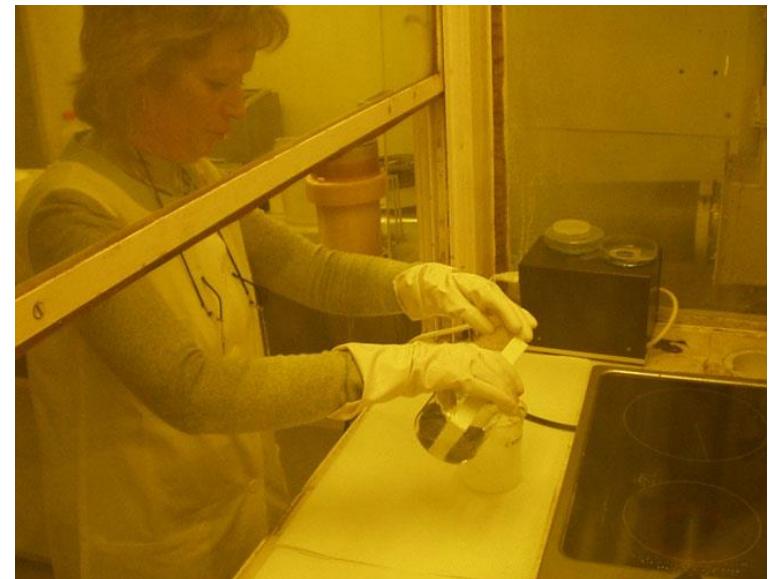
## Photolithography: UV exposure

# Steps of a simple pMOS process



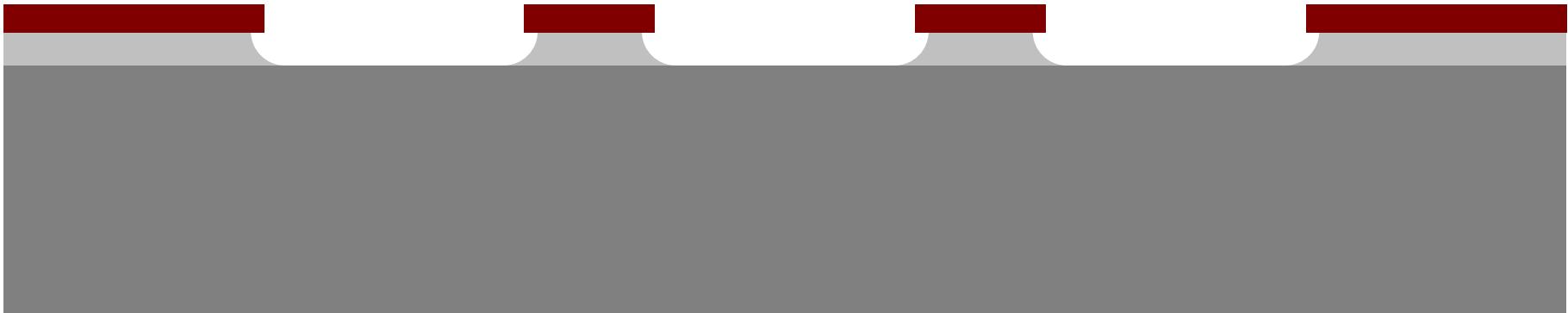
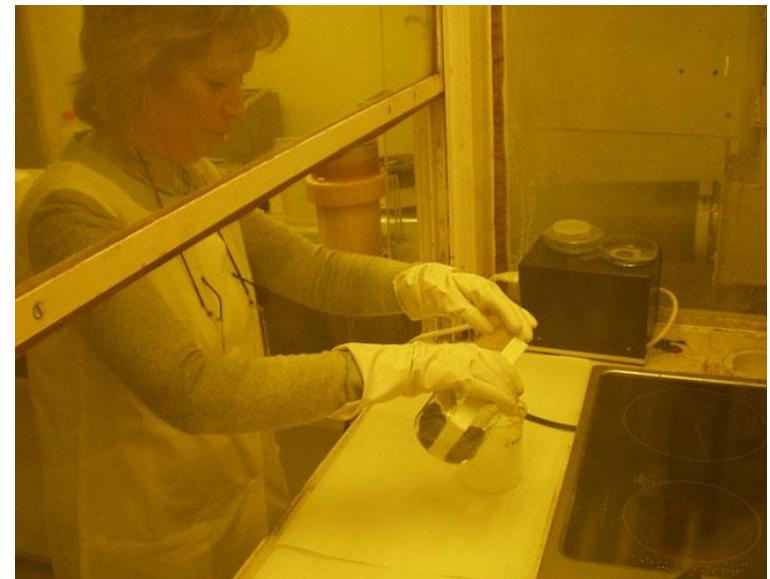
## Photolithography: development

# Steps of a simple pMOS process



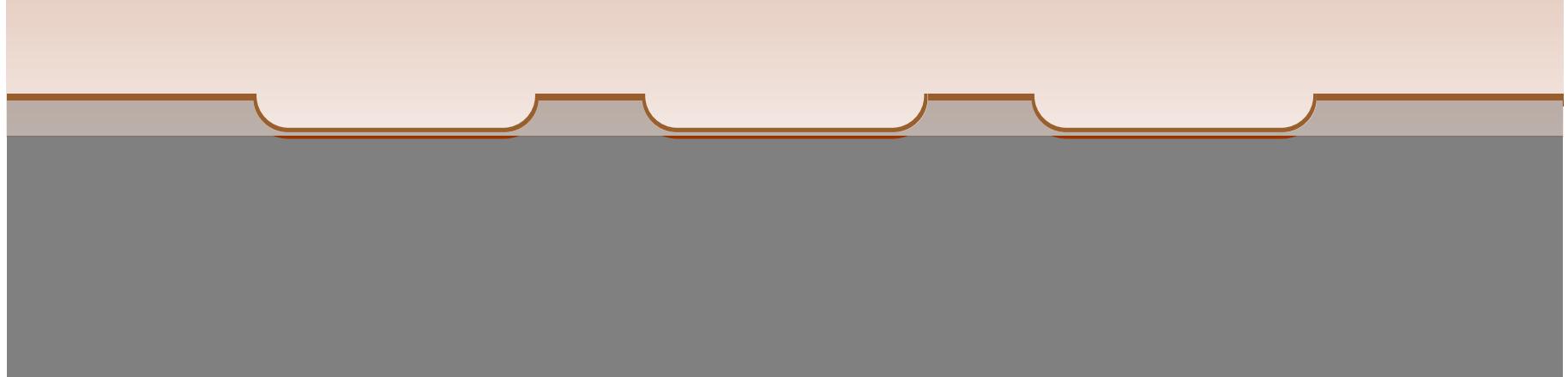
## Patterning: oxide etching

# Steps of a simple pMOS process



Patterning: oxide etching, resist removal

# Steps of a simple pMOS process



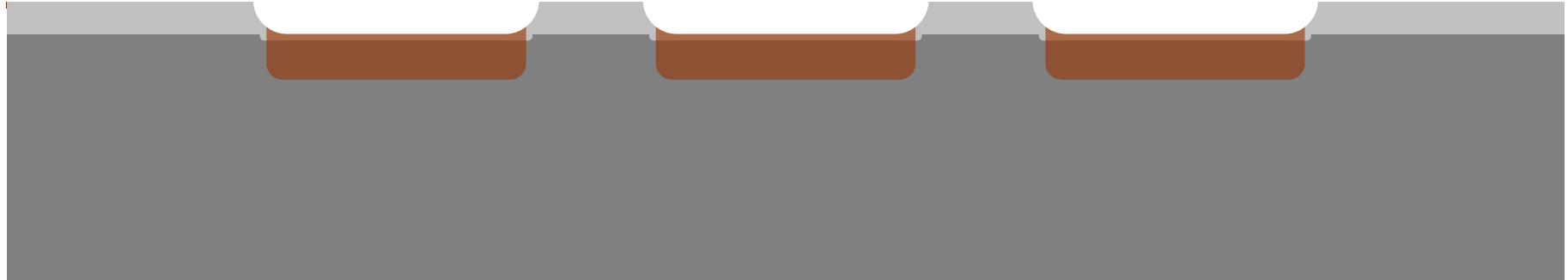
## Diffusion from solid boron (pre-diffusion)

# Steps of a simple pMOS process



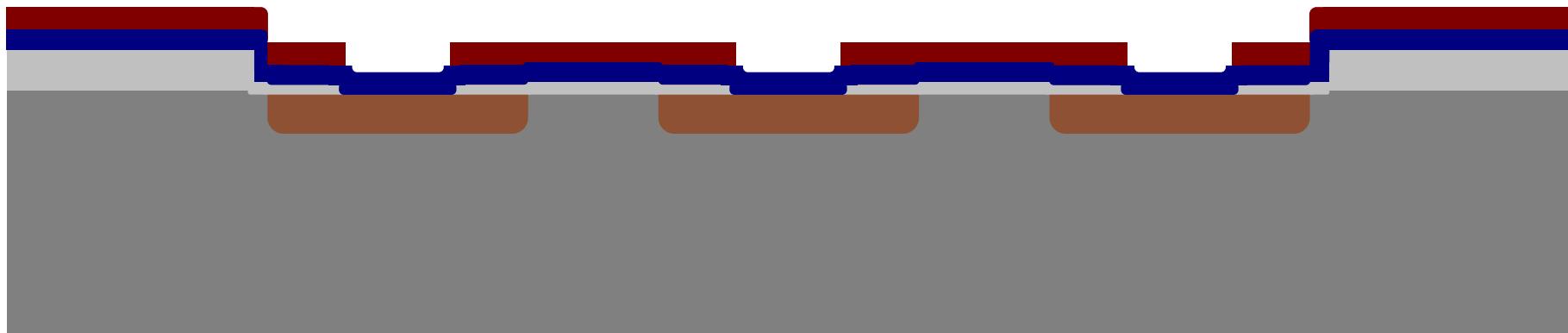
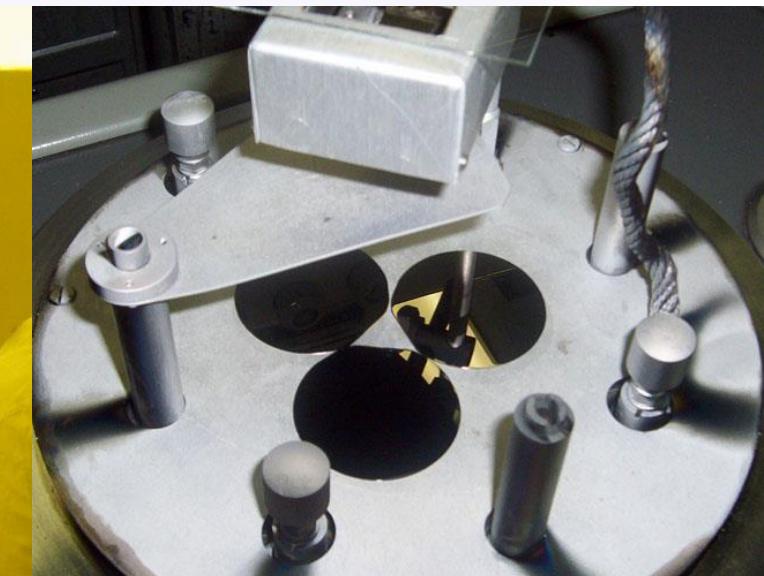
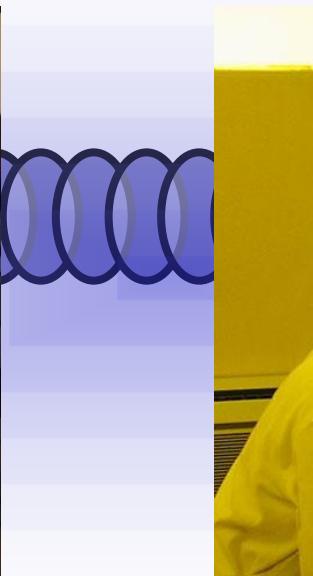
## Removal of boron glass

# Steps of a simple pMOS process



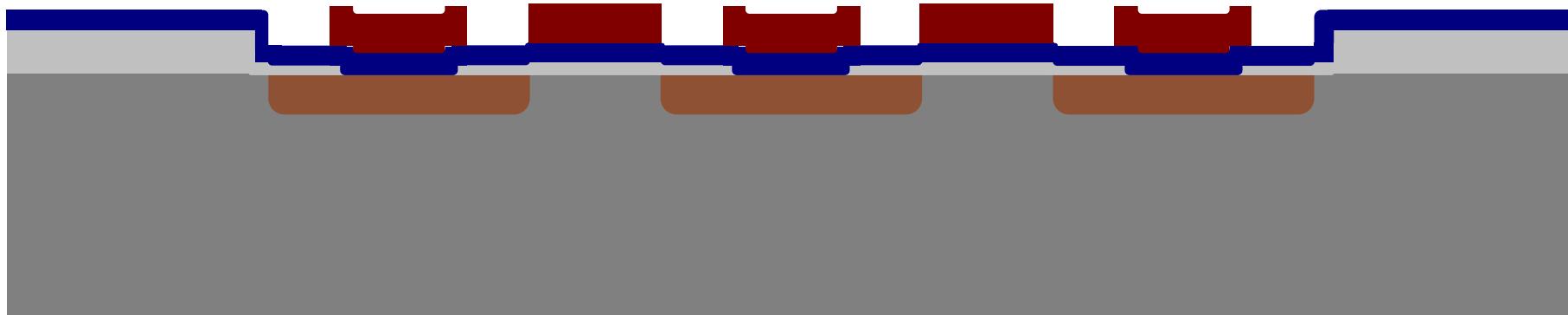
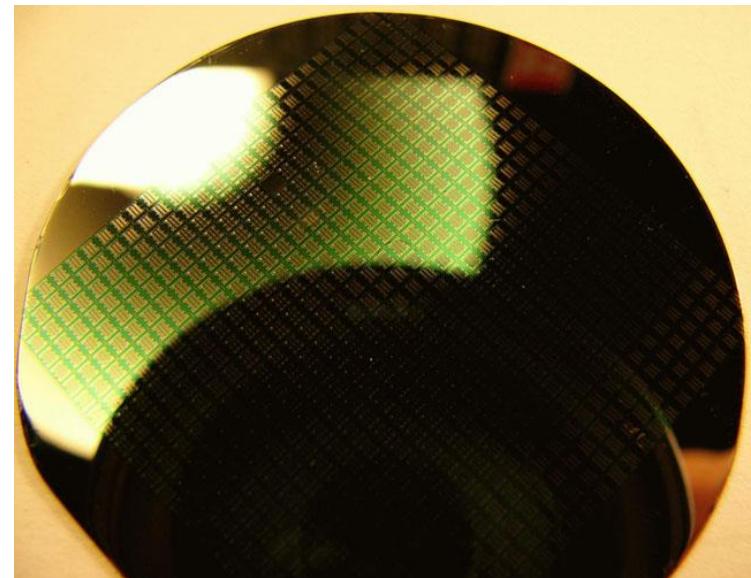
**Boron diffusion, 2<sup>nd</sup> step: driving in (in oxygen)**

# Steps of a simple pMOS process



**Electrostatically controlled plasma polymerization (ECCP) of silicon gate oxide**

# Steps of a simple pMOS process



Wafer lithography - patterning and development

# Steps of a simple pMOS process



## Dicing, bonding

# Pulvis et umbra sumus.

We are but dust and shadow.  
Horace, 65-8 BC, Roman poet

