

FPGA Design Flow

```

graph LR
    1[1. Specifications] --> 2[2. RTL Coding]
    2 --> 3[3. Standard Cell]
    3 --> 4[4. Pre-Layout Timing Analysis Pass?]
    4 --> 5[5. Automatic Placement and Routing]
    5 --> 6[6. Post-Layout Timing Analysis Pass?]
    6 --> 7[7. Logic Verification]
    
    2 -- "VHDL Coding" --> 2
    2 -- "Simulation" --> 2
    
    2 -- "Pass Simulation?" --> 3
    3 -- "Yes" --> 4
    3 -- "No" --> 2
    
    4 -- "Timing Constraints" --> 4
    4 -- "Synthesis" --> 5
    
    5 -- "Placement and routing" --> 5
    5 -- "Timing Analysis" --> 6
    
    6 -- "Verification" --> 6
    6 -- "Timing Analysis" --> 6
  
```

1. HDL Coding

- HDL provide the possibility to implement system with high abstraction levels (Hides complicated implementation details).
- Designer more concerned about the design functionality than the detailed circuit design.

2. Simulation

- For verifying the design functionality (Tool: ModelSim - Mentor Graphics).

3. Synthesis

- Analysing the HDL code and converts it into optimized logic gates (**Netlist**).
- Synthesis is an important tool to improve designers' productivity.
- Input: HDL code, the technology library and constraint file.
- As an output, it will produce the **Netlist** and timing file (*.sdf).
- Synthesis tools for FPGA are: Quartus II (Altera) and ISE (Xilinx).

Ref: Dr. Mahdi Shabany / Sharif University of technology
 Department of Electron Devices - Ali Kareem Abdulrazzaq
 Microelectronics – Digital Design, Lesson 1 21

Digital System Design - Introduction

FPGA Design Flow

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    6 -- "Verification" --> 6
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```

Flag question

What stops the execution of a process?

Select one:

a. The “wait” statement.

b. Either using “wait” statement or no further changes in the values of the sensitivity list.

c. The process is sequentially executed and will not stop executing.

d. No further changes in the values of its sensitivity list.

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ►

Quiz navigation

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19	20	21	22	23	24	25	26	27	28	29	30						

Finish attempt ...

8:27 AM

netlist 537 2/6 Not syncing

```

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    2 -- "VHDL Coding" --> 1
    2 -- "Simulation" --> 2a[Pass Simulation?]
    2a -- No --> 2
    
    3 -- "Timing Constraints" --> 3
    3 --> 4
    
    4 -- "Timing Analysis" --> 4
    4 -- "Yes" --> 5
    4 -- "No" --> 4a[Timing Analysis Pass?]
    4a -- Yes --> 5
    4a -- No --> 4
    
    5 -- "Placement and routing" --> 5
    5 --> 6
    
    6 -- "Timing Analysis" --> 6
    6 -- "Yes" --> 7
    6 -- "No" --> 6a[Timing Analysis Pass?]
    6a -- Yes --> 7
    6a -- No --> 6
    
    7 -- "Verification" --> 7
  
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    4 -- "Timing Analysis" --> 4
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    4 -- "No" --> 4a[Timing Analysis Pass?]
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    4a -- No --> 4
    
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```

Not syncing https://edu.v... English (en)

Home / My courses / Microelectronics - BMEVIEEAB00 2020/21/2 / Midterm and exam / Exam - test questions

Question 28
Not yet answered
Marked out of 1.00
 Flag question

What does the following VHDL statement mean when it appears alone in a line ($B \leq A$)?

Select one:

a. Not correct VHDL statement

b. The value of A will be assigned to B

c. The value of B should be smaller or equal than A

d. The value of B will be assigned to A

[Clear my choice](#)

[Next page](#)

◀ Midterm retake - calculation, essay

Windows 8:27 AM ENG

FPGA Design Flow

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Microelectronics – Digital Design, Lesson 1 21

Digital System Design - Introduction

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```

Not syncing

https://edu.v...

Question 27
Not yet answered
Marked out of 1.00
Flag question

What we call the process of automatically converting the RTL code to netlist

Answer: Synthesis

Next page

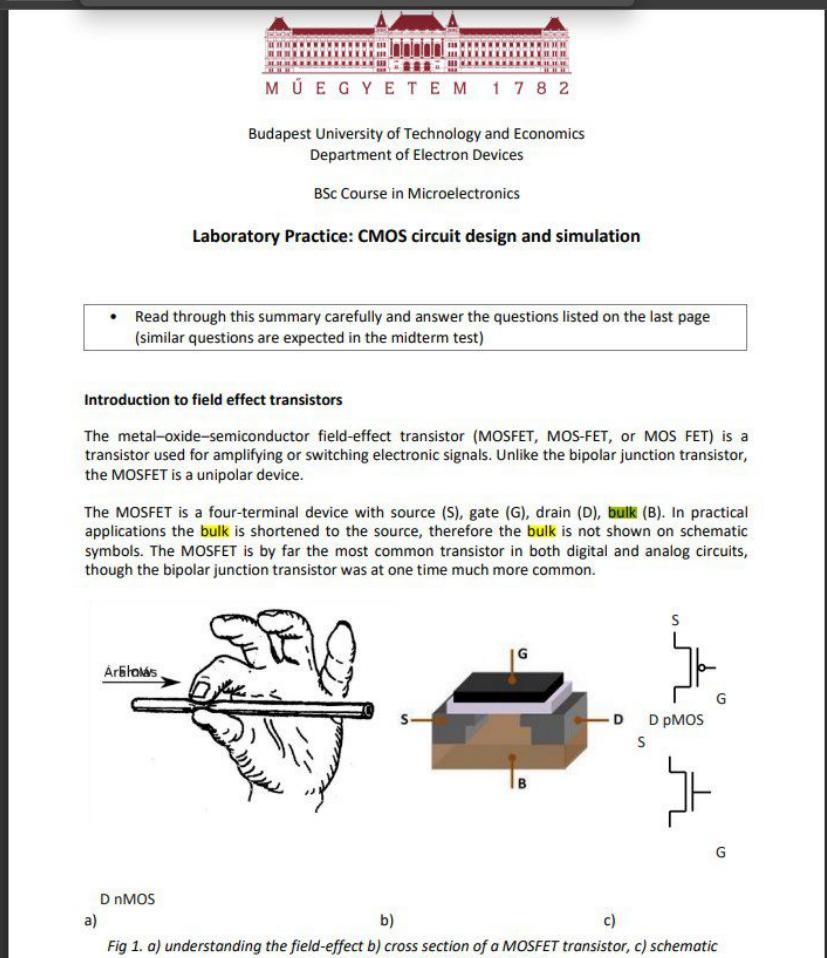
◀ Midterm retake - calculation, essay

Jump to... Exam - calculation, essay, VHDL, schematic ▶

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8:27 AM



Question **26**
Not yet answered
Marked out of 1.00
 Flag question

During the we replace a capacitor with an open circuit and an inductor with a short circuit.

- a. AC analysis
- b. Noise analysis
- c. DC analysis
- d. DC transfer curve analysis

[Clear my choice](#)

► Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ►



Budapest University of Technology and Economics
Department of Electron Devices

BSc Course in Microelectronics

Laboratory Practice: CMOS circuit design and simulation

- Read through this summary carefully and answer the questions listed on the last page (similar questions are expected in the midterm test)

Introduction to field effect transistors

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a transistor used for amplifying or switching electronic signals. Unlike the bipolar junction transistor, the MOSFET is a unipolar device.

The MOSFET is a four-terminal device with source (S), gate (G), drain (D), **bulk** (B). In practical applications the **bulk** is shortened to the source, therefore the **bulk** is not shown on schematic symbols. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common.

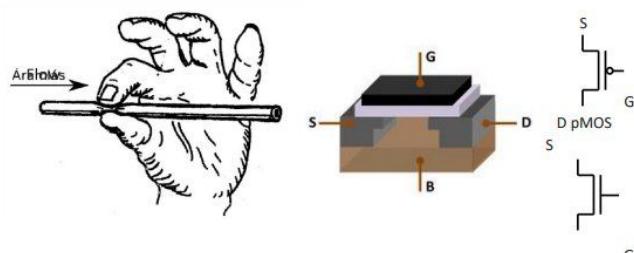


Fig 1. a) understanding the field-effect b) cross section of a MOSFET transistor, c) schematic symbols of pMOS and nMOS transistors

In order to have unique transistors or circuit elements, specified by the manufacturer, we must apply an ... directive with the library path.

a. .INCLUDE

b. .TTRAN

c. .MEAS

d. .MODEL

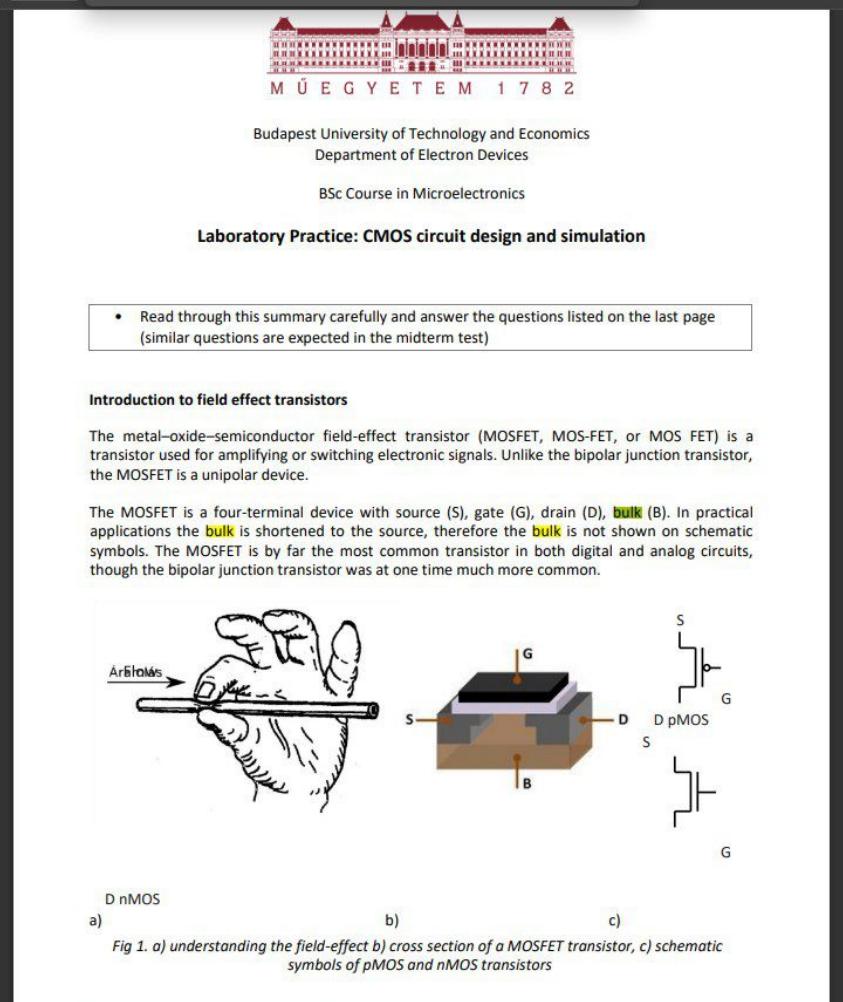
Clear my choice

► Midterm retake - calculation essay

Jump to

Exam - calculation, essay, VHDL, schematic ►

Quiz navigation



Question **24**
Not yet answered
Marked out of 1.00
 Flag question

In statement '.TRAN 1ns 1000NS UIC .OP 40ns' the operating point is calculated at t=...

a. 41 ns.
 b. 40 ns.
 c. 1 ns.
 d. 1000 ns.

[Clear my choice](#)

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[◀ Midterm retake - calculation, essay](#)

Jump to... 

[Exam - calculation, essay, VHDL, schematic ➤](#)



Budapest University of Technology and Economics
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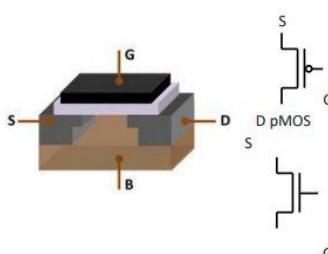
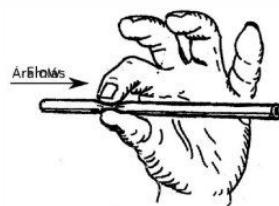


Fig 1. a) understanding the field-effect b) cross section of a MOSFET transistor, c) schematic symbols of pMOS and nMOS transistors

→ ⌂ ⌂ https://edu.v... 🔎 ⭐ ⓘ Not syncing

Flag question

When simulating a CMOS circuitry, it must be ensured that the bulk node of a PMOS is connected to the ...

- a. Drain.
- b. Supply voltage.
- c. GND.
- d. Source.

Clear my choice

► Midterm retake - calculation essay

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Exam - calculation, essay, VHDL, schematic ►

Quiz navigation

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Microelectronics 04.02.2019

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Introduction

Intel fab sites

Fab name	City	Production start year	Process (Wafer, node)
D1X	Hillsboro, Oregon, United States	2013	300 mm, 14/10/7nm
D1D	Hillsboro, Oregon, USA	2003	300 mm, 14/10/7nm
D1C	Hillsboro, Oregon, USA	2001	300 mm, 22/14/10 nm
Fab 12	Chandler, Arizona, USA	1996	300 mm, 65 nm
Fab 32	Chandler, Arizona, USA	2007	300 mm, 14/10 nm
Fab 42	Chandler, Arizona, USA	2020 ¹¹	300 mm, 10/7 nm
Fab 11	Rio Rancho, New Mexico, USA	1993 (Closed)	200 mm, 45/32 nm
Fab 11X	Rio Rancho, New Mexico, USA	1995 upgrade 2020/2021 with 22/14	300 mm, 45/32 nm
Fab 17	Hudson, Massachusetts, USA	1998 (Closed)	200 mm, 130 nm
Fab 24	Leixlip, Ireland	2006	300 mm, 14 nm
Fab 28	Kiryat Gat, Israel	2008	300 mm, 22/10 nm
Fab 68	Dalian, Liaoning, China	2010	300 mm, 65 nm 3D NAND, 3DXPoint ¹²

Microelectronics 04.02.2019

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Flag question

The dicing saw has an air-bearing design, which is needed because:

- a. the vibration of the environment need to be damped.
- b. the temperature is too high.
- c. otherwise the dust particles may contaminate the equipment.
- d. RPM is too high.
- e. the wafer is positioned using vacuum.

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◀ Midterm retake - calculation, essay

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Exam - calculation, essay, VHDL, schematic ▶

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1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

8:23 AM

392 thca

1/7

Because of the temperature gradient heat current of P develops (remember, how the charge carrier concentration gradient causes electric current!).

$$R_{th} = \frac{\Delta T}{P} = \frac{L}{\lambda A} [K/W] \quad (4)$$

where $L[m]$ is the length and $A[m^2]$ is the cross-sectional surface of the brick.

Obviously the temperature of a body cannot change immediately, because the body itself should be filled of heat. The ability of a body to store heat is the heat capacitance. To rise up the temperature of the body by ΔT , a sum of W energy is requested:

$$C_{th} = \frac{W}{\Delta T} = c_v \cdot A \cdot L \quad (5)$$

where $c_v[W/(m^3 * T)]$ is the volumic heat capacity.

The thermal time constant is analogous the time constant of an R-C circuit as follows:

$$\tau_{th} = R_{th} C_{th} \quad (6)$$

The heat which is generated within the chip structure should be transferred to the ambient otherwise the temperature of the chip rises above the safe operation area. It depends on two factors:

- How the heat can be transferred from the chip (more precisely, the place where the heat is generated: the p-n junction) to the chip package (or case): R_{thjc} (read: thermal resistance junction to case).
- How the heat can be transferred towards from the case to the ambient (it depends on the size of the heatsink, convective heat transfer etc.): R_{thca} (read: thermal resistance case to ambient)

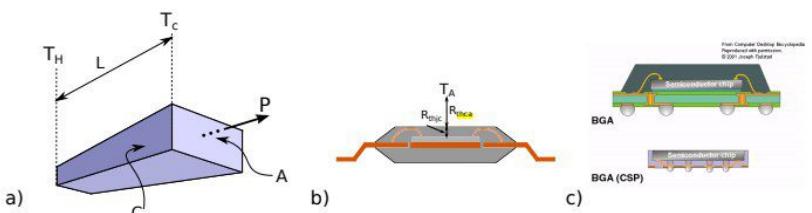


Figure 1: a) Understanding thermal resistance b) DIP package cross section and R_{thca} , R_{thjc} values c) modern BGA and BGA flip chip cross sections

R_{thjc} and R_{thca} are shown on the device's datasheets. Let's consider a device dissipating $100mW$ in DIP package, having $R_{thjc} = 37K/W$ and $R_{thca} = 70K/W$. What will be the junction temperature, if the ambient temperature is $25^\circ C$?

$$T_j = T_{amb} + P(R_{thjc} + R_{thca}) = 25 + 10.7 = 35.7^\circ C \quad (7)$$

Question 20

Not yet answered

Marked out of 1.00

Flag question

What does the value of R_{thca} thermal resistance show?

- a. The thermal resistance between the active (dissipating) zone and the inner edge of the top of the package.
- b. The thermal resistance between the active (dissipating) zone and the ambient.
- c. The thermal resistance between the top of the package and the ambient.
- d. The thermal resistance between the active (dissipating) zone and the PCB board.

Clear my choice

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶



lumenous flux si

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Результатов: примерно 1 900 000 (0,53 сек.)

Показаны результаты по запросу **luminous flux si**Искать вместо этого [lumenous flux si](#)[https://en.wikipedia.org › wiki › Перевести эту страницу](https://en.wikipedia.org/wiki/Luminous_flux)

Luminous flux - Wikipedia

The SI unit of **luminous flux** is the lumen (lm). Until 19 May 2019, one lumen was defined as the luminous flux of light produced by a light source that emits one ...

[Units](#) · [Context](#) · [Relationship to...](#)[https://en.wikipedia.org › wiki › Перевести эту страницу](https://en.wikipedia.org/wiki/SI_unit_of_luminous_intensity)

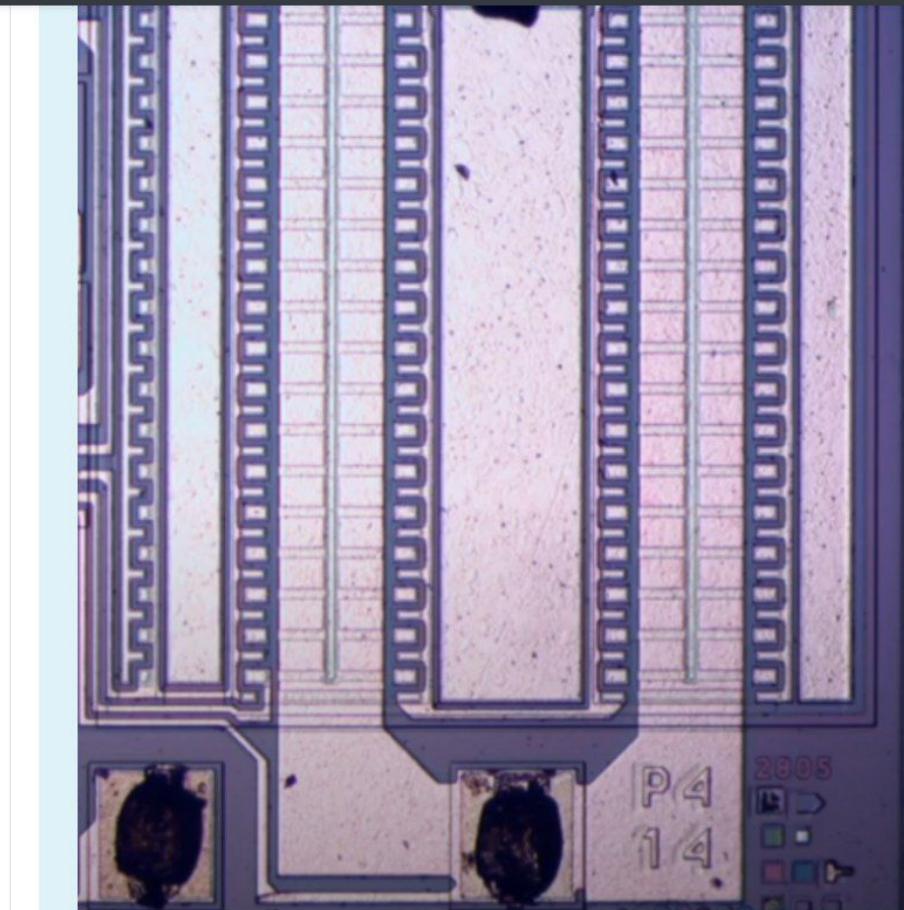
SI unit of luminous intensity - Wikipedia

In photometry, **luminous intensity** is a measure of the wavelength-weighted power emitted per unit solid angle by a light source in a particular direction per unit solid angle, based on ...

[Relationship to other...](#) · [Units](#) · [Usage](#)[https://www.sciencedirect.com › ... › Перевести эту страницу](https://www.sciencedirect.com/science/article/pii/S0031912018303002)

Luminous Flux - an overview | ScienceDirect Topics

The SI unit of **luminous flux** is the lumen (lm). One lumen is defined as the luminous flux of light produced by a light source that emits 1 cd of **luminous intensity** over a solid angle of 1 steradian.



Select one or more:

-
- a. diode

lumenous flux si

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Искать вместо этого [lumenous flux si](#)

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[Units](#) · [Context](#) · [Relationship to...](#)

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SI unit of luminous intensity - - Wikipedia

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[Relationship to other...](#) · [Units](#) · [Usage](#)

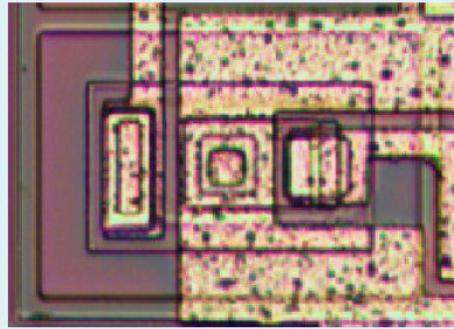
<https://www.sciencedirect.com/science/topics/luminous-flux-an-overview>

Luminous Flux - an overview | ScienceDirect Topics

The SI unit of **luminous flux** is the lumen (lm). One lumen is defined as the luminous flux of light produced by a light source that emits 1 cd of **luminous intensity** over

Flag question

What type of electronic component can you see on the image?



Select one or more:

a. resistor

b. transistor

c. capacitor

d. diode

Next page

◀ Midterm retake - calculation, essay

Jump to

lumenous flux si

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Результатов: примерно 1 900 000 (0,53 сек.)

Показаны результаты по запросу **luminous flux si**

Искать вместо этого [lumenous flux si](#)

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[Units](#) · [Context](#) · [Relationship to...](#)

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SI unit of luminous intensity - Wikipedia

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Not syncing

Not yet answered

Marked out of 1.00

Flag question

Question 17

What is the wavelength of photolithography in the labs of DED?

a. 465 nm

b. 1 μm

c. 13.5 nm

d. 50 nm

e. 0.1 μm

Clear my choice

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶

Not syncing

led efficiency and temperature

Все Картинки Новости Видео Покупки Ещё Настройки Инструменты

результатов: примерно 382 000 000 (0,70 сек.)

оказаны результаты по запросу **led efficiency and temperature**
скажи вместо этого [led efficiency and temperatre](#)

Light Emitting Diode (**LED**) has the advantages over the traditional lamps in the future. ... When operation **temperature** increases from 327 K to 380 K, the light **efficiency** of LED decreases 20%. The **temperature** rising, the radiation at the potential well decreases, so as to decrease the luminous **efficiency**.

<https://www.researchgate.net> › ... › Materials Science › LED

[Effect of temperature and current on LED luminous efficiency](#)

О выделенных описаниях Оставить отзыв

Похожие запросы

- What is the effect of temperature on LED output?
- How hot is too hot for LED?
- In what factors does the efficiency of LED depend?

Flag question

The efficiency of an LED **decreases** as the temperature of the PN junction decreases.

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◀ Midterm retake - calculation, essay

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Exam - calculation, essay, VHDL, schematic ▶

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Finish attempt ...

Time left 0:11:31

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265 p channel 1/5

The MOSFETs

Field effect transistors 3

- Symbols:

a.) b.) c.)

Microelectronics 06-04-2020 5

The MOSFETs

MOSFETs

- More realistic cross-sectional view of enhancement mode MOSFETs:

Not syncing ...

https://edu.v...

English (en) ...

Question 14
Not yet answered
Marked out of 1.00
Flag question

There are _____ different regions in the characteristic of a **MOS inverter**.

Select one:

a. 3 (low, high, indefinite)
 b. 2 (low, high)
 c. 5 (low, high, minimum, maximum, indefinite)
 d. 4 (low-maximum, high-minimum, threshold, indefinite)

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◀ Midterm retake - calculation, essay

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Exam - calculation, essay, VHDL, schematic ▶

Quiz navigation

File | C:/Users/rasi... Not syncing ...

output| 20/49

- Schematically, when the transistor is opened, it can be substituted by a short. When the transistor is closed, it can be substituted by an open.

Digital circuits are commonly built of using both pMOS and nMOS transistors. This type of digital circuits is called CMOS (means complementary MOS). A CMOS circuit is consists a pMOS circuit block connected to the power supply (V_{dd}) and an nMOS circuit block connected to the ground (V_{ss}). Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

CMOS inverter

The simplest digital circuit is the inverter. An inverter has an input and an output. The output is always the opposite value of the input. The figure above describes the way of operation. When the input is '1' (gate voltages are e.g. 5 V) the pMOS closes and the nMOS opens, therefore the output is shorted to the ground. The output voltage equals to the ground potential, the digital value is '0'. If the input is '0' (gate voltages are 0 V) the pMOS opens and the nMOS closes. The output is shorted to the power supply, therefore the output voltage refers to '1' (e.g. 5 V).

IN	OUT
A	NOT A
1	0
0	1

A —————— Y

Fig 2. The inverter operation

Questions

- What MOSFET stands for? What is the difference between nMOS and pMOS? How the terminals are called?

Not syncing ...

https://edu.v...

English (en)

Question 12
Not yet answered
Marked out of 1.00
Flag question

When both nMOS and pMOS transistors of a CMOS logic gates are ON, the output is:

Select one:

a. 0 or ground or LOW state.
 b. 1 or V_{dd} or HIGH state.
 c. cannot be identified due to mutual conduction.
 d. None of the above.

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶

Quiz navigation

368 consumption 11/17 ⌂ ⌃ ⌁ ⌂ ⌃ 18

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CMOS

Power consumption of CMOS inv.:

- Mutual conduction ("short power"):**
 - During a certain period of the rise of the input signal both transistors are "on" if $V_{Tn} < U_{IN} < V_{DD} - V_{Tp}$, this is called mutual conduction

$I_{MAX} = K(V_{DD} / 2 - V_T)^2$

charge flowing through: $\Delta Q = b t_{UD} I_{MAX}$, where t_{UD} is the time while current is flowing, b is a constant depending on the signal shape.
 $b \approx 0.1-0.2$

$$P = f \Delta Q V_{DD} = f V_{DD} b t_{UD} K (V_{DD} / 2 - V_T)^2$$

$$P \sim f V_{DD}^3$$

Microelectronics | 27-04-2020 19

CMOS

Power consumption of CMOS inv.:

- Charge pumping:**
 - At switching the C_L load capacitance is charged to VDD through the p-channel device when the output changes to 1, later, when switching the output to 0, it is discharged towards GND through the n-channel device.

Not syncing

Question 11
Not yet answered
Marked out of 1.00
[Flag question](#)

Regarding the power consumption of CMOS circuitry, it is known that ____.

Select one:

a. the consumption regarding the mutual conduction is proportional to the frequency and the third power of the supply voltage

b. its static consumption is significant

c. the consumption regarding the charge pumping is proportional to the square of the frequency and the supply voltage

d. its dynamic consumption is insignificant

[Clear my choice](#)

[Next page](#)

[◀ Midterm retake - calculation, essay](#)

[Jump to...](#)

File | C:/Users/rasi... Not syncing ...

265 p channel 1/5

The MOSFETs

Field effect transistors 3

- Symbols:

The diagram shows the following symbols:

- JFET**: A symbol with a single arrow pointing from Gate (G) to Source (S), with Drain (D) at the top.
- MOSFET n channel enhancement mode**: A symbol with a single arrow pointing from Gate (G) to Source (S), with Drain (D) at the top. The text "n channel enhancement mode" is written below it.
- MOSFET p channel enhancement mode**: A symbol with a single arrow pointing from Gate (G) to Source (S), with Drain (D) at the top. The text "p channel enhancement mode" is written below it.
- MOSFET depletion mode**: A symbol with a single arrow pointing from Gate (G) to Source (S), with Drain (D) at the top. The text "depletion mode" is written below it.
- p channel**: A symbol showing a vertical line with a small arrow pointing down, labeled "p channel".
- a.)**, **b.)**, **c.)**: Three additional symbols for n-channel depletion-mode MOSFETs, showing different connection schemes for the gate.

Microelectronics 06-04-2020 5

The MOSFETs

MOSFETs

- More realistic cross-sectional view of enhancement mode MOSFETs:

The diagram illustrates a cross-section of an enhancement-mode MOSFET. It shows the following layers from top to bottom:

- Gate Oxide
- Polysilicon Gate
- Field Oxide
- GATE (labeled in red)
- N_A (labeled in green)
- P-Type (labeled in blue)
- Source / Drain Regions (labeled in green)
- Field Oxide

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Question 11
Not yet answered
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 Flag question

Regarding the power consumption of CMOS circuitry, it is known that _____.
Select one:

a. the consumption regarding the mutual conduction is proportional to the frequency and the third power of the supply voltage

b. its static consumption is significant

c. the consumption regarding the charge pumping is proportional to the square of the frequency and the supply voltage

d. its dynamic consumption is insignificant

Next page

◀ Midterm retake - calculation, essay

8:09 AM

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265 p channel 1/5

The MOSFETs

Field effect transistors 3

- Symbols:

The diagram shows symbols for JFETs and MOSFETs in different modes:

- JFET:** n channel symbol with Gate (G), Drain (D), and Source (S).
- MOSFET:**
 - n channel enhancement mode:** Gate (G) to Source (S), Drain (D) to drain terminal.
 - p channel enhancement mode:** Gate (G) to drain terminal, Drain (D) to Source (S).
 - n channel depletion mode:** Gate (G) to Source (S), Drain (D) to drain terminal.
 - p channel depletion mode:** Gate (G) to drain terminal, Drain (D) to Source (S).
 - MOSFET:** p channel symbol with Gate (G), Drain (D), and Source (S).
 - MOSFET:** n channel symbol with Gate (G), Drain (D), and Source (S).

a.) b.) c.)

Microelectronics 06-04-2020 5

The MOSFETs

MOSFETs

- More realistic cross-sectional view of enhancement mode MOSFETs:

The diagram illustrates a cross-section of an enhancement mode MOSFET structure:

- Gate oxide layer on top of the polysilicon gate.
- Polysilicon Gate.
- Field Oxide regions.
- P-Type substrate.
- N_A (Source/Drain Regions) formed by N_A implants.
- Field Oxide regions separating the source and drain regions.

Not syncing

https://edu.v...

Flag question

It is a(n)...

Select one:

a. n channel JFET

b. n channel depletion mode MOSFET

c. p channel JFET

d. p channel enhancement mode MOSFET

Next page

◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶

8:09 AM

reverse region 1/3

Main features

The graph shows Current [mA] on the y-axis (0 to 100) and Voltage [V] on the x-axis (-3 to 1). A red arrow points to the reverse region where current is low ($I \sim 10^{-12} \text{ A/mm}^2$ at $T=300 \text{ K}$). A blue arrow points to the forward region where current increases exponentially ($I \sim \exp(V/V_T)$). A vertical dashed line marks the threshold voltage $V_F \approx 0.7 \text{ V}$.

Rectifies

The characteristic:
 $I = f(V)$

Reverse region
 $I \sim 10^{-12} \text{ A/mm}^2$
 $(\text{Si}, T=300 \text{ K})$

Forward region
 $I \sim \exp(V/V_T)$

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Question 7
 Not yet answered
 Marked out of 1.00
[Flag question](#)

Which region/mode does n channel enhancement MOSFET operate if gate-source voltage is 1.2 V, drain-source voltage is 0.9 V, threshold voltage is 0.4 V?

Select one:

a. forward mode

b. triode region

c. reverse mode

d. saturation region

[Clear my choice](#)

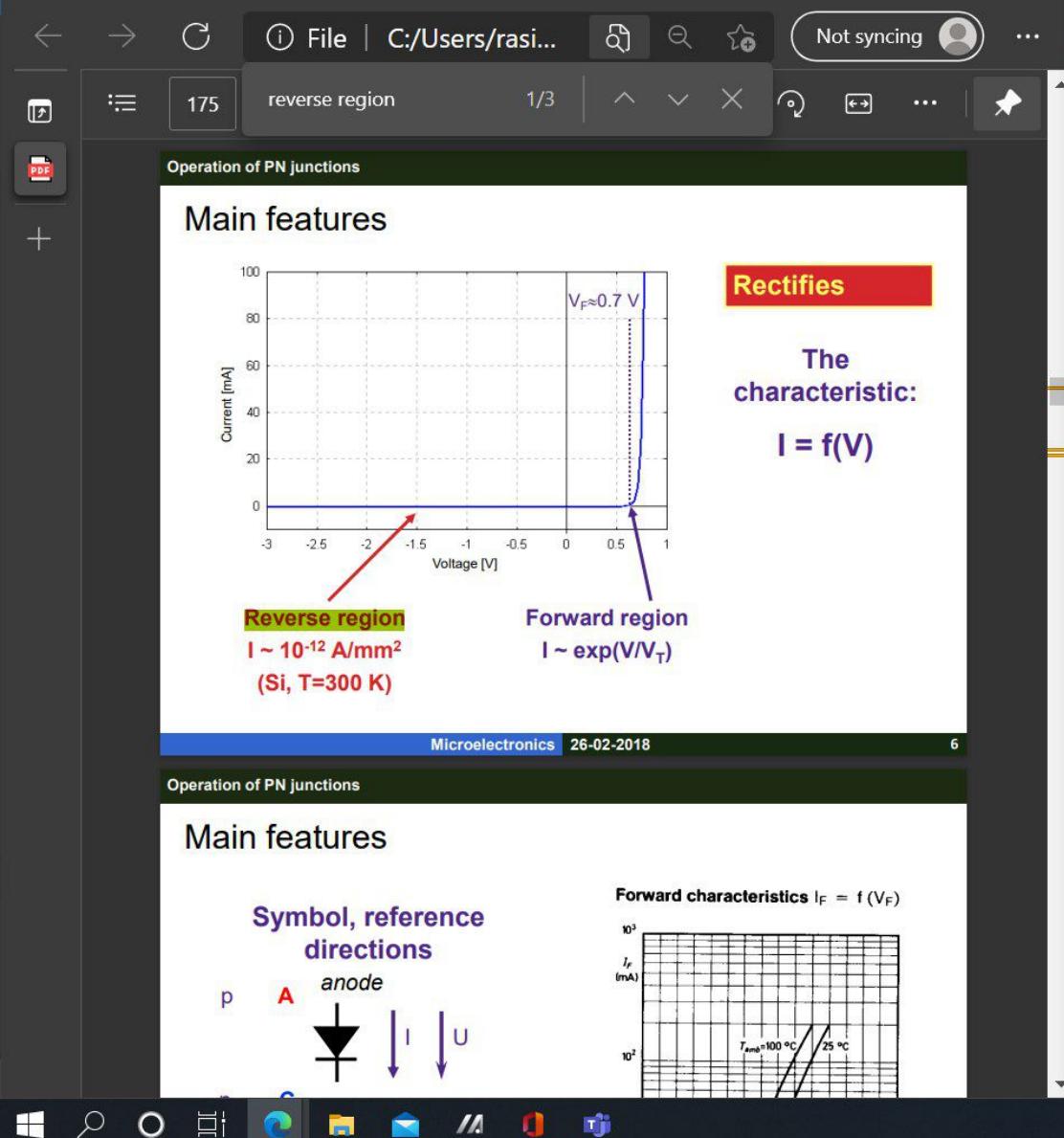
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◀ Midterm retake - calculation, essay

Jump to...

Exam - calculation, essay, VHDL, schematic ▶

8:08 AM



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Question 7
 Not yet answered
 Marked out of 1.00
 Flag question

Which region/mode does n channel enhancement MOSFET operate if gate-source voltage is 1.2 V, drain-source voltage is 0.9 V, threshold voltage is 0.4 V?

Select one:

- a. forward mode
- b. triode region
- c. reverse mode
- d. saturation region

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◀ Midterm retake - calculation, essay

Jump to...

8:08 AM

Exam - test questions (page 5 of 10) + Mi Course BMEV autom Advan +

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Finish attempt ... Time left 0:25:31

Question 5 Not yet answered Marked out of 1.00 Flag question

The increasing dissipation in a chip gives strong limitations

Select one:

- a. memory usage
- b. the clock frequency
- c. die size
- d. number of transistors per chip

Clear my choice

Next page

Midterm retake - Exam - calculation

dissipation 1/10 Microelect... 67 / 584 56% + ⚡ Сервисы Авиабилеты Яндекс Список для чтения

Microelect... 67 / 584 56% + ⚡ Сервисы Авиабилеты Яндекс Список для чтения

Multiple core architectures

Adapted from ARC 2010 presentation by Dr. Ram Krishnamurthy, Intel Research

Microelectronics 04.02.2019 66

Introduction

Increase in dissipation density

- Power consumption growth faster than the die size

CPU Architecture Today Heat becoming unmanageable problem

Dissipation density limits

Power Density (W/cm²)

Sun's Surface
Rocket Nozzle
Nuclear Reactor
Hot Plate
Cooling!!!

4004 8008 8086 8085 286 386

10,000 1,000 100 10

10:34 ENG 28.05.2021 2

Exam - test questions (page 7 of 10) +

← → C 🔒 edu.vik.bme.hu/mod/quiz/attemp... Q ☆ G Y B D ⋮

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Finish attempt ...

Time left 0:23:44

Question 7

Not yet answered

Marked out of 1.00

Flag question

During the reverse operation of the pn junction:

Select one:

- a. the current of the minority charge carriers is insignificant in the depleted region
- b. the potential step between the p and n side of junction decreases
- c. majority carriers injected to the other side by drifting
- d. the drift current becomes dominant

Clear my choice

Next page

◀ Midterm
retake -
calculation,

Jump to... ▾

Exam -
calculation,
essay, VHDL,
simulation

reverse operation

Narrow base structure

- The thickness of p region is smaller than the diffusion length → only a part of the e-s recombination
- No difference in the (current) conduction!
- Electric field moves the holes from the contact to the PN junction
 - Small part of the forward voltage is dropped here*

Microelectronics 26-02-2018 5

Operation of PN junctions

Reverse operation of the diode

- Effect of reverse (negative) U
 - Potential step increases so as the electric field in the space charge region
 - Current balance disrupted: drift current became dominant, e⁻ drift from the p to the n region
- Drift of the minority carriers on both sides towards the other region!
- e⁻ concentration decreases in the p region near the junction

28 мая 2021 г. пятница

Exam - test questions (page 8 of 8) +

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Finish attempt ...

Time left 0:23:31

Question 8
Not yet answered
Marked out of 1.00
Flag question

With the vapor deposition in semiconductors
Select one:

- a. dopants move in the substrate as a consequence of concentration gradient
- b. metal layer is deposited in the top of mask layer
- c. the substrate surface is bombed with accelerated dopants
- d. a new atomic thin layer is formed on the top of the substrate

Next page

Exam - test questions (page 9 of 10) +

← → C 🔍 edu.vik.bme.hu/mod/quiz/attemp... Q ☆ G Y Яндекс | Список для чтения

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Finish attempt ...

Time left 0:22:48

Question 9
Not yet answered
Marked out of 1.00
Flag question

How does the reverse mode operation of the pn junction react to temperature increase?

Select one:

a. the reverse current decreases by ~7-10%/K

b. the reverse voltage decreases by ~7-10%/K

c. the reverse characteristics are temperature independent

d. the reverse voltage increases by ~2mV/K

Next page

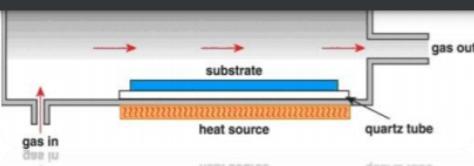
◀ Midterm
retake -
calculation,
essay

Jump to... ▾

Exam -
calculation,
essay, VHDL,
schematic ►

vapor deposition 3/3

Microelect... 89 / 584 | - 56% + | : Список для чтения

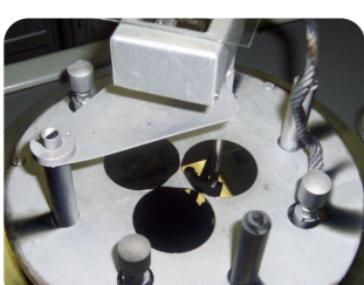
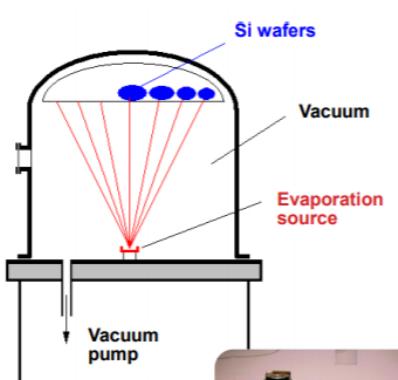


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Vapor deposition

Free mean path > size of the chamber

Metallization
~0.1-0.5 μm



Quiz navigation

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Finish attempt ...

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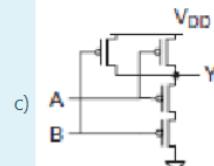
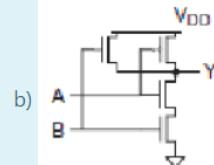
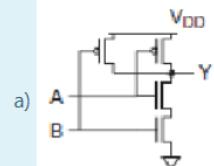
Question 12

Not yet answered

Marked out of 1.00

Flag question

The CMOS logic circuit for NAND gate is:



d) None of the above.

Select one:

a. Two nMOS in series connection and two pMOS in parallel connection



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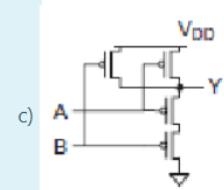
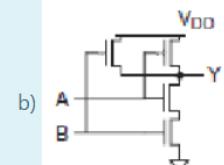


19 20 21 22 23 24

25 26 27 28 29 30

Finish attempt ...

Time left 0:20:29



d) None of the above.

Select one:

- a. Two nMOS in series connection and two pMOS in parallel connection.
- b. Two nMOS in series connection and two other nMOS in parallel connection.
- c. Two pMOS in series connection and two other pMOS in parallel connection.
- d. None of the above.

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Exam - test questions (page 13)

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Finish attempt ...

Time left 0:19:15

Question 13

Not yet answered

Marked out of 1.00

Flag question

A ring oscillator contains _____

Select one:

a. odd number of latches.

b. even number of latches.

c. even number of inverters.

d. odd number of inverters.

Next page

Midterm retake - calculation, essay

Jump to... ▾

Exam - calculation, essay, VHDL, schematic ▾

The screenshot shows a presentation slide titled "Diode characteristics". The slide has a dark background with a white content area. At the top, there is a navigation bar with various icons and text, including "Course", "BMEVI", "autom", "Advan", and search functions. A search bar at the top center contains the text "reverse mode operation". Below the title, there is a bulleted list:

- Forward and reverse mode operation
- Ideal characteristic
- Secondary effects

At the bottom of the slide, there is a footer bar with the text "Microelectronics 26-02-2018". The overall interface suggests a digital classroom or lecture environment.

Exam - test questions (page 18 of 18)

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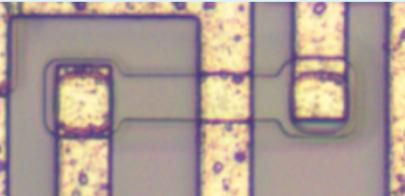
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Finish attempt ...

Question 18
Not yet answered
Marked out of 1.00
[Flag question](#)

What type of electronic component can you see on the image?



Select one or more:

a. capacitor

b. resistor

c. transistor

d. diode

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mecart-cleanrooms.com/learning-cent... | Список для чтения

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MECART CLEANROOMS

Technology clean room, according to the quantity and size of particles per cubic meters of air. The primary authority in the US and Canada is the ISO classification system ISO 14644-1.

This ISO standard includes these clean room classes : ISO 1, ISO 2, ISO 3, ISO 4, ISO 5, ISO 6, ISO 7, ISO 8 and ISO 9. ISO 1 is the "cleanest" class and ISO 9 is the "dirtiest" class. Even if it's classified as the "dirtiest" class, the ISO 9 clean room environment is cleaner than a regular room.

The most common ISO clean room classes are ISO 7 and ISO 8. The Federal Standard 209 (FS 209E) equivalent for these ISO classes are Class 10,000 and Class 100 000.

The old Federal Standard 209E (FS 209E) includes these clean room classes : Class 100,000; Class 10,000; Class 1,000; Class 100; Class 10; Class 1. This standard was replaced in 1999 by ISO-14644-1. It was withdrawn in 2001, but it is still widely used.

Clean rooms must also follow industry-specific and regional standards. For

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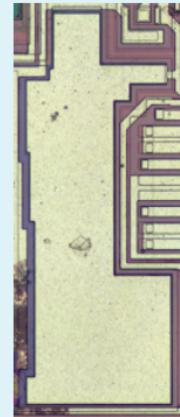
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Finish attempt ... Time left 0:15:21

Question 19 Not yet answered Marked out of 1.00 Flag question

What type of electronic component can you see on the image?



Select one or more:

- a. diode
- b. resistor
- c. transistor
- d. capacitor

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Technologies for clean rooms, according to the quantity and size of particles per cubic meters of air. The primary authority in the US and Canada is the ISO classification system ISO 14644-1.

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Finish attempt ...

Time left 0:14:25

Question 20

Not yet answered

Marked out of 1.00

Flag question

What does the value of R_{thjc} thermal resistance show?

a. The thermal resistance between the active (dissipating) zone and the ambient.

b. The thermal resistance between the active (dissipating) zone and the inner edge of the top of the package.

c. The thermal resistance between the active (dissipating) zone and the PCB board.

d. The thermal resistance between the top and the bottom of the case.

Clear my choice

a - ambient
c - top of package
j - active dissipating zone

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Exam - test questions (page 21)

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Finish attempt ...

Time left 0:14:18

Question 21

Not yet answered

Marked out of 1.00

Flag question

What is the unit of thermal resistance?

a. K/W

b. K-W/s

c. W·s/K

d. W/K

Next page

◀ Midterm
retake -
calculation,
essay

Jump to... ▾

Exam -
calculation,
essay, VHDL,
schematic ►

Microelect... 341 / 584 | 56% + | Список для чтения

Characteristics of inverters, rudiments

- Noise immunity:**
 - Same U_{out} corresponds to a wide U_{in} range
 - There are 3 regions in the characteristic
 - On the L and H sides the characteristic is flat, i.e. any voltage change in the input has negligible effect on the output.

L and H regions

transfer characteristic of an ideal and a realistic inverter

Microelectronics 26-03-2021 17

MOS inverters

Characteristics of inverters, rudiments

- Signal regeneration**
 - depends on the slope of the middle region

10:45 28.05.2021 ENG 2

Exam - test questions (page 22 of 22) +

edu.vik.bme.hu/mod/quiz/attemp... 🔍 ⚡ Сервисы Авиабилеты Яндекс Список для чтения

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Finish attempt ... Time left 0:12:45

Question 22 Not yet answered Marked out of 1.00 Flag question

The space between the chips on the wafer, where the dicing will happen is called ____.

- a. Intel road.
- b. cross-section.
- c. dicing highway.
- d. dicing street.
- e. cutter plane.

Clear my choice

Next page

◀ Midterm retake - calculation, essay Jump to... ▶ Exam - calculation, essay, VHDL, schematic

Micro X Cours X BME X cutter X 🔍 ⚡ Сервисы Авиабилеты Яндекс Список для чтения

cutter plane dicing

Все Картинки Видео Покупки Новости Еще Настройки Инструменты

Результатов: примерно 547 000 (0,59 сек.)

Картинки по запросу cutter plane dicing

Пожаловаться на картинки

→ Показать все

https://en.wikipedia.org/wiki/Wafer_dicing Перевести эту страницу

Wafer dicing - Wikipedia

Cross sectional micrograph of cleavage plane after stealth dicing a Si wafer of 150 µm thickness, compare Ref. Dicing of silicon wafers may also be performed by a ...

Похожие запросы

Exam - test questions (page 23 of 23) +

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Finish attempt ... Time left 0:12:24

Question 23 Not yet answered Marked out of 1.00 Flag question

A sequence of nonlinear operating points calculated while sweeping the input load(s) or a circuit parameter is called...

a. Noise analysis.

b. DC analysis.

c. DC transfer curve analysis.

d. AC analysis.

Next page

Midterm retake - calculation Jump to... Exam - calculation, essay, VHDL

Micro Cours BME cutter +

google.com/search?q=cutter+pla... 🔍 ⚡ Сервисы Авиабилеты Яндекс Список для чтения

cutter plane dicing

Результатов: примерно 547 000 (0,59 сек.)

Картинки по запросу cutter plane dicing

Пожаловаться на картинки

Показать все →

https://en.wikipedia.org/wiki/Wafer_dicing Перевести эту страницу

Wafer dicing - Wikipedia

Cross sectional micrograph of cleavage plane after stealth dicing a Si wafer of 150 µm thickness, compare Ref. Dicing of silicon wafers may also be performed by a ...

Похожие запросы

Exam - test questions (page 24 of 24) +

← → ⌂ 🔍 edu.vik.bme.hu/mod/quiz/attemp... 🔎 ☆ 6x 5x ⚙ Д

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Finish attempt ...

Time left 0:11:26

Question 24

Not yet answered

Marked out of 1.00

Flag question

The statement used to store an estimate of DC operating point during transient analysis is the...

a. .TTRAN

b. .OP

c. .TRAN

d. .OPT

Next page

◀ Midterm retake - calculation

Jump to... ▶

Exam - calculation, essay, VHDL

Answer

 **anushakul1**
Helping Hand • 1 answer

noise analysis
applied ac bias
the gate output is connected either power or ground
vdd+2vtn
reduced by eight

 douwdek0 and 3 more users found this answer helpful

 **THANKS 2**  **1.0** (1 vote)  

 are u sure about these answers 

Exam - test questions (page 25)

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Finish attempt ...

Time left 0:11:09

Question 25

Not yet answered

Marked out of 1.00

Flag question

The statement which bypass initial DC operating point analysis is the...

a. .TRAN

b. .OP

c. .TTRAN

d. .OPT

Next page

Midterm
retake -
calculation,
essay

Jump to...

Exam -
calculation,
essay, VHDL,
schematic

Characteristics of inverters, rudiments

- Noise immunity:
 - Same U_{out} corresponds to a wide U_{in} range
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L and H regions

transfer characteristic of an ideal and a realistic inverter

MOS inverters

Characteristics of inverters, rudiments

- Signal regeneration
 - depends on the slope of the middle region

Exam - test questions (page 26) + 

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Finish attempt ...

Time left **0:10:57**

Question **26**
Not yet answered
Marked out of 1.00


In order to have unique transistors or circuit elements, specified by the manufacturer, we must apply an ... directive with the library path.

a. .MODEL
 b. .MEAS
 c. .TTRAN
 d. .INCLUDE

Next page

 Midterm retake - calculation

Jump to...  

Exam - calculation, essay VHDL

Exam - test questions (page 26) + 

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26	27	28	29	30

Finish attempt ...

Time left **0:10:48**

Question **26**

Not yet answered

Marked out of 1.00

 Flag question

In order to have unique transistors or circuit elements, specified by the manufacturer, we must apply an ... directive with the library path.

a. .MODEL

b. .MEAS

c. .TTRAN

d. .INCLUDE

Next page



Exam - test questions (page 27)

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Finish attempt ...

Time left 0:10:09

Question 27

Not yet answered

Marked out of 1.00

Flag question

What is the scope of a variable (VHDL'87)?

Select one:

a. Process.

b. Variables are not allowed in VHDL'87.

c. Different architectures which are connected to the same entity.

d. Architecture.

Next page

◀ Midterm retake - calculation, essay

Jump to... ▲

Exam - calculation, essay, VHDL, schematic ▶

CMOS inverter 1/13

Characteristics of inverters, rudiments

- Noise immunity:
 - Same U_{out} corresponds to a wide U_{in} range
 - There are 3 regions in the characteristic
 - On the L and H sides the characteristic is flat, i.e. any voltage change in the input has negligible effect on the output.

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transfer characteristic of an ideal and a realistic inverter

Microelectronics 26-03-2021 17

MOS inverters

Characteristics of inverters, rudiments

- Signal regeneration
 - depends on the slope of the middle region

The screenshot shows a browser window with several tabs open at the top. The main content area displays VHDL code examples. One example shows the IEEE library declaration:

```
library IEEE;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
```

Another example shows a user-defined package declaration:

```
library work;
use work.DataTypes_pkg.all;
```

Below the browser window, a slide from a presentation is visible. The slide title is "Digital System Design - Introduction" and the subtitle is "VHDL Structural Elements". The main text on the slide states: "A VHDL design consist of three fundamental design units:" followed by a numbered list under the heading "2. Entity Declaration".

A VHDL design consist of three fundamental design units:

2. Entity Declaration

- **port name**: used to identify pin(s) and providing the ability to connect it to the design unit or other designs units.
- **mode**: give the direction of the port. It can be **in**, **out**, or **inout**, as will be discussed later
- **data type**: define the data type of the port which can be **bit**, **integer**, **std_logic**, and many other types.

Started on Friday, 28 May 2021, 10:53 AM**State** Finished**Completed on** Friday, 28 May 2021, 11:49 AM**Time taken** 56 mins 49 secs**Grade** Not yet graded**Question 1**

Complete

Mark 2.00 out of 2.00

If the doping levels of an abrupt Si diode are

$$N_d = 10^{19}/\text{cm}^3$$

$$N_a = 10^{15}/\text{cm}^3$$

Calculate the diffusion potential at room temperature!

Answer: 0.838

Question 2

Complete

Mark 4.00 out of 4.00

If the doping levels of an abrupt Si diode are

$$N_d = 10^{17}/\text{cm}^3$$

$$N_a = 10^{15}/\text{cm}^3$$

and

$$\epsilon_r = 11.8$$

$$\epsilon_0 = 8.85419e-12 \text{ F/m}$$

$$U = 0$$

Calculate the width of the depletion layers on the less doped side (**um**)!

Answer: 0.969

Question 3

Complete

Mark 4.00 out of 4.00

Calculate the saturation current (**mA**) of a p channel enhancement MOSFET if

- gate-source voltage is -1.2 V
- threshold voltage is -0.3 V
- channel width 0.5 μm
- channel length 0.35 μm
- electron mobility 500 $\text{cm}^2/(\text{V}\cdot\text{s})$
- oxide relative permittivity 3.84
- vacuum permittivity 8.85419E-12 F/m
- oxide thickness 15 nm

Assume that the MOSFET is in saturation!

Answer: 0.065

Question **4**

Complete

Marked out of 10.00

Describe the steps of photolithography. Explain a number of modern photolithography methods!

Steps:

1. Cleaning. The wafers are cleaned from contaminations on the surface.
2. Thermal annealing. The wafer is heated to evaporate humidity from the surface.
3. Adhesion enhancement. By applying chemicals to enhance the adhesion of the photoresist to the wafer.
4. Photoresist coating. The wafer is covered with photoresist by spin coating. There are 2 types: positive and negative photoresists.
5. Soft bake. For evaporating of the excess solvents from the photoresist.
6. Mask alignment and exposure. The mask is aligned properly to the substrate. The photoresist is exposed to UV light that causes a chemical change in it.
7. Development. Portions of the photoresist are dissolved by a chemical developer. If it is a positive resist then the exposed resist is dissolved and the unexposed area remains on the wafer. For the negative resist, it is another way around.
8. Hard bake. The developed photoresist is hardened and stabilized.

Modern photolithography methods:

1. Immersion lithography: the air gap between the final lens and the wafer surface with a liquid medium. It requires multiple patterning due to the resolution limit.
2. Electron-Beam Direct-Write Lithography: the focused beam of electrons draw shapes on a surface covered with electron-sensitive film.
3. Extreme Ultraviolet (EUV) lithography: uses a range of extreme ultraviolet wavelengths.

Question 5

Complete

Marked out of 10.00

Draw the state diagram of a VHDL design that takes d as a serial bit stream input and outputs a logic '1' whenever the sequence "010" occurs.

 [exam.jpg](#)[◀ Exam - test questions](#)

Jump to...

Basic semiconductor physics ►

Microelectronics - BMEVIEEAB00 2020/21/2

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✓		●	✓	

Show one page at a time

Finish review

Started on Wednesday, 3 March 2021, 11:24 AM

State Finished

Completed on Wednesday, 3 March 2021, 11:29 AM

Time taken 5 mins 33 secs

Grade 6.50 out of 10.00 (65%)

Question 1

Incorrect

Mark 0.00 out of 1.00

Flag question

In our laboratory, the aluminum wiring is created by using _____ bonding technique at room temperature.

- a. eutectic
- b. ultrasonic
- c. vaporizing
- d. melting
- e. supersonic



Your answer is incorrect.

Question 2

Correct

Mark 1.00 out of 1.00

Flag question

The gold-silicon compound used in the post process is in _____ compound/liquid phase.

- a. melting
- b. fragmented
- c. eutectic point
- d. vaporizing
- e. plasma



Your answer is correct.

Question 3

Correct

Mark 1.00 out of 1.00

Flag question

What is the typical wafer diameter in the labs of DED?

- a. 5 inch
- b. 10 inch
- c. 20 cm
- d. 10 cm
- e. 2 inch



Your answer is correct.

Question 4

Complete

Mark 1.00 out of 1.00

Flag question

What does class 10000 clean room mean?

10000 clean room means that particles which diameter is less than 0.5 micrometers their number is needed to be less than 10000

Comment:

Question 5

Correct

Mark 1.00 out of

What is the pressure difference between the cleanroom and the outside of the lab?

- a. -50 Pa

1.00

 Flag question

- b. 30 Pa
- c. 100 kPa
- d. 100 Pa
- e. 500 Pa

Your answer is correct.

Question 6

Correct

Mark 1.00 out of 1.00

 Flag question

What is the wavelength of photolithography in the labs of DED?

- a. 465 nm
- b. 13.5 nm
- c. 0.1 μm
- d. 50 nm
- e. 1 μm

Your answer is correct.

Question 7

Incorrect

Mark 0.00 out of 1.00

 Flag question

What kind of high temperature process can we do with our furnaces?

- a. Ion implantation
- b. Diffusion
- c. Sputtering
- d. Epitaxial layer growth
- e. Oxidation

Your answer is incorrect.

Question 8

Partially correct

Mark 0.50 out of 1.00

 Flag question

The dicing saw has an air-bearing design, which is needed because:

- a. RPM is too high.
- b. the wafer is positioned using vacuum.
- c. the vibration of the environment need to be damped.
- d. the temperature is too high.
- e. otherwise the dust particles may contaminate the equipment.

Your answer is partially correct.

You have correctly selected 1.

Question 9

Correct

Mark 1.00 out of 1.00

 Flag questionThe diamond cutter uses   to fix the wafer on the cutting table.

Your answer is correct.

Question 10

Incorrect

Mark 0.00 out of 1.00

 Flag question

Which one is cleaner: ISO class 6 or class 7?

- a. Class 7
- b. Class 6

Your answer is incorrect.

Finish review

Microelectronics - BMEVIEEAB00 2020/21/2

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✓	●	✗			

Show one page at a time

Finish review

Started on Wednesday, 3 March 2021, 10:58 AM

State Finished

Completed on Wednesday, 3 March 2021, 11:09 AM

Time taken 11 mins 20 secs

Grade 8.33 out of 10.00 (83%)

Question 1

Correct

Mark 1.00 out of 1.00

Flag question

The diamond cutter uses the middle of the frame ✓ to position the wafer.

Your answer is correct.

Question 2

Correct

Mark 1.00 out of 1.00

Flag question

What is the temperature accuracy of our hotplate?

- a. $\pm 2^{\circ}\text{C}$
- b. $\pm 10^{\circ}\text{C}$
- c. $\pm 20^{\circ}\text{C}$
- d. $\pm 0.2^{\circ}\text{C}$



Your answer is correct.

Question 3

Correct

Mark 1.00 out of 1.00

Flag question

Which one is cleaner: ISO class 6 or class 7?

- a. Class 6
- b. Class 7



Your answer is correct.

Question 4

Correct

Mark 1.00 out of 1.00

Flag question

What is the pressure difference between the cleanroom and the outside of the lab?

- a. 30 Pa
- b. 100 Pa
- c. 100 kPa
- d. -50 Pa
- e. 500 Pa



Your answer is correct.

Question 5

Correct

Mark 1.00 out of 1.00

Flag question

How do we set the desired thickness of the photoresist?

- a. Speed
- b. Time
- c. Temperature
- d. RPM
- e. PWM
- f. Wavelength



Your answer is correct.

Question 6

Correct

Mark 1.00 out of 1.00

Flag question

The diamond cutter uses vacuum ✓ to fix the wafer on the cutting table.

Your answer is correct.

Question 7

Correct

Mark 1.00 out of
1.00

Flag question

The space between the chips on the wafer, where the dicing will happen is called ____.

- a. cutter plane.
- b. Intel road.
- c. dicing highway.
- d. cross-section.
- e. dicing street.



Your answer is correct.

Question 8

Partially correct

Mark 0.33 out of
1.00

Flag question

What does the bunny suit made of?

- a. flokon
- b. batist
- c. kevlar
- d. metal fiber
- e. wool
- f. carbon
- g. synthetic fiber
- h. silk



Your answer is partially correct.

You have correctly selected 1.

Question 9

Incorrect

Mark 0.00 out of
1.00

Flag question

In our laboratory, the aluminum wiring is created by using _____ bonding technique at room temperature.

- a. eutectic
- b. melting
- c. vaporizing
- d. ultrasonic
- e. supersonic



Your answer is incorrect.

Question 10

Correct

Mark 1.00 out of
1.00

Flag question

What is the wavelength of photolithography in the labs of DED?

- a. 0.1 μm
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Finish review

Microelectronics - BMEVIEEAB00 2020/21/2

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✓	●	✗			

Show one page at a time

Finish review

Started on Wednesday, 3 March 2021, 10:58 AM

State Finished

Completed on Wednesday, 3 March 2021, 11:09 AM

Time taken 11 mins 20 secs

Grade 8.33 out of 10.00 (83%)

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Correct

Mark 1.00 out of 1.00

Flag question

Which one is cleaner: ISO class 6 or class 7?

- a. Class 6
- b. Class 7



Your answer is correct.

Question 4

Correct

Mark 1.00 out of 1.00

Flag question

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- a. 30 Pa
- b. 100 Pa
- c. 100 kPa
- d. -50 Pa
- e. 500 Pa



Your answer is correct.

Question 5

Correct

Mark 1.00 out of 1.00

Flag question

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- c. Temperature
- d. RPM
- e. PWM
- f. Wavelength



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Question 6

Correct

Mark 1.00 out of 1.00

Flag question

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Question 7

Correct

Mark 1.00 out of
1.00

Flag question

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- c. dicing highway.
- d. cross-section.
- e. dicing street.



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Partially correct

Mark 0.33 out of
1.00

Flag question

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- f. carbon
- g. synthetic fiber
- h. silk



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1.00

Flag question

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- b. melting
- c. vaporizing
- d. ultrasonic
- e. supersonic



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1.00

Flag question

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- b. 465 nm
- c. 1 μm
- d. 13.5 nm
- e. 50 nm



Your answer is correct.

Finish review

8
out of
question

?attempt=179251&cmid=29682

Basic of Programm... Budapesti Műszaki... Budapesti Műszaki... SOTE Online booki... Список для чтения

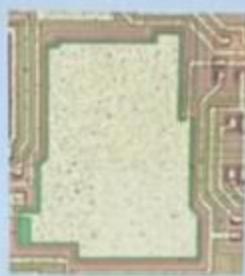
English (en) - Rysaskar Salimbay 0

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?

Select one or more:

- a. transistor
- b. resistor
- c. capacitor
- d. diode



What type of electronic component can you see on the image?

What type of electronic component can you see on the image?

Select one or more:

- a. capacitor
- b. transistor
- c. resistor
- d. diode



Активация Windows
Чтобы активировать Windows, перейдите в раздел
“Параметры”

09:56
22.03.2021
1440x

Flag question

Search Star Shield Puzzle

Список...

English (en) - Rysakar Salimba

What type of electronic component can you see on the image?



Select one or more:

- a. diode
- b. capacitor
- c. transistor
- d. resistor

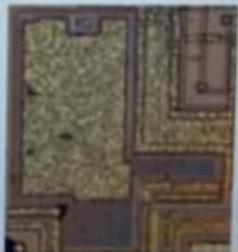
Question 17

Correct

Mark 1.00 out of
1.00

Flag question

What type of electronic component can you see on the image?



What type of electronic component can you see on the image?

Select one or more:

- a. transistor
- b. diode
- c. resistor
- d. capacitor

Активация Windows

Чтобы активировать Windows, перейдите в раздел
“Параметры”.

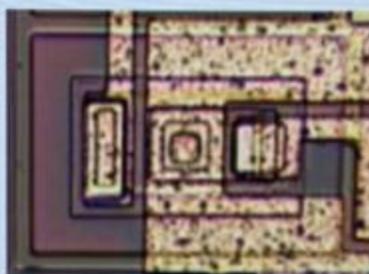
09:56
22.03.2021

744-15

- c. resistor
- d. transistor

Question 15
Correct
Mark 1.00 out of 1.00
Flag question

What type of electronic component can you see on the image?



- Select one or more:
- a. capacitor
 - b. transistor
 - c. resistor
 - d. diode

Question 16
Correct
Mark 1.00 out of 1.00
Flag question

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?



Активация Windows
Чтобы активировать Windows, перейдите в раздел
“Параметры”

view.php?attempt=179251&cmid=29682

Входящие (411) - o... Basics of Programm... Budapesti Műszaki... Budapesti Műszaki... SOTE Online book... Список для изучения

Question 13 Correct Mark 1.00 out of 1.00 Flag question

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?

Select one or more:

- a. capacitor
- b. diode
- c. resistor
- d. transistor



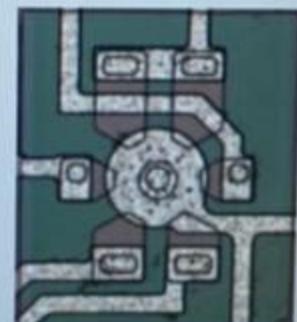
Question 14 Correct Mark 1.00 out of 1.00 Flag question

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?

Select one or more:

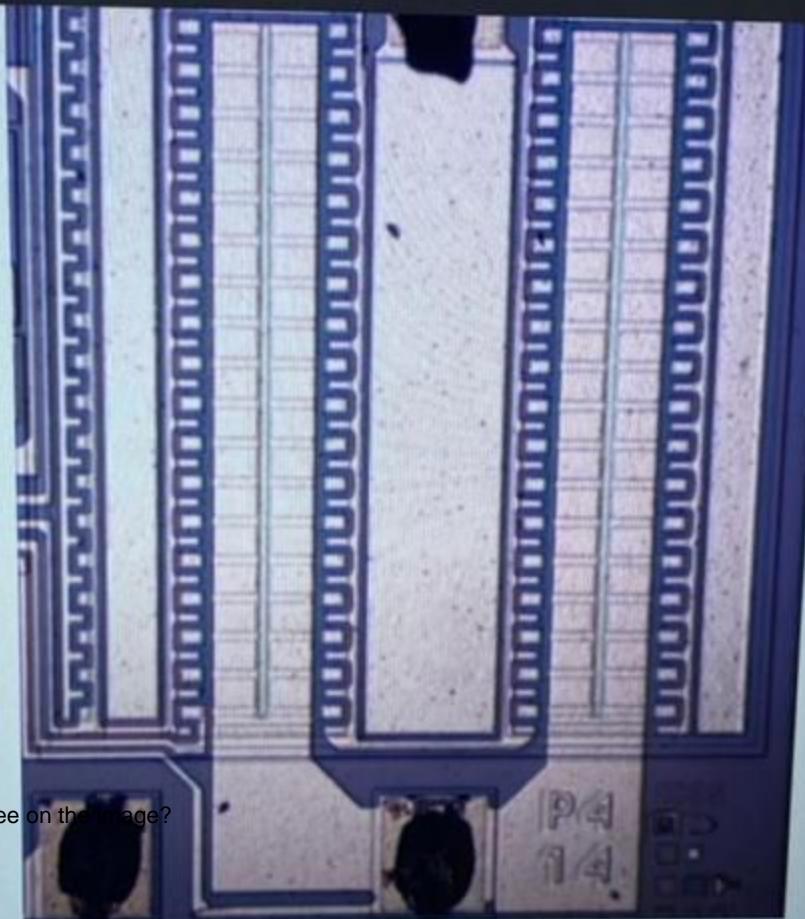
- a. diode
- b. capacitor
- c. resistor
- d. transistor



Активация Windows
Чтобы активировать Windows, перейдите в раздел
«Параметры».

09:56 22.03.2021

144Hz



What type of electronic component can you see on the image?

Select one or more:

- a. diode
- b. resistor
- c. capacitor
- d. transistor

Активация Windows

Чтобы активировать Windows, перейдите в раздел
"Параметры".

Question 11
Correct
Mark 1.00 out of 1.00
Flag question

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?



Select one or more:

- a. capacitor
- b. resistor
- c. diode
- d. transistor

Question 12
Correct
Mark 1.00 out of 1.00
Flag question

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?

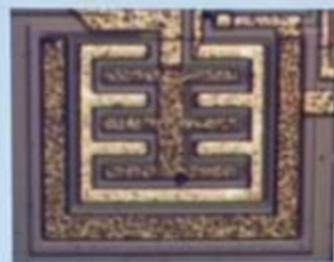


активизация Windows
чтобы активировать Windows, перейдите в раздел
“Параметры”

- 9
1.00 out of
Flag question

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?



Select one or more:

- a. resistor
- b. transistor
- c. capacitor
- d. diode

Question 10

incorrect

Mark 0.00 out of

1.00

Flag question

What type of electronic component can you see on the image?



Select one or more:

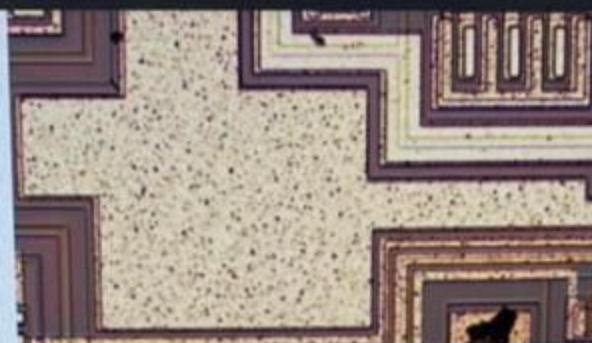
- a. capacitor
- b. resistor
- c. diode
- d. transistor

Активация Windows

Чтобы активировать Windows, перейдите в раздел
“Параметры”.

Question 11
Correct

What type of electronic component can you see on the image?



Select one or more:

- a. diode
- b. resistor
- c. capacitor
- d. transistor

What type of electronic component can you see on the image?

What type of electronic component can you see on the image?



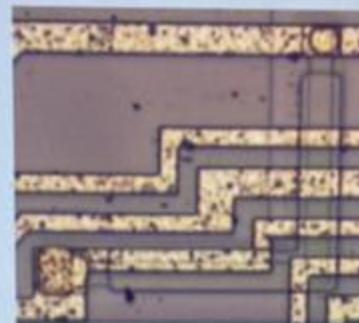
Select one or more:

- a. transistor
- b. diode
- c. capacitor
- d. resistor

Активация Windows

Чтобы активировать Windows, перейдите в раздел
“Параметры”

What type of electronic component can you see on the image?



Select one or more:

- a. capacitor
- b. diode
- c. transistor
- d. resistor

What type of electronic component can you see on the image?



Select one or more:

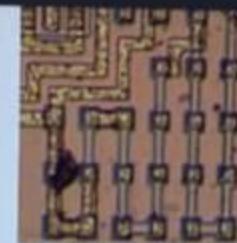
- a. resistor
- b. capacitor

Активация Windows

Чтобы активировать Windows, откройте в разделе
“Параметры”.

Mark 1.00 out of
1.00
Flag question

English (en) Rysaskar Salimbuy



Select one or more:

- a. transistor
- b. diode
- c. capacitor
- d. resistor

What type of electronic component can you see on the image?

Question 4
Correct
Mark 1.00 out of
1.00
Flag question

What type of electronic component can you see on the image?



Select one or more:

- a. resistor
- b. transistor
- c. diode
- d. capacitor

Активация Windows

Перейти к активации Windows переходите в раздел
"Помощь"

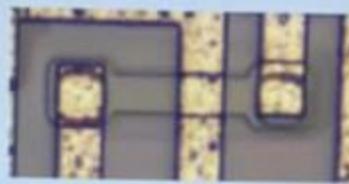
Microelect... | Просмотреть | Integrated circ... | Интегральная | Google Перев... | (1) NPN comm... | как открыть | +

ew.php?attempt=179251&cmid=29682

Входящие (411) - о... Basics of Programm... Budapesti Műszaki... Budapesti Műszaki... SOTE Online booki... Список для

Time taken: 45 mins 50 secs
Grade: 17.00 out of 19.00 (89%)

English (en) - Rysaskar Salimbay

Question 1
What type of electronic component can you see on the image?

Select one or more:
 a. transistor
 b. diode
 c. resistor
 d. capacitor

What type of electronic component can you see on the image?

Question 2
What type of electronic component can you see on the image?

Select one or more:
 a. resistor
 b. transistor
 c. capacitor
 d. diode

Активация Windows
Методы активации Windows 7, определение и устранение ошибок
Параметры

Time taken: 45 mins 50 secs
Grade: 17.00 out of 19.00 (89%)

English (en) - Rysaskar Salimbay

Time taken: 45 mins 50 secs
Grade: 17.00 out of 19.00 (89%)

English (en) - Rysaskar Salimbay

Microelectronics - BMEVIEEAB00 2020/21/2

Started on	Wednesday, 10 March 2021, 11:49 AM
State	Finished
Completed on	Wednesday, 10 March 2021, 11:53 AM
Time taken	4 mins 16 secs
Grade	7.00 out of 7.00 (100%)

Question 1

Correct

Mark 1.00 out of 1.00

Flag question

When the thermal boundary of the virtual system is set that the heat cannot be transferred through the given boundary, then it is called:

- a. Propagating
- b. Conductive
- c. Isothermal
- d. Adiabatic



Your answer is correct.

Question 2

Correct

Mark 1.00 out of 1.00

Flag question

What does the value of R_{thjc} thermal resistance show?

- a. The thermal resistance between the active (dissipating) zone and the inner edge of the top of the package.
- b. The thermal resistance between the active (dissipating) zone and the ambient.
- c. The thermal resistance between the top and the bottom of the case.
- d. The thermal resistance between the active (dissipating) zone and the PCB board.

Your answer is correct.

Question 3

Correct

Mark 1.00 out of 1.00

Flag question

What is the unit of thermal resistance?

- a. W/K
- b. K-W/s
- c. W/s/K
- d. K/W



Your answer is correct.

Question 4

Correct

Mark 1.00 out of 1.00

Flag question

What is the unit of thermal conductance?

- a. K/W
- b. K-W/s
- c. W/K
- d. W-s/K



Your answer is correct.

Question 5

Correct

Mark 1.00 out of
1.00

Flag question

What does the value of R_{thca} thermal resistance show?

a.

The thermal resistance between the active (dissipating) zone and the PCB board.

b.

The thermal resistance between the top of the package and the ambient.



c.

The thermal resistance between the active (dissipating) zone and the inner edge of the top of the package.

d.

The thermal resistance between the active (dissipating) zone and the ambient.

Your answer is correct.

Question 6

Correct

Mark 1.00 out of
1.00

Flag question

What is the unit of thermal capacitance?

a.

K·W/s

b.

W·s/K



c.

W·m/K

d.

s·K/W

Your answer is correct.

Question 7

Correct

Mark 1.00 out of
1.00

Flag question

What is the R_{thja} thermal resistance value of a DIL package with a supply voltage of 3V and with an average current of 0.5A, if there is a 30°C temperature difference between the dissipating region and the outside of the package?

a.

13,33 mK/W

b.

30 W/K

c.

20 K/W



d.

0.05 K/W

Your answer is correct.

Finish review

Quiz navigation

1	2	3	4	5
✓	✓	✓	✓	✓
6	7			

Show one page at a time

Finish review