

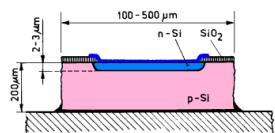
1. Describe the secondary effects of the diode

## Secondary effects

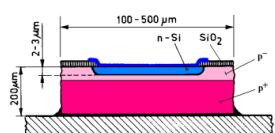
- Series resistance
- Generation current
- Breakdown phenomena (a bit later)
- Recombination current (just mention)

### The series resistance

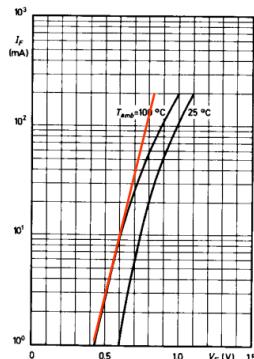
Appears at high current levels. Reason:



Solution: epitaxial structure



### Forward characteristics $I_F = f(V_F)$



Microelectronics 26-02-2018  
Operation of PN junctions

### Secondary effects

#### The series resistance

Calculate the series resistance according to the 100°C characteristic!

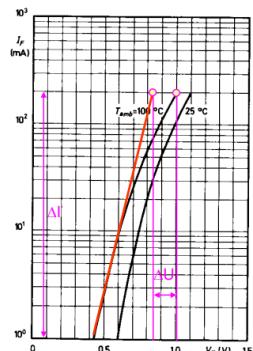
$$\Delta U = 160 \text{ mV}$$

$$I = 200 \text{ mA}$$

$$r_s = 160 / 200 = 0,8 \Omega$$

### Problem

#### Forward characteristics $I_F = f(V_F)$



## The generation current

In reverse region, in theory:

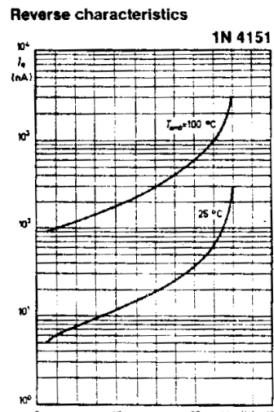
$$I = I_0 (\exp(U/U_T) - 1) \Rightarrow -I_0$$

that would result in pA only

The experience is:

$$g = \frac{n_i}{2\tau}$$

$$I_R = \text{const} \cdot n_i \sqrt{-U_R}$$



Microelectronics 26-02-2018

1

Operation of PN junctions

## Secondary effects

### The recombination current

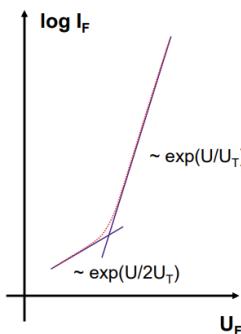
Phenomenon appearing in the forward region

$$I_{Rec} \approx \text{const} \cdot n_i \cdot \exp(U/2U_T)$$

Can be well described by the Shockley-Read-Hall model for semiconductors with indirect band

$$I = I_0 (\exp(U/mU_T) - 1) = -I_0$$

m: non-ideality factor, between 1..2



## 2. Break down phenomena of diode

## Avalanche break-down

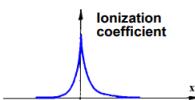
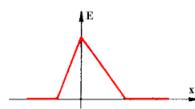
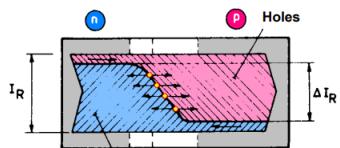
$$I_R = M(U_R) \cdot I_{R0}$$

M – multiplication factor

$$M = \frac{1}{1 - \left( \frac{-U}{U_L} \right)^m}$$

$U_L$  depends on the less doped side:

$$U_L \sim N^{-0.7}$$

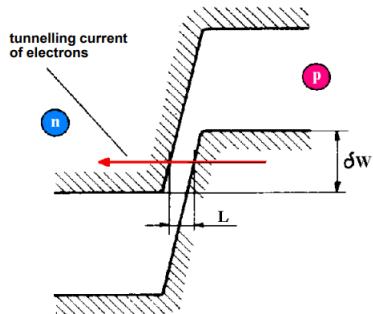


## The Zener effect

Physical reason:

tunneling

$$U_L \sim N^{-1}$$



if the reverse bias applied to an p-n junction is increased, a point will reach when the junction breaks down and reverse current rises sharply to a value limited only by the external resistance connected in series. This specific value of the reverse bias voltage is called breakdown voltage. After breakdown a small further increase in the reverse current is seen. There are 2 process which causes junction breakdown, they are:

- 1) Zener Breakdown
- 2) Avalanche Breakdown

### Zener Breakdown

The PN junction is formed by the combination of the p-type and the n-type semiconductor material. The combination of the P-type and N-type regions creates the depletion region. The width of the depletion region depends on the doping of the P and N-type semiconductor material. If the material is heavily doped, the width of the depletion region becomes very thin.

Zener diodes are heavily diodes that can work reliably in the reverse-biased regions. Here breakdown takes place due to the Zener effect. In the Zener effect when the electric field of the reverse-biased P-N diode is increased, tunneling of the valence electrons into the conduction band takes place. This leads to an increase in the minority charge carriers thereby increasing the reverse current. This phenomenon is known as the Zener effect and the minimum voltage at which this phenomenon starts is known as Zener Breakdown voltage.

### Avalanche Breakdown

In lightly doped diode breakdown takes place due to the Avalanche effect. Here in the Avalanche effect, when a diode is operated in reverse bias due to increased electric field the minority charge carriers gain kinetic energy and collides with the electron-hole pairs, thereby breaking their covalent bond and creating new mobile charge carriers. This increase in

the number of minority charge carriers leads to an increase in reverse current causing breakdown. Here, the breakdown voltage is known as Avalanche breakdown voltage.

$$M = \left( \frac{1}{1 + (V_a/V_b)^n} \right)$$

The breakdown voltage of the commonly available Zener diode varies between 1.2V to 200V.

## **1. Steps of photolithography and modern photolithography methods**

Describe the steps of photolithography. Explain a number of modern photolithography methods!

Steps:

1. Cleaning. The wafers are cleaned from contaminations on the surface.
2. Thermal annealing. The wafer is heated to evaporate humidity from the surface.
3. Adhesion enhancement. By applying chemicals to enhance the adhesion of the photoresist to the wafer.
4. Photoresist coating. The wafer is covered with photoresist by spin coating. There are 2 types: positive and negative photoresists.
5. Soft bake. For evaporating of the excess solvents from the photoresist.
6. Mask alignment and exposure. The mask is aligned properly to the substrate. The photoresist is exposed to UV light that causes a chemical change in it.
7. Development. Portions of the photoresist are dissolved by a chemical developer. If it is a positive resist then the exposed resist is dissolved and the unexposed area remains on the wafer. For the negative resist, it is another way around.
8. Hard bake. The developed photoresist is hardened and stabilized.

Modern photolithography methods:

1. Immersion lithography: the air gap between the final lens and the wafer surface with a liquid medium. It requires multiple patterning due to the resolution limit.
2. Electron-Beam Direct-Write Lithography: the focused beam of electrons draw shapes on a surface covered with electron-sensitive film.
3. Extreme Ultraviolet (EUV) lithography: uses a range of extreme ultraviolet wavelengths.

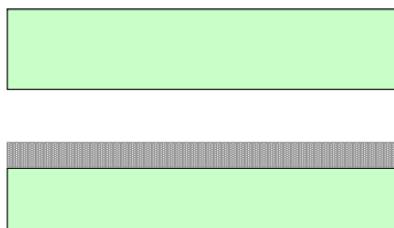
## **2. Describe the steps of the poli-Si gate self aligned nMOS process – indicate when a photomask is needed. Support the description with cross-sectional diagrams of the structure.**

## Steps of the self-aligned poli-Si gate process

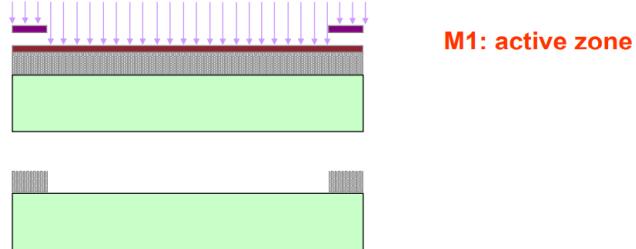
- 1) Open window for the active region
  - photolithography, field oxide etching
- 2) Growth of thin oxide
- 3) Window for hidden contacts
  - Contacts the poli-Si gate (yet to be deposited) with the active region (after doping).
- 4) Deposit poli-Si
- 5) Patterning of poli-Si
- 6) n+ doping:  
Form source and drain regions as well as wiring by diffusion lines.  
Through the hidden contact poli-Si gate will also be connected to diffused lines.
- 7) Deposit phosphor-silica glass (PSG) as insulator
- 8) Open contact windows through PSG-n
- 9) Metallization
- 10) Patterning metallization layer

## Steps:

- Start with: p type substrate (Si wafer)
  - cleaning
  - grow thick  $\text{SiO}_2$  – this is called *field oxide*

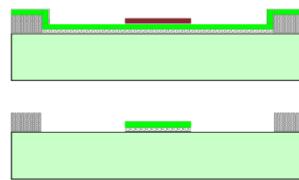


- Create the active zone with photolithography
  - coat with resist,
  - expose to UV light through a mask,
  - development, removal of exposed resists
  - etching of  $\text{SiO}_2$  removal of the resist



▪ Create the gate structure:

- growth of thin oxide
- deposit poly-Si
- pattern poly-Si with photolithography
- etch poly-Si, etch thin oxide



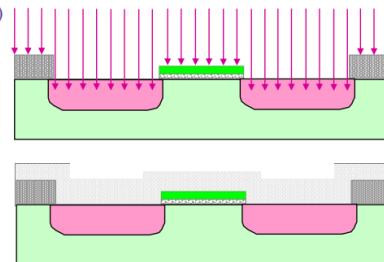
(resist, exposure, develop)

M2: poly-Si pattern

▪ S/D doping (implantation)

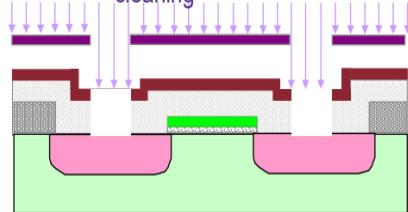
- the oxide (thin, thick) masks the dopants
- this way the self-alignment of the gate is assured

► Passivation: deposit PSG



- Open contact windows through PSG

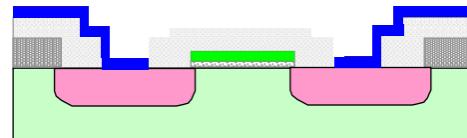
- photolithography (resist, expose pattern, develop)
- etching (copy the pattern)
- cleaning



**M3: contact window pattern**

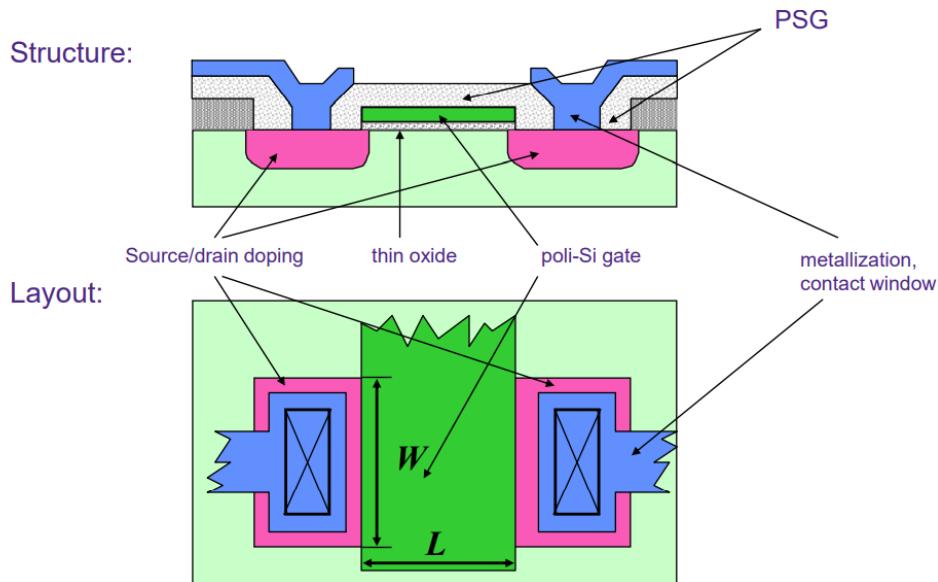
- Metallization

- Deposit Al
- photolithography, etching, cleaning



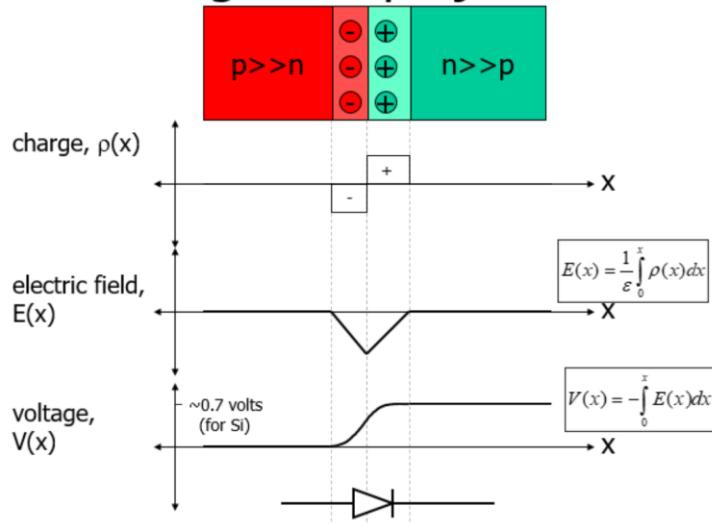
**M4: metallization pattern**

- ▶ The sequence of the process is given, the in-depth structure is determined by the sequence of the masks
- ▶ One needs to specify the shapes on the masks
  - *The set of shapes on subsequent masks is called layout*

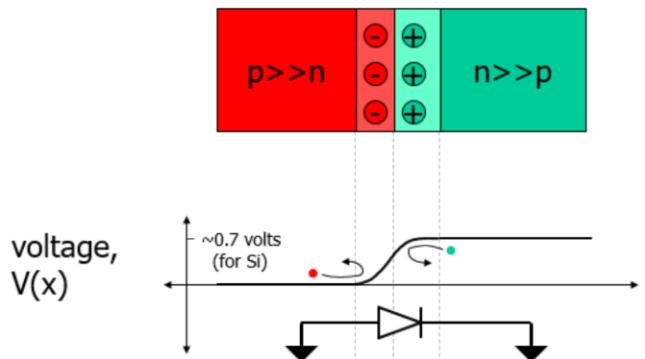


3. Describe the qualitative operation of a diode (explanation, cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

# Voltage in a pn junction



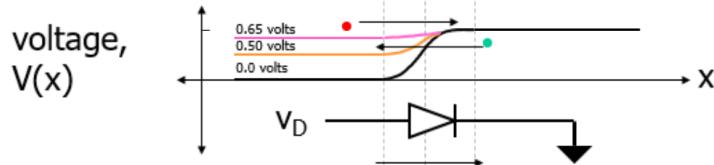
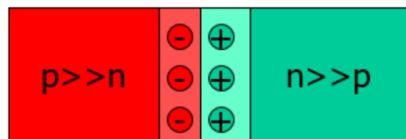
## Zero Bias



At zero bias ( $v_D=0$ ), very few electrons or holes can overcome this *built-in voltage barrier* of  $\sim 0.7$  volts (and exactly balanced by diffusion)

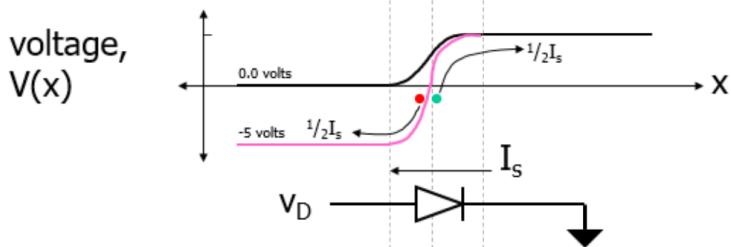
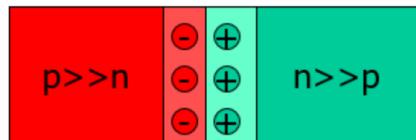
$$\rightarrow i_D = 0$$

## Forward Bias



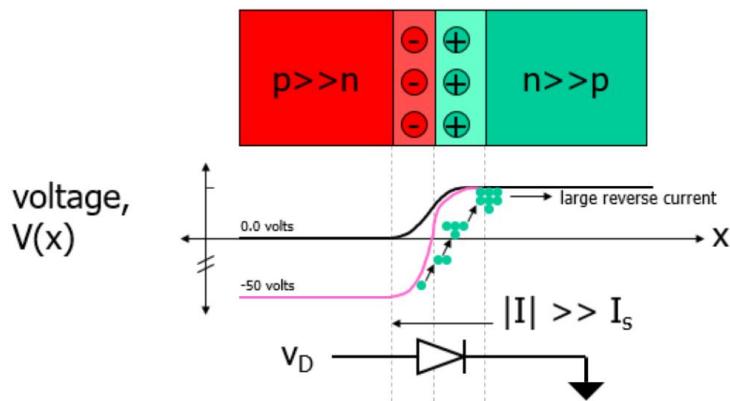
As the bias ( $v_D$ ), increases toward 0.7V, more electrons and holes can overcome the *built-in voltage barrier*.  $\rightarrow i_D > 0$

## Reverse Bias



As the bias ( $v_D$ ) becomes negative, the barrier becomes larger. Only electrons and holes due to broken bonds contribute to the diode current.  
 $\rightarrow i_D = -I_s$

# Breakdown

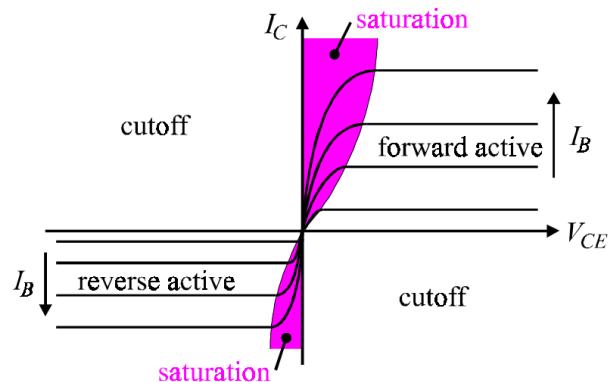


As the bias ( $v_D$ ) becomes very negative, the barrier becomes larger. Free electrons and holes due to broken bonds are accelerated to high energy ( $>E_g$ ) and break other covalent bonds – generating more electrons and holes (avalanche).

4. Describe the qualitative operation of an npn BJT (explanation, cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

## BJT Regions of Operation

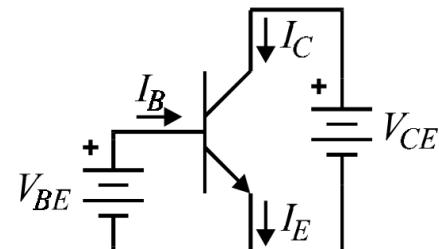
- The bipolar transistor has four distinct regions of operation:
  - Forward Active
  - Reverse Active
  - Saturation
  - Cutoff



## Forward Active Operation - Potentials

---

- When the base-emitter junction is forward biased and the base collector junction is reverse biased (implying  $V_{CE} > V_{BE}$ ), the device is in the forward active region of operation

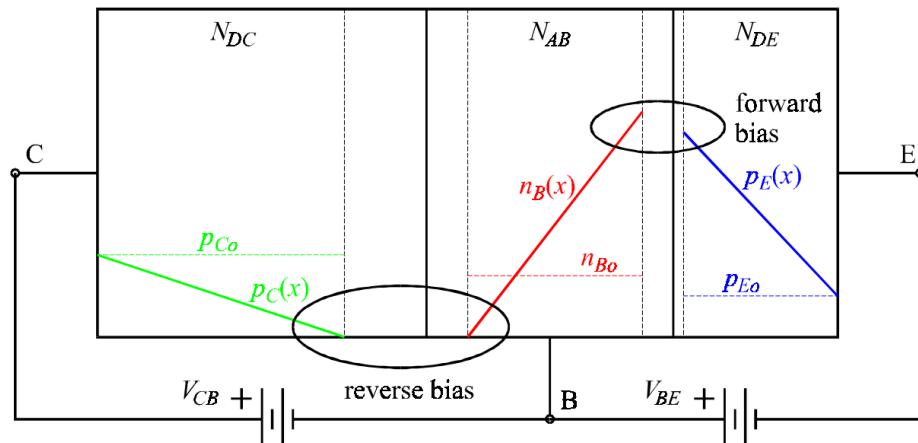


$$V_{CE} > V_{BE}$$

## Forward Active Operation - Minority Carriers

---

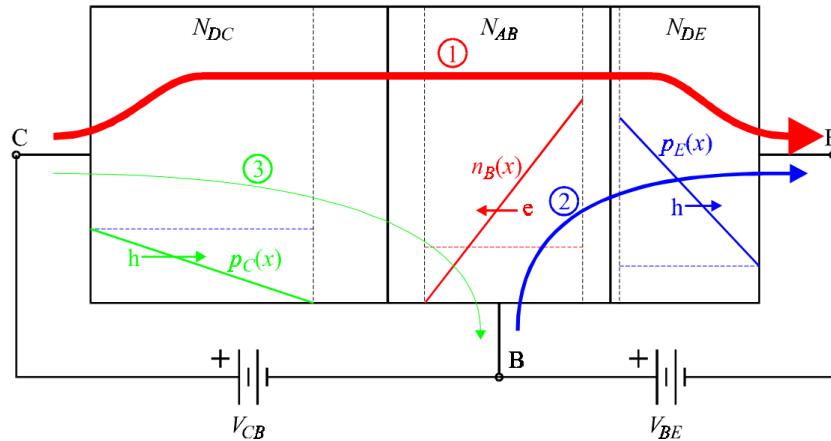
- $V_{BE} > 0$  raises  $p_E(x)$  and  $n_B(x)$  at the BE depletion region edges
- $V_{BC} < 0$  lowers  $p_C(x)$  and  $n_B(x)$  at the BC depletion region edges
- Since all regions are short compared to the minority diffusion lengths, the minority densities change linearly over all regions



## Forward Active Operation - Current Components

---

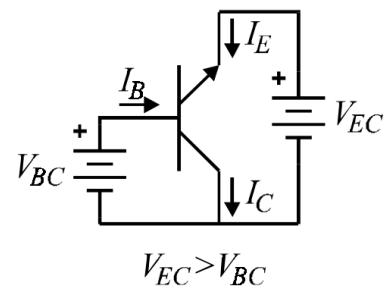
- Three current components in forward active operation, all of which can be characterised from the appropriate minority gradient:
  - “Linking current” due to electron transport from collector to emitter (1)
  - “Back injection” due to hole injection from base to emitter (2)
  - small component due to injection of holes from collector to base (3)



## Reverse Active Region - Potentials

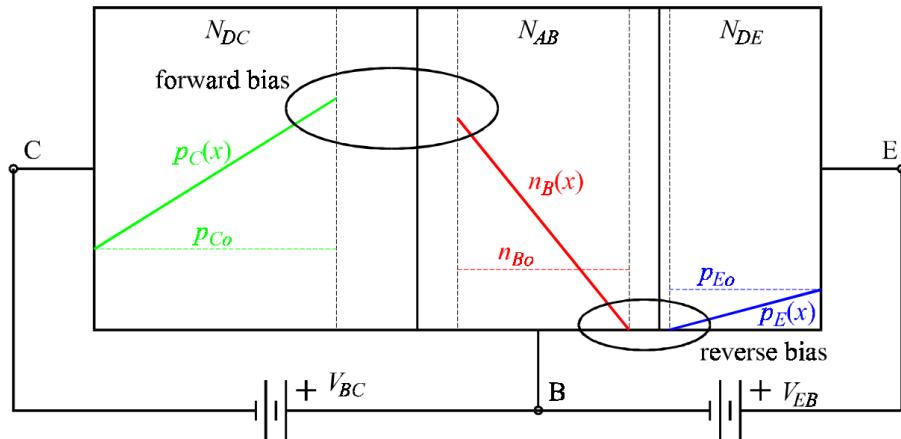
---

- When the base collector junction is forward biased and the base emitter junction is reverse biased (implying  $V_{EC} > V_{BC}$ ), the device is in the reverse active region of operation
- Basically the forward active region with roles of emitter and collector reversed



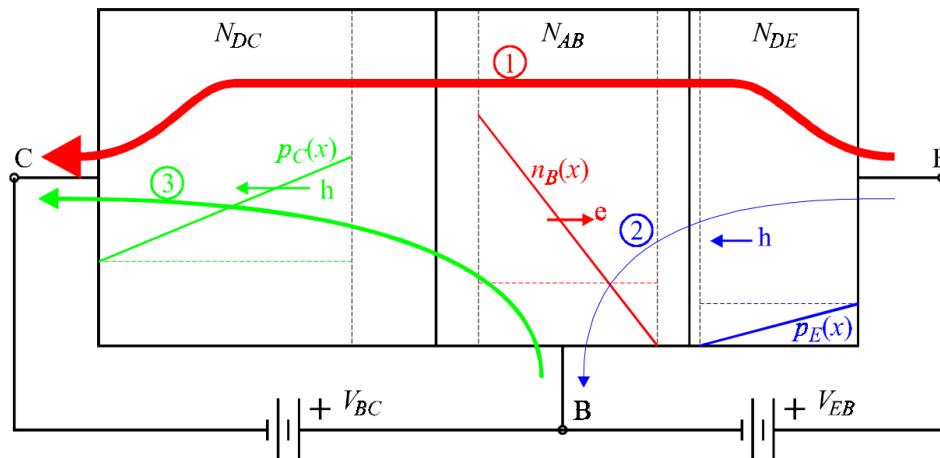
## Reverse Active Region - Minority Carriers

- Similar distributions to forward active, with bias (forward/reverse) of base-collector and base-emitter junctions reversed
- Note that potentials are mislabeled in notes



## Reverse Active Region - Current Components

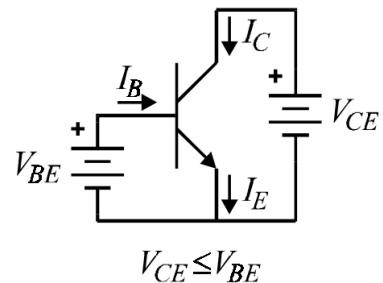
- Three current components in reverse active operation:
  - “Linking current” due to electron transport from emitter to collector (1)
  - small component due to injection of holes from emitter to base (2)
  - “Back injection” due to hole injection from base to collector (3)



## Saturation Region - Potentials

---

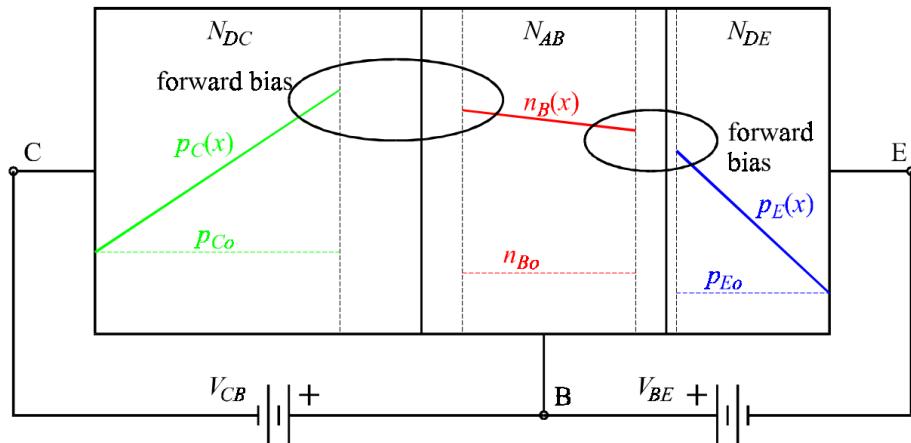
- The saturation region of operation is characterised by forward bias potentials on both the base-emitter and base-collector junctions (implying  $V_{BE} \geq V_{CE}$ )



## Saturation Region - Minority Carriers

---

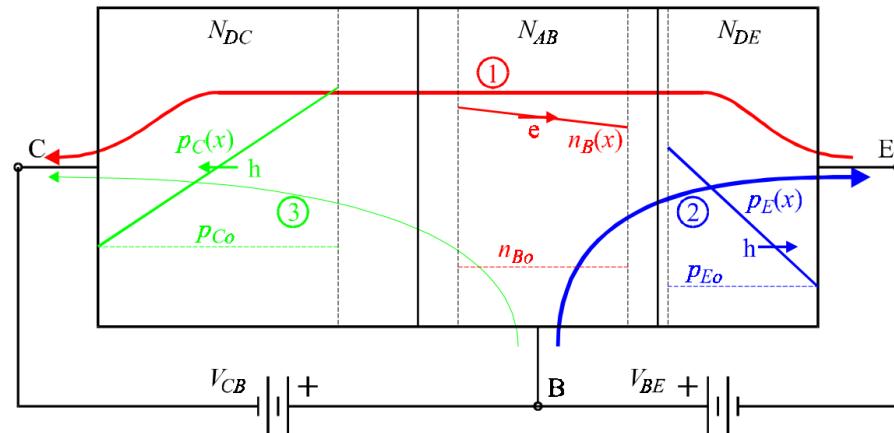
- With both junctions forward biased, the minority carrier densities are raised above their equilibrium values throughout the device
- The values of  $n_B(x)$  on either side of the neutral base region ( $n_{Bo}e^{qVBE/kT}$  and  $n_{Bo}e^{qVBC/kT}$ ) determine the slope of  $n_B(x)$  - depending on the relative values of  $V_{BE}$  and  $V_{BC}$ , the slope may be +ve, -ve or zero



## Saturation Region - Current Components

---

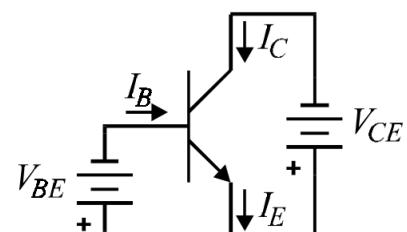
- Three current components in saturation operation:
  - “Linking current” due to electron transport (1) - can be from emitter to collector ( $V_{BE} < V_{BC}$ ), collector to emitter ( $V_{BE} > V_{BC}$ ), or zero ( $V_{BE} = V_{BC}$ )
  - component due to injection of holes from base to emitter (2)
  - component due to injection from base to collector (3)



## Cutoff Region - Potentials

---

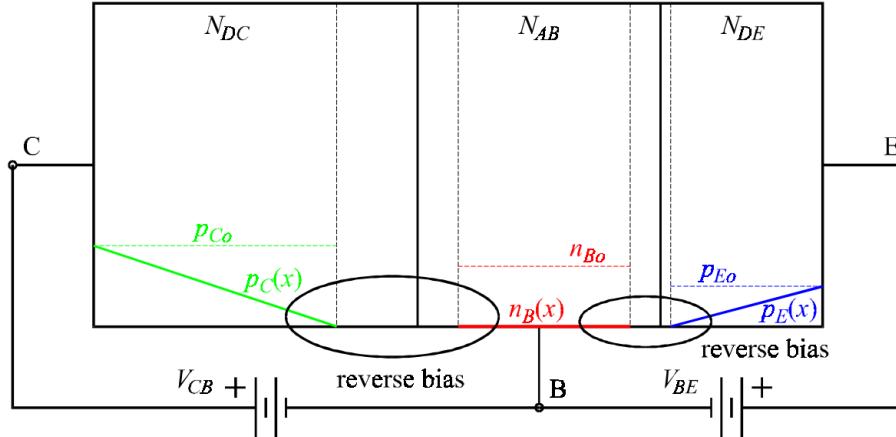
- When both junctions are reverse biased (implying  $V_{BE}$  negative and  $V_{BE} \geq V_{CE}$ ) the device is in the cutoff region of operation



$$V_{CE} \leq V_{BE}$$

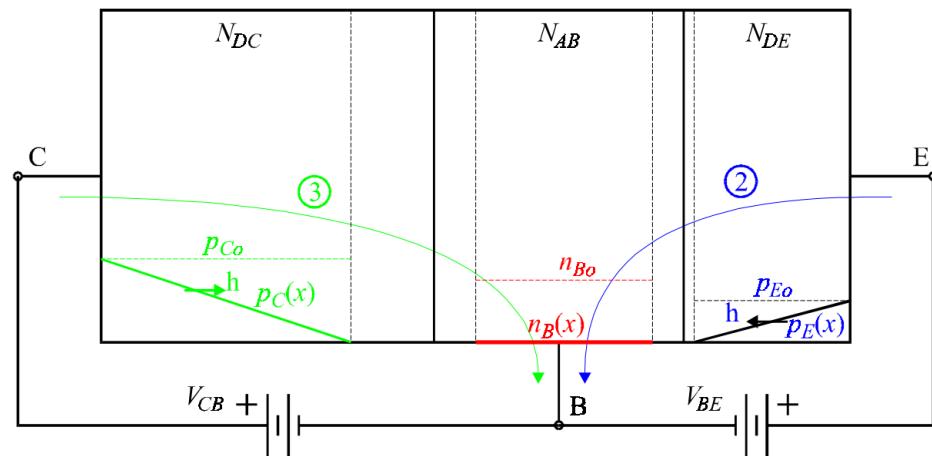
## Cutoff Region - Minority Carriers

- With  $V_{BE}$  and  $V_{BC}$  reverse biased, the minority carrier densities are small at all depletion region edges
- This implies that  $n_B(x)$  is zero over the entire neutral base region, since the distribution must be linear



## Cutoff Region - Current Components

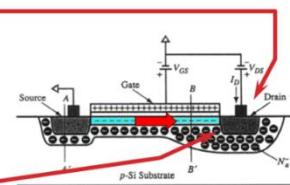
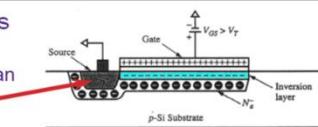
- Only two current components in saturation operation - “linking current” is zero because gradient of  $n_B(x)$  is zero
  - small component due to injection of holes from emitter to base (2)
  - small component due to injection from collector to base (3)



5. Describe the qualitative operation of an n-channel enhancement mode MOSFET (explanation, cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

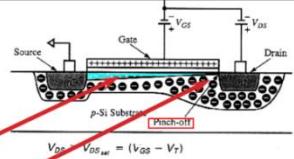
- If  $V_{GS} > V_T$ , inversion layer is formed

- the n+ region at the **source** can inject electrons into the inversion channel
- the positive potential at the **drain** induces flow of electrons in the channel,
- the positive potential of the drain reverse biases the pn junction formed there
- the electrons drifted there are all sunk in the n+ region and the circuit is closed



- the charge density in channel depends on the  $V_{GS}$  voltage

- there is a *voltage drop* in the channel, thus, the thickness of the inversion layer will diminish along the channel
- at a given  $V_{DSsat}$  saturation voltage the thickness will reach 0, this is the so called **pinch-off**



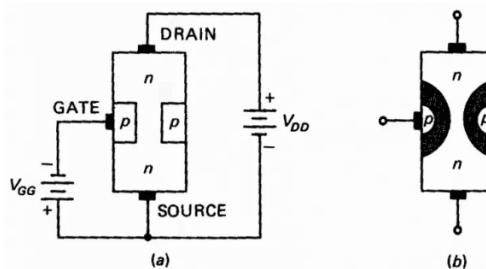
$$V_{DSsat} = V_{GS} - V_T$$

After this voltage is reached, the MOSFET operates **in saturation mode**, **the drain voltage does not influence the drain current any longer**.

6. Describe the qualitative operation of an n-channel enhancement mode JFET (explanation, cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

Both N-channel JFET and **p-channel JFET** operated in the same way, although the charge carriers are inverted i.e. **electrons** are majority carriers in n-channel and **holes** are majority carriers in p-channel. Here we explain n-channel jfet operation because it is more preferable.

The width of the channel varies in accordance with the magnitude of the bias applied to the gate terminal and source-drain terminal. As shown in the figure above we explain how channel width change when we apply either a positive voltage or negative across it. Let's have a detailed look at it.



### **(i) No voltage:**

When neither any voltage is applied across source to drain terminal i.e.  $V_{ds} = 0$  nor any bias is applied to the gate terminal i.e.  $V_{gs} = 0$ , the depletion region around the p-n junction are of equal thickness and symmetrical in nature.

### **(ii) Negative Voltage:**

When the gate is negative bias with respect to the source and drain is applied with a positive bias with respect to the source, the p-n junction got reverse biased and forms depletion region. When the drain current flows through the channel, there is a voltage drop along its length. The result is that the reverse bias at the drain end is more than that at the source end making the width of depletion layer more at the drain. With the increasing resistance and reducing current  $I_d$ , the channel starts narrowing. If we further increase the negative voltage across the gate, depletion layers meet at the centre and the drain current cut off completely. Similarly, if we reduce the negative voltage across the gate, the depletion layers start reducing causing decrease in resistance and increase in drain current  $I_d$ .

### **(iii) Positive voltage:**

When a positive voltage is applied to the drain terminal with respect to source terminal without connecting the gate terminal to the supply, the electrons starts moving from source terminal to drain terminal whereas conventional drain current  $I_d$  flows through the channel from Drain to the source. Due to this flow of current, the uniform voltage drop occurs across the channel resistance which reverse bias the diode. The gate is more negative to those points in the channel which are nearer to drain than the source. Therefore, depletion layers penetrate more deeply into the channel at points which are more closer to drain than the source. As a result, the wedge-shaped depletion regions are formed when  $V_{ds}$  is applied across the terminals.

7. Describe the Ebers-Moll model and the operating modes of the bipolar transistor! Provide the equations of the Ebers-Moll model as well! Indicate the different operating modes in the model as well as in the equations!

## Ebers-Moll model

- Ebers-Moll model is transistor analytical model which describes the operating states of a transistor.
- This model is useful to obtain information about the d.c characteristic curves of a transistor.
- The transistor operates in active region when emitter junction is forward biased and collector junction is reverse biased.
- **The behaviour of a transistor is generalized by Ebers-Moll model by taking the inverted mode of operation of the transistor into account.**

This gives:

$$I_E = I_{ES} (e^{V_{BE}/V_T} - 1) - \alpha_R I_{CS} (e^{V_{BC}/V_T} - 1)$$

$$I_C = \alpha_F I_{ES} (e^{V_{BE}/V_T} - 1) - I_{CS} (e^{V_{BC}/V_T} - 1)$$

$$I_B = (1 - \alpha_F) I_{ES} (e^{V_{BE}/V_T} - 1) + (1 - \alpha_R) I_{CS} (e^{V_{BC}/V_T} - 1)$$

These are called the Ebers-Moll Equations for the bipolar transistor (see Fig. 2.3).

**2.3 Modes of Operation**  
The Ebers-Moll BJT Model is a good large-signal, steady-state model of the transistor and allows the state of conduction of the device to be easily determined for different modes of operation of the device. The different modes of operation are determined by the manner in which the junctions are biased. The charge profiles for each mode are shown in Fig. 2.4.

**(a) Forward Active Mode**  
B-E forward-biased,  $V_{BE}$  positive      B-C reverse biased,  $V_{BC}$  negative

$$e^{V_{BE}/V_T} \gg 1 \quad e^{V_{BC}/V_T} \ll 1$$

Then from the model,

$I_E \approx I_{ES} e^{V_{BE}/V_T}$	relatively large
$I_C \approx \alpha_F I_{ES} e^{V_{BE}/V_T} = \alpha_F I_E$	relatively large
$I_B \approx (1 - \alpha_F) I_{ES} e^{V_{BE}/V_T} = (1 - \alpha_F) I_E$	small

**(b) Reverse Active Mode**

B-E reverse biased,  $V_{BE}$  negative

B-C forward biased,  $V_{BC}$  positive

$$e^{V_{BE}/V_T} \ll 1,$$

$$e^{V_{BC}/V_T} \gg 1$$

Essentially the transistor conducts in the opposite direction.  
From the model,

$$I_E \approx -\alpha_R I_{CS} e^{V_{BC}/V_T} \quad \text{moderately high}$$

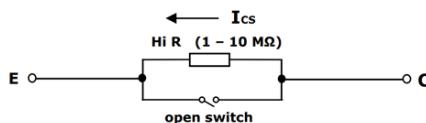
$$I_C \approx -I_{CS} e^{V_{BC}/V_T} \quad \text{moderate}$$

$$I_B \approx (1 - \alpha_R) I_{CS} e^{V_{BC}/V_T} \quad \text{as high as } 0.5 |I_C|$$

This mode does not provide useful amplification but is used, mainly, for current steering in switching circuits, e.g. TTL.



This is equivalent to a very low conductance between collector and emitter as shown in Fig. 2.5, i.e. an open switch.



**(d) The Saturation Mode**

B-E forward biased,  $V_{BE}$  positive  
positive

B-C forward biased,  $V_{BC}$

$$e^{V_{BE}/V_T} \gg 1$$

$$e^{V_{BC}/V_T} \gg 1$$

Note: both junctions are forward biased

Then,

$$I_E \approx I_{ES} e^{V_{BE}/V_T} - \alpha_R I_{CS} e^{V_{BC}/V_T}$$

$$I_C \approx \alpha_F I_{ES} e^{V_{BE}/V_T} - I_{CS} e^{V_{BC}/V_T}$$

$$I_B \approx (1 - \alpha_F) I_{ES} e^{V_{BE}/V_T} + (1 - \alpha_R) I_{CS} e^{V_{BC}/V_T}$$

7



In this case, with both junctions forward biased

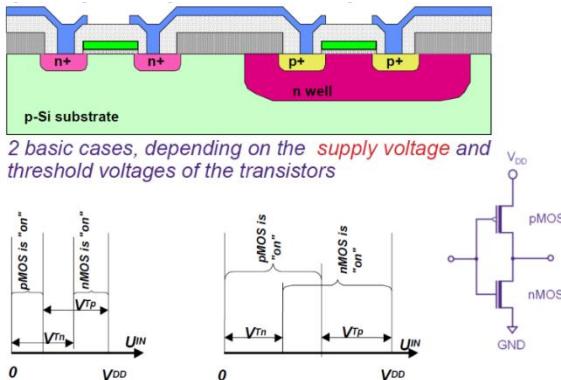
$$V_{BE} \approx 0.8V$$

$$V_{BC} \approx 0.7V$$

$$V_{CE} = V_{BE} - V_{BC} = 0.1V$$

There is a 0.1V drop across the transistor from collector to emitter which is quite low while a substantial current flows through the device. In this mode it can be considered as having a very high conductivity and acts as a closed switch with a finite resistance or conductivity.

8. Describe the qualitative operation of a CMOS inverter (cross-section view, characteristic figures and equations, capacitances, power consumption)! The deduction of the equations are not needed.



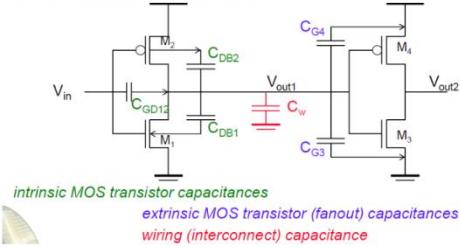
1. small supply voltage:

$V_{DD} < V_{Tn} + |V_{Tp}|$   
only one transistor is "on" at a time

2. larger supply voltage

$V_{DD} > V_{Tn} + |V_{Tp}|$   
when switching over, both transistors are "on" at the same time

- ▶ Intrinsic capacitances of the driving stage
- ▶ Input capacitance of the loading stage (next gate) – extrinsic or fanout capacitances
- ▶ wiring (interconnect) capacitance



## Power consumption of CMOS inv.:

- ▶ There is no static consumption since there is no static current
- ▶ There is dynamic consumption during switching which consists of 2 parts:
  - Mutual conduction:
    - During the rise of the input voltage both transistors are "on"

$$V_{Tn} < U_{IN} < V_{DD} - V_{Tp}$$

- Charge pumping:

- At switching over the output to 1 the  $C_L$  loading capacitor is charged to the supply voltage through the p transistor, then it is discharged towards the ground through the n transistor.

*Charge is pumped from VDD to GND.*



9. Describe the issues of global IC design and manufacturing! (major and minor problems, costs of manufacturing, design, ways of reducing costs, proportional costs)

► Functionality

► Costs

- One-time, fix costs or *non-recurring engineering costs (NRE)* – e.g. labor cost of design
- proportional costs (*RE*) – materials, packaging, testing

► Reliability, robustness

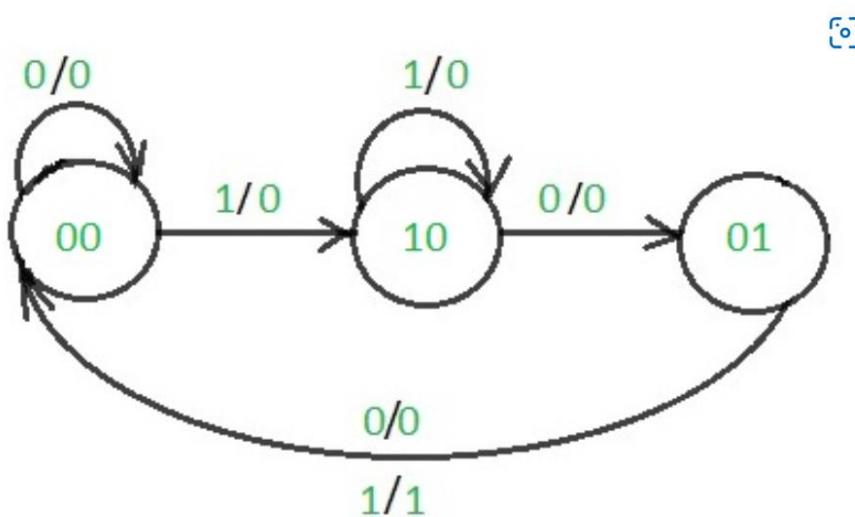
- noise margins
- noise immunity

► Performance

- speed (delays)
- dissipation (energy consumption)

► Time-to-market

10. Draw the state diagram of a VHDL design that takes d as a serial bit stream input and outputs a logic '1' whenever the sequence "101" occurs



## Coding for VHDL circuit

### Dataflow

```
1. library ieee;
2. use ieee.std_logic_1164.all;
3.
4. entity half_adder is
5.   port (a, b: in std_logic;
6.         sum, carry_out: out std_logic);
7. end half_adder;
8.
9. architecture dataflow of half_adder is
10. begin
11.   sum <= a xor b;
12.   carry_out <= a and b;
13. end dataflow;
```

### Behavioural

```
1. library ieee;
2. use ieee.std_logic_1164.all;
3.
4. entity half_adder is
5.   port (a, b: in std_logic;
6.         sum, carry_out: out std_logic);
7. end half_adder;
8.
9. architecture behavior of half_adder is
10. begin
11.   ha: process (a, b)
12.   begin
13.     if a = '1' then
14.       sum <= not b;
15.       carry_out <= b;
16.     else
17.       sum <= b;
18.       carry_out <= '0';
19.     end if;
20.   end process ha;
21.
22. end behavior;
```



### Structural

```
1. library ieee;
2. use ieee.std_logic_1164.all;
3.
4. entity half_adder is -- Entity declaration for half adder
5.   port (a, b: in std_logic;
6.         sum, carry_out: out std_logic);
7. end half_adder;
8.
9. architecture structure of half_adder is -- Architecture body for half adder
10.
11.   component xor_gate -- xor component declaration
12.   port (i1, i2: in std_logic;
13.         o1: out std_logic);
14.   end component;
15.
16.   component and_gate -- and component declaration
17.   port (i1, i2: in std_logic;
18.         o1: out std_logic);
19.   end component;
20.
21. begin
22.   xor_gate port map (a, b, sum);
23.   and_gate port map (a, b, carry_out);
24. end structure;
```

# CSA: Concurrent Signal Assignment

- Each architecture consists of concurrent statements, which are executed concurrently with respect to simulated time
  - The order of execution of the statements is dependent upon the flow of values and not on the textual order of the program
- CSA: Concurrent Signal Assignment
  - This is a major difference between VHDL and ordinary computer languages Types
    - Simple CSAs
    - Conditional CSAs: **when statement**
    - Selected CSAs: **with – select statements**

```
b <= "1000" when a = "00" else
      "0100" when a = "01" else
      "0010" when a = "10" else
      "0001" when a = "11";
```

```
with a select b <=
  "1000" when "00",
  "0100" when "01",
  "0010" when "10",
  "0001" when "11";
```

VHDL sequential statement example:

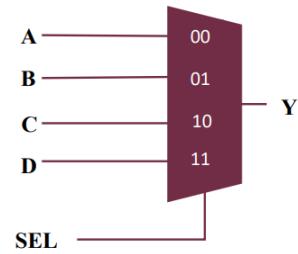
```
architecture behavioral of Question1 is
begin
  process(D)
  begin
    case D is
      when "0000" | "1110" =>
        Y <= "0011";
      when "0001" | "0100" | "0101" | "0110" | "0111" | "1010" | "1011" | "1100" | "1111" =>
        Y <= "0000";
      when "0010" | "1001" =>
        Y <= "0110";
      when "0011" | "1101" =>
        Y <= "1100";
      when "1000" =>
        Y <= "1001";
      when others =>
        null;
    end case;
  end process;
end architecture behavioral;
```

## Case Statement

- Syntax:

```
case expression is
    when choice1 => {statements}
    when choice2 => {statements}
    when others => {statements}
End case;
```

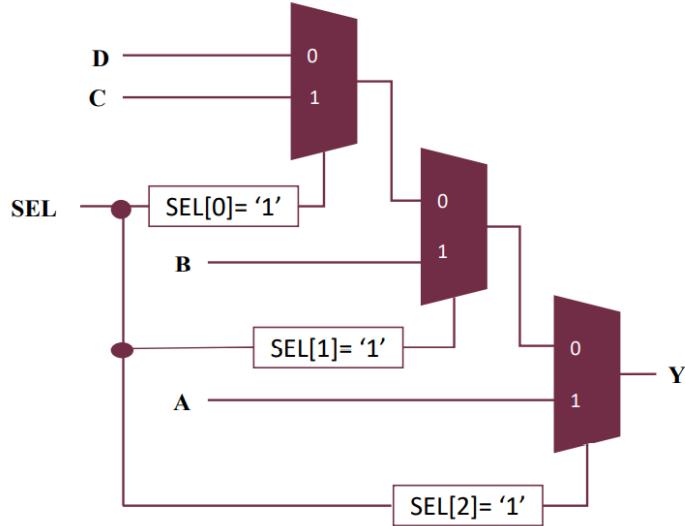
```
process (sel, a, b, c, d)
begin
case sel is
    when "00" => Y <=a;
    when "01" => Y <=b;
    when "10" => Y <=c;
    when others => Y <=d;
end case;
end process;
```



- “Case” statement is a series of parallel checks to check a condition.
- Statements following each “when” clause is evaluated only if the choice value matches the expression value.
- Corresponds to “with...select” in concurrent statements

## If Statement

```
process (sel, a, b, c, d)
begin
if sel(2) = '1' then
    y <= a;
elsif sel(1) = '1' then
    y <= b;
elsif sel(0) = '1' then
    y <= c;
else
    y <= d;
end if;
end process
```



Generates a priority structure.

Corresponds to “when-else” command in the concurrent part.

## Process statement

- Two types of processes
  - Combinatorial (asynchronous)
  - Clocked (synchronous)

### Combinatorial Process (asynchronous)

- Generates combinational logic.
- All inputs must be present in the sensitivity list.

```
process (a, b, c)
begin
  x <= (a and b) or c;
end process;
```

### Clocked Process (synchronous)

Any signal assigned under a clk' event generates a flip-flop

```
process (clk)
begin
  if (clk' event and clk = '1') then
    Q <= Data;
  end if;
end process;
```



### -- Edge-triggered flip flop/register

```
entity DFF is
  port (D,CLK: in bit;
        Q: out bit);
end DFF;
architecture behave of DFF is
begin
  process(clk) -- "process sensitivity list"
  begin
    if (clk'event and clk='1') then      -- rising edge of clk
      Q <= D;                         -- optional "after x" for delay
      QB <= not D;
    end if;
  end process;
end:
```

