# Analog Circuit Design II.
# Circuit simulation of CMOS logic gates

In this lab, we will use LTspice XVII again with the AMS 350 nm integrated technology library.

Start the circuit design tool by clicking its icon on your desktop or by using the Start menu shortcut (path: "C:\Program Files\LTC\ LTspiceXVII\XVIIx64.exe").

Use the File - New Schematic command to create a new wiring diagram. Components, wiring and simulation commands can be placed here.

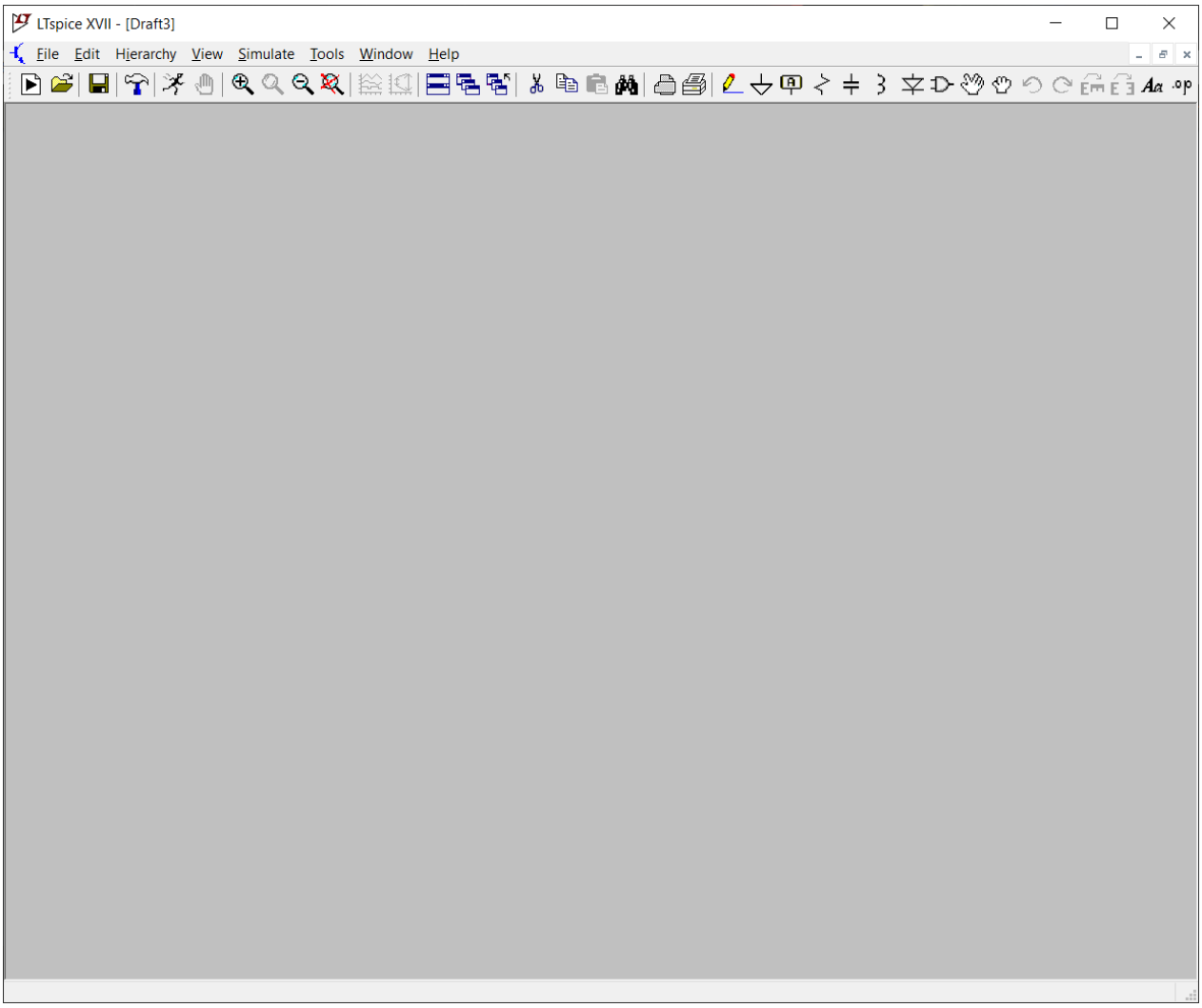


*Figure 1. Schematic design window of LTspice*

Click on the Edit drop-down menu to see a list of commands needed to create the schematic, with shortcuts enclosed in apostrophes. Some follow logical pattern (e.g. resistance - 'R'), but there are some interesting ones (e.g. wire - F3, undo (Ctrl + Z) - F9).

## Simulation of a NAND gate

Select Edit – Component 'F2', where we can select a component from the default folder (*C:\Users\USERNAME\Documents\LTspiceXVII\lib\sym\).* The folders are in square brackets, and they contain more components. Please choose *AMScellsDigit* folder, and ***n4*** component*, and place two.* (If you cannot find *AMScellsDigit* here, please try to copy the content of the .zip file into the right folder). Now go back to Edit – Component 'F2', select *AMScellsDigit* folder, and ***p4*** component, and place two, (Fig. 2).

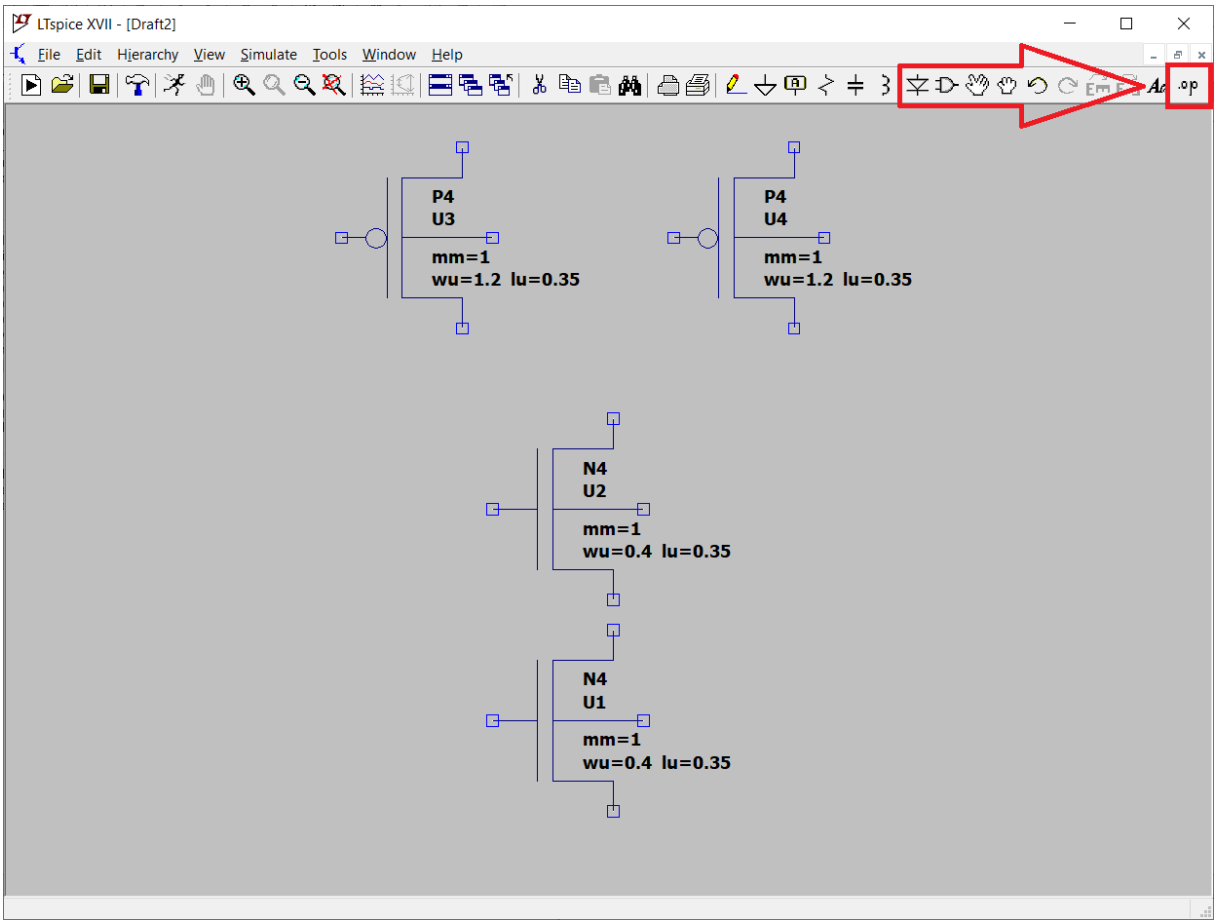


*Figure 2. Placement of MOS transistors*

Now we have to click on the .op button (indicated in Fig.2.) to create a SPICE Directive. Here we can define the path of the model file. Insert this line below:

```
.include c:\ltspice\sub\AMSLev49Digit.sub
```

And place it somewhere on the schematic (like in Fig.3.).

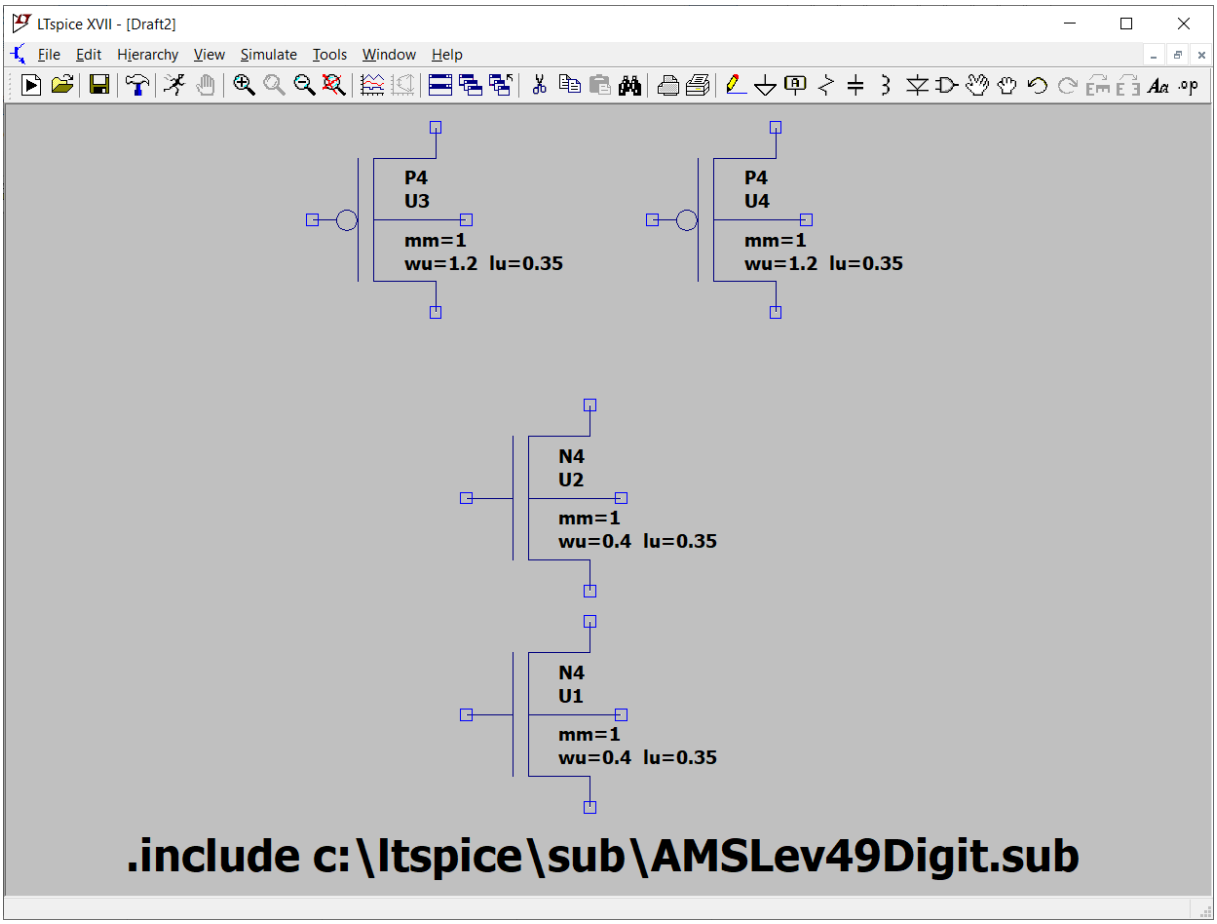


*Figure 3. Adding SPICE Directive*

Now we have to insert three voltage sources, one for the power supply, and two for the inputs.

From Edit – Component ’F2’ choose ’voltage’ (you might have to go back from a subfolder clicking on[..]), and place three of it.

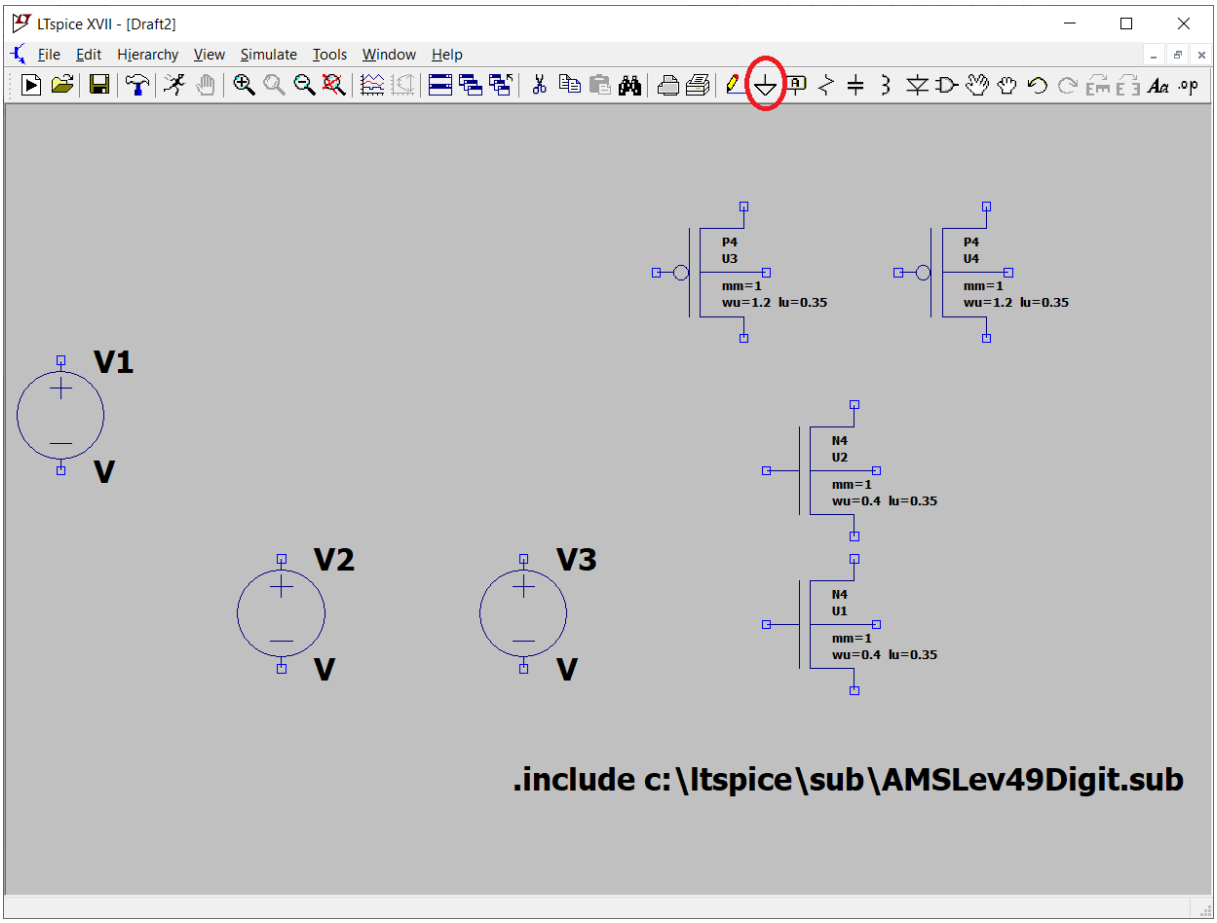


*Figure 4. Insert the Grounds*

Now place four Ground components (see Fig. 4.). After you finished it, add an output port to the circuit. Select  button, and Set the Port Type to Output, and write *out* into the input field.

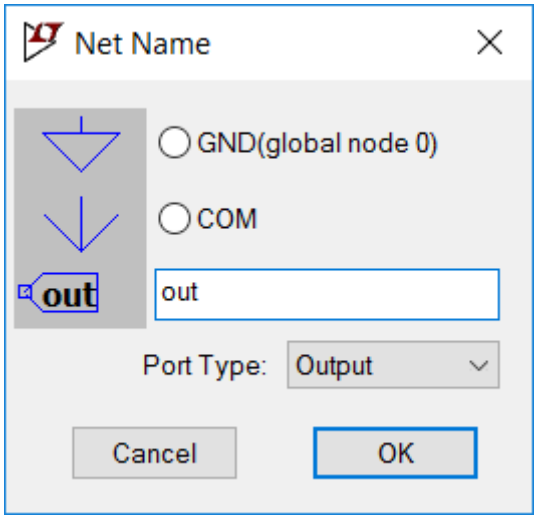


*Figure 5. Naming the net*

Instead of complicated wiring, we can use net labels. If the name of two wire labels is the same, the wires are (virtually) connected together.

But first, wire some part of the circuitry using Edit – Draw wire ‘F3’ command, as it can be seen in Fig. 5.

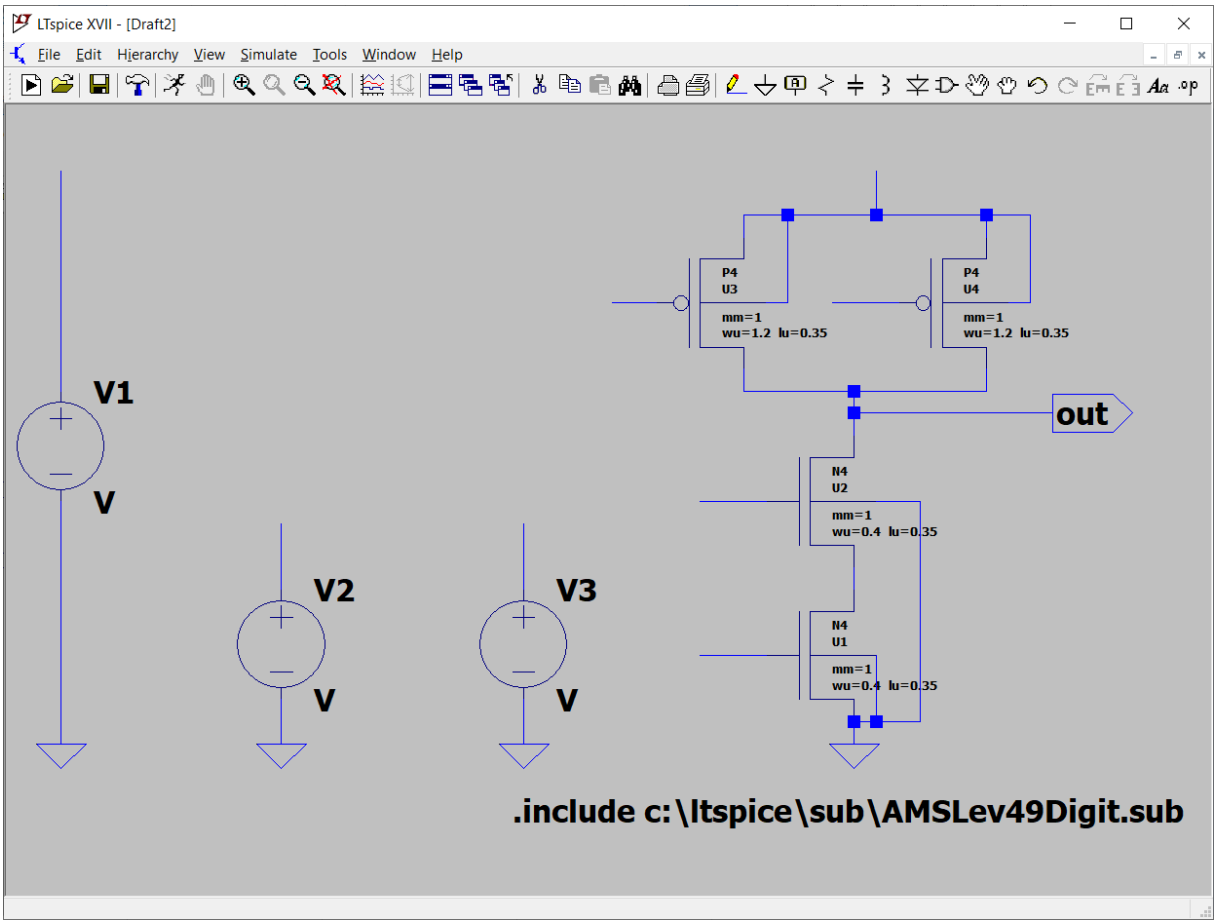


*Figure 6. Wiring the schematic*

Now we have to add the labels. Two *vdd*s for positive power supply, three *A*s for input signal A, and three *B*s for input signal B. To do this, please click on Label Net icon  .

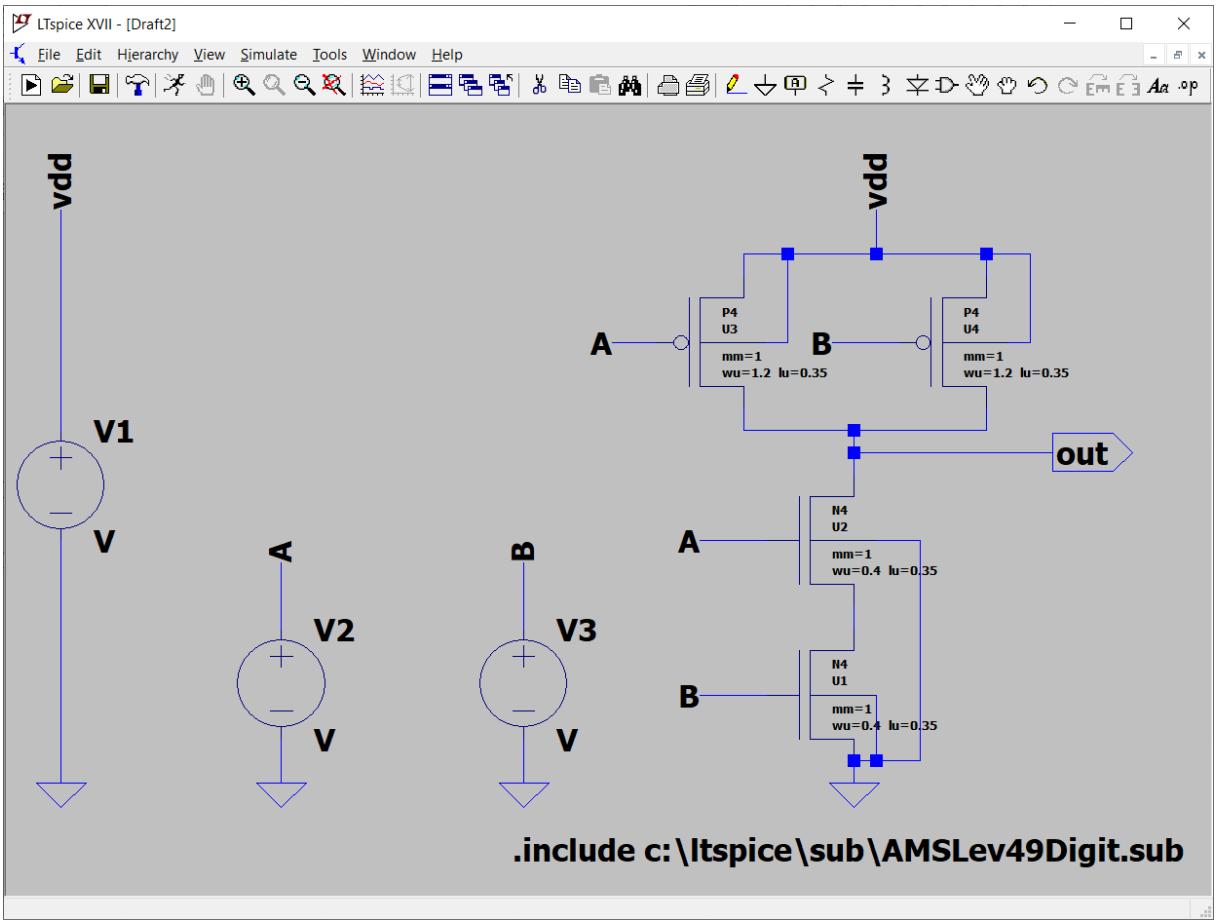


*Figure 7. Wired schematic*

Now we have to set the voltage of the voltage sources. We can do it by clicking the right mouse button on it. The power supply voltage (vdd) has to be 5 V (see Fig.6.).

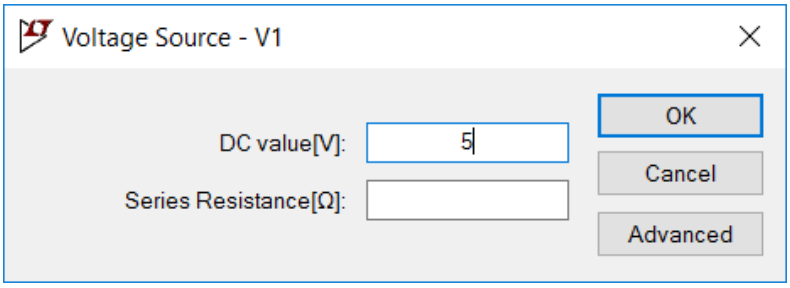


*Figure 8. Power supply voltage*

At this point, we need to create the input waveform. Let set A as LSB. The frequency is 100 MHz,50% duty cycle, 5 V of amplitude, 10psec long rising and falling edge.

Right mouse click on V2 source (A signal), Advanced, Function: PULSE and set the parameters according to Figure 9.

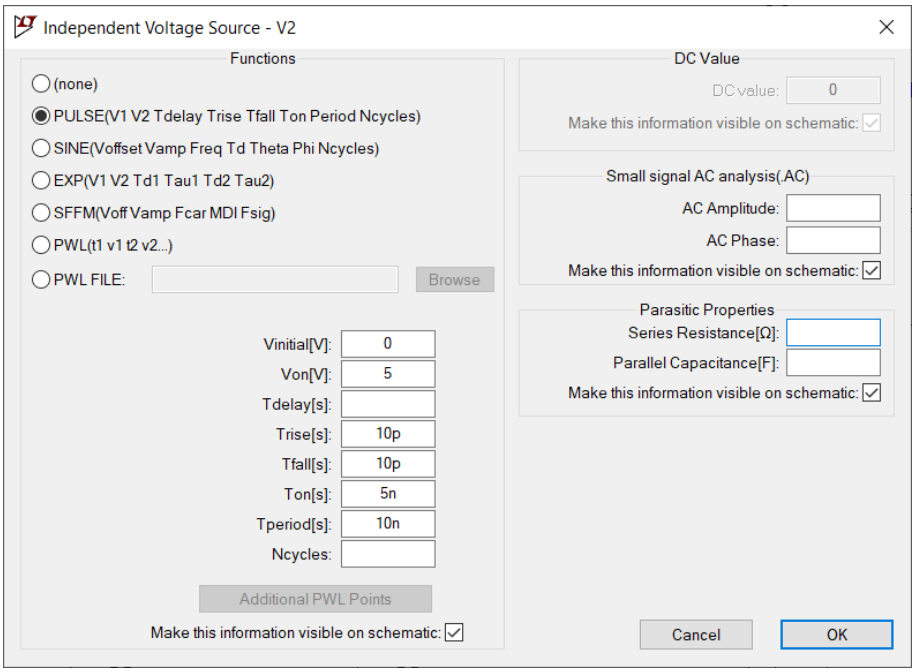


*Figure 9. Settings for signal A*

For signal B, the period and the $T_{on}$ have to be double (Figure 10).

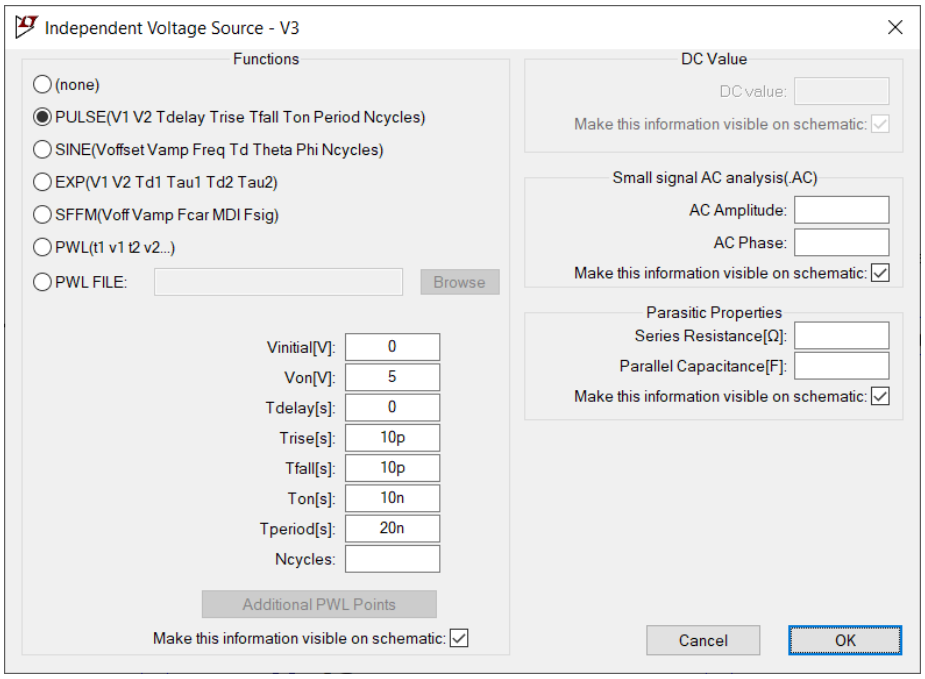


*Figure 10. Settings for signal B*

## Transient simulation

Now we are ready for the simulation. Select Simulate – Edit Simulation Cmd, and choose Transient tab. Fill the input field, as it can be seen in Figure 11.

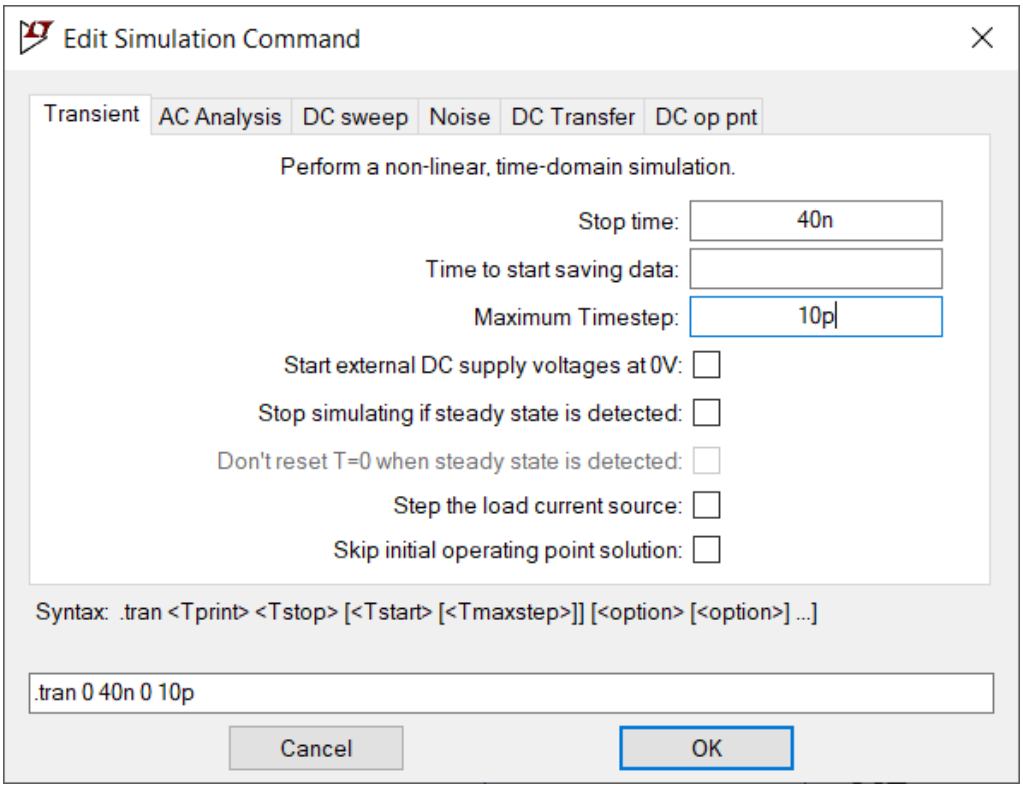


*Figure 11. Transient simulation settings*

If you are done, click on OK, and place the simulation command on the schematic. Select  button to perform the simulation. If everything is done, you can see an empty diagram like in Figure 12.

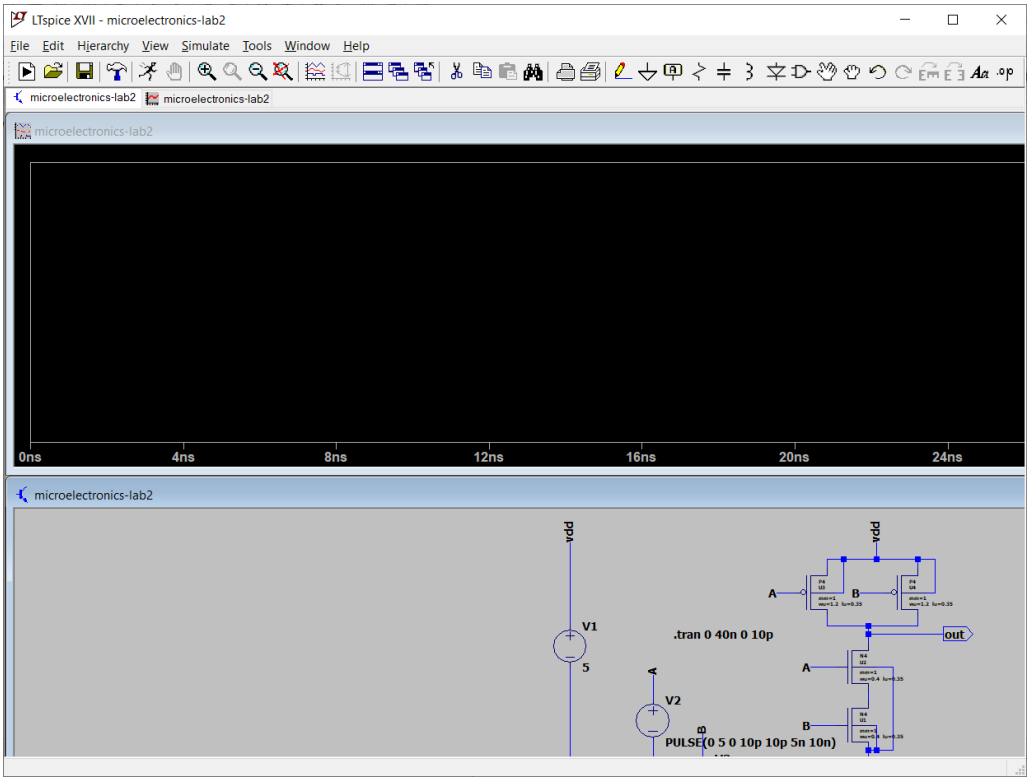


*Figure 12. Simulation diagram without waveforms.*

If you click on the input wires (the wire from the positive terminals of the V2 and V3 voltage sources) and the output wire, you can get the transient response of the logic gate. Please insert the screenshot of the waveforms.

## Decrease the frequency of the input signal to 10 MHz (for the LSB)

- Hints:
  - There are TWO sources.
  - Don't forget to maintain the simulation stop time.

Compare the waveform with the result of the previous simulation.

## Simulation and identification of a complex logic gate

Please modify the schematic (or you can start with an empty schematic) to get the same as it can be seen in Figure 13.

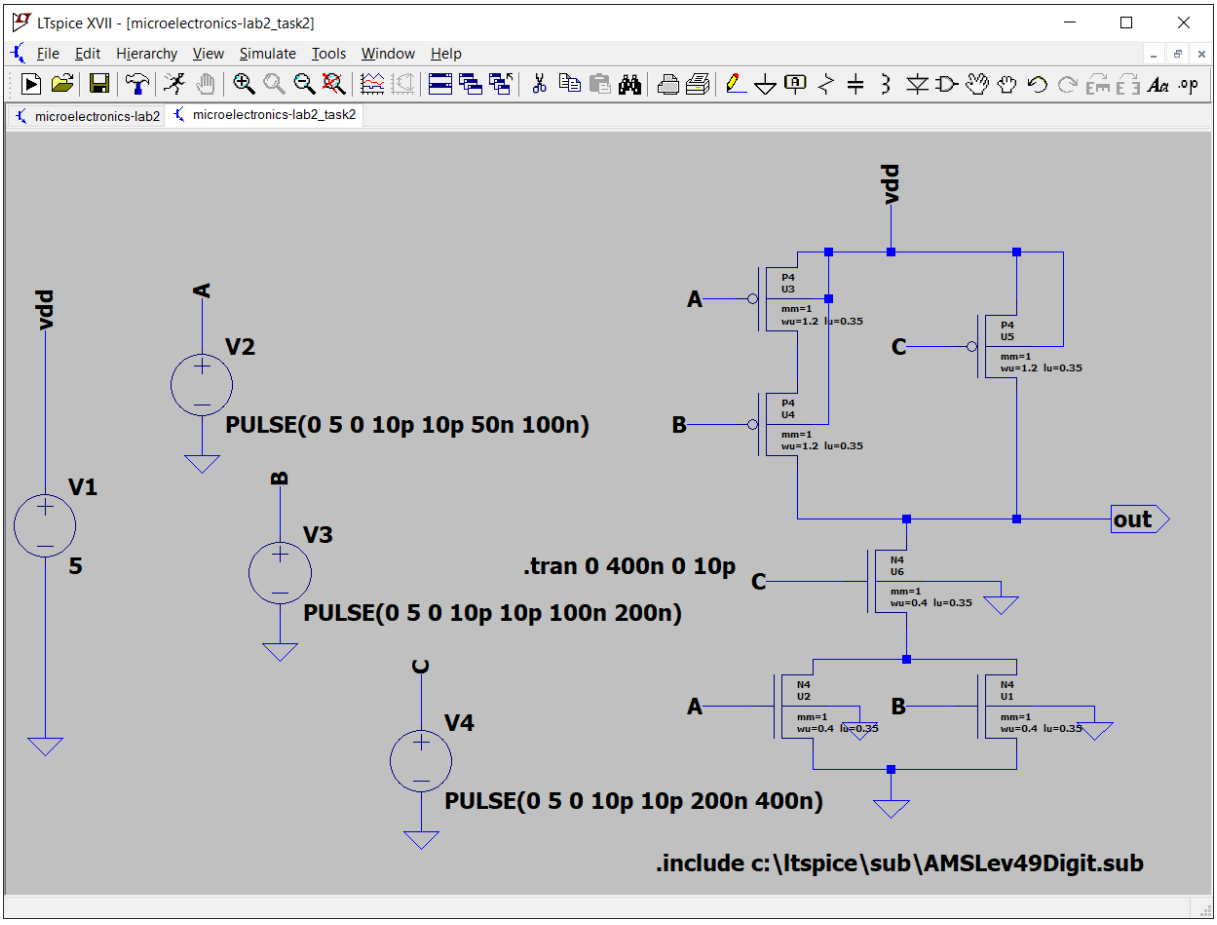


*Figure 13. Schematic diagram of a CMOS complex logic gate*

Perform a transient simulation with the same settings as in the previous task. Plot the inputs (A, B, and C, and the output waveforms), and insert them to the lab report.

Create a truth table. Try to find out the logic function of the complex gate.