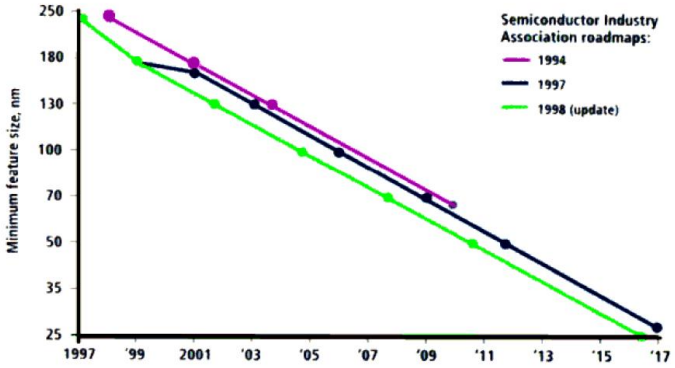
I. Short questions (2 points each)

1. What is the MFS? What is the size of the MFS today?

Minimal Feature Size,
– the smallest (thinnest) feature that you can create on the top of a silicon wafer (substrate)
14 nm or even less



2. What is a wafer? What is the size of a wafer today?

Thin slice of semiconductor material such as crystalline silicon.

► Today at around 30cm in diameter (8") or even 12"

3. What is a cleanroom? What does Class 100 cleanroom means?

A room where the tiny structures are created on the wafers.
Cleanrooms are classified according to number and size of particles permitted per volume of air. 29(>=5um)

4. Describe Moore's law! What is "more than Moore integration"?

►In every 14..18 months, the number of transistors integrated in a chip will double(exponential growth)

This prediction is valid even today.

►*More than Moore*: further increase of integration density, e.g. 3D stacking of chips (RAM-s, pen drives)

5. List at least 3 main properties of the Silicon?

Crystal structure,
Semiconductor,
Abundant

---

6. What does <100> orientation means? For which type of semiconductor does good for?

The related symbol [abc] indicates the direction in the crystal normal to the (abc) plane.
Silicon wafers are usually cut along the (100) plane to obtain good device performance

7. What does <1111> orientation means? For which type of semiconductor does good for?

New material layer is formed over the entire surface of the wafer
Growth of epitaxial layer (continues the Si-lattice but doped
Oxidation (deposit/grow SiO_2) evaporation (e.g. deposit metal such as Al)

---

8. What does layer growth means? Describe two layer growth processes!

New material layer is formed over the entire surface of the wafer
Growth of epitaxial layer (continues the Si-lattice but doped
Oxidation (deposit/grow SiO_2) evaporation (e.g. deposit metal such as Al)

9. What does layer deposition means? Describe two deposition process!

New material layer is formed over the entire surface of the wafer
Deposition of a photo-sensitive lack (photoresist)
In-depth deposition of external material: ion implantation

---

10. What does patterning deposition means? Describe two patterning process!

Some patterns are formed in the deposited layer
Deposition of a photo-sensitive lack (photoresist)
Photographing the pattern onto the lack
Developing the photoresist: pattern formed in the resist layer

---

11. Describe the procedure of the diffusion!

- Dopants diffuse in the high temperature Si-lattice
- The energy of the Si atoms helps the dopants move

12. Describe the procedure of the ion implantation!

- From an ion beam one selects the ions that target the Si and penetrate the lattice
- Initial distribution of deposited dopants depends on the energy and the dose of the ion beam
- Thermal treatment follows the implantation
  - restore the Si-lattice
  - drive-in the dopants (form final doping profile)

~100 kV voltage is used

It is a **low temperature** process.
Advantage: existing profiles are less effected

---

13. What are the energy bands in the lattice?
14. What is the valance band in the lattice?
15. What is the conductance band in the lattice?
16. Describe the generation in the lattice!
17. Describe the recombination in the lattice!

알쥐??

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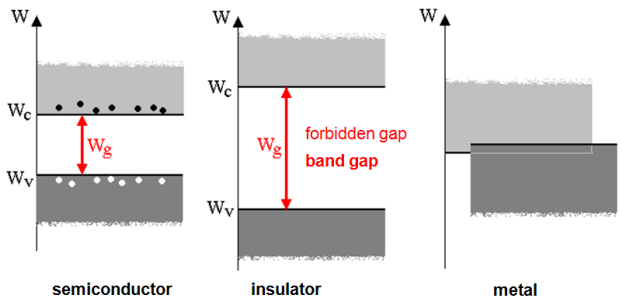
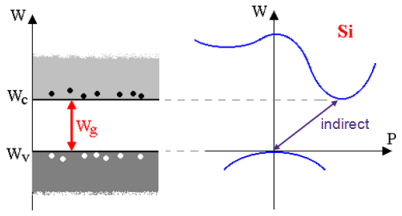
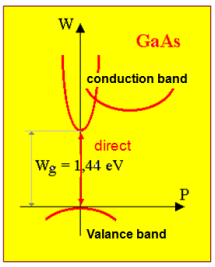
18. What is the difference between conductor, semiconductor and a metal, in terms of energy bands?



19. What does indirect band mean?
20. What does direct band mean?



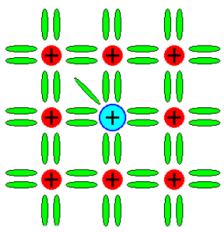


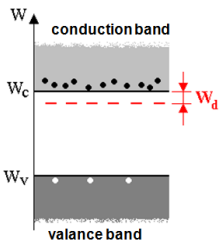
$$W = \frac{1}{2m} p^2 \rightarrow W = \frac{1}{2m_{eff}} P^2$$

$$F = \frac{dP}{dt} \qquad P = \frac{h}{2\pi} k$$

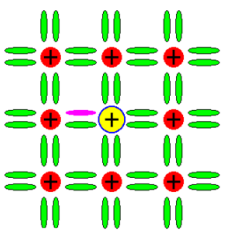
GaAs: direct band ⇒ opto-electronic devices (LEDs)
Si: indirect band

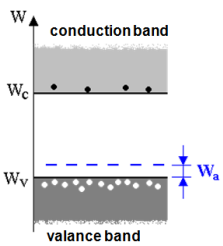
21. What does donor-doping mean?





22. What does acceptor-doping mean?





23. What is the Fermi-level?

The energy level where the probability of occupancy is 0.5

$$f(W) = \frac{1}{1 + \exp\left(\frac{W - W_F}{kT}\right)} = 0.5$$

---

24. Describe the mass action law!

$$n \cdot p = n_i^2$$

Mass action law

25. What is the doping profile?

Doping profile: dopant concentration as function of depth

---

26. Briefly describe temperature dependence of a diode!

If T is increased,
Majority carrier concentration is not changed.
The only minority carrier concentration is increased according to

$n_i^2 =$ $$n \cdot p = const \cdot T^3 \exp\left(-W_g / kT\right)$$

27. Briefly describe temperature dependence of an npn BJT!

???

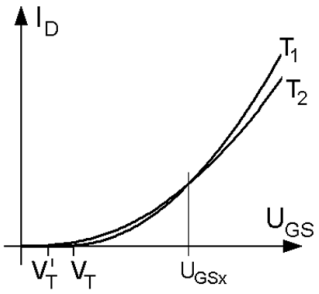
28. Briefly describe temperature dependence of a MOSFET!

T is increased, Vt is decreased

$$I_D = \frac{W}{L}\frac{\mu C_0}{2}(U_{GS} - V_T)^2$$

$$\frac{1}{\mu}\frac{d\mu}{dT} = -0{,}003 \ldots -0.006 / ^{o} C$$

$$\frac{\partial V_T}{\partial T} = -1{,}5 \ldots -4\, mV / ^{o} C$$



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29. Provide the total current equation for the electrons in semiconductors! Name each parameter!

$$\overline{J_n} = qn\mu_n \overline{E} + q D_n \overline{\text{grad}\ n}$$

$$\overline{J_p} = qp\mu_p \overline{E} - q D_p \overline{\text{grad}\ p}$$

q : charge
n : density of electrons
p : density of holes
u_n : electron mobility
u_p : hole mobility
D : coefficient of diffusion current.

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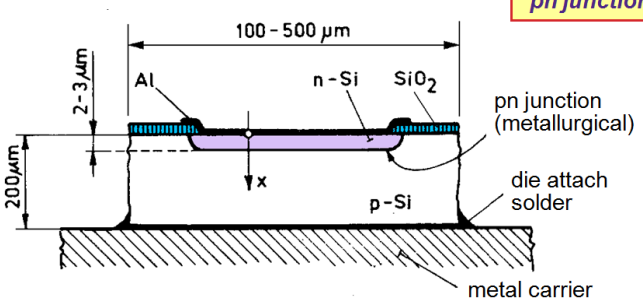
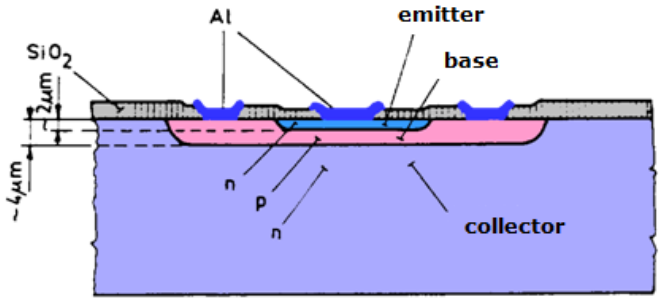
30. Draw and provide the cross sectional view and the characteric equation of a diode!

"pn junction"

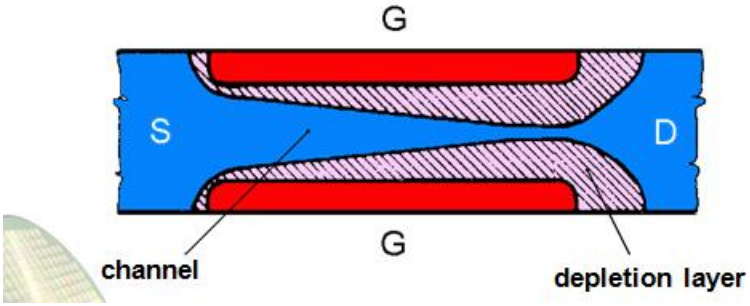


31. Draw and provide the cross sectional view and the characteric equation of an npn BJT!



I_E = I_C + I_B

32. Draw and provide the cross sectional view and the characteric equation of a JFET



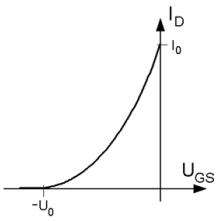
$$I_D = I_0\left[F(U_{GS}) - F(U_{GD})\right]$$

For all regions!

$$F(U) = \begin{cases} 3\dfrac{U}{U_0} + 2\left(\dfrac{-U}{U_0}\right)^{3/2} & if \quad U \geq -U_0 \\ F(-U_0) = -1 & if \quad U < -U_0 \end{cases}$$

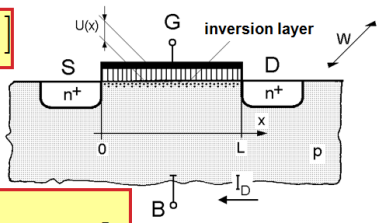
Only in saturation:

$$I_D = I_0\left(3\frac{U_{GS}}{U_0} + 2\left(\frac{-U_{GS}}{U_0}\right)^{3/2} + 1\right)$$



33. Draw and provide the cross sectional view and the characteric equation of a MOSFET!

$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left[(U_{GS} - V_T)^2 - (U_{GD} - V_T)^2\right]$$



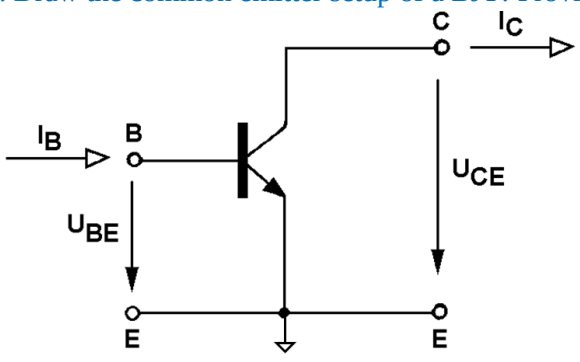
$$I_D = \frac{W}{L}\frac{\mu C_0}{2}\left[F(U_{GS}) - F(U_{GD})\right]$$

$$F(U) = \begin{cases} (U - V_T)^2 & \text{if} \quad U > V_T \\ 0 & \text{if} \quad U \leq V_T \end{cases}$$

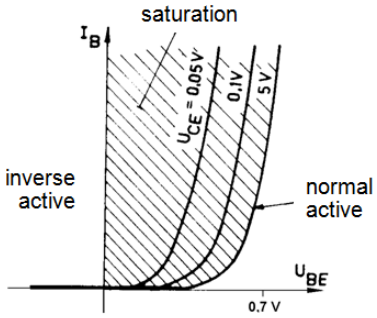
For all regions of operation!

---

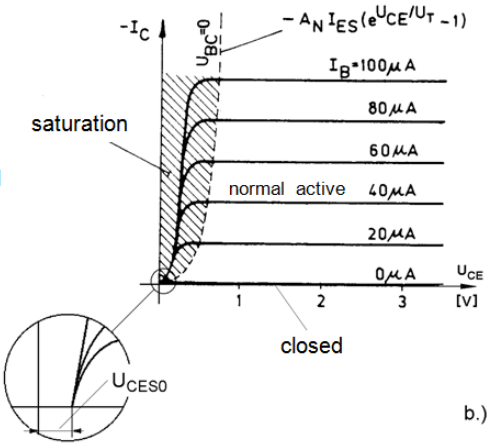
34. Draw the common emitter setup of a BJT! Provide the output characteristics as well!



Input characteristic:

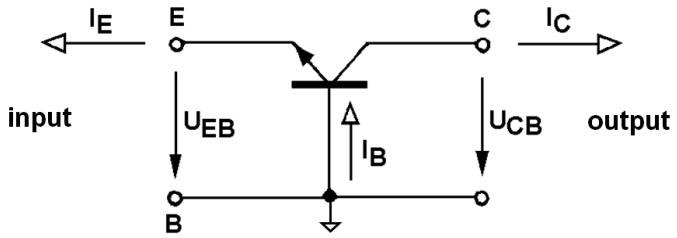


Output characteristic:

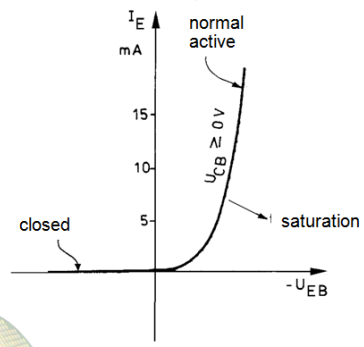


a.) b.)

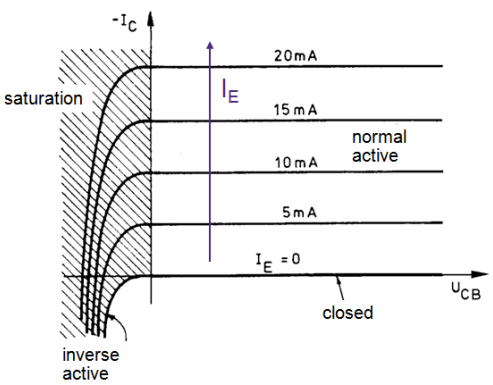
35. Draw the common base setup of a BJT! Provide the output characteristics as well!



Input characteristic:



Output characteristic:



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36. Briefly describe two secondary effects in the BJT! (1-1 sentence)

- Series resistance
- The Early effect - The output voltage influences the input characteristic dependence of current gain
- Voltage dependence : due to the Early effect

37. Briefly describe two secondary effects in the diode! (1-1 sentence)

- Series resistance – Appears at the high current levels
  - Solution : Epitaxial structure
- Generation current – In reverse region
- Recombination current – Phenomenon appearing in the forward region

38. Briefly describe two secondary effects in the MOSFET! (1-1 sentence)

Channel length reduction : Vt is decreased – velocity saturation
Narrow channel operation : Vt is increased

Temperature dependence
Subthreshold current

---

39. What are the rules of thumb to follow if you want to design two “identical” components in an IC? (“Identical” means “as similar as possible”.) List at least 3 aspects!

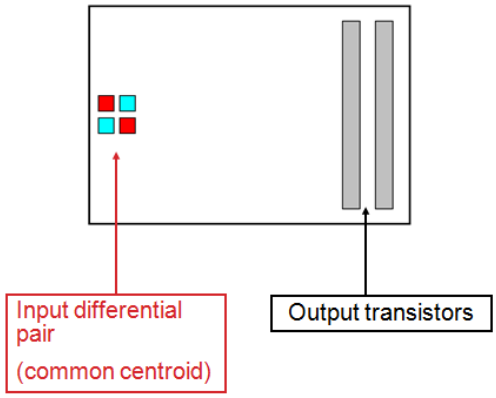
Same layout shape
Same position / orientation
Same temperature
Close to each other
Larger than minimal size

---

40. What is the stability simulation good for?
41. What is the DC simulation good for?
42. What is the AC simulation good for?
43. What is the transient simulation good for?

---

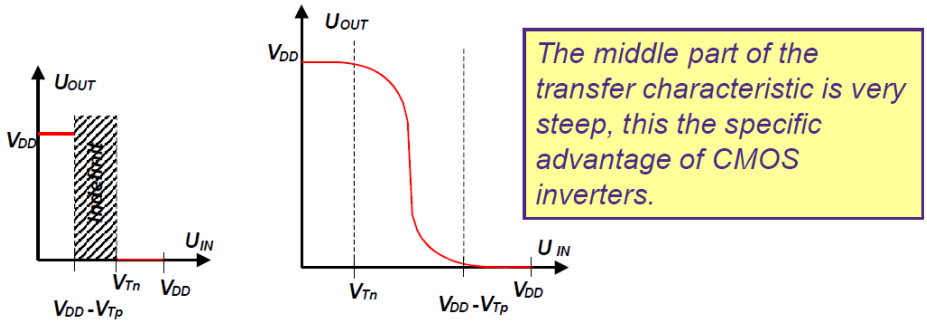
44. Considering thermal management concepts: where should we put the main dissipater on the substrate? Why?



Because of thermal effects in the output impedance

---

45. Draw the static transfer characteristic of a CMOS inverter!



46. Draw the tstatic transfer characteristic of a CMOS inverter!

---

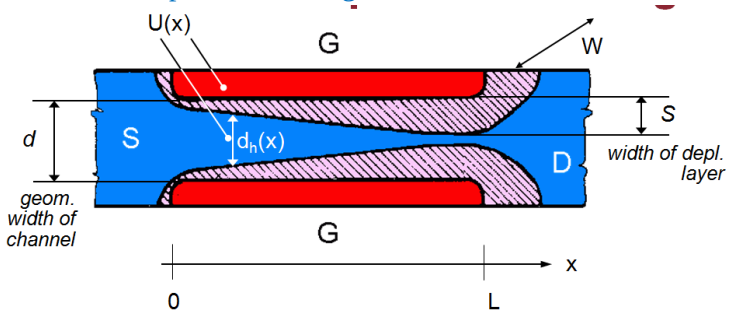
47. Provide 3 design issues in digital IC design! (1-1 sentence)

Cost reduction

Design and manufacturing separated

Increasing complexity

48. Determine the pinch off voltage of a Si JFET, if the ….



Pinch off: *d* geom. width = 2 x width of depletion layer

$$d = 2\sqrt{\frac{2\varepsilon}{qN_d}}\sqrt{U_D - U} = 2\sqrt{\frac{2\varepsilon}{qN_d}}\sqrt{U_D + |U_0|} \qquad U_0 = \frac{qN_d}{8\varepsilon}d^2$$

49. Calculate the depletion layer thickness for an abrupt Si diode with…

$$S_p = \sqrt{\frac{2\varepsilon}{qN_a}}\sqrt{U_{np}} = \sqrt{\frac{2\varepsilon}{qN_a}}\sqrt{U_D - U} \qquad S_n = \frac{N_a}{N_d}S_p$$

50. The saturation current of a Si diode is I0=2x10-13A. Calculate the V_F forward voltage of this diode (assuming a known, fixed temperature) provided that the actual forward current of the device is I_F = 50 mA.
(For more calculations please have a look at the slides.)

$$I = I_0\left(\exp\left(U/U_T\right) - 1\right) \qquad U = U_T \ln(I/I_0 + 1)$$

Problem

Saturation current of Si diode: $I_0=10^{-13}$ A.
What is U_F, if I_F is 10 mA?

$$U \cong 0.026 \cdot \ln(10^{-2}/10^{-13}) = 0.658\ V$$

Problem

How much should we increase the forward voltage if we want to increase the current 10x ?

$$\Delta U = U_2 - U_1 \cong U_T\left(\ln(I_2/I_0) - \ln(I_1/I_0)\right) = U_T \ln(I_2/I_1)$$

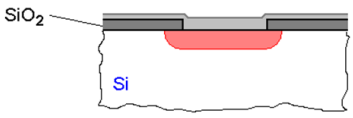
$$\Delta U = 0.026 \cdot \ln 10 \cong 0.06\ V = 60\ mV$$

III. Essay question (max 10 points):

1. Describe the steps of photolithography. Explain a number of modern photolithography methods!

Window opening

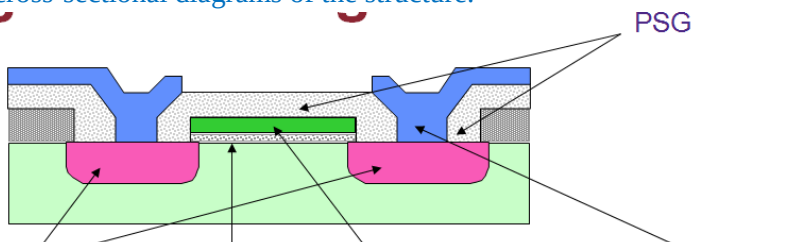
- With photolithography – always the first step of any **patterning**
- Problem of oxide steps: step coverage



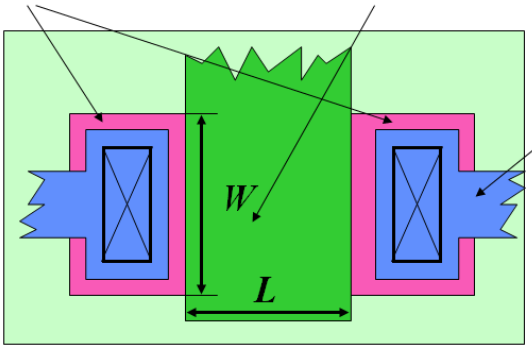
spin-coating with resist
mask alignment
UV exposure
development
oxide etching
resist removal

2. Describe the steps of the poli-Si gate self aligned nMOS process – indicate when a photomask is needed. Support the description with cross-sectional diagrams of the structure.

Structure:



Layout:



1) Open window for the active region **M**
   - photolitography, field oxide etching
2) Growth of thin oxide
3) Window for hidden contacts **M**
   - Contacts the poli-Si gate (yet to be deposited) with the active region (after doping).
3) Deposit poli-Si
4) Patterning of poli-Si **M**
5) Open window through the thin oxide (etching only)

6) n+ doping:

Form source and drain regions as well as wiring by diffusion lines. Through the hidden contact poli-Si gate will also be connected to diffused lines.

7) Deposit phosphor-silica glass (PSG) as insulator

8) Open contact windows through PSG-n **M**

9) Metallization

10) Patterning metallization layer **M**

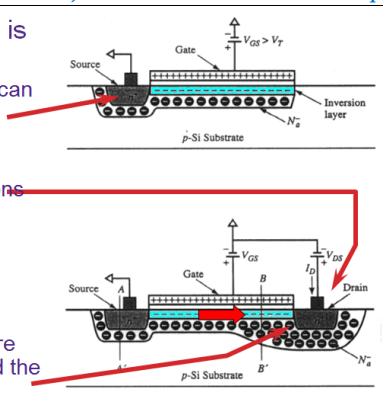
---

3. Describe the qualitative operation of a diode (**explanation,** cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

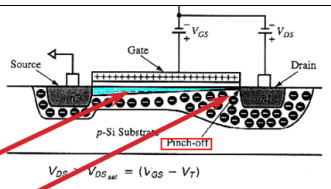
4. Describe the qualitative operation of an npn BJT (**explanation,** cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

5. Describe the qualitative operation of an n-channel enhancement mode MOSFET (**explanation,** cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

- If $V_{GS} > V_T$, inversion layer is formed
  - the n+ region at the *source* can inject electrons into the inversion channel
  - the positive potential at the *drain* induces flow of electrons in the channel,
  - the positive potential of the drain *reverse biases* the pn junction formed there
  - the electrons drifted there are all sank in the n+ region and the circuit is closed



- the charge density in channel depends on the V_{GS} voltage
- there is a *voltage drop* in the channel, thus, the thickness of the inversion layer will deminish along the channel
- at a given V_{DSsat} *saturation voltage* the thickness will reach 0, this is the so called pinch-off



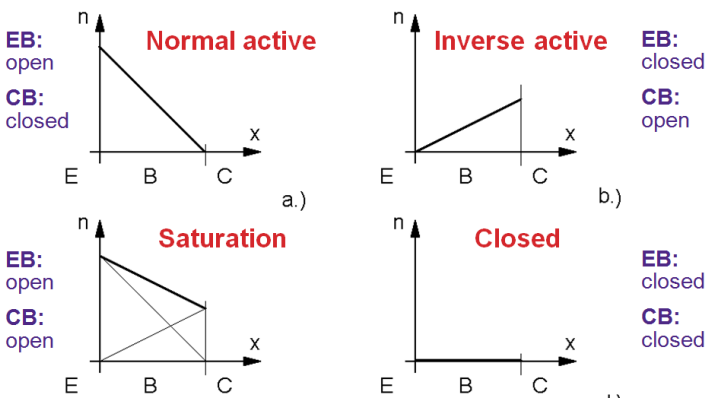
$V_{DSsat} = V_{GS} - V_T$

After this voltage is reached, the MOSFET operates ***in saturation mode, the drain voltage does not influence the drain current any longer.***

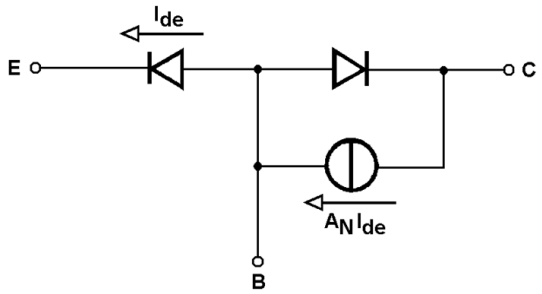
6. Describe the qualitative operation of an n-channel enhancement mode JFET (**explanation,** cross-section view, characteristic figures and equations)! The deduction of the equations are not needed.

---

7. Describe the Ebers-Moll model and the operating modes of the bipolar transistor! Provide the equations of the Ebers-Moll model as well! Indicate the different operating modes in the model as well as in the equations!

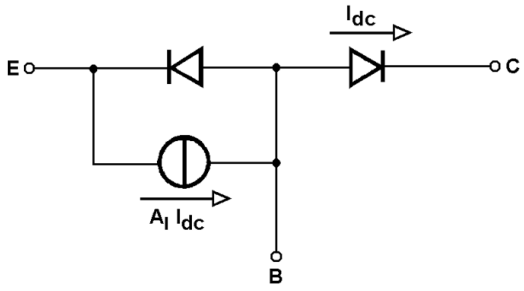


Equivalent circuit in *normal active* mode:

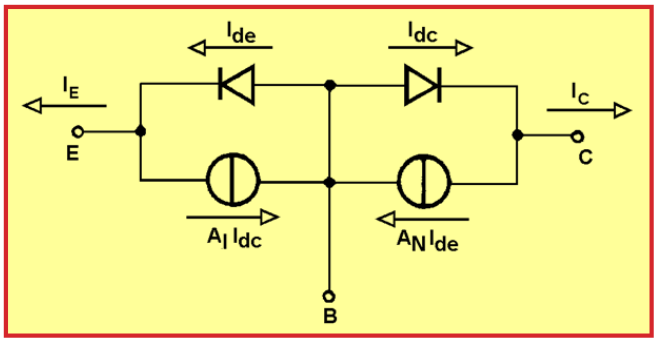


$$I_{de} = I_{ES}\left(\exp(U_{BE}/U_T)-1\right)$$

Equivalent circuit in *inverse active* mode:



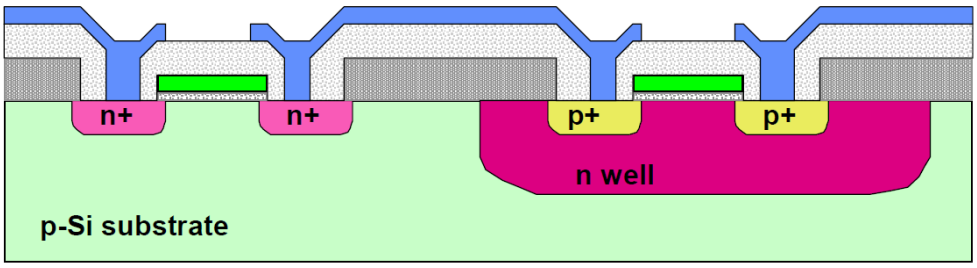
$$I_{dc} = I_{CS}\left(\exp(U_{BC}/U_T)-1\right)$$



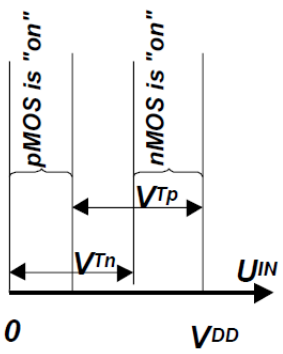
$$\begin{bmatrix} I_E \\ I_C \end{bmatrix} = \begin{bmatrix} 1 & -A_I \\ -A_N & 1 \end{bmatrix} \cdot \begin{bmatrix} I_{ES}\left(\exp(U_{BE}/U_T)-1\right) \\ I_{CS}\left(\exp(U_{BC}/U_T)-1\right) \end{bmatrix}$$

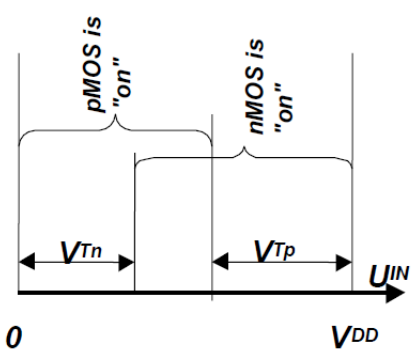
<<<<<< Saturation 이야

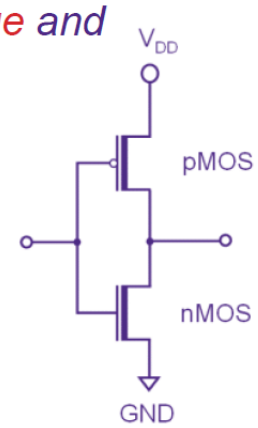
8. Describe the qualitative operation of a CMOS inverter (cross-section view, characteristic figures and equations, capacitances, power consumption)! The deduction of the equations are not needed.



2 basic cases, depending on the supply voltage and threshold voltages of the transistors







1. small supply voltage:

$V_{DD} < V_{Tn} + |V_{Tp}|$

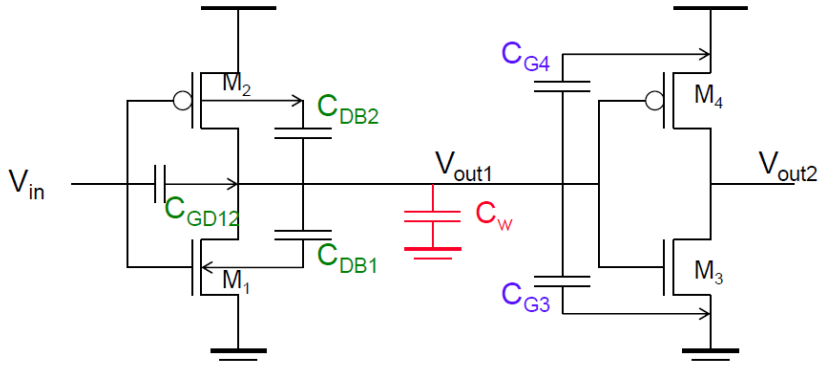
only one transistor is "on" at a time

2. larger supply voltage

$V_{DD} > V_{Tn} + |V_{Tp}|$

when switching over, both transistors are "on" at the same time

- Intrinsic capacitances of the driving stage
- Input capacitance of the loading stage (next gate) – extrinsic or fanout capacitances
- wiring (interconnect) capacitance



intrinsic MOS transistor capacitances

extrinsic MOS transistor (fanout) capacitances

wiring (interconnect) capacitance

Power consumption of CMOS inv.:

- There is no static consumption since there is no static current
- There is dynamic consumption during switching which consists of 2 parts:
  - **Mutual conduction:**
    - During the rise of the input voltage both transistors are "on"

$$V_{Tn}<U_{IN}<V_{DD}-V_{Tp}$$

  - **Charge pumping:**
    - At switching over the output to 1 the $C_{L\ loading}$ capacitor is charged to the supply voltage through the *p* transistor, then it is discharged towards the ground through the *n* transistor.

Charge is pumped from VDD to GND.

9. Describe the issues of global IC design and manufacturing! (major and minor problems, costs of manufacturing, design, ways of reducing costs, proportional costs)

- Functionality
- Costs
  - One-time, fix costs or *non-recurring engineering costs* (*NRE*) – e.g. labor cost of design
  - proportional costs (*RE*) – materials, packaging, testing
- Reliability, robustness
  - noise margins
  - noise immunity
- Performance
  - speed (delays)
  - dissipation (energy consumption)
- Time-to-market