JL2x01 1000M RGMII Delay Timing Application Note

版本信息

- 2022-02-16 初版

1. 介绍

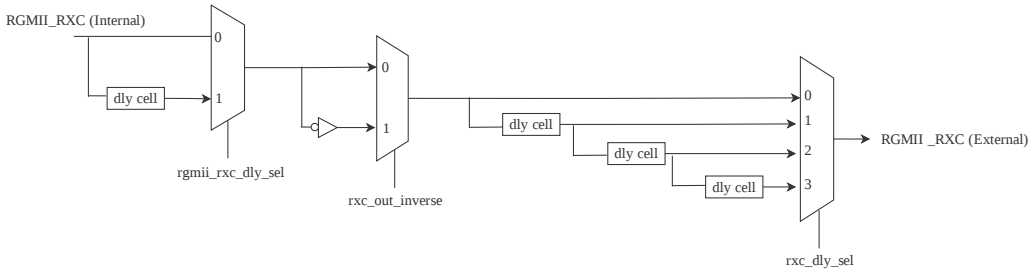
文档为用户提供JL2x01芯片在千兆模式下配置RGMII RX以及TX Delay的方法

1.1 RGMII RX DELAY

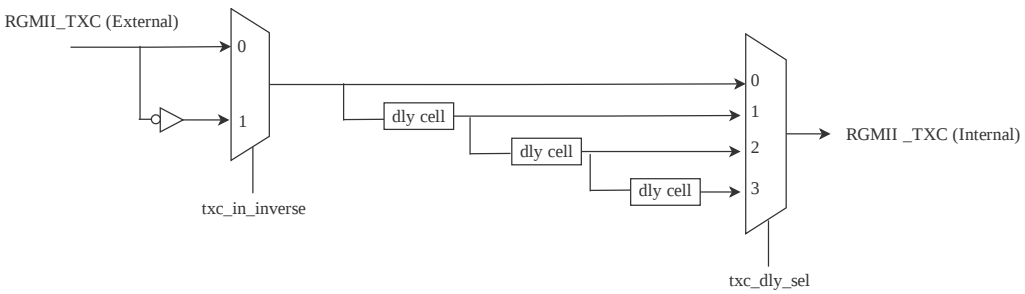
RGMII RXC Dly主要涉及到如下的几个寄存器，分别是:

- rgmii_rxc_dly_sel
- rxc_out_inverse
- rxc_dly_sel

具体的延时结构如下所示，其中RGMII_RXC (Internal)表示内部的RGMII_RXC时钟，RGMII_RXC(External)表示被延时过之后最终输出的RGMII_RXC。



1.2 RGMII TX DELAY



2. 配置寄存器

请注意，下面的寄存器中的其它字段为保留字段，不能改变。另外，需要在**软复位之后再**配置如下的寄存器，配置完立即生效。

2.1 RGMII DELAY CTRL0 REGISTER (PAGE = 171, REGISTER = 16)

Bits	Name	Default	Description
[14]	txc_in_inverse	0x0, RW	
[13:12]	txc_dly_sel	0x0, RW	
[11]	rxc_out_inverse	0x0, RW	
[10:9]	rxc_dly_sel	0x0, RW	

2.2 RGMII DELAY CTRL1 REGISTER (PAGE = 171, REGISTER = 17)

Bits	Name	Default	Description
[0]	rgmii_rxc_dly_sel	0x0, RW	

3. 例子

3.1 配置组合

RGMII RX Delay

rxc_dly_sel	rgmii_rxc_dly_sel	rxc_out_inverse	rxc dly result (参考)
0	1	0	-2ns
1	1	0	-2ns+2/3ns
2	1	0	-2ns+4/3ns
3	1	0	-2ns+2ns
0	0	0	0ns (RXDLY:0)
1	0	0	2/3ns
2	0	0	4/3ns
3	0	0	2ns
0	1	1	2ns (RXDLY:1)
1	1	1	2ns+2/3ns
2	1	1	2ns+4/3ns
3	1	1	2ns+2ns

RGMII TX Delay

txc_dly_sel	txc_in_inverse	txc dly result
0	0	0 (TXDLY:0)
1	0	2/3ns
2	0	4/3ns (TXDLY:1)
3	0	2ns
0	1	4ns
1	1	4ns+2/3ns
2	1	4ns+4/3ns
3	1	6ns

3.2 例子

配置rxc_dly_sel = 2, rgmii_rxc_dly_sel = 1, rxc_out_inverse = 1

```
write(reg = 31, val = 171)
rdata = read(reg = 16)
rdata = rdata & ~(7 << 9) # [11:9] = 0
rdata = rdata | (1 << 11) # [11] rxc_out_inverse = 1
rdata = rdata | (2 << 9)  # [10:9] rxc_dly_sel = 2
write(reg = 16, val = rdata)

write(reg = 31, val = 171)
rdata = read(reg = 17)
rdata = rdata & ~(1 << 0) # [0] = 0
rdata = rdata | (1 << 0)  # [0] rgmii_rxc_dly_sel = 1
write(reg = 17, val = rdata)
```

配置txc_dly_sel = 2, txc_in_inverse = 1

```
write(reg = 31, val = 171)
rdata = read(reg = 16)
rdata = rdata & ~(7 << 12) # [14:12] = 0
rdata = rdata | (1 << 14) # [14] txc_in_inverse = 1
rdata = rdata | (2 << 12)  # [13:12] txc_dly_sel = 2
write(reg = 16, val = rdata)
```