Applying RMA in Real-Life
(It can do more than one might think!)

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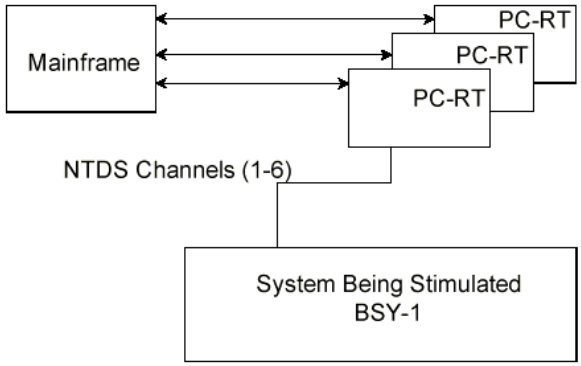
Lecture #17

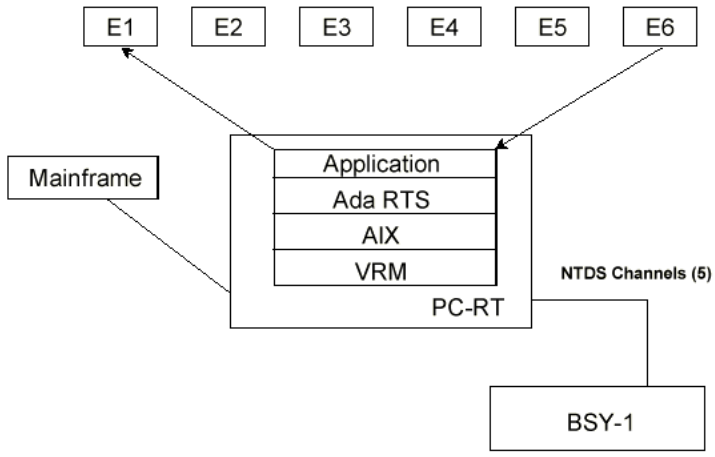
Overview of BSY-1 Submarine Trainer

- This case study is interesting for several reasons:
  - RMS is not used, yet the system is analyzable using RMA
  - "Obvious" solutions would not have helped
  - RMA correctly diagnosed the problem
- Insights to be gained:
  - Devastating effects of non-preemption
  - How to apply RMA to a round-robin scheduler?
  - Contrast conventional wisdom about interrupt handlers with the results of RMA

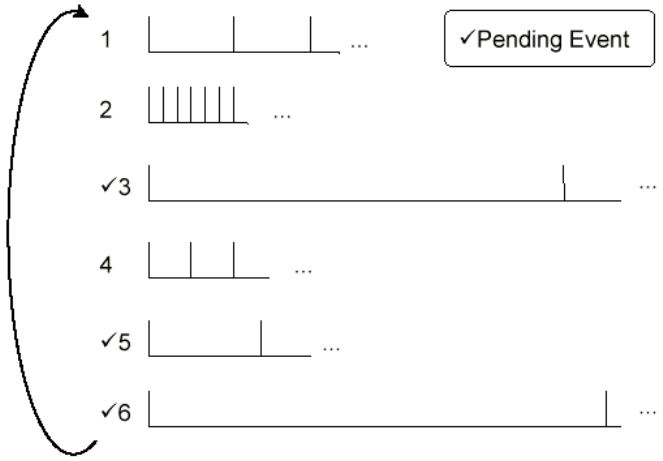
System Configuration



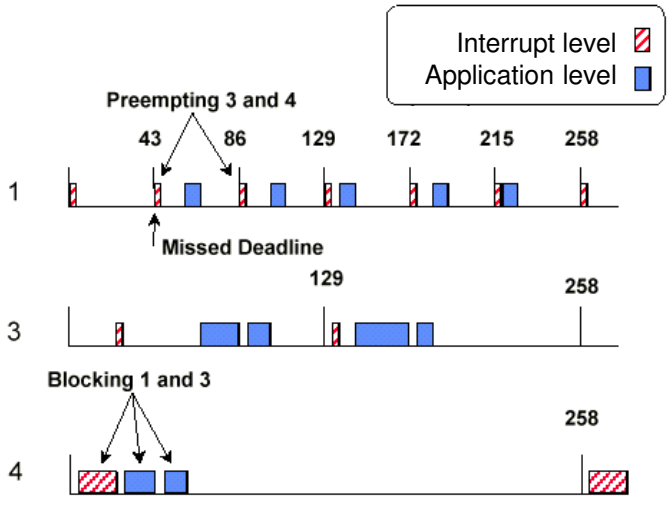
Software Design



Scheduling Discipline



Execution Sequence: Original Design



Problem Analysis by Development Team

- During integration testing, the PC-RT could *not* keep up with the mainframe computer.
- The problem was perceived to be inadequate throughput in the PC-RT.
- Actions planned to solve the problem:
  - move processing out of the application and into OS interrupt handlers.
  - improve the efficiency of AIX (IBM's Unix) signals.
  - eliminate the use of Ada in favor of C.

Data from RMA Investigation

$C = C_i$ (interrupt time) + C_a (application time)

	C_i (msec)	C_a (msec)	C (msec)	T (msec)	U
Event 1	2.0	0.5	2.5	43	0.059
Event 2	7.4	8.5	15.9	74	0.215
Event 3	6.0	0.6	6.6	129	0.052
Event 4	21.5	26.7	48.2	258	0.187
Event 5	5.7	23.4	29.1	1032	0.029
Event 6	2.8	1.0	3.8	4128	0.001
Total					0.543

$U_i = C_i/T_i$

- Observe that total utilization is only 54%; the problem is **not** insufficient throughput.

Schedulability Model: Original Design

$$(1)\ \frac{C_1}{T_1}+\left\lceil\frac{C_2+C_3+C_4+C_5+C_6}{T_1}\right\rceil\le U(1)$$

Preemption Execution Blocking

$$(2)\ \left\lceil\frac{C_{1,I}}{T_1}\right\rceil+\frac{C_2}{T_2}+\left\lceil\frac{C_{1,A}+C_3+C_4+C_5+C_6}{T_2}\right\rceil\le U(2)$$

$$(3)\ \left\lceil\frac{C_{1,I}}{T_1}+\frac{C_{2,I}}{T_2}\right\rceil+\frac{C_3}{T_3}+\left\lceil\frac{C_{1,A}+C_{2,A}+C_4+C_5+C_6}{T_3}\right\rceil\le U(3)$$

$$(4)\ \left\lceil\frac{C_{1,I}}{T_1}+\frac{C_{2,I}}{T_2}+\frac{C_{3,I}}{T_3}\right\rceil+\frac{C_4}{T_4}+\left\lceil\frac{C_{1,A}+C_{2,A}+C_{3,A}+C_5+C_6}{T_4}\right\rceil\le U(4)$$

(5) ....
(6) ....

Schedulability Test: Original Design

$$(1)\ \frac{2.5}{43}+\left\lceil\frac{15.9+6.6+48.2+29.1+3.8}{43}\right\rceil\le U(1)$$

$$(2)\ \left\lceil\frac{2.0}{43}\right\rceil+\frac{15.9}{74}+\left\lceil\frac{(0.5)+6.6+48.2+29.1+3.8}{74}\right\rceil\le U(2)$$

$$(3)\ \left\lceil\frac{2.0}{43}+\frac{7.4}{74}\right\rceil+\frac{6.6}{129}+\left\lceil\frac{(0.5+8.5)+48.2+29.1+3.8}{129}\right\rceil\le U(3)$$

$$(4)\ \left\lceil\frac{2.0}{43}+\frac{7.4}{74}+\frac{6.6}{129}\right\rceil+\frac{48.2}{258}+\left\lceil\frac{(0.5+8.5+0.6)+29.1+3.8}{258}\right\rceil\le U(4)$$

$$(5)\ \left\lceil\frac{2.0}{43}+\frac{7.4}{74}+\frac{6.6}{129}+\frac{21.5}{258}\right\rceil+\frac{29.1}{1032}+\left\lceil\frac{(0.5+8.5+0.6+26.7)+3.8}{1032}\right\rceil\le U(5)$$

$$(6)\ \left\lceil\frac{2.0}{43}+\frac{7.4}{74}+\frac{6.6}{129}+\frac{21.5}{258}+\frac{5.7}{1032}\right\rceil+\frac{3.8}{4128}+\left\lceil\frac{(0.5+8.5+0.6+26.7+23.4)}{4128}\right\rceil\le U(6)$$

Utilization: Original Design

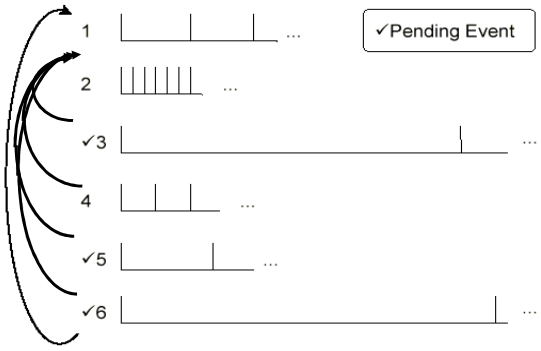
	Period (msec)	Preempt	Execute	Blocking	Total U
Event 1	43	0.000	0.059	2.410	2.469
Event 2	74	0.047	0.215	1.192	1.454
Event 3	129	0.147	0.052	0.699	0.898
Event 4	258	0.194	0.187	0.165	0.546
Event 5	1032	0.278	0.029	0.039	0.346
Event 6	4128	0.284	0.001	0.015	0.300
Total			0.543		

- The problem is excessive blocking ("priority inversion") for events 1, 2 and 3.
  - Remember that U *cannot* be greater than 1.0 for any system and for RMS, it can even be lower for non-harmonic tasksets.

Process Events in RM Order

	E1	E2	E3	E4	E5	E6
U	5.9%	21.5%	5.2%	18.7%	2.9%	0.1%
C_i (msec)	2.0	7.4	6.0	21.5	5.7	2.8
C_a (msec)	0.5	8.5	0.6	26.7	23.4	1.0
T **(msec)**	43	74	129	258	1032	4128

start: *i* = 1;
cont: if event *i* pending,
process event *i*
go to start
else
i = (*i*+1) mod *n*
go to cont
endif



Schedulability Model: RM Design

$$(1)\ \frac{C_1}{T_1}+\left\lceil\frac{\max(C_{2,A},C_{3,A},C_{4,A},C_{5,A},C_{6,A})+C_{2,I}+C_{3,I}+C_{4,I}+C_{5,I}+C_{6,I}}{T_1}\right\rceil$$

Preemption Execution Blocking

$$(2)\ \left\lceil\frac{C_1}{T_1}\right\rceil+\frac{C_2}{T_2}+\left\lceil\frac{\max(C_{3,A},C_{4,A},C_{5,A},C_{6,A})+C_{3,I}+C_{4,I}+C_{5,I}+C_{6,I}}{T_2}\right\rceil$$

$$(3)\ \left\lceil\frac{C_1}{T_1}+\frac{C_2}{T_2}\right\rceil+\frac{C_3}{T_3}+\left\lceil\frac{\max(C_{4,A},C_{5,A},C_{6,A})+C_{4,I}+C_{5,I}+C_{6,I}}{T_3}\right\rceil$$

$$(4)\ \left\lceil\frac{C_1}{T_1}+\frac{C_2}{T_2}+\frac{C_3}{T_3}\right\rceil+\frac{C_4}{T_4}+\left\lceil\frac{\max(C_{5,A},C_{6,A})+C_{5,I}+C_{6,I}}{T_4}\right\rceil$$

$$(5)\ \left\lceil\frac{C_1}{T_1}+\frac{C_2}{T_2}+\frac{C_3}{T_3}+\frac{C_4}{T_4}\right\rceil+\frac{C_5}{T_5}+\left\lceil\frac{C_6}{T_5}\right\rceil$$

(6) ....

Schedulability Test: RM Order

$$(1)\ \frac{2.5}{43}+\left\lceil\frac{26.7+7.4+6.0+21.5+5.7+2.8}{43}\right\rceil\le U(1)$$

$$(2)\ \left\lceil\frac{2.5}{43}\right\rceil+\frac{15.9}{74}+\left\lceil\frac{(26.7)+6.0+21.5+5.7+2.8}{74}\right\rceil\le U(2)$$

$$(3)\ \left\lceil\frac{2.5}{43}+\frac{15.9}{74}\right\rceil+\frac{6.6}{129}+\left\lceil\frac{(26.7)+21.5+5.7+2.8}{129}\right\rceil\le U(3)$$

$$(4)\ \left\lceil\frac{2.5}{43}+\frac{15.9}{74}+\frac{6.6}{129}\right\rceil+\frac{48.2}{258}+\left\lceil\frac{(23.4)+5.7+2.8}{258}\right\rceil\le U(4)$$

$$(5)\ \left\lceil\frac{2.5}{43}+\frac{15.9}{74}+\frac{6.6}{129}+\frac{48.2}{258}\right\rceil+\frac{29.1}{1032}+\left\lceil\frac{3.8}{1032}\right\rceil\le U(5)$$

$$(6)\ \left\lceil\frac{2.5}{43}+\frac{15.9}{74}+\frac{6.6}{129}+\frac{48.2}{258}+\frac{29.1}{1032}\right\rceil+\frac{3.8}{4128}\le U(6)$$

Utilization: RM Design

	Period (msec)	Preempt	Execute	Blocking	Total U	Previous Total
Event 1	43	0.000	0.059	1.631	1.690	2.469
Event 2	74	0.059	0.215	0.848	1.122	1.454
Event 3	129	0.274	0.052	0.440	0.766	0.898
Event 4	258	0.326	0.187	0.124	0.637	0.546
Event 5	1032	0.513	0.029	0.004	0.546	0.346
Event 6	4128	0.542	0.001	0.000	0.543	0.300
Total			0.543			

- *Note:* Events 3 through 6 will meet their deadlines.

Increasing Preemptability

	E1	E2	E3	E4	E5	E6
U	5.9%	21.5%	5.2%	18.7%	2.9%	0.1%
C_i (msec)	2.0	7.4 (1.5)	6.0	21.5	5.7	2.8
C_a (msec)	0.5	8.5 (1.7)	0.6	26.7 (4.5)	23.4 (3.9)	1.0
T (msec)	43	74	129	258	1032	4128

Preemptible IO

Packetized Data Movement

Schedulability Test: Packetized Data and Preemptible I/O

$$(1)\quad \frac{2.5}{43}+\left[\frac{(4.5)+1.5+6.0+21.5+5.7+2.8}{43}\right]\le U(1)$$

$$(2)\quad \left[\frac{2.5}{43}\right]+\frac{15.9}{74}+\left[\frac{(4.5)+6.0+21.5+5.7+2.8}{74}\right]\le U(2)$$

$$(3)\quad \left[\frac{2.5}{43}+\frac{15.9}{74}\right]+\frac{6.6}{129}+\left[\frac{(4.5)+21.5+5.7+2.8}{129}\right]\le U(3)$$

$$(4)\quad \left[\frac{2.5}{43}+\frac{15.9}{74}+\frac{6.6}{129}\right]+\frac{48.2}{258}+\left[\frac{(3.9)+5.7+2.8}{258}\right]\le U(4)$$

$$(5)\quad \left[\frac{2.5}{43}+\frac{15.9}{74}+\frac{6.6}{129}+\frac{48.2}{258}\right]+\frac{29.1}{1032}+\left[\frac{3.8}{1032}\right]\le U(5)$$

$$(6)\quad \left[\frac{2.5}{43}+\frac{15.9}{74}+\frac{6.6}{129}+\frac{48.2}{258}+\frac{29.1}{1032}\right]+\frac{3.8}{4128}\le U(6)$$

Utilization: Packetized Data and Preemptable I/O

	Period (msec)	Preempt	Execute	Blocking	Total U	Previous Total
Event 1	43	0.000	0.059	0.977	1.035	1.690
Event 2	74	0.059	0.215	0.548	0.822	1.122
Event 3	129	0.274	0.052	0.268	0.594	0.766
Event 4	258	0.326	0.187	0.049	0.562	0.637
Event 5	1032	0.513	0.029	0.004	0.546	0.546
Event 6	4128	0.542	0.001	0.000	0.543	0.543
Total			0.543			

Note: Events 2 through 6 meet their deadlines.

Streamlined Interrupt Handler

	E1	E2	E3	E4	E5	E6
U	5.9%	21.5%	5.2%	18.7%	2.9%	0.1%
C_i (msec)	2.0	7.4 (1.5)	6.0	21.5 (6.5)	5.7	2.8
C_a (msec)	0.5	8.5 (1.7)	0.6	26.7 (4.5)	23.4 (3.9)	1.0
T **(msec)**	43	74	129	258	1032	4128

Schedulability Test: Streamlined Interrupt Handler

(1) $\frac{2.5}{\quad} + \left[\frac{(4.5)+1.5+6.0+6.5+5.7+2.8}{43}\right] \le U(1)$

(2) $\left[\frac{2.5}{43}\right] + \frac{15.9}{74} + \left[\frac{(4.5)+6.0+6.5+5.7+2.8}{74}\right] \le U(2)$

(3) $\left[\frac{2.5}{43} + \frac{15.9}{74}\right] + \frac{6.6}{129} + \left[\frac{(4.5)+6.5+5.7+2.8}{129}\right] \le U(3)$

(4) $\left[\frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129}\right] + \frac{48.2}{258} + \left[\frac{(3.9)+5.7+2.8}{258}\right] \le U(4)$

(5) $\left[\frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} + \frac{48.2}{258}\right] + \frac{29.1}{1032} + \left[\frac{3.8}{1032}\right] \le U(5)$

(6) $\left[\frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} + \frac{48.2}{258} + \frac{29.1}{1032}\right] + \frac{3.8}{4128} \le U(6)$

Utilization: Streamlined Interrupt Handler

	Period (msec)	Preempt	Execute	Blocking	Total U	Previous Total
Event 1	43	0.000	0.059	0.628	0.687	1.035
Event 2	74	0.059	0.215	0.345	0.619	0.822
Event 3	129	0.274	0.052	0.152	0.478	0.594
Event 4	258	0.326	0.187	0.049	0.562	0.562
Event 5	1032	0.513	0.029	0.004	0.546	0.546
Event 6	4128	0.542	0.001	0.000	0.543	0.543
Total			0.543			

Note: **All** events meet their deadlines.

BSY-1 Trainer Case-Study Summary

- Recall original action plan:
  - improve efficiency of AIX signals
  - move processing from application to interrupts
  - recode 17,000 lines of Ada to C
- Final actions:
  - increase preemption and improve AIX
  - move processing from interrupts to application
  - modify 300 lines of Ada code
  - RMA took 3 people and 3 weeks

Summary of Lecture

- Applying RMA to real-time systems
  - Can be applied to systems that did not use Rate-Monotonic Scheduling or Deadline-Monotonic Scheduling
    - can be applied to systems doing round-robin scheduling, for example
- Conclusions drawn without understanding real-time scheduling theory can be widely off.
- Knowing real-time scheduling theory, simple fixes at the right places can solve what seem to be fundamental design and performance problems.