RTES Lab4 Writeup

Mengwen He

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1. When and why would you want to compile your kernel in NO_HZ configuration?
   Answer:
   When the macro HZ being set at compile time and varying between around 100 to 1500, it enables a timer tick to interrupt the kernel HZ times per second. Therefore, when we want a tickless kernel, we need to compile the kernel in NO_HZ configuration. The reason is that running without a timer tick means the kernel does less work when idle and can potentially save power because it does not have to wake up regularly just to service the timer.

2. What kernel subsystem decides which sleep state the processor enters and what parameters does it use to make the decision?
   Answer:
   The kernel cpuidle subsystem decides which sleep state the processor enters. The kernel uses the struct cpuidle_state to make the decision.

3. What are advantages and disadvantages of the wake locks solution adopted by the Android fork of the Linux kernel?
   Answer:
   Wake locks are power-managing software mechanisms, which make sure that the Android device doesn't go into deep sleep. The advantage is that the wake locks can keep the cpu to run some background applications. The disadvantage is that the abuse of wake locks leads to anomalous battery drain.

4. In the kernel you are working on for Nexus 7, does voltage change when frequency changes?
   Answer:
   Yes, the voltage changes when the frequency changes because we find the DVFS in the Nexus 7's kernel cpufreq_governor.

5. In ARM architecture, what instruction can be used to enter a low-power processor state?
   Answer:
   The arm_enter_idle_state or cpuidle_generic_enter function can be used to enter a low-power state.

	WFD			BFD			LST		
	FREQ	POWER	ENERGY	FREQ	POWER	ENERGY	FREQ	POWER	ENERGY
Test 1	1200	1277	47523	1200	1277	46141	1200	2555	45308
Test 2	1200	2555	91179	1200	2555	90155	1200	2555	58525
Test 3	1200	1916	64873	1200	1916	48859	1200	2555	79688
Test 4	1200	1916	76433	1200	1916	47492	860	1509	38652
Test 5	1200	1916	80771	1200	1916	57996	760	1246	36280

Test 1						
	C	T	U	WFD-bin	BFD-bin	LST-bin
T1	801	818	0.979218	3	3	3
T2	260	775	0.335484	2	2	2
T3	107	869	0.12313	2	2	1
T4	85	962	0.088358	2	2	0
T5	5	400	0.0125	2	3	0
Total			1.53869			

Test 2						
	C	T	U	WFD-bin	BFD-bin	LST-bin
T1	145	146	0.993151	3	3	3
T2	870	911	0.954995	2	2	2
T3	264	550	0.48	1	1	1
T4	137	432	0.31713	1	1	0
T5	182	580	0.313793	0	0	0
Total			3.059069			

Test 3						
	C	T	U	WFD-bin	BFD-bin	LST-bin
T1	901	903	0.997785	3	3	3
T2	418	490	0.853061	2	2	2
T3	370	945	0.391534	1	1	1
T4	112	491	0.228106	1	1	0
T5	50	338	0.147929	1	1	0
Total			2.618415			

Test 4						
	C	T	U	WFD-bin	BFD-bin	LST-bin
T1	404	576	0.701389	3	3	3
T2	60	97	0.618557	2	2	2
T3	390	943	0.413574	1	1	1
T4	242	957	0.252874	1	2	0
T5	132	781	0.169014	2	3	0
Total			2.155408			

Test 5						
	C	T	U	WFD-bin	BFD-bin	LST-bin
T1	548	921	0.595005	3	3	3
T2	418	738	0.566396	2	2	2
T3	423	952	0.444328	1	1	1
T4	270	984	0.27439	1	3	0
T5	53	943	0.056204	2	3	0
Total			1.936323			

	LST			LST with ES-RHS+		
	FREQ	POWER	ENERGY	FREQ	POWER	ENERGY
Test 1	760	1246	33467	1200	2555	46909
Test 2	1200	2555	73652	1200	2555	62186
Test 3	1200	2555	120492	1200	2555	98955
Test 4	1200	2555	77958	1200	2555	70493
Test 5	1200	2555	69239	1200	2555	37417

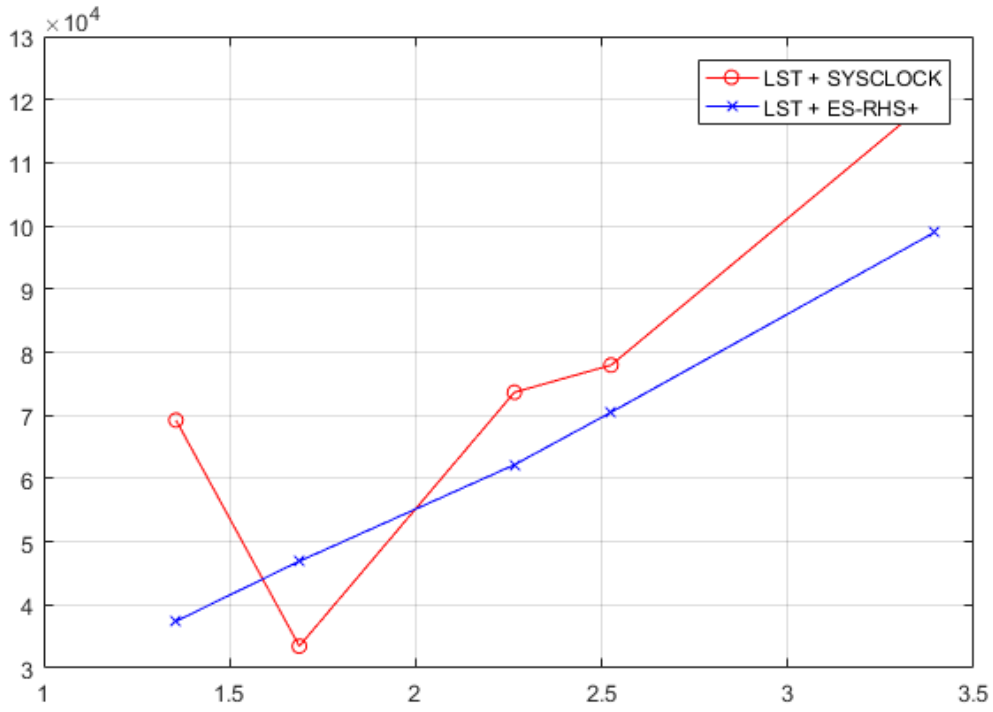
Test 1				
	C	T	U	LST-bin
T1	540	1000	0.54	3
T2	302	667	0.452774	2
T3	179	702	0.254986	1
T4	172	699	0.246066	0
T5	129	667	0.193403	0
Total			1.687229	

Test 2				
	C	T	U	LST-bin
T1	882	982	0.898167	3
T2	461	562	0.820285	2
T3	157	670	0.234328	1
T4	191	856	0.223131	0
T5	33	369	0.089431	0
Total			2.265342	

Test 3				
	C	T	U	LST-bin
T1	385	429	0.897436	3
T2	191	227	0.84141	2
T3	483	583	0.828473	1
T4	377	590	0.638983	0
T5	121	645	0.187597	0
Total			3.393899	

Test 4				
	C	T	U	LST-bin
T1	684	766	0.89295	3
T2	288	426	0.676056	2
T3	270	577	0.467938	1
T4	189	547	0.345521	0
T5	92	645	0.142636	0
Total			2.525101	

Test 5				
	C	T	U	LST-bin
T1	545	994	0.54829	3
T2	219	648	0.337963	2
T3	106	544	0.194853	1
T4	110	722	0.152355	0
T5	64	523	0.122371	0
Total			1.355832	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LST + SYSCLOCK
LST + ES-RHS+