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Fast DC Off-Board Charger for Electric Vehicles

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Abstract

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Part I

AC/DC Conversion

Chapter 1

Introduction to AC/DC Conversion

The electrical power supplied by wall outlets varies globally, offering either 50Hz or 60Hz AC (Alternating Current) with a nominal voltage of approximately 120VAC or 230VAC. However, for devices like phones and laptops, which run on low voltage DC (Direct Current), an adapter is typically required. Despite the ubiquity of DC-powered electronic equipment, mains power distribution employs AC. Understanding the historical and technical reasons behind this choice provides insight into the development of our modern power systems.

AC gained prominence in distributed networks for several compelling reasons. Firstly, the early AC generators were simpler, leading to rapid improvements in reliability. Secondly, the ability to easily change the voltage using transformers became a pivotal advantage. Lastly, the use of multiple pole alternators reduced the rotation speed of more powerful generators. This three-pronged approach made AC a practical choice for widespread power distribution.

One historical obstacle for DC power distribution was introduced by Thomas Edison, who championed DC systems. Edison faced challenges as he attempted to compete with AC by using generator sets. While low voltage DC motors for step-up purposes were easy to manufacture, high-voltage DC motors for the corresponding step-down process proved unreliable, leading to frequent system breakdowns. In the end, even Edison abandoned the DC distribution concept in favor of alternating current power distribution[1].

The choice of AC over DC also considered the issue of power losses in transmission lines. As more houses were connected to the power grid, the losses in a cable with resistance (I^2R loss) increased. By doubling the voltage, the current could be halved, allowing the same power cable to carry the current four times further. This principle applied to both DC and AC power transmission, but the use of transformers made it more convenient to step up the AC supply voltage for long-distance transmission and step it back down at the destination.

Currently, modern technologies enable efficient bidirectional conversion between AC and DC with high power and efficiency. While AC mains voltages are likely to remain standard soon, there is a growing interest in reconsidering DC power distribution due to our increasing dependence on electrical power. Modern power distribution involves multiple interconnected sources forming a power grid. Transmitting power over long distances ($>800\text{km}$) using high voltage DC has become more appealing because it eliminates impedance losses, and generators do not need to be synchronized to the same frequency or voltage.

For instance, a notable example of high voltage DC power transmission is a 2000MW link con-

necting England and France. This interconnection allows the two countries to exchange power based on domestic demand, highlighting the advantages of high voltage DC in a modern power grid. As technology continues to evolve, the debate between AC and DC power distribution will persist, driven by factors such as efficiency, cost, and the demands of our increasingly interconnected and power-dependent world.

AC/DC converters are the backbone components for expanding and improving the functioning of electrical vehicles (EVs). Primarily, an outlet delivers AC power, whereas EV batteries function with DC power for charging the battery. Thus, there is a need for an AC/DC converter for converting AC power to DC power. It is also the major component of an EV battery charger and enhances the input current shape for power-factor correction and harmonic reduction.

The power range of fast charging is above 50 kW, which is considered high according to industry standards. So there is a need for a larger AC/DC converter to supply this extra power for fast charging. Thus, high-power charging is best carried out where AC/DC converters are built into the charging station and not installed inside the vehicle due to size constraints[2]. We will focus on off-board fast chargers for electric vehicles, but before this, we will discuss rectification and its topologies further more.

1.1 What is Rectification?

Rectification refers to the process of transforming an alternating current (AC) waveform into a direct current (DC) waveform, producing a signal with a single polarity. It is essential to note that a DC voltage or current does not necessarily have to be constant; it simply means the signal's polarity remains unchanged. In some cases, a varying amplitude DC signal is referred to as pulsating DC.

The concept of rectification is fundamental in modern electronic circuits as many electronic devices require a stable, unvarying DC voltage to power their internal circuitry. Given that residential and commercial power distribution is typically in the form of AC, some form of AC to DC conversion is necessary.

Rectifiers, which perform the conversion of AC to DC, are classified into two categories based on the type of conversion: half-wave rectifiers and full-wave rectifiers. The former involves converting half cycles of AC into DC, while the latter processes full cycles of AC into DC. Understanding the differences between half-wave and full-wave rectifiers, as well as a brief exploration of each type, facilitates a clearer grasp of their distinct functionalities.

1.1.1 Half-Wave Rectification

A half-wave rectifier is a circuit that transforms only half of the alternating current (AC) cycle into direct current (DC). The typical configuration of a half-wave rectifier involves a semiconductor diode, and the circuit and output waveform are depicted in Figure 1.1.

In the process of half-wave rectification, the AC is initially supplied to the diode. Here is how the rectification unfolds: During the positive half cycle of AC, the diode, operating in a forward-biased state, acts as a short circuit, allowing electric current to pass through. Conversely, during the negative half cycle of AC, the diode becomes reverse-biased, acting as an open circuit and preventing conduction. Consequently, the voltage at the load terminals is present only during the positive half

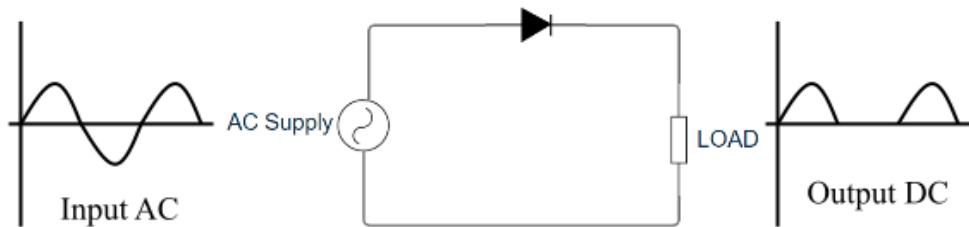


Figure 1.1: Half-wave rectification process

cycle of AC. Thus, the alternating current is converted into direct current, flowing in a single direction, but only during one half cycle of AC.

1.1.2 Full-Wave Rectification

In contrast to half-wave rectifier, a full-wave rectifier transforms the entire cycle of alternating current into direct current. The circuit for a full-wave rectifier comprises four semiconductor diodes. Two of the four terminals of the diodes are connected to the AC supply, while the other two terminals link to the load resistor.

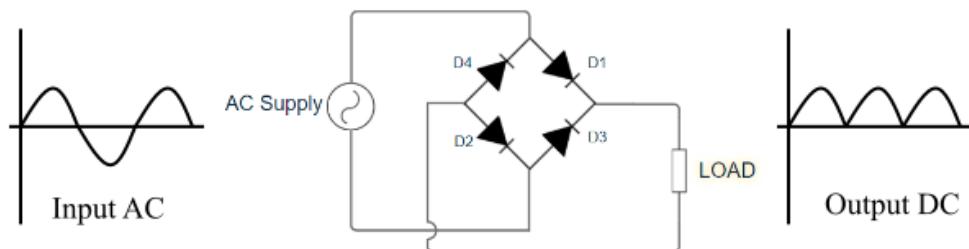


Figure 1.2: Full-wave rectification process

During the positive half cycle of AC, diode D_1 and diode D_2 are forward biased, and diode D_3 and diode D_4 are reverse biased. Consequently, diodes D_1 and D_2 conduct, allowing current to flow through D_1 , D_2 and the load resistor R_L . In the negative half cycle of AC, the situation reverses: diodes D_1 and D_2 become reverse biased, and diodes D_3 and D_4 become forward biased. Only diodes D_3 and D_4 are conducted during this negative half cycle, and the current flows through D_3 , D_4 and the load resistor R_L . The circuit and output voltage waveform for the full-wave rectifier are illustrated in Figure 1.2. This way, a full-wave rectifier efficiently converts the entire AC cycle into DC [3].

While the explanations above focus on a single-phase AC system, they can be extended to three-phase systems commonly used in fast-charging offboard chargers. In a three-phase half-wave rectifier, the system requires three diodes, and for the full-bridge system, six diodes are necessary. The adaptability of rectification principles to different configurations underscores their significance in converting AC to DC, a crucial requirement for many electronic devices and power systems.

Chapter 2

Topologies for AC/DC Conversion Stage

The AC-DC converter of an offboard charger is a front-end rectifier before the DC-DC conversion stage of the complete EV fast charging station. Various topologies are available that convert AC power from the utility grid to DC power. Such topologies are expected to manage high power fed directly to the battery as part of an EV fast charging solution.

2.1 Three-Phase Passive Rectifier

The simplest rectifier configuration is the three-phase diode rectifier, comprising six diodes, AC side inductors, and a DC side capacitor (refer to 2.1).

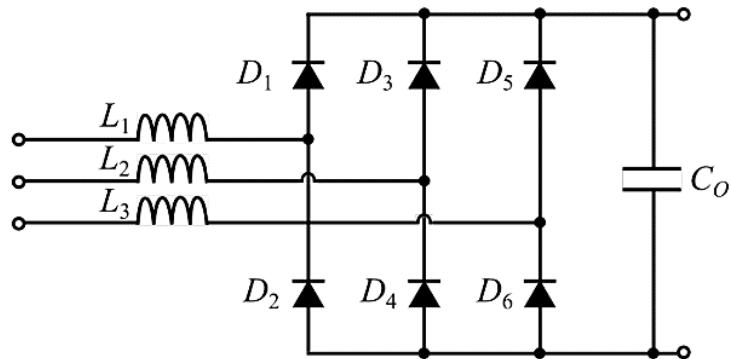


Figure 2.1: Three-phase passive rectifier

As it runs without active switches, this converter drops the need for a control system or gate drivers, streamlining its functionality. Diodes switch at the grid frequency without active current shaping or control over the output voltage. However, diode rectifiers can introduce a Total Harmonic Distortion (THD) of 40–70% into grid currents, potentially stressing the grid, especially with numerous fast high-power passive rectifiers. Due to its lower efficiency, unidirectional power flow, and higher THD, this conventional passive rectifier topology is not recommended for fast charging applications.

Unlike passive rectifiers, active rectifiers, when employed, allow for controlled DC link voltage, keeping the desired voltage level across varying loads. This helps minimize THD, achieving both

high efficiency and power factor. The later comparison focuses on three boost-type bidirectional active converters: Three-phase two-level six-switch boost-type rectifier, Three-phase three-level neutral point clamped converter, and Three-phase three-level T-type converter.

2.2 Three-Phase Vienna Rectifier

The three-phase Vienna rectifier, illustrated in 2.2, includes three input inductors for voltage boosting, followed by six diodes for rectification and six semiconductor switches. Additionally, two split capacitors are incorporated in the output. Its functioning is akin to a traditional three-phase boost Power Factor Correction (PFC) rectifier, but unlike the latter, it does not ease bidirectional power flow. The Vienna rectifier employs a straightforward control mechanism, ensuring unity power factor operation and minimizing Total Harmonic Distortion (THD). Its notable efficiency, particularly in power-dense applications, makes it well-suited for high-power scenarios such as fast-charging Electric Vehicles (EVs).

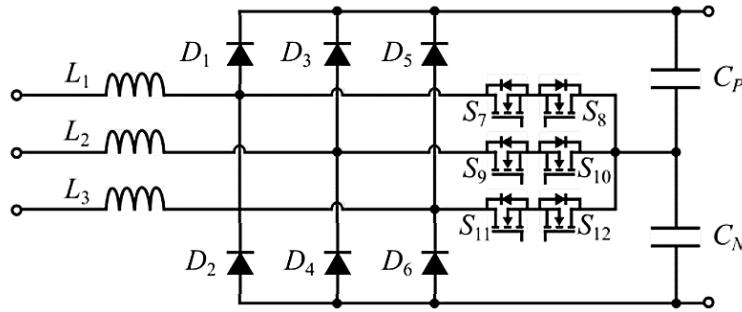


Figure 2.2: Three-phase vienna rectifier

To enable bidirectional power flow, the Vienna rectifier can be changed by replacing diodes with switches, a modification especially beneficial in Vehicle-to-Grid (V2G) applications. The Vienna rectifier typically runs using modulation methods like carrier-based Pulse Width Modulation (PWM), Space Vector PWM, and discontinuous PWM. However, in the case of interleaved Vienna rectifiers, Space Vector PWM can introduce distortions in input current waveforms, while the other two PWM techniques may lead to undesirable ripples. To address these challenges, a hybrid Space Vector PWM approach is employed, effectively mitigating the issues associated with the modulation techniques.

2.3 Three-Phase Two-Level Six-Switch Boost-Type Rectifier

The configuration for the three-phase two-level boost-type rectifier is depicted in 2.3. It forms six active switches (MOSFETs or IGBTs), AC side boost inductors, and a DC side filter capacitor. Known for its simplicity, robustness, and familiarity, the two-level six-switch rectifier topology needs larger-volume input inductors and is constrained by a maximum switching frequency compared to three-level converters.

The rectifier, being of a boosting nature, imposes a lower limit on the DC link voltage. For instance, if the rectifier is connected to a three-phase grid with a 400 V RMS line-to-line voltage, the smallest DC link voltage would be 565 V, equal to the line-to-line voltage amplitude. Ideally, keeping a DC link voltage 15–20

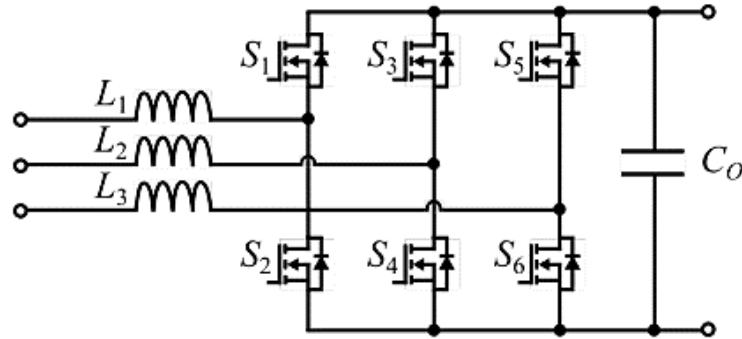


Figure 2.3: Three-phase two-level six-switch boost-type rectifier

In a two-level topology line-to-neutral rectifier, the voltage is either zero or matches the DC link voltage. Consequently, this gives rise to a three-level line-to-line voltage.

2.4 Three-Phase Three-Level Neutral Point Clamped Converter

The configuration of a three-phase three-level neutral point clamped (NPC) converter is illustrated in 2.4. Comprising twelve active switches, six diodes, and filters, this three-level topology offers advantages over the two-level converter. Notably, switches in this arrangement experience reduced voltage stress and lower switching losses, while the passive filter size is also smaller. However, the trade-off involves an increased part count, leading to potential drawbacks in system reliability, complexity, and implementation effort.

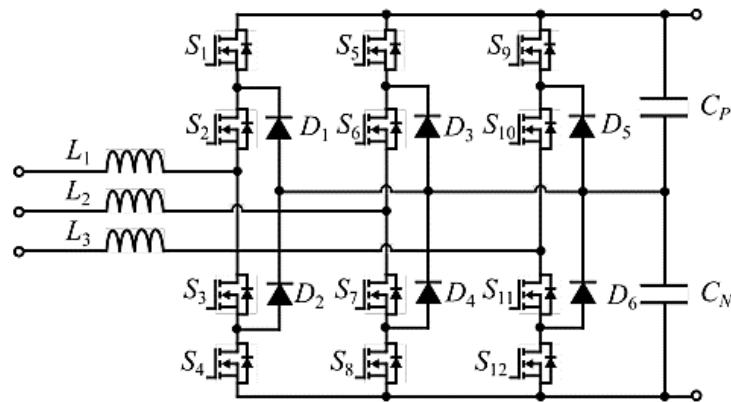


Figure 2.4: Three-phase three-level neutral point clamped converter

In a three-level topology, the line-to-neutral voltage can take values of 0.5 VDC, zero, or -0.5 VDC, resulting in a five-level line-to-line voltage. Despite the increase in complexity, the NPC converter keeps a sinusoidal grid side current similar to the two-level topology, featuring harmonics around the switching frequency and its multiples during harmonic analysis.

The primary limitation of the NPC topology lies in its use of twelve active and six passive switches, resulting in increased costs and complexity. Despite these drawbacks, it offers notable advantages such as a substantial reduction in inductor size and ensures that all switches are exposed to only half the DC link voltage. However, this configuration needs two capacitors in series, leading to higher capacitance values and lower capacitor voltage ratings.

2.5 Three-Phase Three-Level T-Type Converter

Three-phase three-level T-type converter is a bidirectional variation of the three-phase Vienna rectifier. The topology is shown in 2.5. This rectifier uses twelve active switches, compared to the original unidirectional topology that uses six diodes and six active switches. Moreover, it has three boost inductors on the AC side and a split capacitor on the DC side. This is a three-level topology similar to NPC. However, it has lower semiconductor losses for low switching frequencies compared to NPC, and it can be implemented using standard six-pack modules. This topology uses switches for two different voltage ratings.

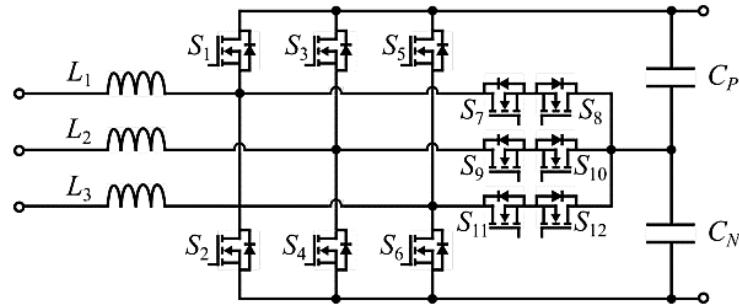


Figure 2.5: Three-phase three-level T-type converter

The three-level T-type rectifier also generates a three-level line-to-neutral voltage and five-level line-to-line voltage. The current is quite similar to the NPC converter current, also it uses similar filter sizes and filter ratings as the NPC. The main difference is the number and rating of the switches.

The two switches between positive and negative DC link block voltages between 0.5 VDC and VDC, so they must be rated for VDC. However, when these devices are switching, the voltage level changes between zero and 0.5 VDC, which results in lower switching losses compared to switching with full VDC. The devices connected between the phase leg midpoint and DC link midpoint block 0.5 VDC, so they only need to be rated for 0.5 VDC. Moreover, they also switch between zero and 0.5 VDC. Overall, the reduced number of components compared to NPC, while keeping switching from 0.5 VDC, results in higher efficiency than NPC. The efficiency of the T-type rectifier at full load is 98.95%.

Chapter 3

Implementation of Closed-Loop AC/DC Converter

We will now address challenges through the design and implementation of a closed-loop AC/DC rectifier system. The closed-loop architecture, with its feedback mechanism, promises not only enhanced control over the rectification process but also the mitigation of issues associated with traditional rectifiers. The journey towards an optimized closed-loop system involves a meticulous exploration of key components, each playing a pivotal role in achieving the desired efficiency and stability.

The aims of this research encompass a detailed examination of critical aspects, including filter selection, DC-link configuration, phase-locked loop (PLL), Clarke and Park transformations, and Proportional-Integral-Derivative (PID) control.

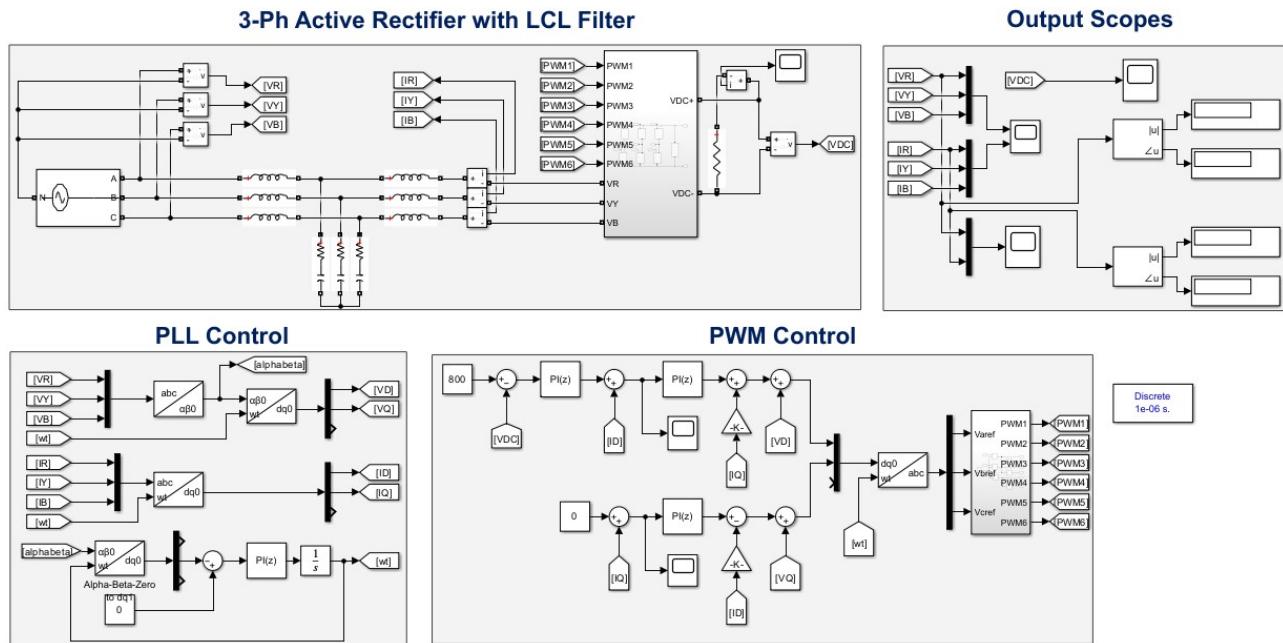


Figure 3.1: The implemented model of 10KW system using VOC

3.1 Proportional Integral Derivative (PID)

A proportional–integral–derivative controller (PID controller) is a control loop mechanism employing feedback that is widely used in industrial control systems and a variety of other applications requiring continuously modulated control. As implied by its name, the PID controller combines proportional control with added integral and derivative adjustments, helping the unit to automatically compensate for changes in a system.

Proportional-Integral-Derivative (PID) control is the most common control algorithm used in industry and has been universally accepted in industrial control. The popularity of PID controllers can be attributed partly to their robust performance in a wide range of operating conditions and partly to their functional simplicity, which allows engineers to run them in a simple, straightforward manner. The PID algorithm consists of three basic coefficients; proportional, integral, and derivative which are varied to get best response.

PID controller keeps the output such that there is zero error between process variable and set point (desired output) by closed loop operations and tuning PID parameters. PID uses three basic control behaviors.

3.1.1 P-Controller

Proportional or P- controller gives an output that is proportional to error $e(t)$. It compares the desired or set point with the actual value or feedback process value.

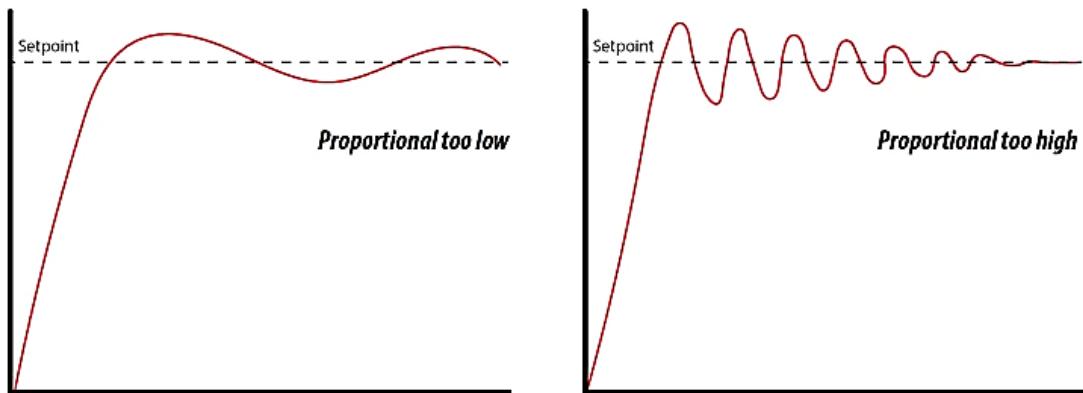


Figure 3.2: The effect of P-gain on a system

The resulting error is multiplied with a proportional constant to get the output. If the error value is zero, then this controller output is zero. This controller requires biasing or manual reset when used alone. This is because it never reaches the steady-state condition. It supplies stable operation but always keeps the steady-state error. The speed of the response is increased when the proportional constant K_p increases. P-Controller Equation:

$$u(t) = K_p e(t) \quad (3.1)$$

3.1.2 I-Controller

Due to the limitation of p-controller where there always exists an offset between the process variable and set-point, I-controller is needed, which supplies necessary action to cut the steady-state error.

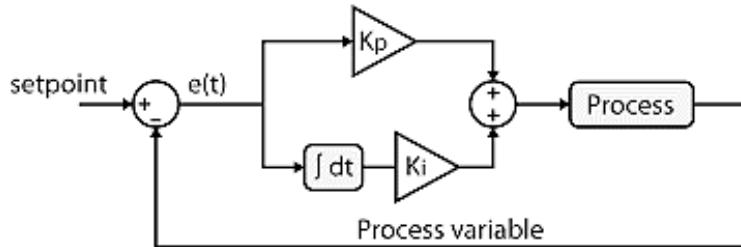


Figure 3.3: PI-control process

It integrates the error over a period of time until the error value reaches zero. It holds the value to the final control device at which the error becomes zero. Integral control decreases its output when a negative error takes place. It limits the speed of response and affects the stability of the system. The speed of the response is increased by decreasing integral gain, K_i . PI-Controller Equation:

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau \quad (3.2)$$

3.1.3 D-Controller

I-controller does not have the capability to predict the future behavior of error. So, it reacts normally once the set-point is changed. D-controller overcomes this problem by expecting the future behavior of the error. Its output depends on the rate of change of error with respect to time, multiplied by derivative constant. It gives the kick start for the output thereby increasing system response.

In 3.4, response of D, the controller is more, compared to the PI controller, and also settling time of output is decreased. It improves the stability of the system by compensating for phase lag caused by I- controller. PID Controller Equation:

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau + K_d \frac{de(t)}{dt} \quad (3.3)$$

The following figure shows the structure of the PID controller. It consists of a PID block which gives its output to the process block. Process/plant consists of final control devices like actuators, control valves, and other control devices to control various processes of industry/plant. A feedback signal from the process plant is compared with a set point or reference signal $r(t)$ and the corresponding error signal $e(t)$ is fed to the PID algorithm.

According to the proportional, integral, and derivative control calculations in the algorithm, the controller produces a combined response or controlled output which is applied to plant control devices.

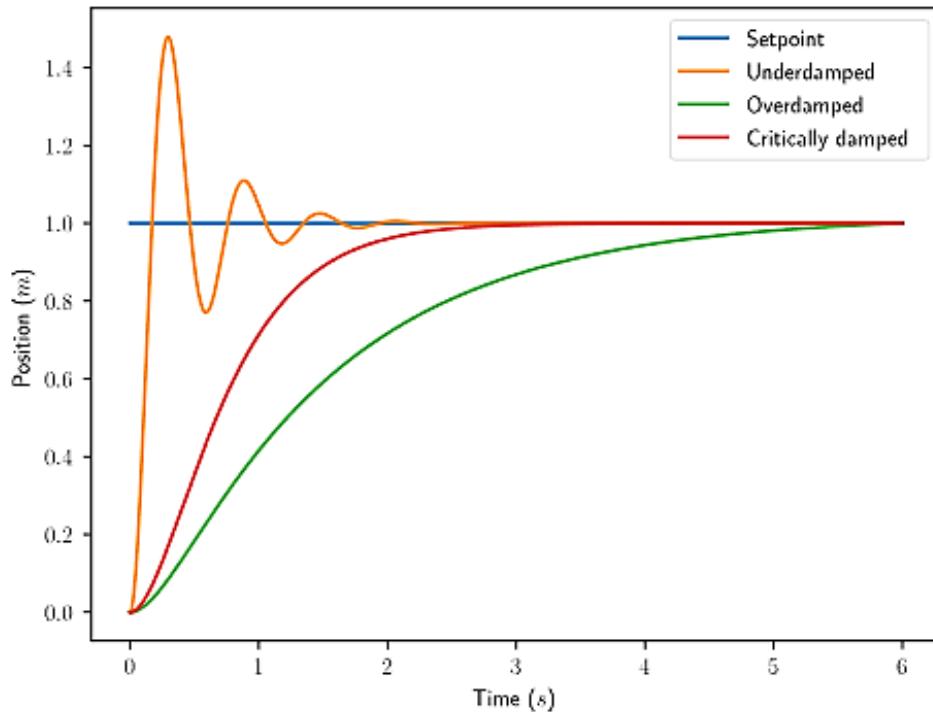


Figure 3.4: PID control on a system

3.1.4 Tuning of PID Controller

Before the working of PID controller takes place, it must be tuned to suit the dynamics of the process to be controlled. Several types of tuning methods are developed to tune the PID controllers and require much attention to select the best values of proportional, integral, and derivative gains. Some of these methods are Trial and Error method, Process reaction curve technique and Zeigler-Nichol's method. We used Trial and Error method in our project as it is simple and time effective. It is done by firstly setting k_i to zero then increasing k_p until the system reaches oscillating behavior at constant rate. Once it is oscillating, it is time to adjust k_i so that oscillations are reduced.

3.1.5 The Main Control Circuit

The following figure shows the main control circuit which is used to control the voltage with the outer loop and the current with the inner loop and finally generates the corresponding PWM signals that are used to run and control the inverter.

There are a lot of methods to control but we used a Voltage Oriented Control for its simplicity [4]. In voltage-oriented control (VOC), the line input current is oriented with respect to the line voltage vector. The line voltage vector can be obtained by measurement by using sensors or estimation. In synchronous rotating reference frame, the d-axis is aligned with the line voltage vector. The d-axis component of the line current “ i_d ” is proportional to the active power and its q-axis component is proportional to reactive power. To achieve unity power factor the reactive component of current reference i_q^* is set to zero. While the active component of current reference i_d^* is obtained from the PI controller, which gives the output by comparing the dc link voltage at the output with the reference

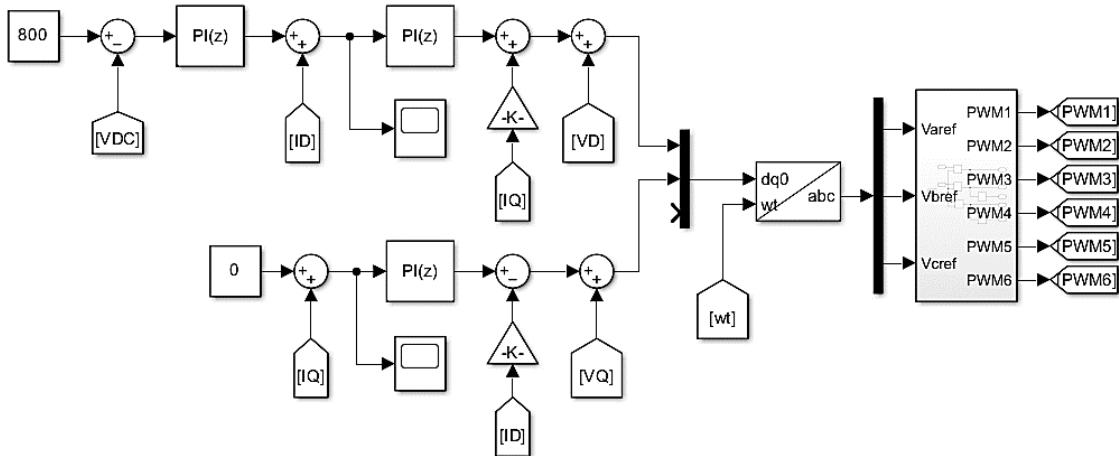


Figure 3.5: Control circuit of AFE (Active Front-end Rectifier) with 800V output voltage

voltage set as per the load requirements.

Coupling occurs due to voltage drop across inductors due to orthogonal current component coming in phase with the voltage components. Decoupling is essential to have proper control.

$$V_{sd} = V_{ld} - L \frac{di_d}{dt} + \omega L i_q \quad (3.4)$$

$$V_{sq} = V_{lq} - L \frac{di_q}{dt} - \omega L i_d \quad (3.5)$$

The voltage V_{lq} is zero by aligning the line voltage vector along the d-axis and q-axis current is regulated to zero. The current controller is decoupled as

$$V_{sd} = \omega L i_{lq} + V_{ld} + \Delta V_d \quad (3.6)$$

$$V_{sq} = -\omega L i_{ld} + \Delta V_q \quad (3.7)$$

where

$$\Delta V_d = K_p (i_d^* - i_d) + K_i \int (i_d^* - i_d) dt \quad (3.8)$$

$$\Delta V_q = K_p (i_q^* - i_q) + K_i \int (i_q^* - i_q) dt \quad (3.9)$$

In VOC it is possible to calculate the voltage across the input inductor by differentiating the current flowing through it. It is then possible to estimate the line voltage by adding voltage drop across the inductor with rectifier input voltage.

3.2 Phase-Locked Loop (PLL)

The reason why we need PLL is: suppose we want to send an active current to the grid the current should be in phase with the voltage that means that for grid connected inverters we need synchronization, so a reference signal is generated which is in phase with the actual voltage with an amplitude of 1, -1 using phase-locked loop (PLL).

The signal is used as a reference for the implementation of current controller in the grid connected inverters. There are two methods of phase locked loop implementation:

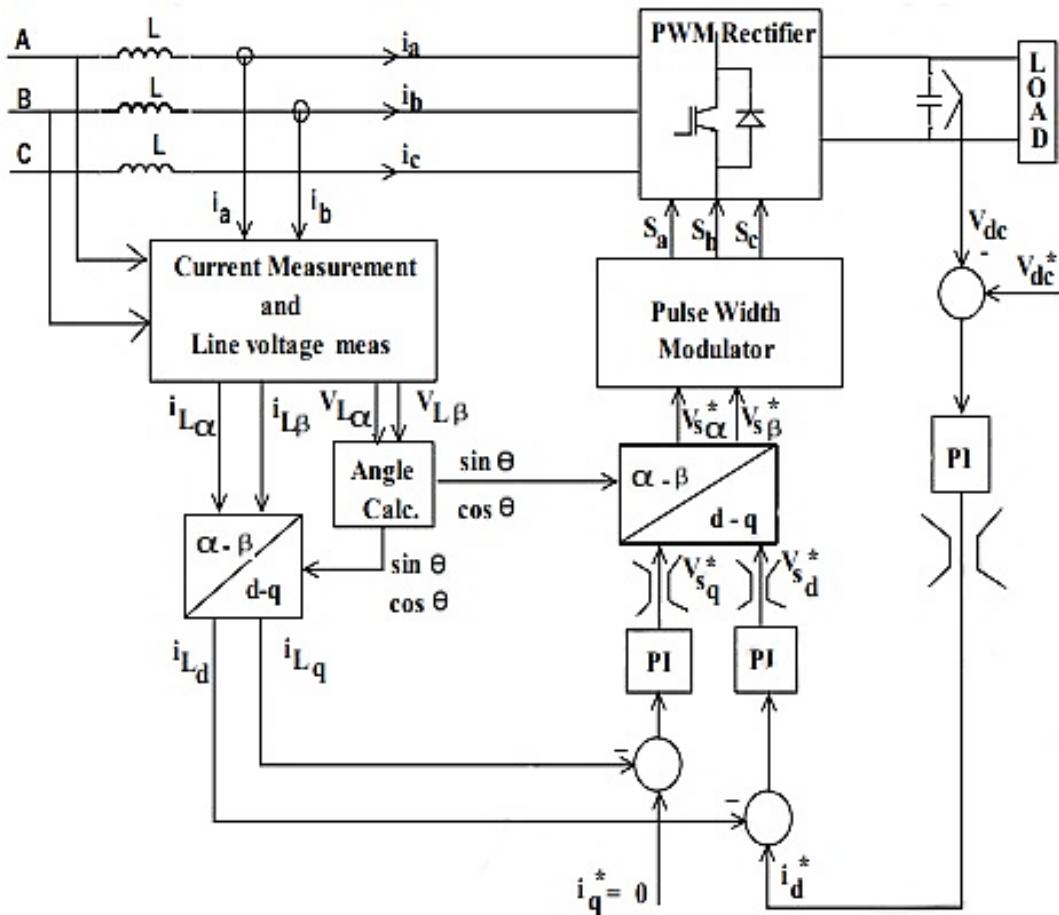
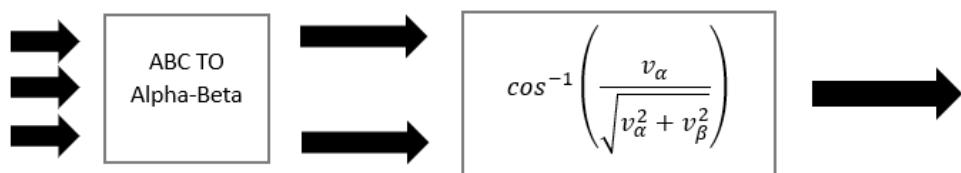


Figure 3.6: PI control loop of AFE

3.2.1 Method I

Here ABC voltages are converted into α, β voltages taking the equation shown in the diagram below giving us the angle information and from this angle information we generate reference signal but, there are few problems with this method and not used in many applications.



The problems are mainly:

- It is merely an algebraic method with simple mathematics involved.
- Open loop system so any outer effects or conditions can lead the grid to unstable condition so PLL cannot withstand harmonics, surges, noise, and spikes.
- Drift of angle and giving wrong angle information due to the mentioned effects.

But we can get rid of these problems by using closed loop phase locked loop (PLL).

3.2.2 Method II

Here we also start by transforming ABC signals into $\alpha - \beta$ signals then into dq voltages as shown in the figure below, this method is also called voltage oriented control (VOC), where the line input current is oriented with respect to the line voltage vector [5].

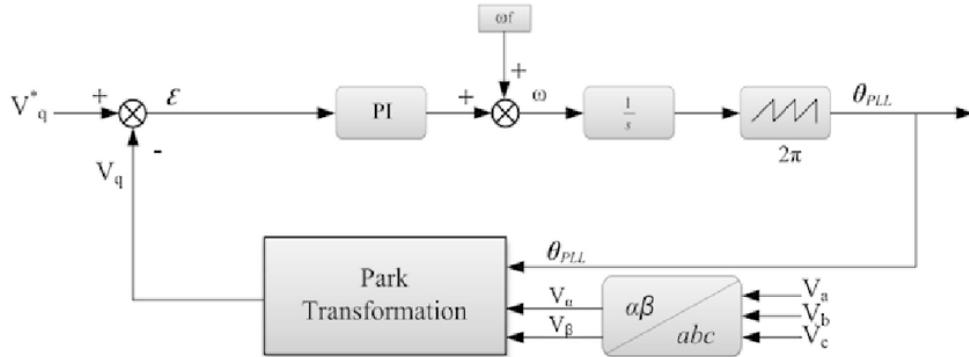


Figure 3.7: PLL control using VOC method

We can observe from the phasor diagram that D-axis is not aligned with the grid voltage so, by using the control mechanism shown in the figure we can make $V_q = 0$ using a PI controller and then the o/p is given to an integrator to find ωt .

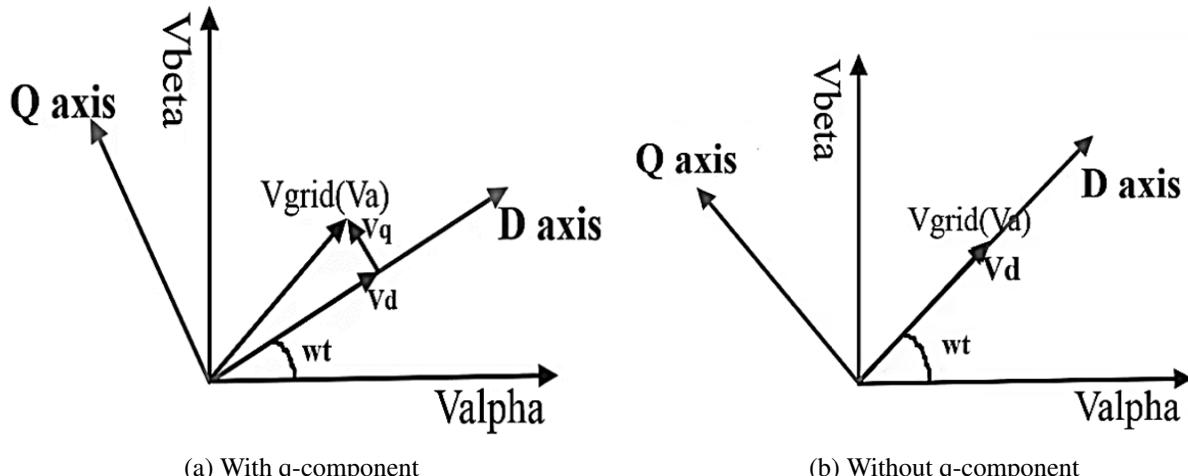


Figure 3.8: $\alpha - \beta$ signals to d-q signals

After making the V_q equal to zero the D-axis got aligned with the grid voltage and the angle between alpha-component and the D-axis has also changed to a new value which will be used in generating the reference signal.

3.3 Clarke and Park Transformations

Clarke and Park transforms are commonly used in field-oriented control of three-phase AC machines. The Clarke transform converts the time domain components of a three-phase system (in ABC frame) to two components in an orthogonal stationary frame ($\alpha - \beta$). The Park transform converts the two

components in the $\alpha - \beta$ frame to an orthogonal rotating reference frame (d-q). Implementing these two transforms in a consecutive manner simplifies computations by converting AC current and voltage waveform into DC signals.

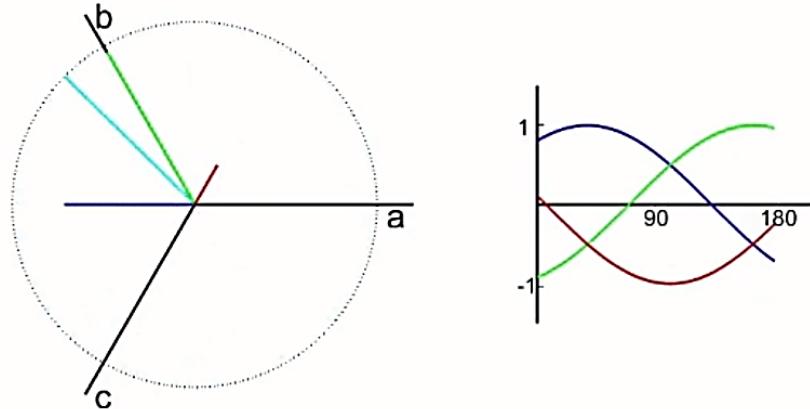


Figure 3.9: ABC frame

3.3.1 Clarke Transform

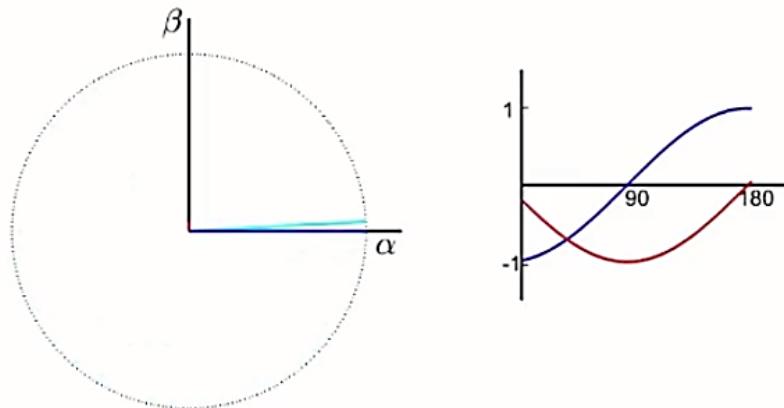


Figure 3.10: Clarke transform

The Clarke Transform converts the time-domain components of a three-phase system in an ABC reference frame to components in a stationary $\alpha\beta\gamma$ reference frame. For a balanced system, the zero part is equal to zero. The block implements the Clarke transform as

$$\begin{bmatrix} \alpha \\ \beta \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3.10)$$

where

- a, b, and c are the components of the three-phase system in the ABC reference frame.
- α and β are the components of the two-axis system in the stationary reference frame.
- 0 is the zero component of the two-axis system in the stationary reference frame.

3.3.2 Park Transform

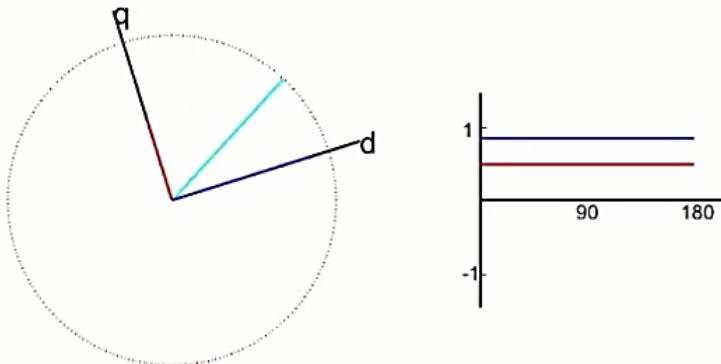


Figure 3.11: Park transform

The Park Angle Transform block converts the alpha, beta, and zero components of Clarke Transformer in a stationary reference frame to direct, quadrature, and zero components in a rotating reference frame. For balanced three-phase systems, the zero components are equal to zero.

The Clarke to Park Angle Transform block implements the transform for an a-phase to q-axis alignment as

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) & 0 \\ \cos(\theta) & \sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \\ 0 \end{bmatrix} \quad (3.11)$$

where

- α and β are the components of the two-axis system in the stationary reference frame.
- 0 is the zero component of the two-axis system in the stationary reference frame.
- d and q are the direct-axis and quadrature-axis components of the two-axis system in the rotating reference frame.

Chapter 4

AC/DC Converter Simulation

It is very crucial to simulate the circuit before diving in hardware design to make sure that the circuit would work fine when it's fabricated. Therefore, for this chapter we will provide the steps to simulate an AC/DC converter of both low and high ratings and their results.

Refer to figure 3.1 that shows the model circuit diagram that was built on MATLAB Simulink for 10KW system which is almost the same implementation for the low-rating system in aspect of circuit diagram, the main differences between the two systems will be represented in the following two sections. Note that for the low-rating system the reference voltage of the DC-link is set to be 200V.

The design of the filter design and the DC-link capacitor calculations will be discussed in details in a later chapter.

The implementation of the PLL of the 1KW and 10KW systems is shown in the following figure with the value of its PI-controller to produce zero-shift.

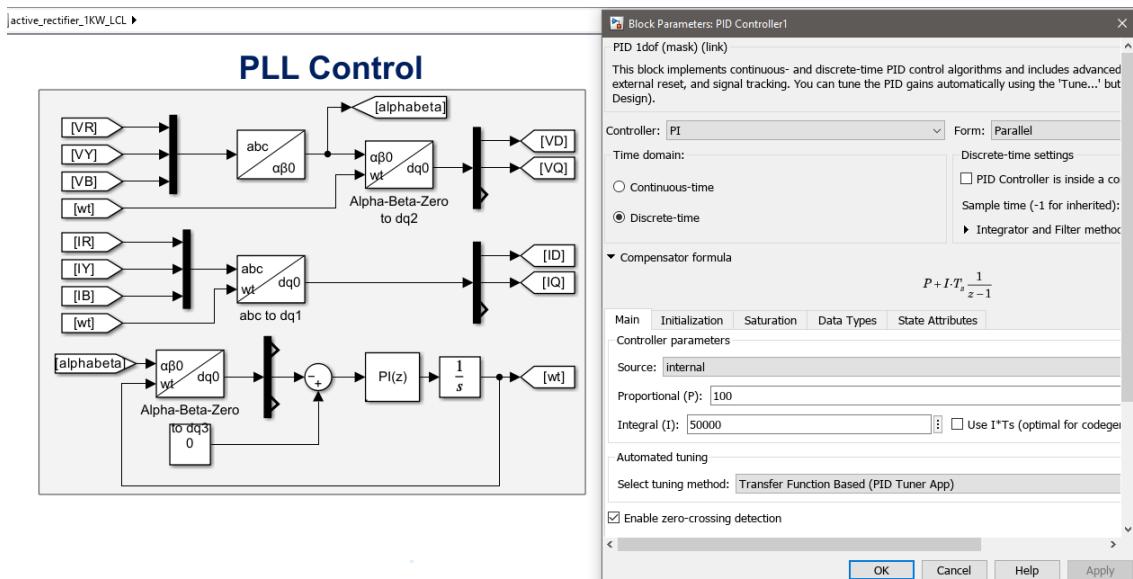


Figure 4.1: The implementaion of PLL for 1KW and 10KW systems

4.1 Low-Rating System (1KW)

The implementation of a three-phase low-rating rectifier was done to produce 200V at the DC-link as an output while the input line-to-line voltage was 100V at 50Hz frequency. The parameters of the system is as follows:

$$C_f = 15.915\mu F$$

$$L_i = 4mH$$

$$L_g = 95.492\mu H$$

$$R_f = 0.8027\Omega$$

$$C_{dc} = 1000\mu F$$

After the DC-link, a load was set in parallel to limit the current to produce exactly 1KW power at the output. The value of the this resistance was set to be 40Ω .

The PWM control block is implemented using three PI-controllers as discussed previously (refer to figures 4.2 ~ 4.4).

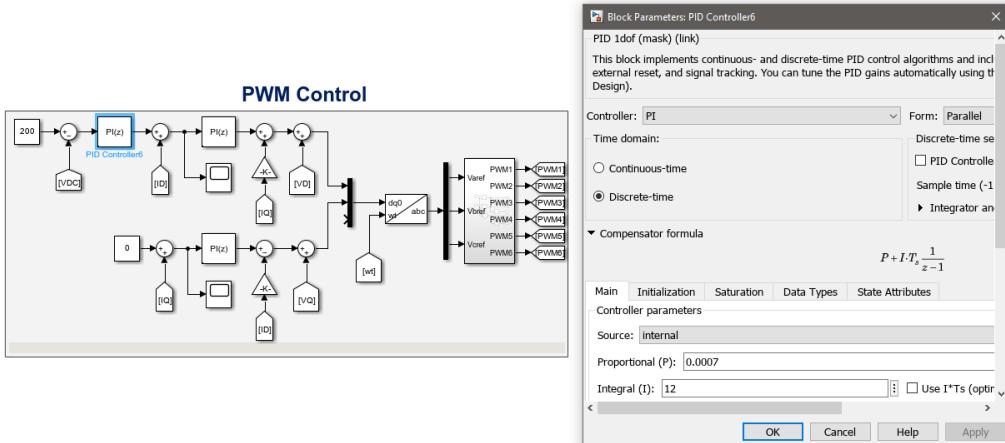


Figure 4.2: The outer loop PI-control block of 1KW system

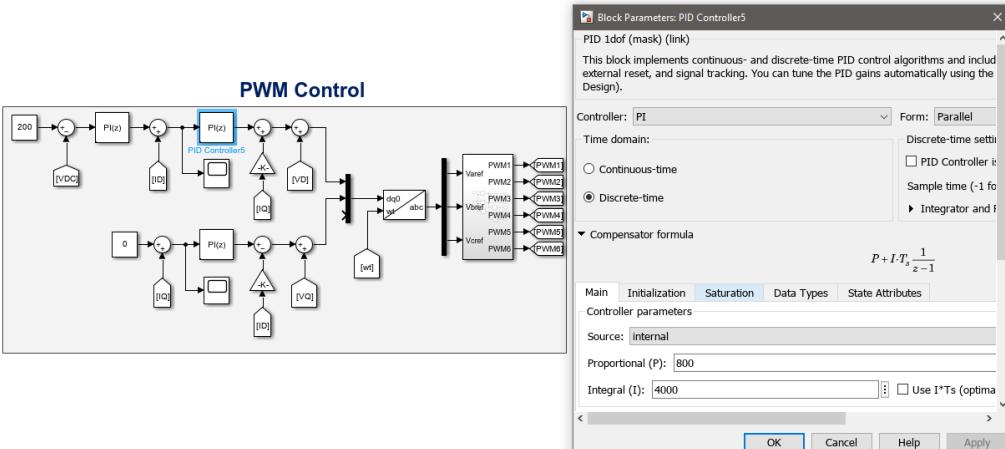


Figure 4.3: The inner loop PI-control block of 1KW system

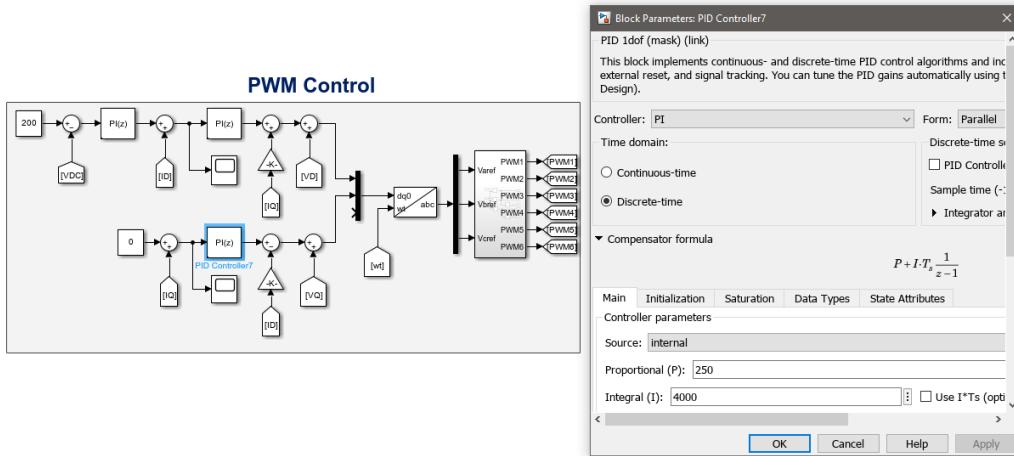


Figure 4.4: The quadrature PI-control block of 1KW system

The following results were obtained to show the input voltages and currents, the synchronism between the current and the voltage to show the power factor correction and the DC-link output voltage.

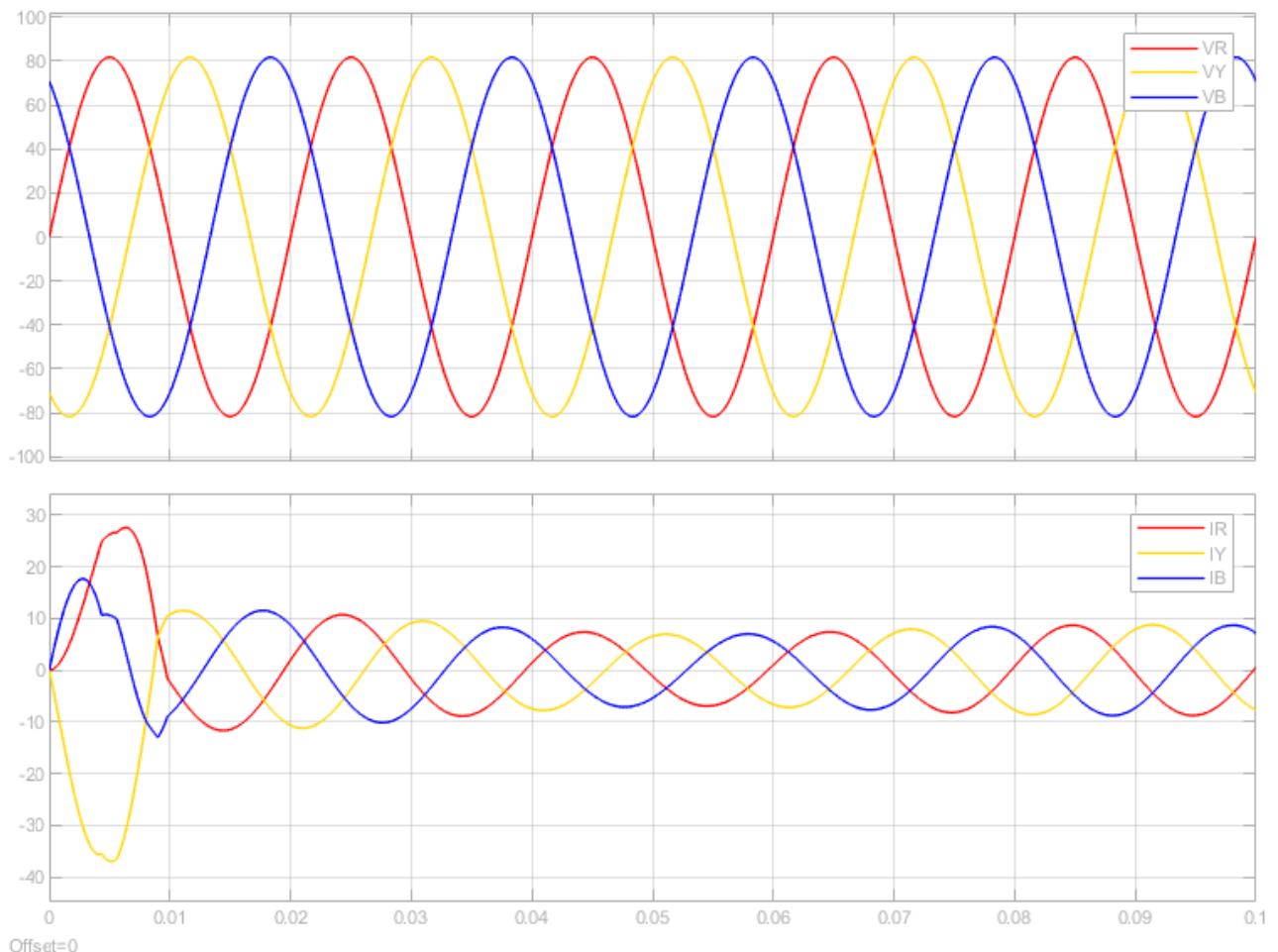


Figure 4.5: The three-phase input voltage and current of 1KW system

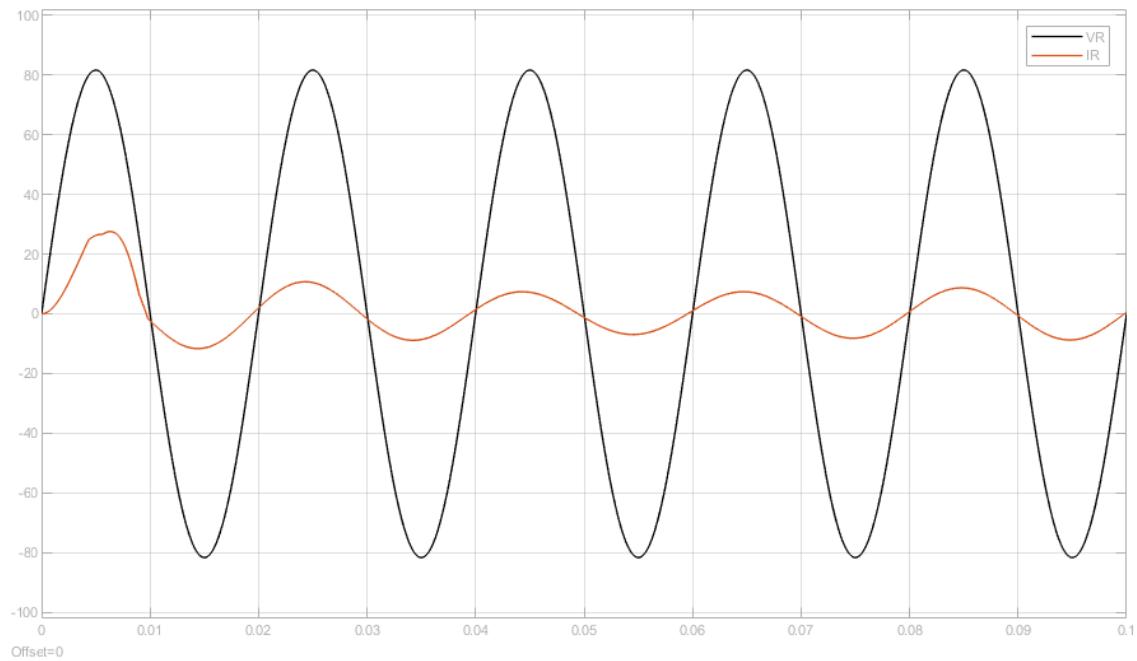


Figure 4.6: The input voltage and current of phase-R of 1KW system

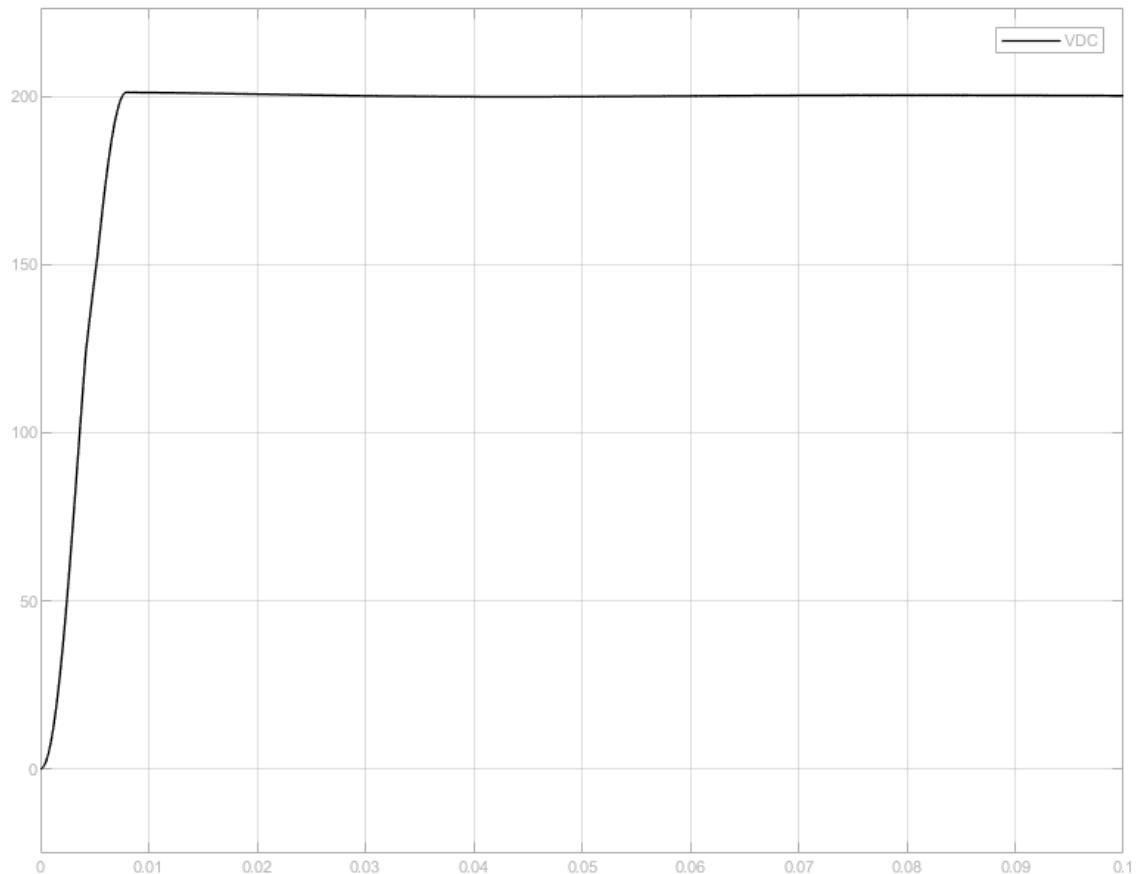


Figure 4.7: The DC-link output of 1KW system

4.2 High-Rating System (10KW)

The implementation of a three-phase low-rating rectifier was done to produce 800V at the DC-link as an output while the input line-to-line voltage was 380V at 50Hz frequency. The parameters of the system is as follows:

$$C_f = 11\mu F$$

$$L_i = 6.23mH$$

$$L_g = 0.138mH$$

$$R_f = 1.168\Omega$$

$$C_{dc} = 625\mu F$$

After the DC-link, a load was set in parallel to limit the current to produce exactly 10KW power at the output. The value of the this resistance was set to be 64Ω .

The PWM control block is implemented using three PI-controllers as discussed previously (refer to figures 4.8 ~ 4.10).

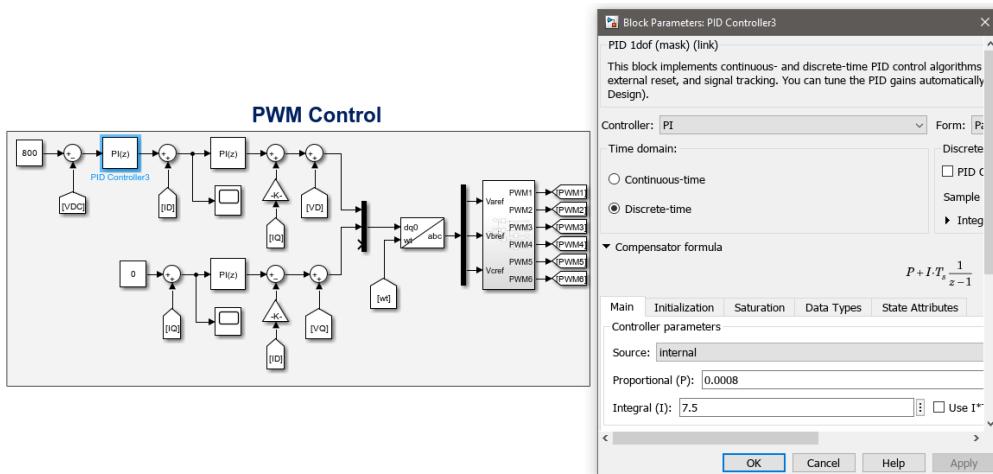


Figure 4.8: The outer loop PI-control block of 10KW system

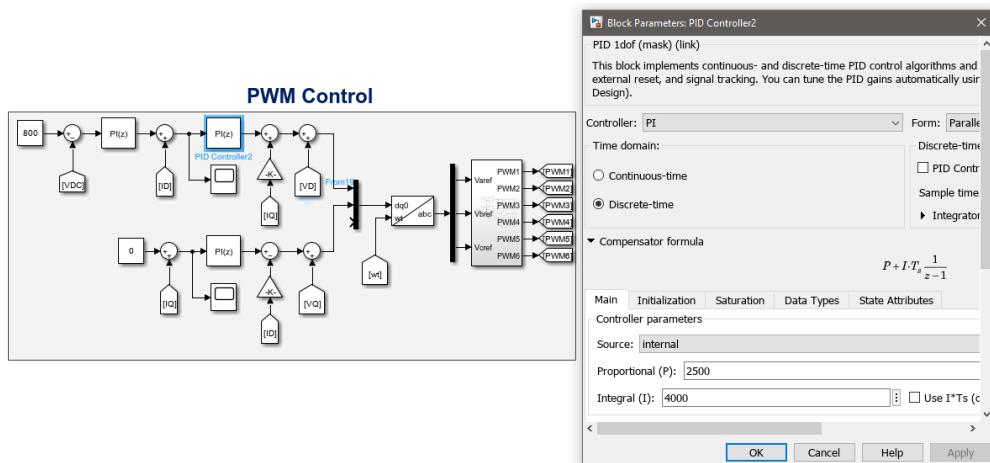


Figure 4.9: The inner loop PI-control block of 10KW system

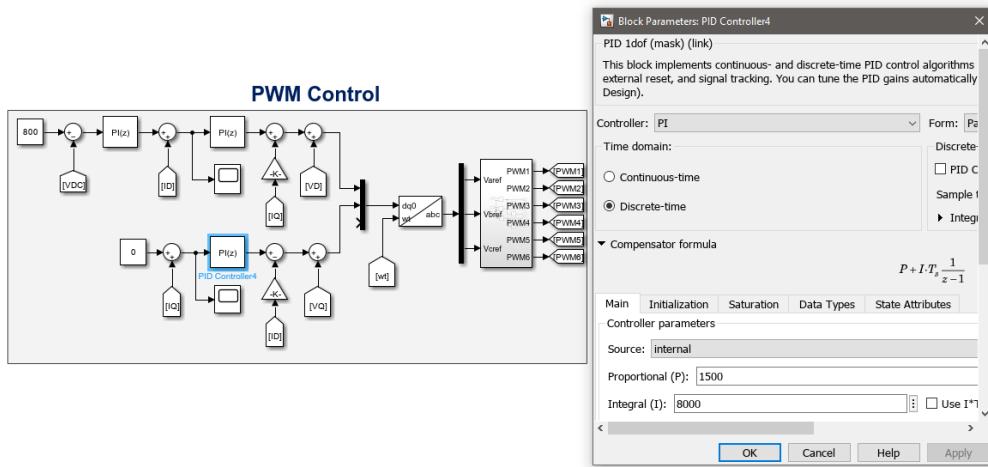


Figure 4.10: The quadrature PI-control block of 10KW system

The following results were obtained to show the input voltages and currents, the synchronism between the current and the voltage to show the power factor correction and the DC-link output voltage.

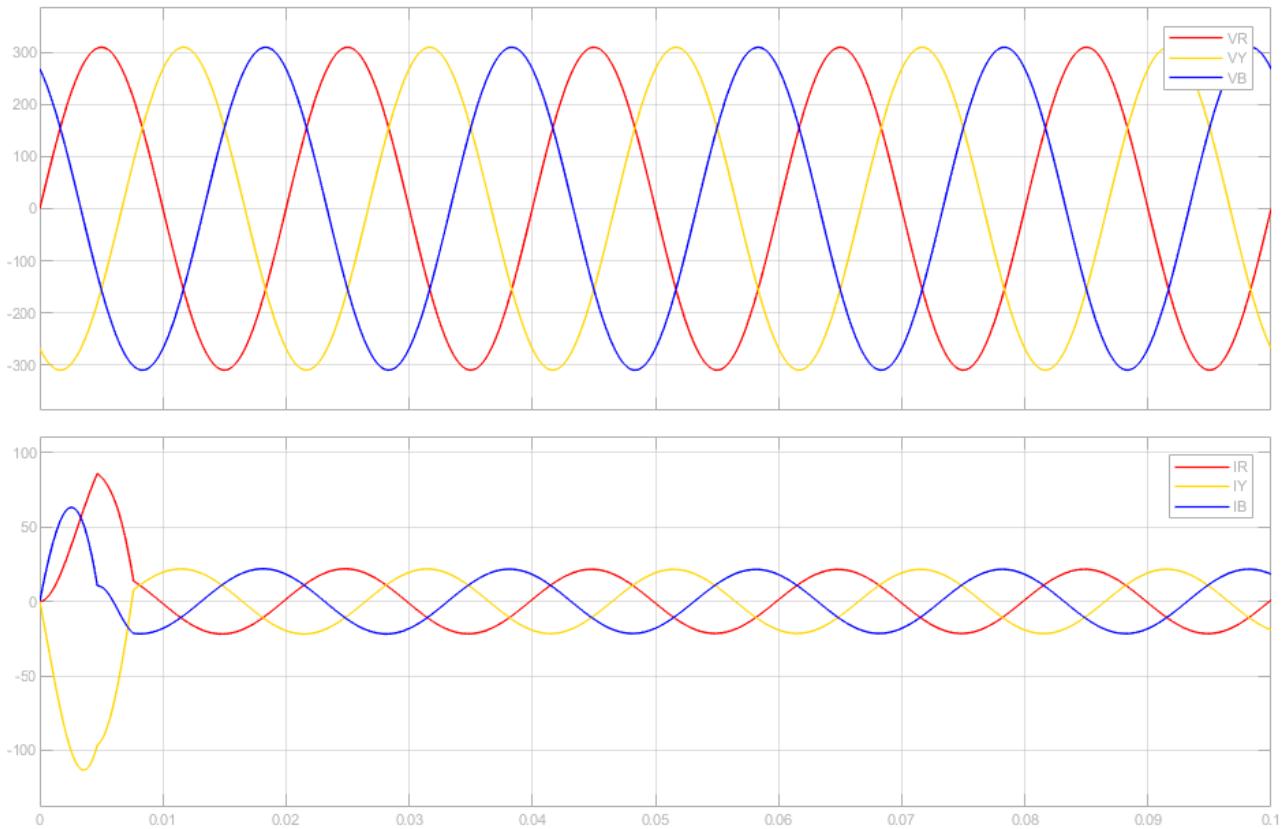


Figure 4.11: The three-phase input voltage and current of 10KW system

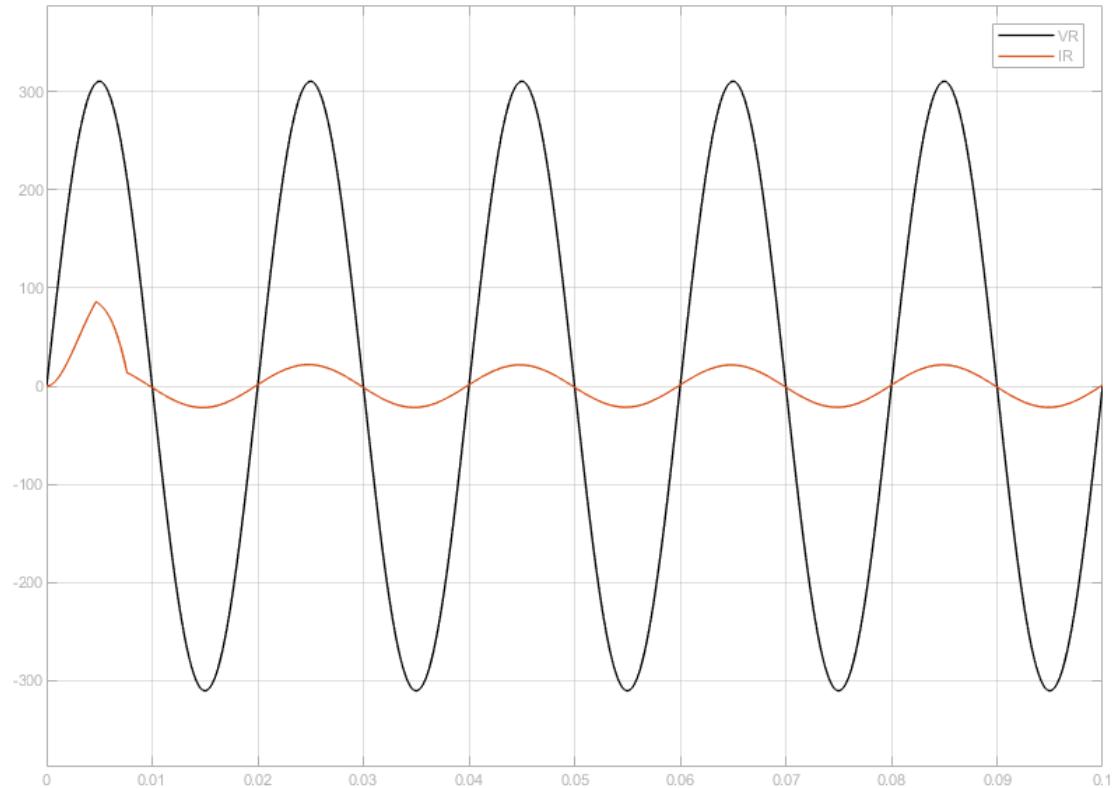


Figure 4.12: The input voltage and current of phase-R of 10KW system

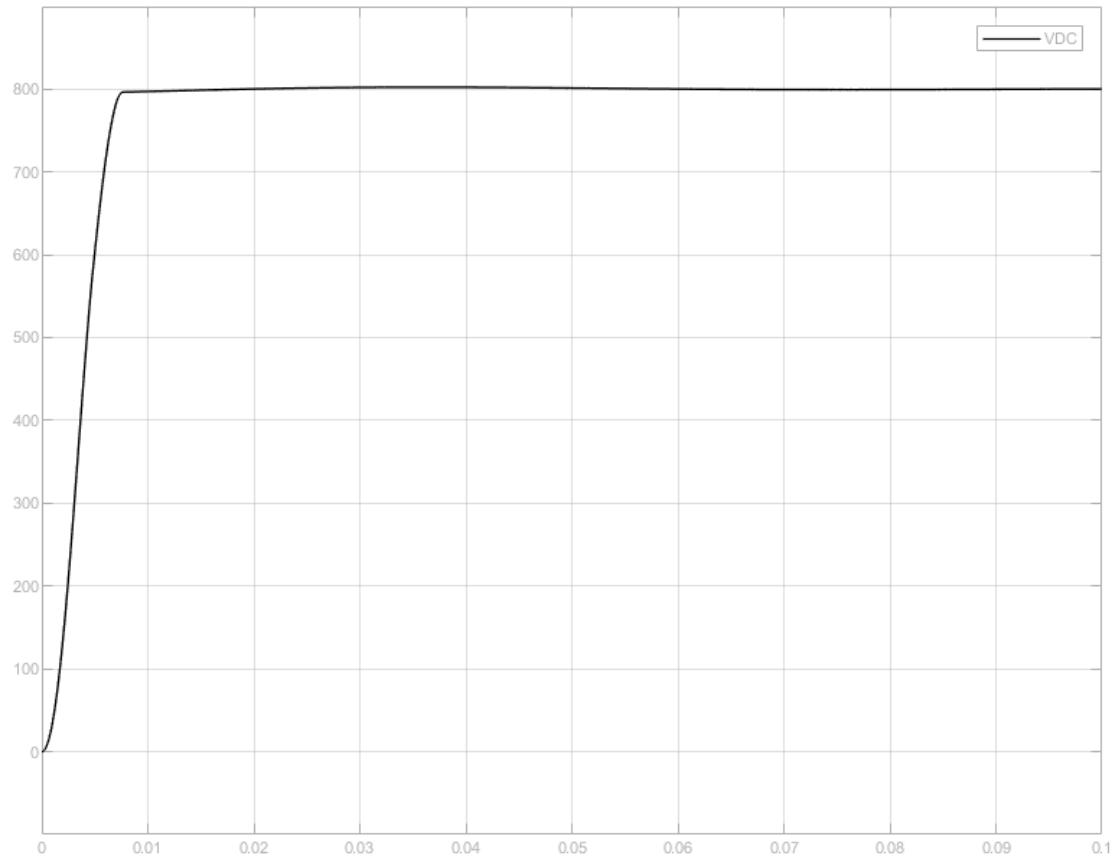


Figure 4.13: The DC-link output of 10KW system

Chapter 5

AC/DC Converter Design

This chapter delves into the realm of AC/DC converter design, shedding light on key aspects such as Filter Design, DC-Link Capacitor Selection, and Hardware Design. These components play a crucial role in the functionality of the converter, akin to building blocks that contribute to its optimal performance.

Firstly, we explore Filter Design, where we discuss various methods to improve the converter's performance using different types of filters. The aim is to provide a clear understanding of these methods, enabling practitioners to choose the most suitable one for their specific applications.

Moving on, DC-Link Capacitor Selection takes center stage, emphasizing the importance of selecting the right component for effective converter operation. This section guides through the considerations involved in making informed choices.

The chapter then addresses Hardware Design, focusing on the configuration of electronic components to ensure seamless functionality. We will discuss the software program used to design the PCB boards and each board schematic will be presented for elaboration.

The discussion on the significance of precise calculations in determining system parameters forms a critical part of this chapter. These calculations are essential, especially in the design of fast offboard chargers for electric vehicles. By carefully considering factors like filter tuning and DC-link optimization, engineers can make informed decisions, aligning the converter with the demanding requirements of electric vehicle technology.

In essence, this chapter serves as a guide for practitioners, providing insights into the nuanced world of AC/DC converter design, where methodical considerations and informed choices pave the way for an efficient and reliable product.”

5.1 Filter Design

As we are concerned about our health, we use water filters to purify the water. The same happens with electricity; there are impurities in it called harmonics, which are not wanted in our electrical systems. Harmonics affect electrical equipment, increasing its heat, reducing its lifetime and efficiency, and introducing noise to any system connected to the grid. These are just a few of the negativities of harmonics.

So, we use filters, which are devices that filter the frequency of electronic signals by manipulating the waves' amplitude and phase shift. As we know, the sine wave has its amplitude and phase shift, so anything outside the boundaries of its amplitude and phase shift is not desired and needs to be eliminated. This leads us to Fourier series, a mathematical theory that analyzes the signal into the fundamental wave and its harmonics.

There are two types of filters: active and passive. Not all filters are suitable for every application, and not all filters remove all harmonic frequencies. Therefore, we need to carefully choose the suitable filter for each application.

5.1.1 Active Filters

They are called active because they need an external power source to operate and are built of op-amps. The main advantage of these filters is that the output signals meet low resistance, allowing the signals to be amplified, and we can also control the gain's value to control the output signal amplitude. Some common types of active filters are low-pass filters, high-pass filters, band-pass filters, and band-stop filters.

These filters are used at low frequencies, so we cannot use inductors in active filters as we know that $X_L = 2\pi fL$. At low frequencies, the reactance would be extremely low, so the low-frequency harmonics would not be eliminated; we can say that they would not be noticed by the filter. Therefore, if there is an application or system that operates at low frequencies, it is more efficient to use active filters.

5.1.2 Passive Filters

They are used in high switching frequency systems because op-amps cannot manage this range of power and frequency and grid-connected systems. We need to cut the harmonics that accompany the current out of the grid as they are called passive, so they do not need an external power source to operate. We can logically estimate why these passive filters are very well used in grid-connected systems. We need to purify the signals out from the grid, so we cannot use them to supply the active filter. Therefore, we use passive filters. There are three types of passive filters: L, LC, and LCL filters. There are also two types, one called a trap filter and the other called a notch filter, but we are not interested in these types in this paper.

L-Type Filter

The simplest and most widely used passive filter is the L-type filter, consisting of a single inductor connected in series with the inverter output. It offers low-pass filtering characteristics, effectively attenuating high-frequency harmonics while allowing fundamental frequency components to pass through. However, its effectiveness is limited to lower switching frequencies and may require larger inductors for higher power applications, leading to higher costs. This leads to LC and LCL filters.

LC-Type Filter

An LC-type filter incorporates both an inductor (L) and a capacitor (C) in a series-parallel configuration. It supplies enhanced filtering performance compared to the L-type filter, offering a higher attenuation rate and broader harmonic suppression. However, its disadvantage, like the L-filter, is that at high switching frequencies, we need to use bulky inductors, leading to the same cost problem as before.

LCL-Type Filter

The LCL-type filter is a more advanced filter topology, featuring two inductors (L) separated by a capacitor (C). It offers superior harmonic suppression and a lower resonant frequency compared to the LC-type filter, making it suitable for higher power applications and higher switching frequencies. However, its design is more complex, and its main disadvantage is that there is some instability in frequencies near the resonant frequency. Damping resistors are added in series or parallel to the capacitor to prevent resonance-related instability.

5.1.3 Grid-Connected Inverters

The main consideration in choosing between LC and LCL filters is whether the system is connected to the grid or not. Suppose we have an inverter connected to the grid, as in Figure 5.1. We cannot use an LC filter here.

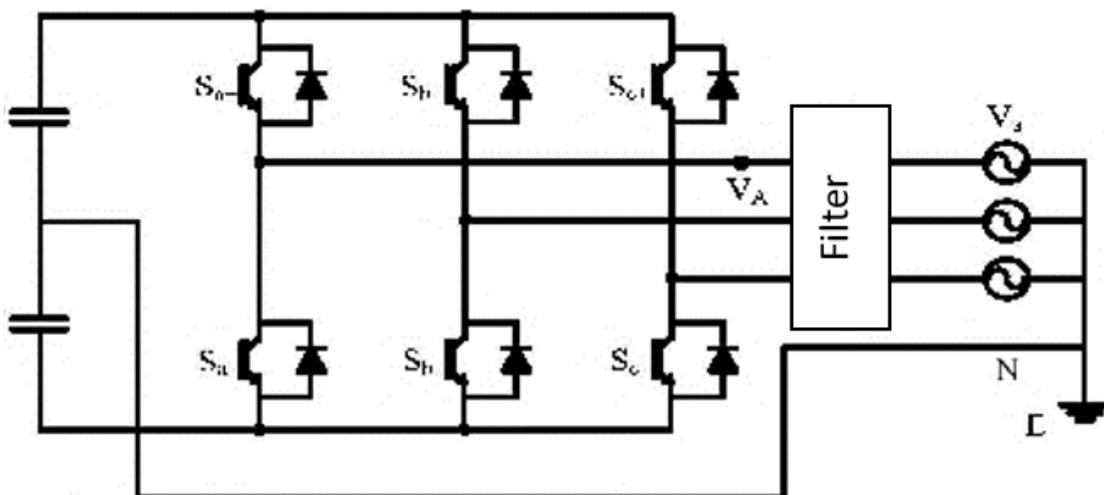


Figure 5.1: Three-phase inverter with passive filter

If we use an LC filter, the capacitors would be considered capacitive loads to the grid, so the power factor (PF) would be leading. This means that the voltage across the capacitors would come before the grid's voltage, and the output current from the inverter would not pass through to the grid but would flow to the capacitors.

In high-frequency harmonics, the grid impedance is less than the capacitive reactance, so in an LC filter, the current will flow to the grid with harmonics. However, in the case of an LCL filter,

the grid-connected inductor will block the current, and it will flow to the capacitors. Therefore, we use LCL filters in grid-connected inverters because of the tiny impedance of the grid, which causes a problem in high frequencies.

Here are some specific scenarios where an LCL filter would be a better choice than an LC filter:

- Grid-connected inverters: LCL filters are commonly used in grid-connected inverters to attenuate harmonics and follow grid harmonics standards. The lower resonant frequency of LCL filters makes them less susceptible to resonances caused by the grid impedance.
- High-power applications: In high-power applications, the switching frequency of the power converter is often higher to reduce the size and weight of the inductors and capacitors. This higher switching frequency can lead to more harmonics, so an LCL filter is often necessary to supply adequate attenuation.
- Applications with a sensitive load: If the load is sensitive to harmonics, such as a motor or a computer system, an LCL filter can help to protect the load from damage.

5.1.4 Method I

This method discusses the empirical design of L filter. Note that this method is not based on any reference but practical experience in the field. L filter was extremely popular until IEEE 519- 1992 standards were introduced. Because to meet all the requirements in the standards, the L filter rating and size become remarkably high.

The following parameters are needed for the design: E_n – Line to line RMS voltage (rectifier input), f_g – grid frequency and S_{rated} – apparent rated power. The base impedance is calculated using equation 5.1

$$Z_b = \frac{E_n^2}{S_{rated}} \quad (5.1)$$

We can assume that the inductive reactance (X_L) is roughly around 5% to 10% of the base impedance. Thus, we can calculate the inductive reactance and the inductance using the following equations:

$$X_L = (0.05 \text{ to } 0.1)Z_b \quad (5.2)$$

where

$$L = \frac{X_L}{2\pi f_g} \quad (5.3)$$

The addition of a resistor in series with the inductor in an L filter is crucial for maintaining stability, protecting components, and complying with EMI standards in grid-connected inverter applications. This resistor value can be empirically calculated as third of the inductive reactance as shown in the following equation:

$$R = \frac{X_L}{3} \quad (5.4)$$

Design Example

A step-by-step procedure to obtain parameters of the filter with considering the following given data, needed for the filter design: $E_n = 380V$ - line to line RMS voltage, $P_{rated} = 1000W$ - rated active power,

$f_g = 50\text{Hz}$ -grid frequency.

Considering a unity power factor system:

$$S_{rated} = P_{rated} = 1000\text{VA}$$

Therefore, the base impedance and the base capacitance are:

$$Z_b = \frac{380^2}{1000} = 144.4\Omega$$

The filter inductive reactance can be calculated by:

$$X_L = 0.1 * 144.4 = 14.4\Omega$$

To calculate the inductance:

$$L = \frac{14.4}{2\pi * 50} = 45mH$$

Therefore, the resonant frequency satisfies the equation, and the damping resistance can be calculated as follows:

$$R = \frac{14.4}{3} = 4.8\Omega$$

Simulation

A simulation of method I was done on MATLAB-Simulink to check the performance of the system with the filter using the design example that was mentioned previously in that method. Here is the output voltage V_{DC} :

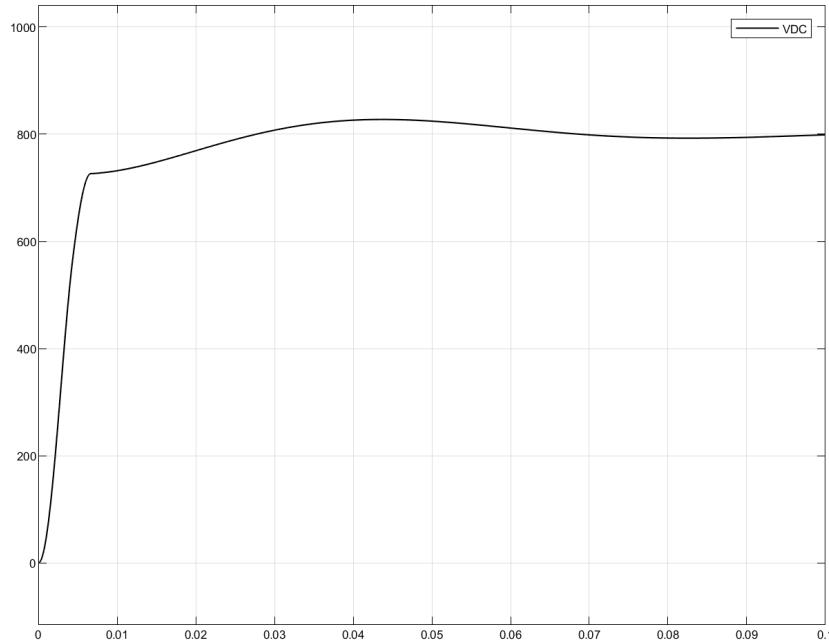


Figure 5.2: The output voltage on the DC-link – method I

Also, we had to check the phase shift between voltage and current of one of the phases as shown in Figure 5.3:

Note that this is not the actual waveform of the current but a multiple of it. It was multiplied by fifty just so we can observe the two wave-forms at the same time.

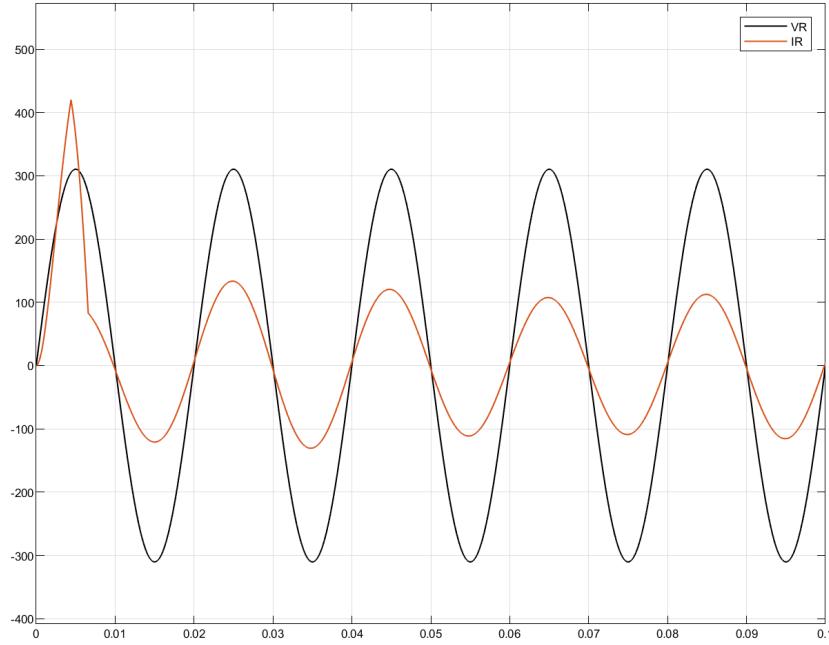


Figure 5.3: The current and the phase voltage of phase R – method I

5.1.5 Method II

The design of LCL filters must consider several critical constraints, including current ripple, filter size, and switching ripple attenuation. As noted in [6], the reactive power variation introduced by the capacitor can cause resonance, potentially destabilizing the system. To address this issue, a damping mechanism, such as a resistor in series with the capacitor, is recommended.

This method meticulously outlines the LCL filter design process, emphasizing the importance of proper damping to prevent resonance. The algorithm for selecting LCL filter parameters utilizes the converter's power rating, grid frequency, and switching frequency as inputs.

The following parameters are needed for the design: E_n – Line to line RMS voltage (rectifier input), V_{ph} – phase voltage (rectifier input), P_n – rated active power, V_{DC} – DC bus voltage, f_g – grid frequency, f_{sw} – switching frequency and f_{res} – resonance frequency.

The base impedance and base capacitance are defined by equations 5.5 and 5.6. Thus, the filter values will be referred in % of the base values:

$$Z_b = \frac{E_n^2}{P_n} \quad (5.5)$$

$$C_b = \frac{1}{\omega_n Z_b} \quad (5.6)$$

For the design of the filter capacitance, it is considered that the maximum power factor variation seen by the grid is 5%, as it is multiplied by the value of base impedance of the system: $C_f = 0.05 C_b$, where L_i is inverter side inductor. A 10% ripple of the rated current for the design parameters is given by:

$$\Delta I_{Lmax} = 0.1 I_{max} \quad (5.7)$$

where

$$I_{max} = \frac{P_n \sqrt{2}}{3V_{ph}} \quad (5.8)$$

$$L_i = \frac{V_{DC}}{6f_{sw}\Delta I_{Lmax}} \quad (5.9)$$

The main objective of the LCL filter design is in fact to reduce the expected 10% current ripple limit to 20% of its own value, resulting in a ripple value of 2% of the output current. To calculate the ripple reduction, the LCL filter equivalent circuit is first analyzed considering the inverter as a current source for each harmonic frequency.

The following equations give the relation between the harmonic current generated by the inverter and the once injected in the grid:

$$L_g = \frac{\sqrt{\frac{1}{K_a^2} + 1}}{C_f \omega_{sw}^2} \quad (5.10)$$

where, K_a is the desired attenuation.

A resistor in series (R_f) with the capacitor attenuates part of the ripple on the switching frequency to avoid the resonance. The value of this resistor should be one third of the impedance of the filter capacitor at the resonant frequency and the resistor in series with the filter capacitance is given by 5.13.

$$\omega_{res} = \sqrt{\frac{L_i + L_g}{L_i L_g C_f}} \quad (5.11)$$

$$10f_g < f_{res} < 0.5f_{sw} \quad (5.12)$$

It is necessary to check resonant frequency to satisfy 5.12. If it does not, the parameters should be re-chosen.

$$R_f = \frac{1}{3\omega_{res} C_f} \quad (5.13)$$

Design Example

A step-by-step procedure to obtain parameters of the filter with considering the following given data, needed for the filter design: $E_n = 380V$ - line to line RMS voltage, $V_{ph} = 220V$ - phase RMS voltage, $P_n = 1000W$ - rated active power, $V_{DC} = 800V$ - DC bus voltage, $f_g = 50Hz$ -grid frequency, $f_{sw} = 10KHz$ -switching frequency, $K_a = 20\%$ - attenuation factor is done.

Therefore, the base impedance and the base capacitance are:

$$Z_b = \frac{380^2}{1000} = 144.4\Omega$$

$$C_b = \frac{1}{2\pi * 50 * 144.4} = 22\mu F$$

The filter capacitance can be calculated by:

$$C_f = 0.05 * 22 * 10^{-6} = 1.1\mu F$$

To calculate the inverter-side inductor:

$$I_{max} = \frac{1000\sqrt{2}}{3 * 220} = 2.14A$$

$$\Delta I_{Lmax} = 0.1 * 2.14 = 0.214A$$

$$L_i = \frac{800}{6 * 10000 * 0.214} = 62.3mH$$

For the grid-side inductor:

$$L_g = \frac{\sqrt{\frac{1}{0.2^2} + 1}}{1.1 * 10^{-6} (2\pi * 10000)^2} = 1.38mH$$

Now, we shall check if the system is within the stable region to avoid resonance:

$$\omega_{res} = \sqrt{\frac{1.38 * 10^{-3} + 62.3 * 10^{-3}}{1.38 * 10^{-3} * 62.3 * 10^{-3} * 1.1 * 10^{-6}}} = 25949rad$$

$$f_{res} = \frac{25949}{2\pi} = 4129.92Hz$$

$$10 * 50 < f_{res} < 0.5 * 10000$$

Therefore, the resonant frequency satisfies the equation, and the damping resistance can be calculated as follows:

$$R_f = \frac{1}{3 * 2\pi * 4129.92 * 1.1 * 10^{-6}} = 11.68\Omega$$

Simulation

A simulation of method II was done on MATLAB-Simulink to check the performance of the system with the filter using the design example that was mentioned previously in that method. Here is the output voltage V_{DC} :

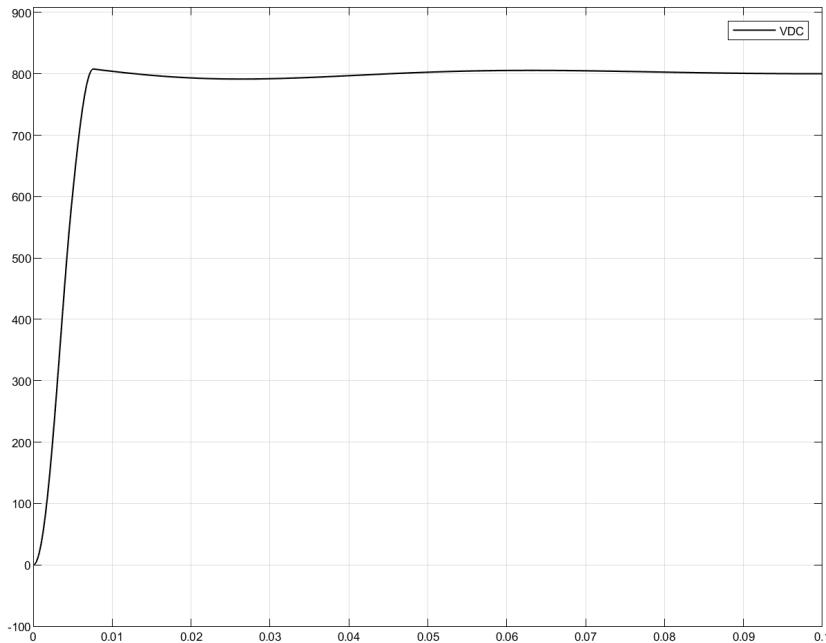


Figure 5.4: The output voltage on the DC-link – method II

Also, we had to check the phase shift between voltage and current of one of the phases as shown in Figure 5.5:

Note that this is not the actual waveform of the current but a multiple of it. It was multiplied by fifty just so we can observe the two wave-forms at the same time.

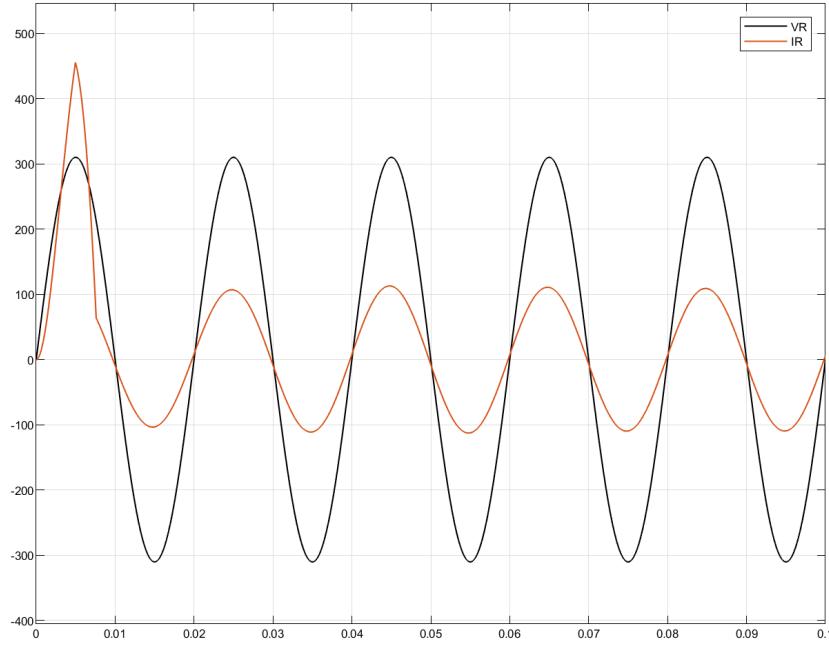


Figure 5.5: The current and the phase voltage of phase R – method II

5.1.6 Method III

The design of LCL filters plays a crucial role in grid-connected inverter applications, ensuring efficient power transfer and minimizing harmonic distortion. This method, inspired by [7], provides a comprehensive framework for designing LCL filters that meet specific performance requirements while addressing potential stability issues. The method delves into the fundamental principles of LCL filter dynamics, enabling designers to make informed decisions about filter parameter selection.

To design the filter using this method, some parameters must be provided which are: S_{rated} – apparent rated power, V_{ph} – phase voltage (rectifier input), f_g – grid frequency and f_{sw} – switching frequency.

The filter capacitance is calculated at reactive power equals 5% of the rated apparent power of the system. The reactive power is calculated as follows:

$$Q_{rated} = C_f \omega_n V_{ph}^2 \quad (5.14)$$

where ω_n is the grid angular frequency. Therefore, the filter capacitance can be calculated according to equation 5.15.

$$C_f = \frac{0.05 S_{rated}}{2\pi f_g V_{ph}^2} \quad (5.15)$$

It is worth mentioning that the resonance frequency can be calculated as in the following equation:

$$f_{res} = \frac{f_{sw}}{10} \quad (5.16)$$

The value of the inverter-side inductor is selected based on the switching current. According to IEEE, the switching current is only 0.3% of the rated grid current.

$$I_{sw} = 0.003 I_{grid} \quad (5.17)$$

where

$$I_{grid} = \frac{S_{rated}}{3V_{ph}} \quad (5.18)$$

Now, for a triangular PWM scheme, minimum value of the switching voltage at switching frequency is 90% of the grid phase voltage as shown in equation 5.19.

$$V_{sw} = 0.9V_{ph} \quad (5.19)$$

Using the equations above inductance can be calculated as:

$$L_{min} = \frac{1}{|\omega_{sw} \frac{I_{sw}}{V_{sw}} \left(1 - \frac{\omega_{sw}^2}{\omega_{res}^2}\right)|} \quad (5.20)$$

Inverter-side inductor and grid-side inductor can be assumed to have the same value which is half of the calculated inductance (L_{min}).

$$L_g = L_i = \frac{L_{min}}{2} \quad (5.21)$$

These are the minimum values of the required inductances. The maximum values are calculated based on the voltage drop across it. Voltage drop is always limited to 20% of the grid phase voltage. So maximum inductance is given by:

$$L_{max} = \frac{0.2 V_{ph}}{2\pi f_g I_{grid}} \quad (5.22)$$

Design Example

To derive the parameters essential for filter design, follow these step-by-step procedures using the provided data: $V_{ph} = 220V$ - phase RMS voltage, $P_{rated} = 1000W$ - rated active power, $f_g = 50Hz$ -grid frequency, $f_{sw} = 10KHz$ - switching frequency.

Therefore, rated apparent power can be calculated as follow:

$$S_{rated}^2 = (0.05S_{rated})^2 + 1000^2$$

$$S_{rated} \cong 1000VA$$

To calculate the filter capacitance:

$$C_f = \frac{0.05 * (\frac{1000}{3})}{2\pi * 50 * 220^2} = 1.1\mu F$$

The resonance frequency is achieved by:

$$f_{res} = \frac{10000}{10} = 1000Hz$$

Calculating the minimum value of the inductance:

$$I_{grid} = \frac{1000}{3 * 220} = 1.51A$$

$$I_{sw} = 0.003 * 1.51 = 4.45mA$$

$$V_{sw} = 0.9 * 220 = 198V$$

$$L_{\min} = \frac{1}{|(2\pi * 10000)^{\frac{4.45*10^{-3}}{198}} \left(1 - \frac{(2\pi*10000)^2}{(2\pi*1000)^2}\right)|} = 7.15mH$$

So, the minimum value of the inverter-side and grid-side inductors is equal to:

$$L_g = L_i = \frac{7.15 * 10^{-3}}{2} = 3.58mH$$

To get the maximum value of the inductance:

$$L_{\max} = \frac{0.2 * 220}{2\pi * 50 * 1.51} = 92.75mH$$

The maximum value of the inverter-side and grid-side inductors is:

$$L_g = L_i = \frac{92.75 * 10^{-3}}{2} = 46.37mH$$

Simulation

A simulation of method III was done on MATLAB-Simulink to check the performance of the system with the filter using the design example that was mentioned previously in that method. Here is the output voltage V_{DC} :

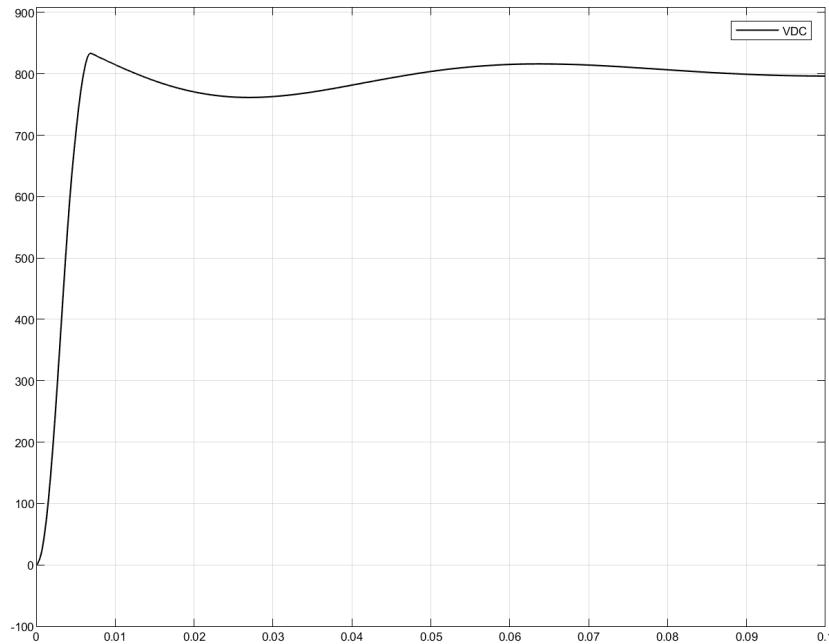


Figure 5.6: The output voltage on the DC-link – method III

Also, we had to check the phase shift between voltage and current of one of the phases as shown in Figure 5.7:

Note that this is not the actual waveform of the current but a multiple of it. It was multiplied by fifty just so we can observe the two wave-forms at the same time.

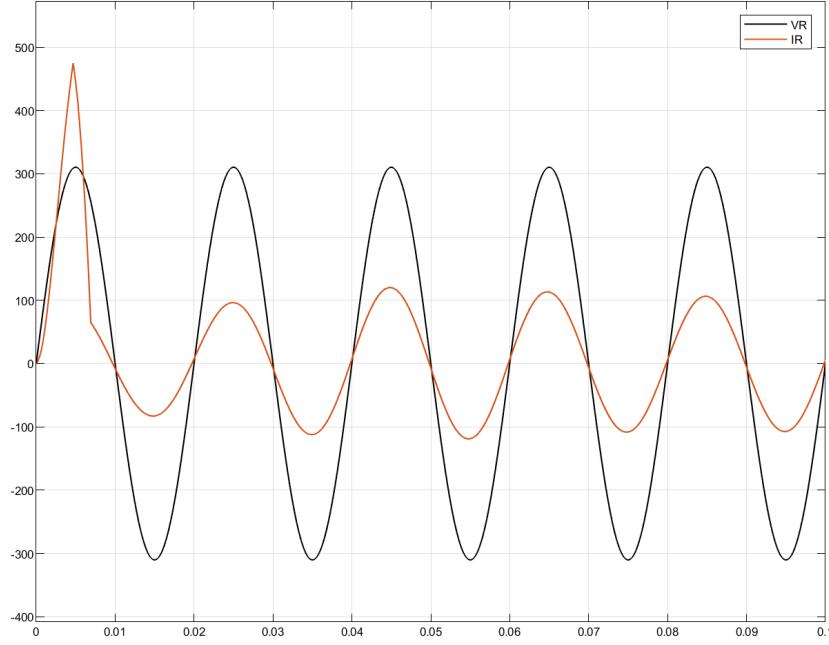


Figure 5.7: The current and the phase voltage of phase R – method III

5.1.7 Method IV

This method according to [8] deals with a design method of LCL filter for grid-connected three-phase inverters. By analyzing total harmonic distortion of the current (THD_i) in the inverter-side inductor and the ripple attenuation factor of the current (RAF) injected to the grid through the LCL network, the parameter of LCL can be clearly designed.

The base impedance of the system must be known before choosing the LCL filter parameters. The base values of the impedance, inductance, and capacitance are defined as in equations 5.23 ~ 5.25.

$$Z_b = \frac{E_n^2}{P_n} \quad (5.23)$$

$$L_b = \frac{Z_b}{\omega_n} \quad (5.24)$$

$$C_b = \frac{1}{\omega_n Z_b} \quad (5.25)$$

The inductance of inverter-side inductor is obtained by setting THD_i within 10% to 30%. If THD_i is set below 10%, the inductance is increased, and the resonant frequency decreases. If THD_i is increased more than 30%, the resonant frequency increases. The resonant frequency should be set between the bandwidth of the controller and switching frequency.

$$L_i = \frac{f_g}{f_{sw}} \times \frac{L_b}{\text{THD}_i} \times \sqrt{\frac{\pi^2}{18} \times \left(\frac{3}{2} - \frac{4\sqrt{3}}{\pi} m_a + \frac{9}{8} m_a^2 \right)} \quad (5.26)$$

where m_a is the modulation index.

$$m_a = \frac{V_{ph} 2\sqrt{2}}{V_{DC}} \quad (5.27)$$

Filter capacitance must be set properly by setting x less than 5% of base capacitance as follows:

$$C_f \leq x \frac{1}{\omega_n Z_b} \quad (5.28)$$

Use equation 5.29 to extract the grid-side inductance. After setting proper RAF, calculate the grid-side inductance.

$$L_g = \frac{RAF + 1}{RAF C_f \omega_{sw}^2} \quad (5.29)$$

Make sure the total inductance of inductor which is sum of the inductance of inverter-side inductor and grid-side inductor is less than 10% of the base value of the inductance.

Design Example

A step-by-step procedure to obtain parameters of the filter with considering the following given data, needed for the filter design: $E_n = 380V$ - line to line RMS voltage, $V_{ph} = 220V$ - phase RMS voltage, $P_n = 1000W$ - rated active power, $V_{DC} = 800V$ - DC bus voltage, $f_g = 50Hz$ -grid frequency, $f_{sw} = 10KHz$ - switching frequency, $THD_i = 20\%$ - total harmonic distortion of the current, $RAF = 20\%$ - attenuation factor is done.

Therefore, the base impedance and the base capacitance are:

$$\begin{aligned} Z_b &= \frac{380^2}{1000} = 144.4\Omega \\ L_b &= \frac{144.4}{2\pi * 50} = 0.4596H \\ C_b &= \frac{1}{2\pi * 50 * 144.4} = 22\mu F \end{aligned}$$

The filter capacitance can be calculated by:

$$C_f \leq 0.05 * 22 * 10^{-6} = 1.1\mu F$$

The modulation index is as follows:

$$m_a = \frac{220 * 2\sqrt{2}}{800} = 0.778$$

To calculate the inverter-side inductor:

$$L_i = \frac{50}{10000} \times \frac{0.4596}{0.2} \times \sqrt{\frac{\pi^2}{18} \times \left(\frac{3}{2} - \frac{4\sqrt{3}}{\pi} * 0.778 + \frac{9}{8}(0.778)^2 \right)} = 5.8mH$$

For the grid-side inductor:

$$L_g = \frac{0.2 + 1}{0.2 * 1.1 * 10^{-6} (2\pi * 10000)^2} = 1.38mH$$

To make sure the design is correct:

$$\begin{aligned} L_g + L_i &< 0.1L_b \\ 1.38 * 10^{-3} + 5.8 * 10^{-3} &< 0.1 * 0.4596 \end{aligned}$$

Therefore, the filter is well designed.

Simulation

A simulation of method IV was done on MATLAB-Simulink to check the performance of the system with the filter using the design example that was mentioned previously in that method. Here is the output voltage V_{DC} :

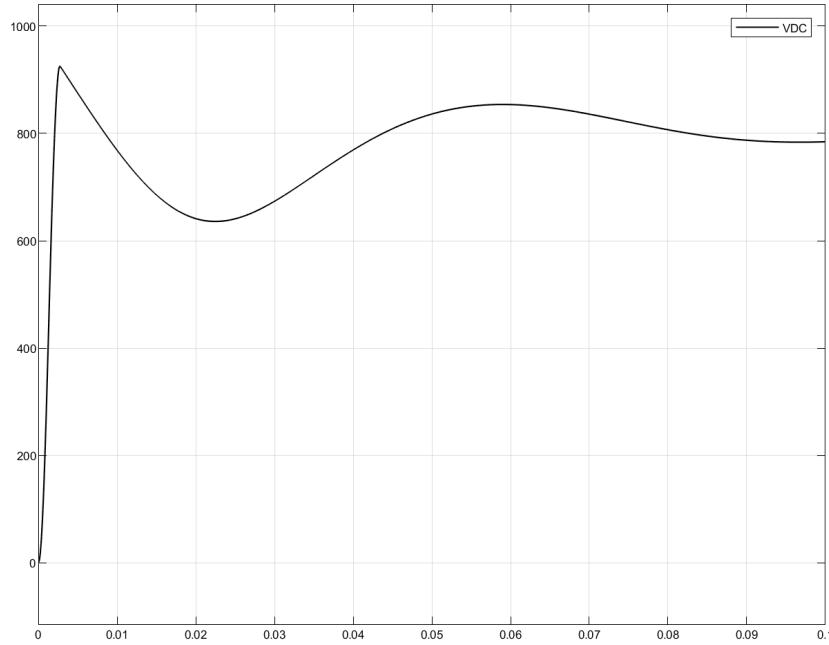


Figure 5.8: The output voltage on the DC-link – method IV

Also, we had to check the phase shift between voltage and current of one of the phases as shown in Figure 5.9:

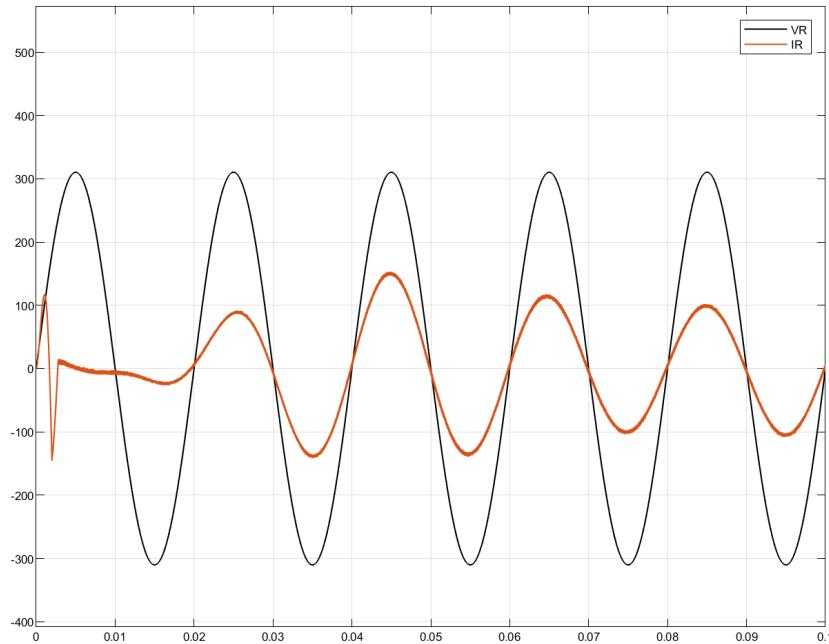


Figure 5.9: The current and the phase voltage of phase R – method IV

Note that this is not the actual waveform of the current but a multiple of it. It was multiplied by fifty just so we can observe the two wave-forms at the same time.

5.1.8 Method V

The design of LCL filter can also be done via MATLAB code that was mentioned in [9]. You may enter the system inputs like: P_n – active rated power, V_{ph} – phase voltage (rectifier input), V_{DC} – DC bus voltage, f_g – grid frequency and f_{sw} – switching frequency.

It is worth mentioning that the code that is present in [9] is for a single-phase grid-connected inverter but some of the data was changed to suit the three-phase grid-connected inverter, which is our case.

Design Example

To derive the parameters essential for filter design, follow these step-by-step procedures using the provided data: $V_{ph} = 220V$ - phase RMS voltage, $P_{rated} = 1000W$ - rated active power, $f_g = 50Hz$ -grid frequency, $f_{sw} = 10KHz$ - switching frequency, $r = 0.6$. Therefore, the MATLAB code is as follows:

```
% System parameters
Pn = 1000; % Inverter power
Vph = 220; %Grid phase RMS voltage
Vdc=800; %DC link voltage
fn = 50; %Grid frequency
fsw = 10000; %Switching frequency

En = Vph*sqrt(3);
wn = 2*pi*fn;
wsw = 2*pi*fsw;

% Base values
Zb = (En^2)/Pn
Cb = 1/(wn*Zb)

% Filter parameters
delta_Ilmax=0.1*((Pn*sqrt(2))/(3*Vph))
Li=Vdc/(8*fsw*delta_Ilmax) %Inverter side inductance
x = 0.05;
Cf = x*Cb %Filter capacitor

% Calculation of r, between Linv and Lg
r = 0.6;

% Grid side inductance
Lg = r*Li

% Calculation of frequency of the filter
wres = sqrt((Li+Lg)/(Li*Lg*Cf));
```

```
fres=wres/(2*pi)

%Damping resistance
Rd = 1/(3*wres*Cf)
```

And the LCL filter parameters as the output values of the code are as follow:

$$C_f = 1.1\mu F$$

$$L_i = 46.7mH$$

$$L_g = 28mH$$

$$R_f = 42.11\Omega$$

Simulation

A simulation of method V was done on MATLAB-Simulink to check the performance of the system with the filter using the design example that was mentioned previously in that method. Here is the output voltage V_{DC} :

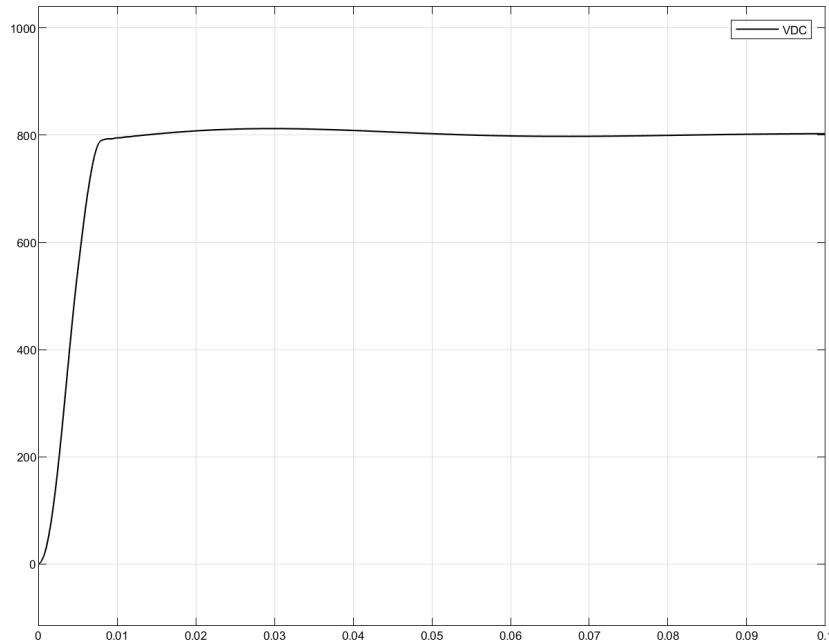


Figure 5.10: The output voltage on the DC-link – method V

Also, we had to check the phase shift between voltage and current of one of the phases as shown in Figure 5.11:

Note that this is not the actual waveform of the current but a multiple of it. It was multiplied by fifty just so we can observe the two wave-forms at the same time.

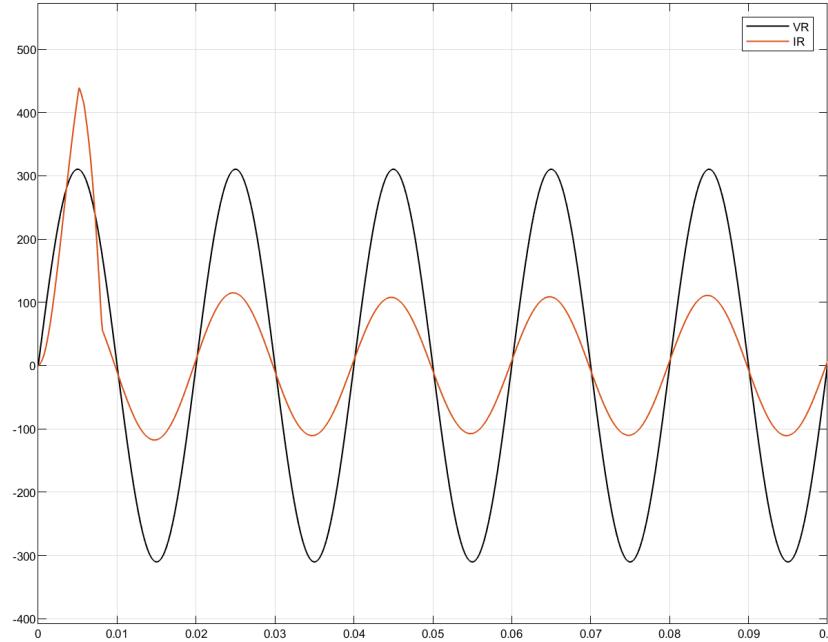


Figure 5.11: The current and the phase voltage of phase R – method V

5.1.9 Comparison

After discussing multiple methods, it is now time to compare the output of each method. The following table (Table 5.1) contains the output of each method.

Method	L_i (mH)	L_g (mH)	C_f (μ F)
Method I	45	-	-
Method II	62.3	1.38	1.1
Method III	3.58 – 46.37	3.58 – 46.37	1.1
Method IV	5.8	1.38	1.1
Method V	46.7	28	1.1

Table 5.1: Comparison between the output of different design methods

After learning all the different methods, each method shall be considered carefully to get the optimum output for the desired system. In our case, we have done multiple simulations to notice the output of each method. It was observed that each method produced the same output with slight differences.

Yet, Method IV had the worst output as the phase current was full of ripples even by substituting by different values of inductance within the calculated range, also the output voltage had the highest settling time.

Method II and method V had the lowest overshoot compared to the rest in this specific case, but method V had a smoother output. But at higher power (10k watt), method II had a way better response than method V leading it to be our preferred method. The PI controllers were calibrated in a way to have a leading power factor of 0.9998 with settling time of less than a half cycle with settling error of 0.5%. Also, the second method's design was checked by equation 5.12, to make sure that the design would avoid resonance problems.

5.1.10 Chosen Method

Two designs were done based on method II for both the low-rating system (1kW) and the high-rating system (10kW) to check its output.

Design Example: Low-Rating System (1KW)

A step-by-step procedure to obtain parameters of the filter with considering the following given data, needed for the filter design: $E_n = 100V$ - line to line RMS voltage, $V_{ph} = 57.73V$ - phase RMS voltage, $P_n = 1000W$ - rated active power, $V_{DC} = 200V$ - DC bus voltage, $f_g = 50Hz$ -grid frequency, $f_{sw} = 10KHz$ - switching frequency, $K_a = 20\%$ - attenuation factor is done. Therefore, the base impedance and the base capacitance are:

$$Z_b = \frac{100^2}{1000} = 10\Omega$$

$$C_b = \frac{1}{2\pi * 50 * 10} = 3.18 * 10^{-4}F$$

The filter capacitance can be calculated by:

$$C_f = 0.05 * 3.18 * 10^{-4} = 15.915\mu F$$

To calculate the inverter-side inductor:

$$I_{max} = \frac{1000\sqrt{2}}{3 * 57.73} = 8.16A$$

$$\Delta I_{Lmax} = 0.1 * 8.16 = 0.816A$$

$$L_i = \frac{200}{6 * 10000 * 0.816} = 4mH$$

For the grid-side inductor:

$$L_g = \frac{\sqrt{\frac{1}{0.2^2} + 1}}{15.915 * 10^{-6} (2\pi * 10000)^2} = 95.492\mu H$$

Now, we shall check if the system is within the stable region to avoid resonance:

$$\omega_{res} = \sqrt{\frac{4 * 10^{-3} + 95 * 10^{-6}}{4 * 10^{-3} * 95 * 10^{-6} * 15.915 * 10^{-6}}} = 25952.26rad$$

$$f_{res} = \frac{25952.26}{2\pi} = 4130.4Hz$$

$$10 * 50 < f_{res} < 0.5 * 10000$$

Therefore, the resonant frequency satisfies the equation, and the damping resistance can be calculated as follows:

$$R_f = \frac{1}{3 * 2\pi * 4130.4 * 16 * 10^{-6}} = 0.8027\Omega$$

Design Example: High-Rating System (10KW)

A step-by-step procedure to obtain parameters of the filter with considering the following given data, needed for the filter design: $E_n = 380V$ - line to line RMS voltage, $V_{ph} = 220V$ - phase RMS voltage, $P_n = 10\text{KW}$ - rated active power, $V_{DC} = 800V$ - DC bus voltage, $f_g = 50\text{Hz}$ -grid frequency, $f_{sw} = 10\text{KHz}$ - switching frequency, $K_a = 20\%$ - attenuation factor is done. Therefore, the base impedance and the base capacitance are:

$$Z_b = \frac{380^2}{10000} = 14.44\Omega$$

$$C_b = \frac{1}{2\pi * 50 * 14.44} = 220\mu F$$

The filter capacitance can be calculated by:

$$C_f = 0.05 * 22 * 10^{-6} = 11\mu F$$

To calculate the inverter-side inductor:

$$I_{max} = \frac{10000\sqrt{2}}{3 * 220} = 21.4A$$

$$\Delta I_{Lmax} = 0.1 * 21.4 = 2.14A$$

$$L_i = \frac{800}{6 * 10000 * 2.14} = 6.23mH$$

For the grid-side inductor:

$$L_g = \frac{\sqrt{\frac{1}{0.2^2} + 1}}{11 * 10^{-6}(2\pi * 10000)^2} = 0.138mH$$

Now, we shall check if the system is within the stable region to avoid resonance:

$$\omega_{res} = \sqrt{\frac{0.138 * 10^{-3} + 6.23 * 10^{-3}}{0.138 * 10^{-3} * 6.23 * 10^{-3} * 11 * 10^{-6}}} = 25949rad$$

$$f_{res} = \frac{25949}{2\pi} = 4129.92Hz$$

$$10 * 50 < f_{res} < 0.5 * 10000$$

Therefore, the resonant frequency satisfies the equation, and the damping resistance can be calculated as follows:

$$R_f = \frac{1}{3 * 2\pi * 4129.92 * 11 * 10^{-6}} = 1.168\Omega$$

5.2 DC-Link Capacitor Calculations

The DC link capacitor in a three-phase grid-connected inverter is a crucial component that serves multiple purposes, including:

- *Smoothing pulsating DC voltage:* The DC voltage often exhibits pulsations due to the inherent characteristics of these sources. The DC link capacitor acts as a reservoir, smoothing out these pulsations and providing a stable DC voltage to the inverter.

- *Energy storage:* During transient conditions, such as sudden changes in load, the DC link capacitor can provide or absorb energy to maintain the desired DC voltage level.
- *Filtering harmonics:* The switching operation of the inverter generates harmonic currents that can pollute the DC bus. The DC link capacitor helps to filter these harmonics, ensuring a cleaner DC supply for the inverter.
- *Limiting fault currents:* In the event of a fault, the DC link capacitor can limit the surge of fault current, protecting both the inverter and the connected equipment.

The selection of the appropriate DC link capacitor size is critical for the proper operation of the inverter. Several factors influence the capacitor selection, including:

1. Power rating of the inverter: The capacitor should be able to manage the maximum power output of the inverter.
2. DC voltage level: The capacitor must be rated for the DC voltage level of the system.
3. Permissible ripple current: The capacitor should be able to withstand the ripple current generated by the inverter's switching operation.
4. Desired ripple voltage: The capacitor selection determines the ripple voltage, which influences the inverter's efficiency and performance.
5. Transient response requirements: The capacitor should be able to support the transient energy demands of the system.
6. Environmental factors: The capacitor must be selected to withstand environmental conditions, such as temperature, humidity, and vibration.

There are two methods for calculating the DC-link capacitor value which we will discuss.

5.2.1 Method I

To calculate the DC link capacitor size based on [10], consider the following steps:

1. Determine the maximum DC power (P_{dc})
2. Calculate the RMS ripple current (I_{rms})

$$I_{rms} = m * \frac{P_{dc}}{2 * \sqrt{3} * V_{dc}} \quad (5.30)$$

3. Select an allowable ripple voltage (V_r): This is typically between 1% and 5% of the DC voltage.
4. Calculate the DC link capacitor capacitance (C_{dc}): Use the following formula:

$$C_{dc} = \frac{2 * P_{dc} * V_r}{I_{rms}^2 * \omega * V_{dc}} \quad (5.31)$$

where

- m is the modulation index
- V_{dc} is the DC voltage.
- ω is the angular frequency ($2\pi * \text{switching frequency}$)

5.2.2 Method II

Using capacitor's stored energy law:

$$C_{dc} = \frac{2 * P_{dc}}{V_{dc}^2 * f} \quad (5.32)$$

where

- f is the grid frequency
- V_{dc} is the DC voltage.
- P_{dc} is the maximum DC power.

5.2.3 Chosen Method

Two designs were done based on method II for both the low-rating system (1kW) and the high-rating system (10kW) to check its output.

Design Example: Low-Rating System (1KW)

A step-by-step procedure to obtain parameters of the filter with considering the following given data, needed for the filter design: $P_n = 1\text{kW}$ - rated active power, $V_{DC} = 200\text{V}$ - DC bus voltage, $f_g = 50\text{Hz}$ - grid frequency. Therefore, the DC-link capacitance is equal to:

$$C_{dc} = \frac{2 * 1000}{200^2 * 50} = 1mF$$

Design Example: High-Rating System (10KW)

A step-by-step procedure to obtain parameters of the filter with considering the following given data, needed for the filter design: $P_n = 10\text{kW}$ - rated active power, $V_{DC} = 800\text{V}$ - DC bus voltage, $f_g = 50\text{Hz}$ -grid frequency. Therefore, the DC-link capacitance is equal to:

$$C_{dc} = \frac{2 * 10000}{800^2 * 50} = 0.625mF$$

5.3 Component Selection

5.3.1 The Inverter Module

We have chosen an inverter module to begin with, to make the prototype of the main board of the AC/DC Rectification stage in our project.

We need to build a charger that can reach 7K watt to reach 22K watt by cascading, so we begin to build a prototype with lower rating to confirm that our topology is working well before evaluating it in high power rating.

Our prototype ratings are 1K watt with 200 V DC and 5 A at output, so we have chosen a 3-ph inverter ic_IKCM30F60GDXKMA1, its rating is 600V, 35A.

The Features

Fully isolated Dual In-Line molded module

- TRENCHSTOP™ IGBTs
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11V for signal transmission at VBS=15V
- Integrated bootstrap functionality
- Over current shutdown
- Temperature monitor
- Under-voltage lockout at all channels
- Low side emitter pins accessible for all phase current monitoring (open emitter)
- Cross-conduction prevention
- All six switches turn off during protection.
- Lead-free terminal plating; RoHS compliant
- Extremely low thermal resistance due to DCB

We bias the bootstrap with 15V using DC/DC transformer to make an isolation. Build the protection circuit from over-current and overheating. The Module can shutdown itself with the ITRIP pin that has a thermistor and send a signal (Volt Fault Out) to the micro-controller to alarm the fault.

5.3.2 The Current Sensor

The core of our topology is the closed loop feedback, so the measurement must be as we could to be accurate. We have chosen CAS transducer, the latest version of the LTS series. The nominal current is 25A to help us with future product.

The transducer has a multi-functional primary circuit that changes the nominal current lower to get more accuracy. In our Prototype we used the second technique that nominal current 12A. The

Number of primary turns	Primary nominal current rms I_{PN} [A]	Nominal* output voltage V_{out} [V]	Primary resistance R_p [mΩ] (typ.) at $+25^\circ C$	Recommended connections
1	± 25	2.5 ± 0.625	0.24	
2	± 12	2.5 ± 0.600	1.08	
3	± 8	2.5 ± 0.600	2.16	

Table 5.2: Recommended connections for different sensitivities

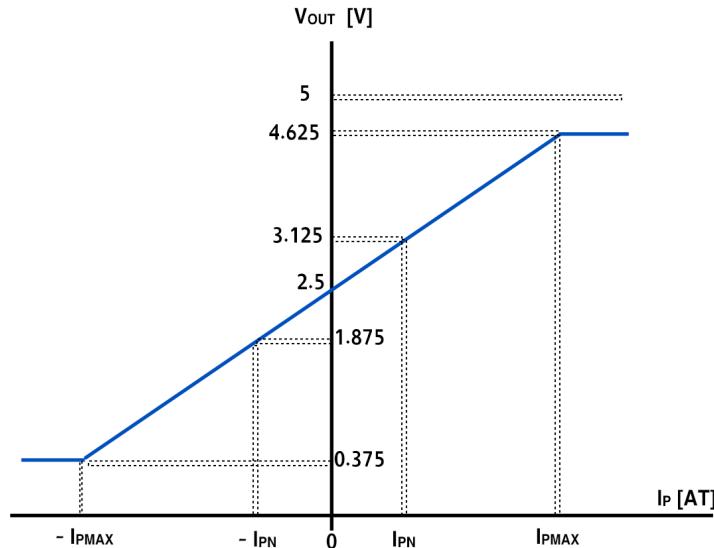


Figure 5.12: V_{out} versus I_p plot

most advantage is that the output signal does not need to re-scale or biasing and ready to send to the micro-controller.

5.3.3 The Voltage Sensor

We have chosen LV 25-P voltage transducer to get the voltage feedback

The Features

- Current equal to 10mA and Voltage ranging from 10V up to 500V

- Excellent accuracy
- Incredibly good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

This transducer needs an external circuit to re-scale and biasing the output signal before the controller, so we used an op-amp circuit after simulating it and get the desired output.

The transducer and the op-amp needed a positive and negative source power, so we used this topology to get the negative source. The following figure shows the internal connection of the sensor:

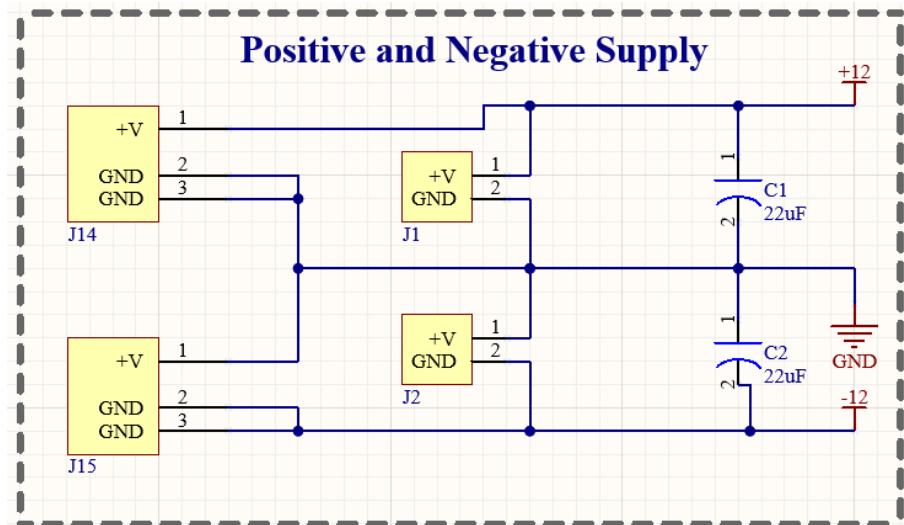


Figure 5.13: The schematic of the supply for the voltage sensor

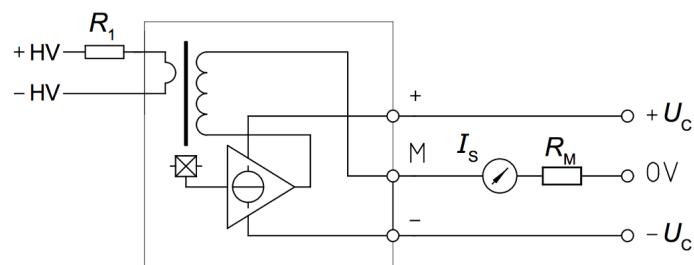


Figure 5.14: The internal connection of the voltage sensor

Primary Side (High Voltage):

- P1 and P2: terminals Connected to the voltage to be measured.
- R1 (External Resistor): Sets the primary voltage range corresponding to primary current of 10 mA.

Secondary Side (Low Voltage):

- +Vc: Connect this terminal to a positive power supply (5 to 15 V DC).
- -Vc: Connect this terminal to the negative power supply.
- OUT: signal to the micro-controller
- Rm (Scaling Resistor): Sets the output voltage range and sensitivity.

The resistors values can be calculated using the following equations:

$$R_m = \frac{V_{out}}{I_{out}} = 132\Omega \quad (5.33)$$

where

- V_{out} is the desired output voltage. (designed for 3.3V)
- I_{out} is the secondary circuit current.

$$R_1 = \frac{V_{in}}{I_p} = 50K\Omega \quad (5.34)$$

where V_{in} is equal to 500V and I_p is 10mA.

Interfacing with Micro-Controller - Op-Amp Technique

In case of AC voltage measurements, DSP can not receive negative voltage So we need to shift the signal out of the transducer to the positive and re-scale it to get the desired output. Op-amp adder circuit will perform this operation to convert $(-3.3V, 3.3V)$ to $(0V, 3.3V)$. *Procedures to Design the Op-Amp circuit:*

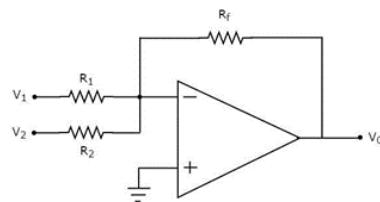


Figure 5.15: Op-amp circuit

where the first terminal represents the scale of input signal and the second terminal is the shift for scaled signal.

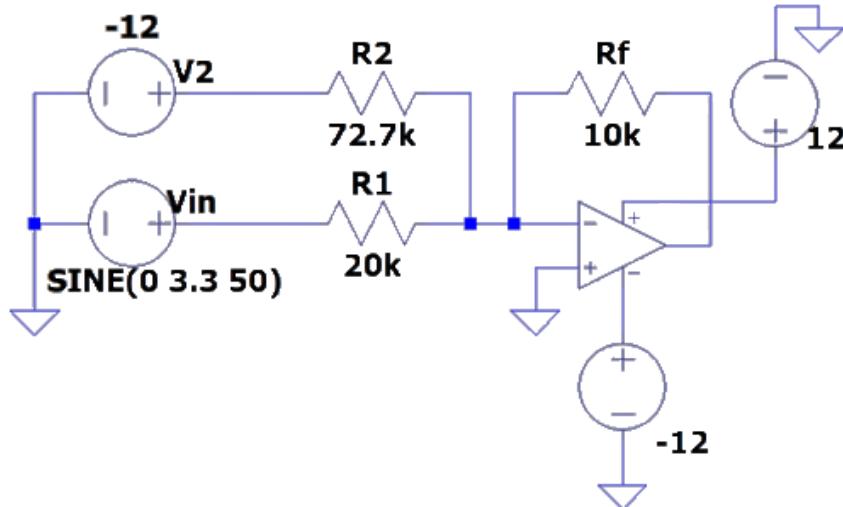


Figure 5.16: The circuit diagram of the op-amp

For input signal from sensor ,the AC voltage is first scaled to half, then shifted above x axis by this scaled value to obtain its peak positive value (V_{in}) and 0V.

$$-V_{out} = \left(\frac{R_f}{R_1} * V_{in} \right) + \left(\frac{R_f}{R_2} * V_2 \right) \quad (5.35)$$

for AC $V_{in} = 3.3V$

1. Scale the input signal to $\frac{1}{2}V_{in}$
 $\frac{R_f}{R_1} * V_{in} = 3.3/2$, assume $R_f = 10k\Omega$, so $R_1 = 20k\Omega$
2. Shift by $\frac{1}{2}V_{in}$
 $\frac{R_f}{R_2} * (V_2) = 3.3/2$, assume $V_2 = -12v$, so $R_2 = 72.7k\Omega$

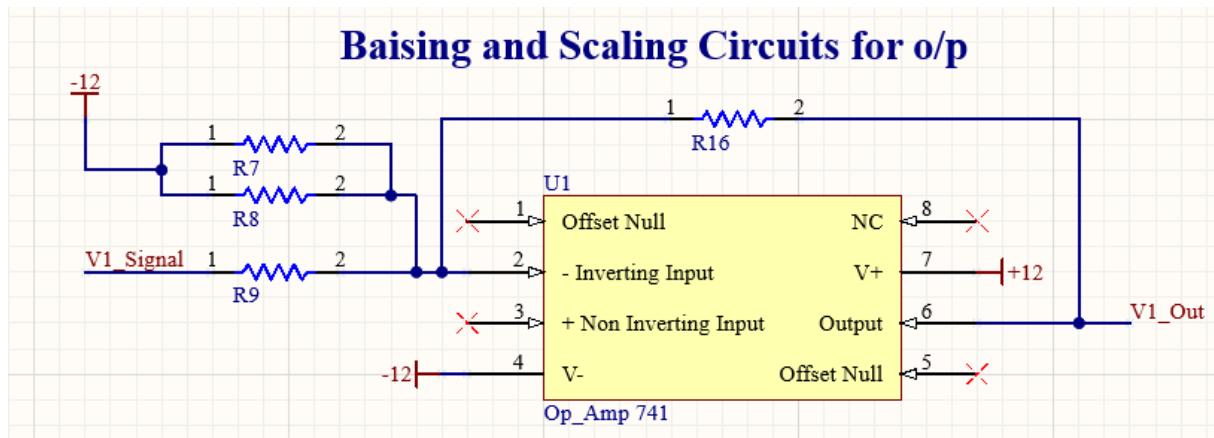


Figure 5.17: The schematic of the op-amp circuit

5.3.4 The Micro-Controller

We have chosen to use DSP LaunchpadF28069M, because it is the easier controller to generate our model on it. We built a DSP interfacing with the inverter using optocoupler circuit to make the suitable isolation. For further references click here: [datasheet](#).

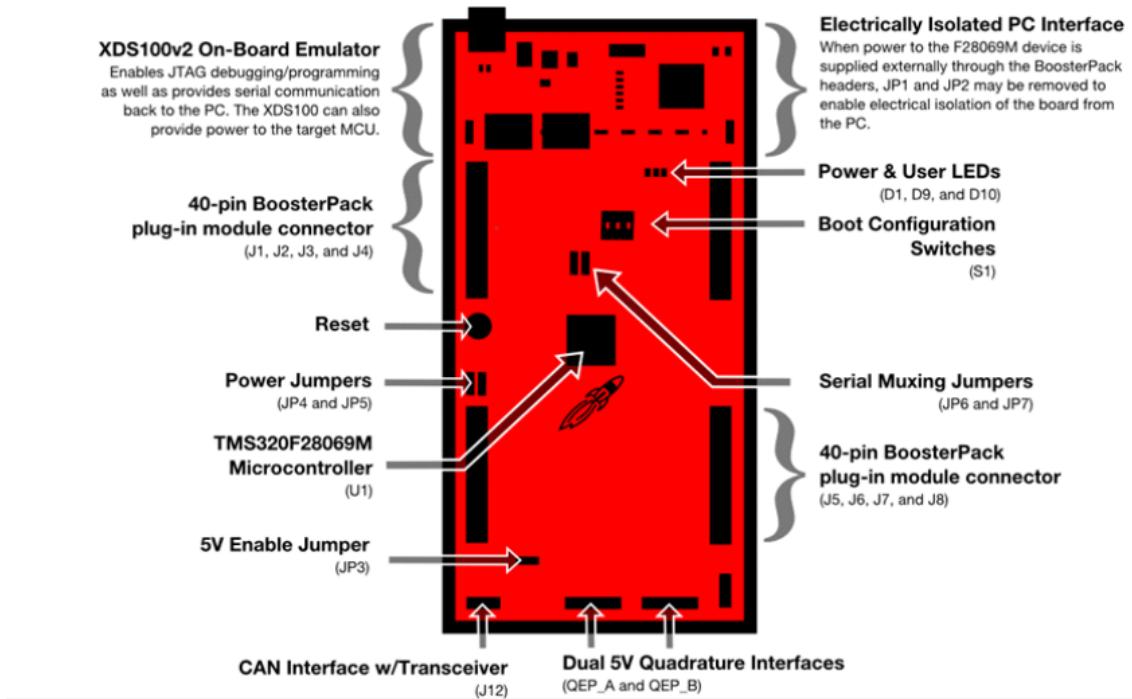


Figure 5.18: DSP LaunchpadF28069M

5.4 Hardware Design

Our hardware design process involved developing five specialized PCBs—Inverter module, DC-link board, current sensors board, voltage sensors board for feedback, and a micro-controller interfacing board. Altium Designer, version 2024, played a pivotal role in this endeavor, chosen over alternatives like Eagle for specific reasons.

Altium Designer's selection hinged on its robust feature set. Its advanced tools facilitated precise design implementation, crucial for our intricate requirements.

Choosing Altium Designer over Eagle was a strategic decision based on its advanced features, multi-board design capabilities, documentation quality, community support, and scalability. This choice streamlined our PCB design for the inverter system efficiently.

5.4.1 The Inverter Module

This board is considered the main board as it interfaces with the micro-controller and the DC-link board, also it interfaces to collect the feedback from the current and the voltage sensors boards. This

board has indicating green LED to indicate the power connection, a red LED to indicate faults, several test points, IDC connecting cable to interface with the micro-controller and bootstrap circuits.

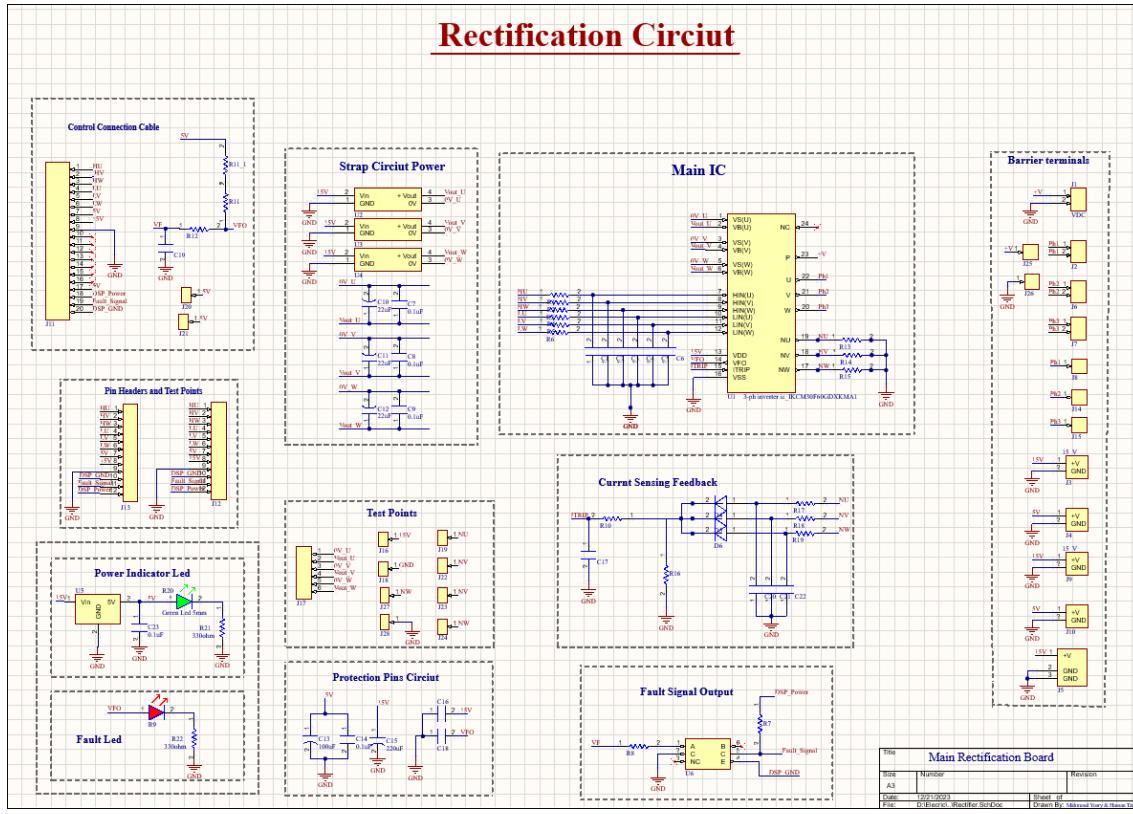
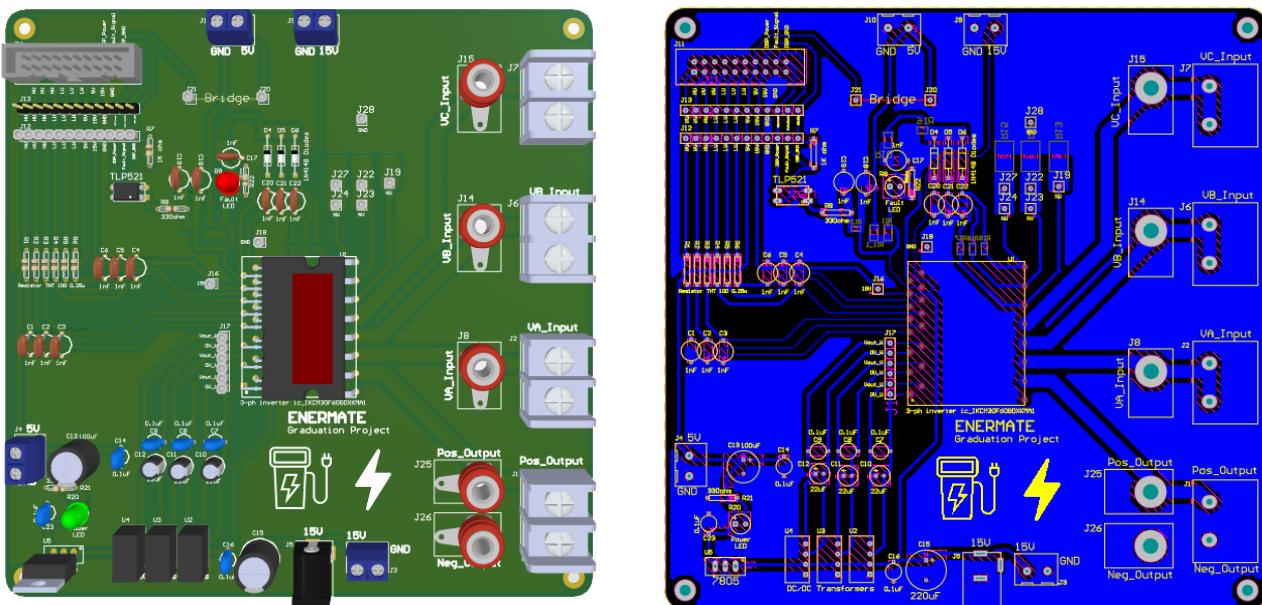


Figure 5.19: The schematic of the inverter module board



(a) Inverter module PCB 3D design

(b) Inverter module board - bottom layer

Figure 5.20: Inverter module hardware board design

5.4.2 DC-Link

According to our calculations that we have done in previous sections, we have designed a DC-Link to suit our project to literally link between the AC/DC Conversion and the DC/DC Conversion boards.

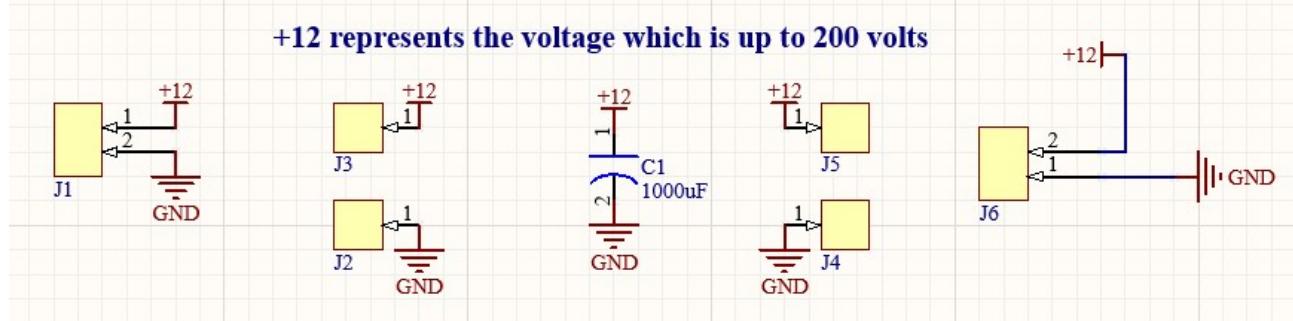
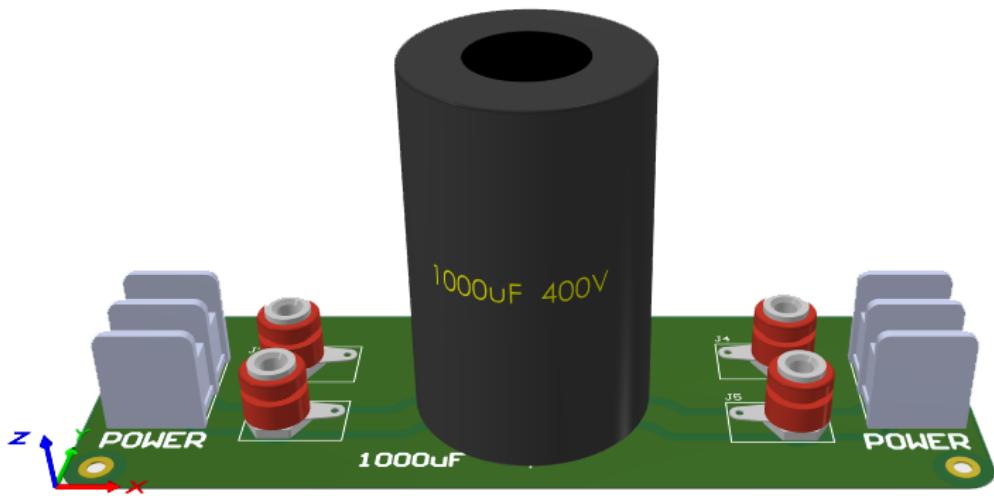
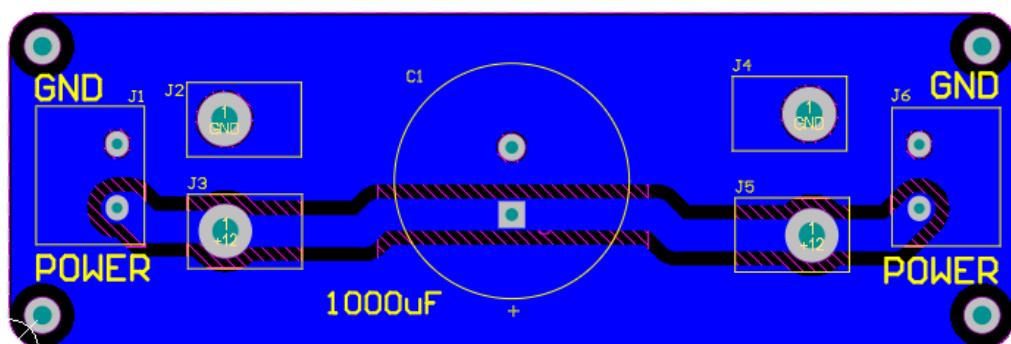


Figure 5.21: The schematic of the DC-link board



(a) DC-link PCB 3D design



(b) DC-link board - bottom layer

Figure 5.22: DC-link hardware board design

5.4.3 Current Sensors

This board is designed for three current sensors. It also has LED indicator to indicate the power connection. It interfaces with the main board to provide current feedback.

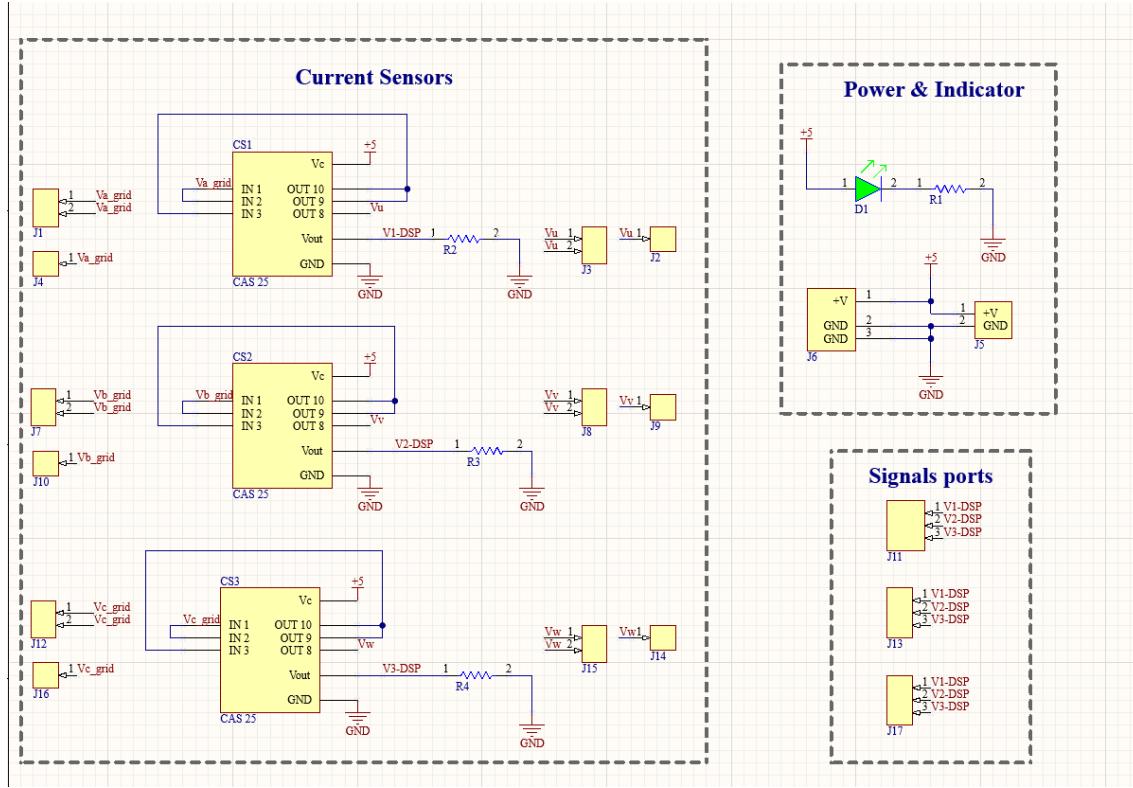


Figure 5.23: The schematic of the current sensors board

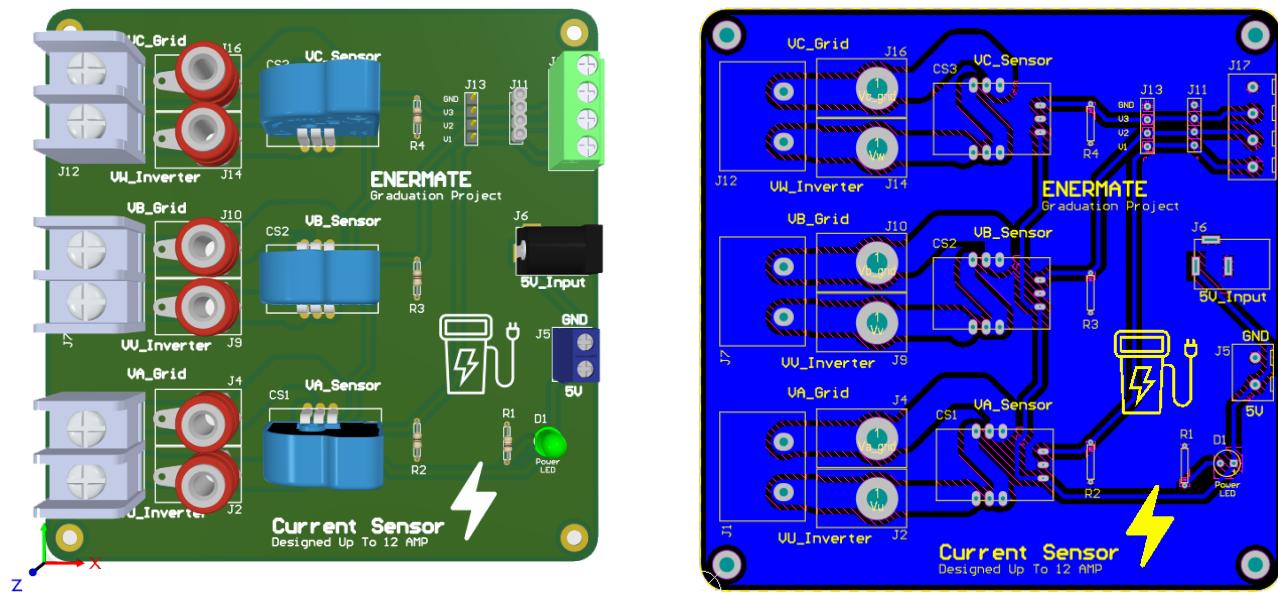


Figure 5.24: Current sensors hardware board design

5.4.4 Voltage Sensors

This board is designed for three voltage sensors, two of them will be used as a feedback of the input line voltage and the last one will be used as a feedback for the output DC voltage. It also has LED indicator to indicate the power connection.

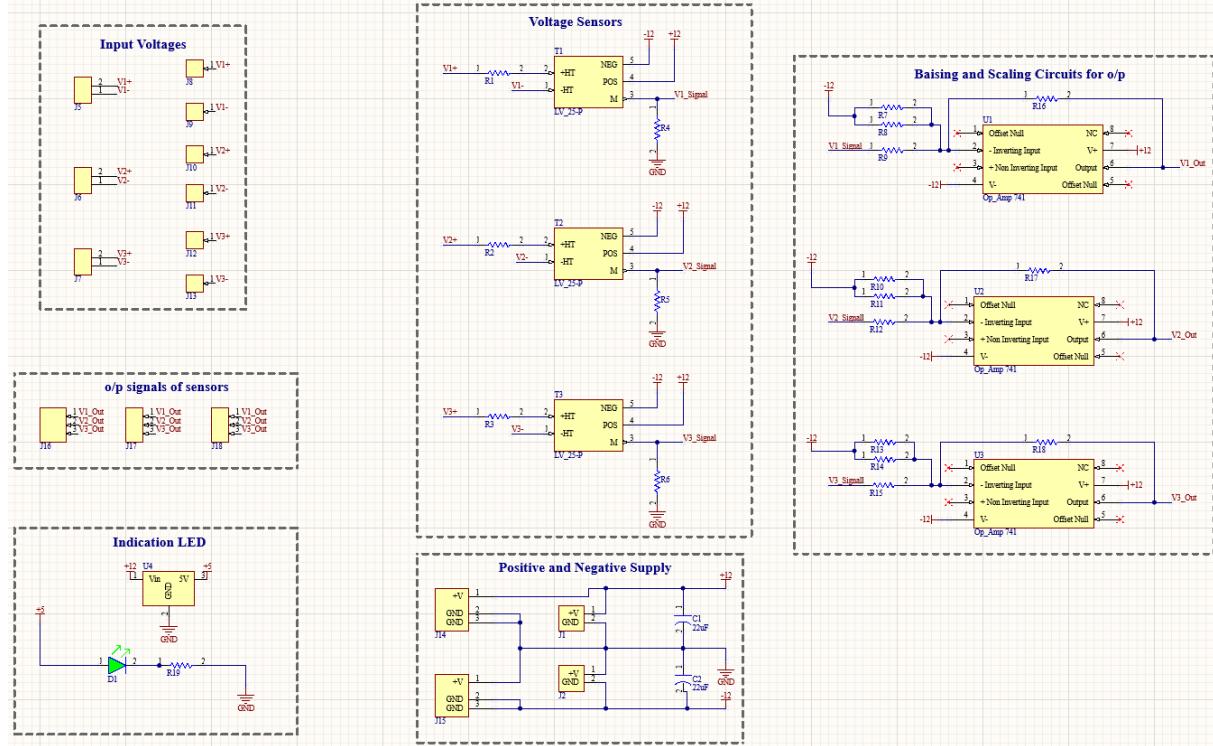


Figure 5.25: The schematic of the voltage sensors board

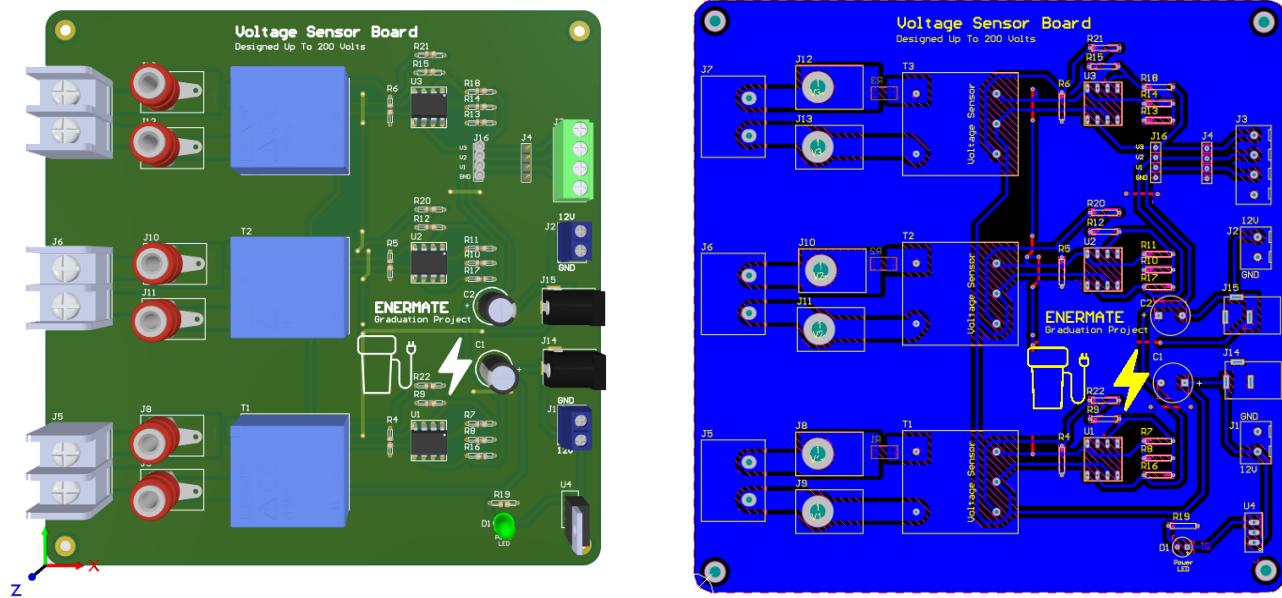


Figure 5.26: Voltage sensors hardware board design

5.4.5 Micro-Controller Interfacing

This board acts as a shield for the DSP. It has several isolation optocouplers to protect the microcontroller from any fault.

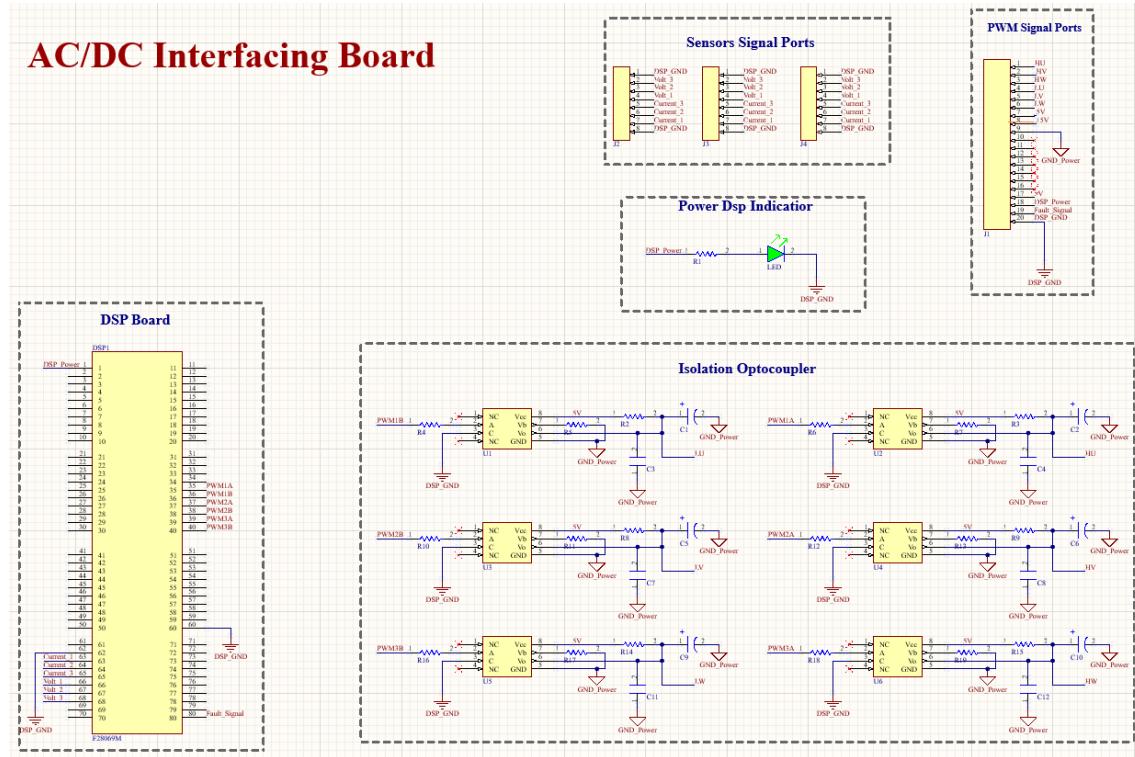


Figure 5.27: The schematic of the DSP interfacing board

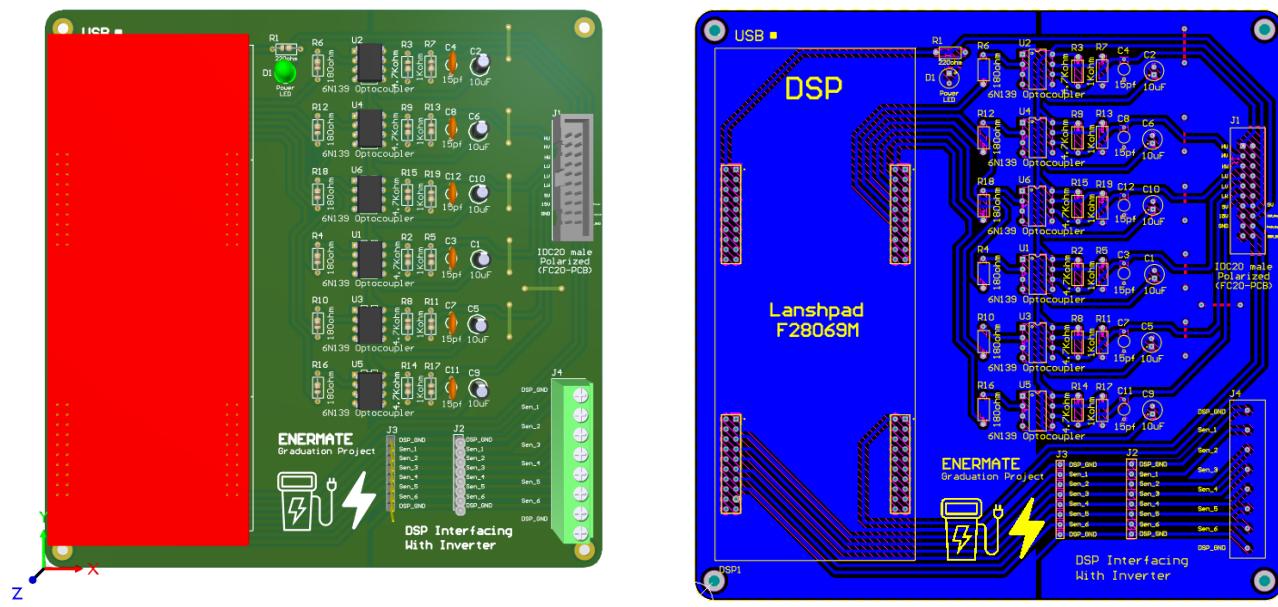


Figure 5.28: DSP interfacing hardware board design

Chapter 6

Hardware Configuration

This chapter includes tests of various components such as voltage sensor, current sensor, etc. Also, it includes the final hardware product and its operation.

6.1 Testing of Voltage Sensor (LV 25-P)

6.1.1 Objective

Evaluate the performance of the voltage sensor, ensuring accurate output and proper biasing within predefined voltage ranges.

6.1.2 Equipment

- Voltage sensor LV 25-P.
- Designed R_{in} , R_m values of the sensor.
- Op-amp circuit with calculated resistor values.
- Single-phase auto-transformer.
- Micro-controller (DSP LaunchPad F28069M).

6.1.3 Procedure

1. Voltage Circuit Setup:

- Connect the voltage circuit with designed R_m value for required output voltage of the transducer. This will regulate the output voltage feeding into the op-amp circuit.
- Design R_{in} for the required ratings of the measured voltage.

2. Op-Amp Biasing Circuit Construction:

- Build the biasing circuit using the op-amp adder configuration with pre-calculated resistor values. This sets the desired output voltage delivered to the DSP (including biasing and gain adjustments for the op-amp input signal).

3. Primary Side Connection:

- Connect the primary side of the sensor to the auto-transformer.

4. Biasing Verification:

- With 0V input, measure the output voltage. This should correspond to the predetermined op-amp biasing value.

5. Output Voltage Verification:

- Apply various input voltage values.
- Compare measured output voltages with pre-calculated values for accuracy.
- Ensure the maximum output voltage never exceeds 3.3V.

6. Sensor Calibration:

- Connect the sensor circuit output (output of op-amp circuit) to the DSP.
- Utilize the DSP's ADC block to convert the analog signal to a digital reading.
- Set the pin name corresponding to the connected output.
- Expect the analog reading to match the digital reading after multiplying by (3.3/4095) (considering 12-bit ADC with reference voltage of 3.3V).
- Account for the biasing value shifting the signal above the x-axis in the analog domain.
- Subtract the measured practical shift from the signal to center it around the x-axis.
- Determine the actual maximum value achieved.
- Apply a gain factor to scale the measured input voltage to match the sensor's expected output range.

6.1.4 Documentation

- Record all measured data (input voltages, output voltages, biasing values).
- Calculate discrepancies between measured and expected values.
- Note any observations regarding sensor behavior or circuit limitations.

6.1.5 Notes

- Exercise caution when handling high voltage. Ensure proper safety procedures are followed.
- Double-check all connections and resistor values before applying power.

6.2 Testing of Current Sensor (LTS 25-P)

Part II

DC/DC Conversion

aw

Chapter 7

Introduction to DC-DC Converters

DC-DC converters are essential components in modern electronic systems, facilitating the efficient conversion of one DC voltage level to another. These converters play a pivotal role in a wide array of applications, ranging from portable electronic devices to large-scale power distribution systems. By altering voltage levels, DC-DC converters enable the optimization of power delivery, enhancing energy efficiency and system performance.

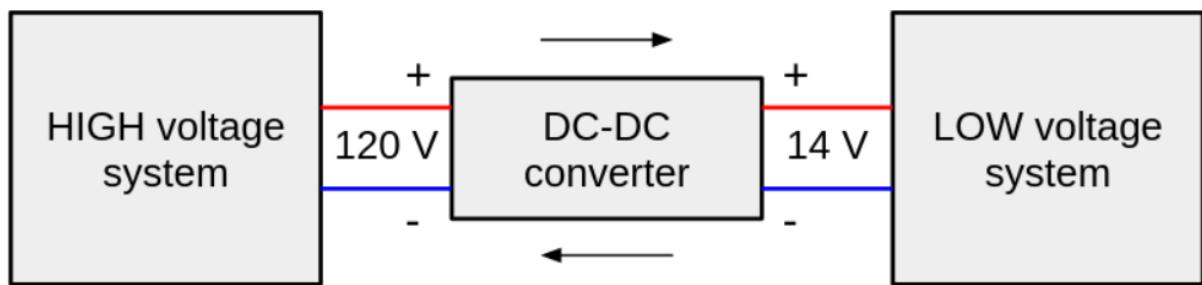


Figure 7.1: DC-DC Conversion from one voltage level to another

Furthermore, DC-DC converters are essential electronic circuits that play a critical role in modern power management systems. Their primary function is to convert the voltage of a direct current (DC) source from one level to another, ensuring stable and efficient power delivery to various electronic devices and systems. In applications where input voltage levels can fluctuate due to factors such as battery discharging over time or changes in load conditions, DC-DC converters maintain a constant output voltage, providing reliable power to the system's components.

One significant advantage of DC-DC converters is their superior power conversion efficiency. By using switching techniques, DC-DC Converters can minimize power losses associated with resistive elements, such as transformers or linear regulators, which typically generate heat and waste energy. This results in better overall efficiency and prolonged battery life in portable devices. Moreover, DC-DC converters offer the flexibility to step up or down voltage levels, allowing for efficient power distribution management in electronic systems. They can also provide galvanic isolation, separating the input and output grounds to reduce the risk of ground loops and safeguard sensitive components from voltage spikes and noise.

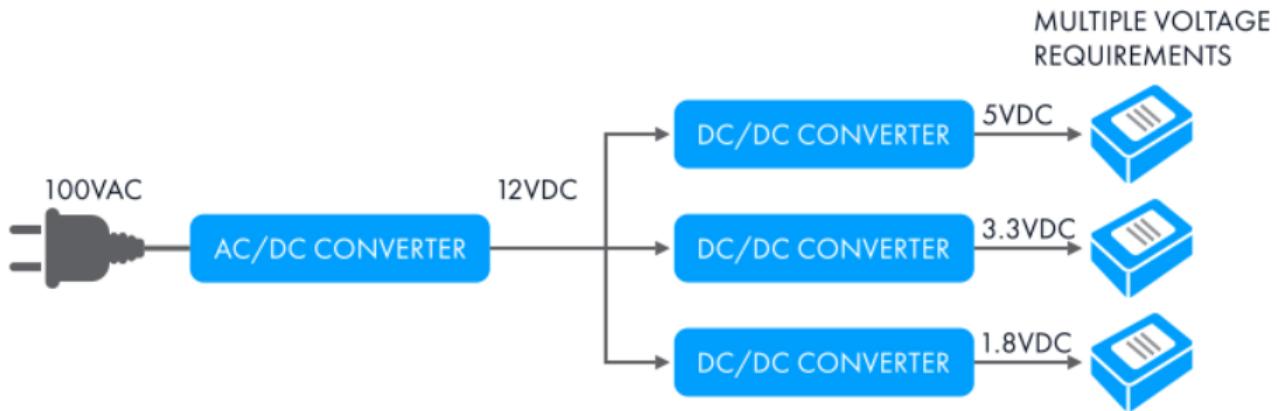


Figure 7.2: DC-DC Converters for Multiple Voltage Requirements

Another noteworthy feature of DC-DC converters is their precise voltage regulation. Some converters can maintain output voltage accuracy within a narrow range, typically with less than a 1 percent deviation. This level of precision is vital for ensuring the proper operation of electronic devices and systems that require stable power supplies.

DC-DC converters come in various topologies and configurations, catering to a broad range of applications and power requirements. They can be designed as standalone devices, integrated into larger power management systems, or embedded into individual components, such as microprocessors or micro-controllers.[11]

7.1 Principle of Operation

The fundamental principle behind DC-DC converters is the conversion of electrical energy from one voltage level to another. This conversion is achieved through the manipulation of electrical components such as semiconductor switches (transistors), inductors, capacitors, and diodes.

DC-DC converters operate on the principle of energy storage and transfer. They utilize switches to control the flow of electrical current through inductive and capacitive elements, thereby altering the voltage levels while maintaining the continuity of power delivery.

The operation of DC-DC converters involves switching cycles where the input voltage is modulated to produce the desired output voltage. Control mechanisms such as pulse-width modulation (PWM), voltage regulation feedback loops, and control algorithms ensure precise voltage regulation and efficient power conversion.

Power supply designers often use isolated DC/DC converters to realize galvanic isolation, meet safety requirements and enhance noise immunity. When designing an isolated DC/DC converter, output voltage regulation accuracy is one of many design objectives to consider and the required level can vary from one application to the next. Better than ± 5 percent overall voltage regulation is adequate in some while ± 10 percent might be necessary for others.

The many power management topologies and regulating schemes for isolated DC/DC converters differ widely in voltage regulation accuracy. For example, the feedback and control of a closed-loop isolated DC/DC converter is shown in Figure 7.3. [12]

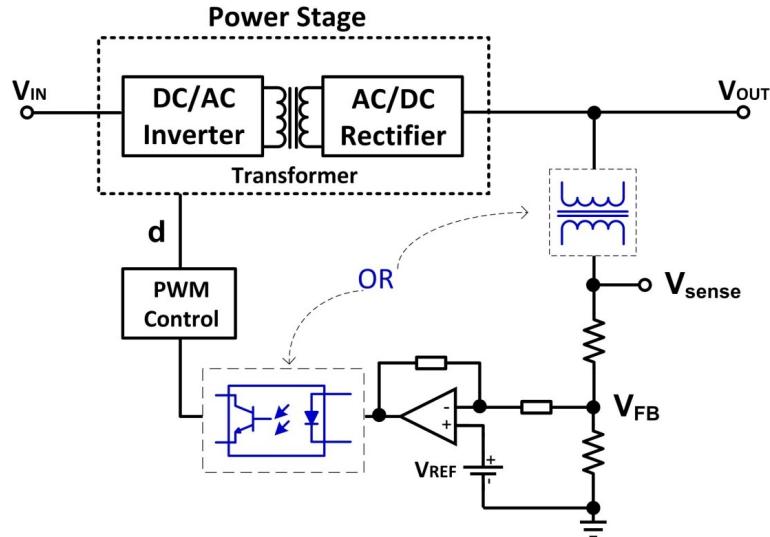


Figure 7.3: Feedback and Control of a Closed-loop Isolated DC/DC Converter

In this example, a transformer is used to electrically isolate the output from the input of the power stage. In a closed-loop isolated DC/DC converter, the feedback circuitry senses the output voltage and generates an error by comparing the sensed voltage with a voltage reference. The error is then used to adjust the control variable, for example duty cycle, to compensate the output deviation. Galvanic isolation between control circuitry on the primary side and secondary side is also essential. Such isolation can be achieved by utilizing either a transformer or an optocoupler. Assuming the reference voltage is precise and stable over temperature changes, regulation accuracy mainly depends on output voltage sensing accuracy. In other words, how well V_{SENSE} resembles V_{OUT} .

7.2 Types of DC-DC Converters

Buck Converter (Step-Down Converter): The buck converter is a widely used DC-DC converter that produces an output voltage lower than the input voltage. It achieves this by intermittently connecting the input voltage source to the output load through a semiconductor switch (usually a MOSFET). The energy stored in the inductor during the ON state of the switch is transferred to the output during the OFF state, resulting in a lower output voltage.[13]

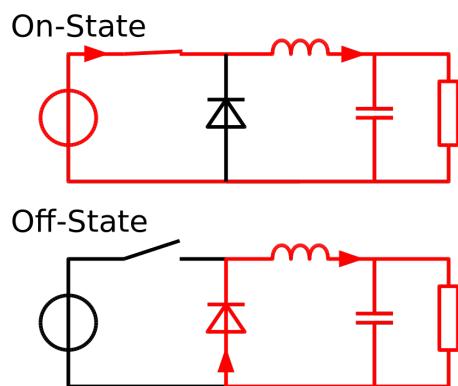


Figure 7.4: ON and OFF States of Buck Converter

Boost Converter (Step-Up Converter): The boost converter increases the output voltage level compared to the input voltage. It operates by storing energy in an inductor while the switch is ON and releasing it to the output during the OFF state. This continuous energy transfer results in an output voltage higher than the input voltage.[14]

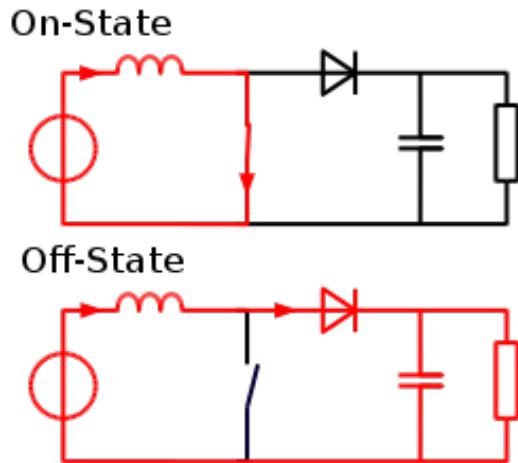


Figure 7.5: ON and OFF States of Boost Converter

Buck-Boost Converter: The buck-boost converter is capable of producing an output voltage either higher or lower than the input voltage. It combines the principles of both buck and boost converters by intelligently controlling the duty cycle of the switch. The buck-boost converter is ideal for applications requiring versatile voltage regulation capabilities.[15]

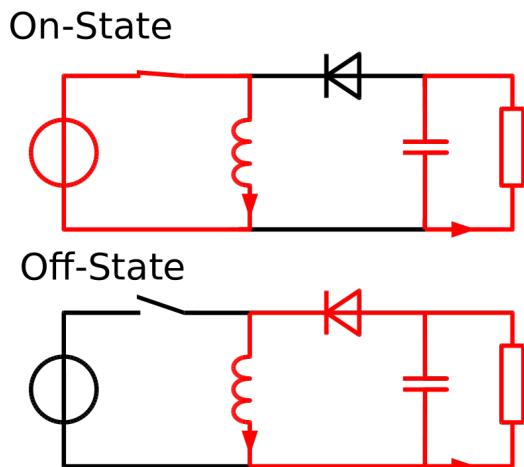


Figure 7.6: ON and OFF States of Buck-Boost Converter

7.3 Applications

There are many DC-DC converters applications across a wide range of industries and systems:

Portable Electronics: Mobile phones, laptops, tablets, and other battery-powered devices rely on DC-DC converters to efficiently manage power consumption and extend battery life.

Renewable Energy Systems: Solar photovoltaic systems and wind turbines employ DC-DC converters to interface with the electrical grid and efficiently convert variable DC voltages into usable power.

Automotive Electronics: Electric vehicles (EVs), hybrid vehicles, and onboard electronics utilize DC-DC converters for voltage regulation, battery charging, and power distribution.

Industrial Automation: Robotics, motor drives, PLCs (Programmable Logic Controllers), and factory automation systems benefit from DC-DC converters for precise voltage regulation and power efficiency.

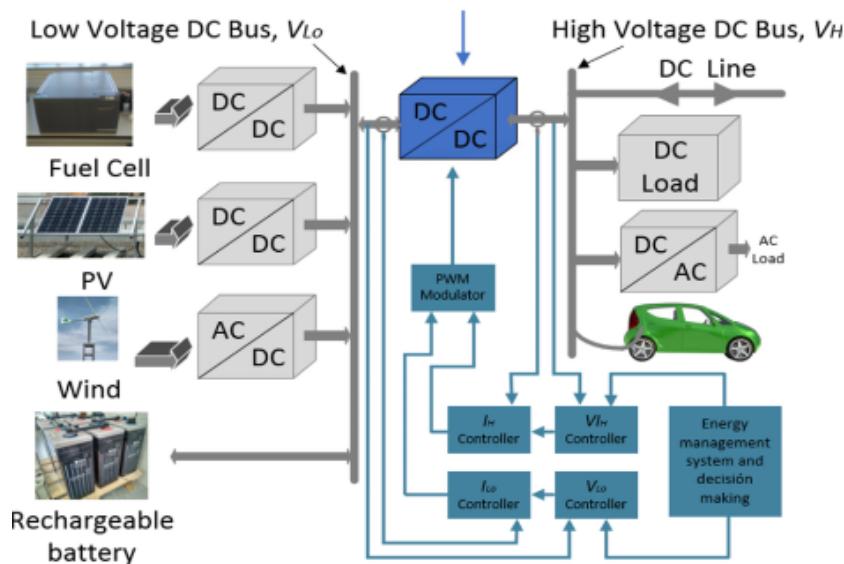


Figure 7.7: Applications of DC-DC Converters

In addition, DC-DC Converters can be used in many other applications like Medical Devices, Smart Lightning and other small-scale electronic appliances.[16]

Chapter 8

Buck Converters

Introduction

The most common non-isolated DC/DC topology is the buck converter. The Buck Converter is used in SMPS circuits where the DC output voltage needs to be lower than the DC input voltage. The DC input can be derived from rectified AC or from any DC supply. It is useful when electrical isolation is not needed between the switching circuit and the output, but when the input is from a rectified AC source, isolation between the AC source and the rectifier could be provided by an isolating transformer.

The evolution of buck converters is illustrated in figure below , starting from the switching mechanism for the loss-free power conversion. The power flow is controlled by timing the connection of “AC” or “BC” through the single-pole-double-throw (SPDT) relay. The voltage signal, V_{sw} , is pulsating due to the on/off switching operation, which is high for the “AC” connection to the source and zero for the “BC” connection to the ground.

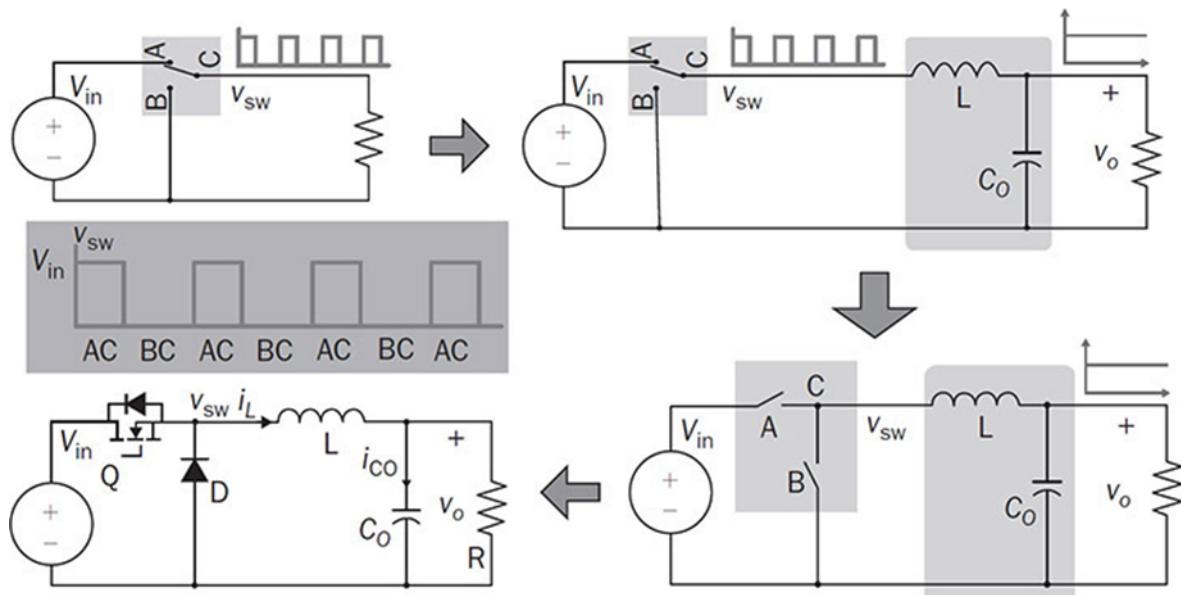


Figure 8.1: Lossless switching concept and evolution of buck converter.

The LC filter is added before the load to mitigate ripples of v_{sw} and realize a smooth voltage crossing the load, v_o . The SPDT switch is replaced by two power semiconductor switches to perform the same switching operation in high frequency. The active switch, Q, is controlled by the applied PWM signal to achieve the required power flow and the desired output voltage, v_o . The freewheeling diode (D) is a passive switch that automatically acts as the “BC” connection and allows the inductor current to continuously flow during the off-state of Q.

Steady-State Analysis

In a steady state, the averaged values of i_L and v_o are constant in each switching cycle over a predefined period. The variation refers to ripples caused by the on/off switching and the interaction with the passive components. The steady-state analysis starts with the conventional buck topology, as shown in Figure 8.2:

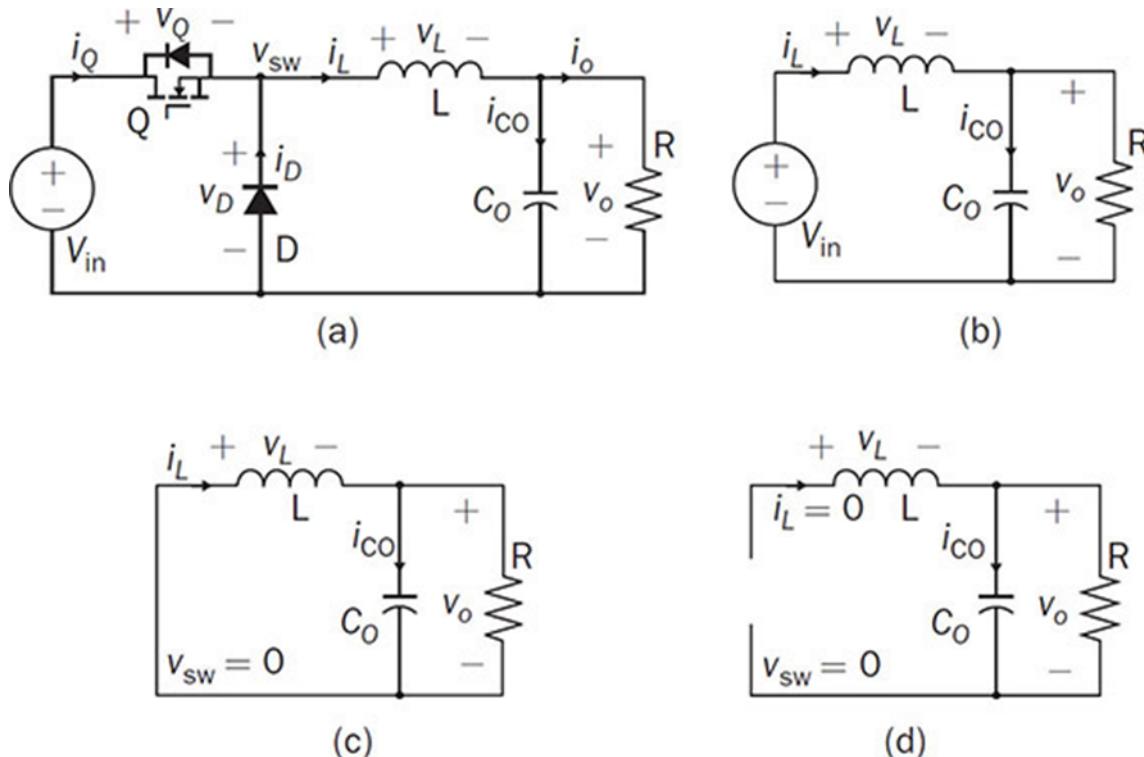


Figure 8.2: Buck converter: (a) circuit; (b) on-state; (c) off-state; (d) zero-state

When the active switch, Q, is turned on for conducting, the voltage at the switching node is connected to the voltage source and causes the flywheel diode reverse-biased due to $v_{sw} = v_i$. The level of the inductor current (i_l) is expected to increase. The moment is indicated as T_{on} or T_{up} , as marked in figure 8.3 and referred to as the “on-state” for the active switch, or “up-state” for the inductor current. When the active switch, Q, is turned off, the inductor current (i_l) forces the diode forward-biased for conducting due to the effect of $v_l = L \frac{di}{dt}$ losing the connection with the voltage source. The level of the inductor current (i_l) is expected to go down due to $v_l = -v_o < 0$ and $\frac{V_l}{L} = \frac{di}{dt}$.

The stored magnetic energy is released to supply the load, R, and maintain the voltage crossing the capacitor, v_o . The period is indicated as T_{off} or T_{down} .

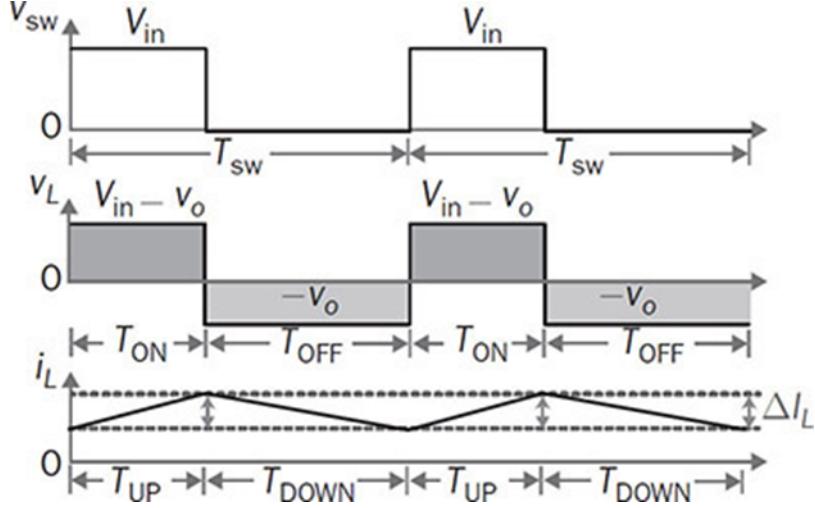


Figure 8.3: Steady-state waveforms in continuous conduction mode (CCM).

According to the steady-state definition, the averaged value of i_L is equal in each switching cycle. The rising amplitude of i_L is equal to the dropping ripple, which is marked as ΔI_L . The value of ΔI_L commonly refers to the peak-to-peak amplitude of the inductor current ripple in steady state. In discrete time, the rising amplitude during the on-state and The dropping amplitude during the off-state expressed by:

$$+\Delta I_L = \frac{V_{in} - v_o}{L} T_{ON}, -\Delta I_L = \frac{-v_o}{L} T_{DOWN} \quad (8.1)$$

Combining the two equations the ripple equivalence of the inductor current leads to the voltage conversion ratio in a steady state for the buck converter:

$$\frac{V_o}{V_{in}} = \frac{T_{on}}{T_{on} + T_{down}} \quad (8.2)$$

8.1 Continuous Conduction Mode

The active switch, Q, is operated for either the on-state or off-state in each switching cycle, and $T_{on} + T_{off} = T_{sw}$, T_{sw} represents the period of one switching cycle related to the switching frequency, F_{sw} .

In continuous conduction mode (CCM), the inductor current is always above and never saturated at zero levels in steady state. The term “continuous conduction mode (CCM)” is used when a diode is used as the low-side switch in the buck converter circuit, Following the waveform of i_L , the up-state and down-state are defined according to the increasing and decreasing i_L , respectively. The periods of up-state and down-state are marked as T_{up} and T_{down} , respectively.

Thus, the CCM can be mathematically expressed by $T_{on} = T_{up}$ and $T_{off} = T_{down}$. The CCM indicates $T_{down} = T_{sw} - T_{on}$. The voltage conversion ratio can be represented by the on-state duty ratio in CCM and becomes:

$$\frac{V_o}{V_{in}} = D_{ON} \quad (8.3)$$

8.2 Discontinuous Conduction Mode

The Discontinuous Conduction Mode (DCM) happens since the diode only allows current to conduct in one direction. In DCM, the inductor current is saturated at zero levels for a certain time during each switching cycle at steady state. In DCM, both switches are off-state for a certain time in each switching cycle. Figure 8.4 illustrates the steady-state waveforms of v_{sw} , v_L , and i_L when the operation enters DCM.

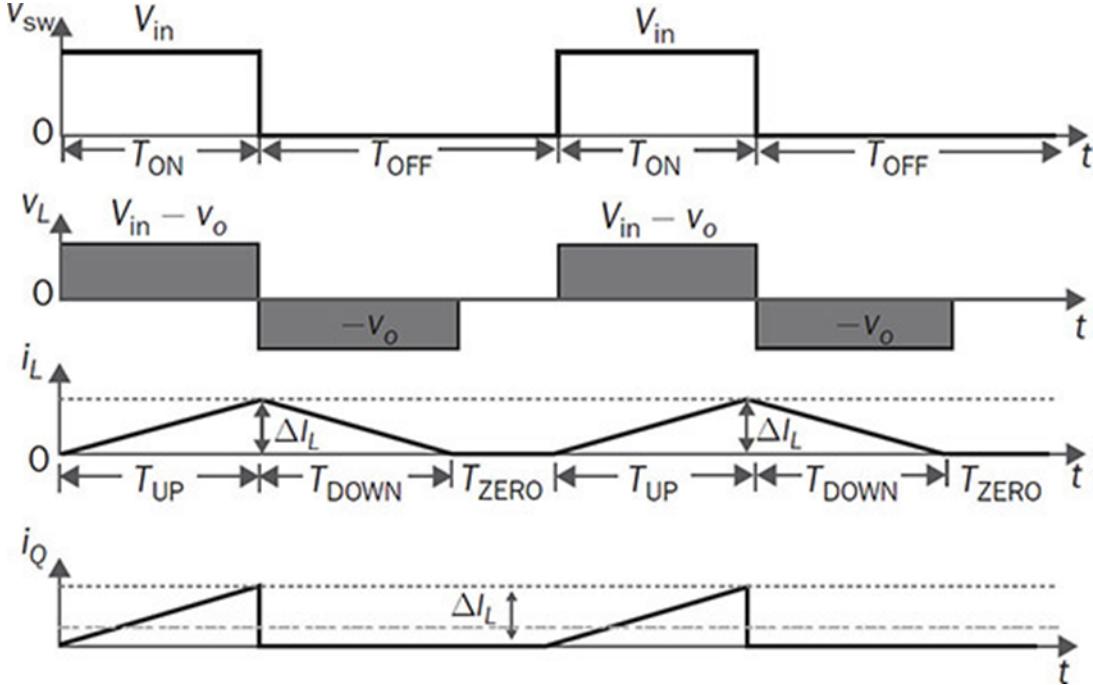


Figure 8.4: Steady-state waveforms in discontinuous conduction mode (DCM)..

Following the waveform of i_L , the “zero-state” is added and indicated by T_{zero} , following the up-state and down-state. During the off-state period, T_{off} , the stored inductor energy is fully released, which results in $i_L = 0$ and $v_L = 0$, and leads to the zero-state, T_{zero} . The diode stops conduction and breaks the connection. Different from the CCM, the mathematical expression becomes: $T_{off} = T_{down} + T_{zero}$ therefore, the conversion ratio cannot follow the same. The on-state duty ratio, D_{ON} , is no longer the direct representative of the voltage conversion ratio in DCM.

The DCM can be mathematically expressed by $AVG(i_L) < \frac{\Delta i_L}{2}$ where $AVG(i_L)$ depends on the load condition in steady state. When loss is ignored, the power balance between the input and output leads to:

$$V_{in} \times AVG(i_Q) = \frac{V^2}{R} \quad (8.4)$$

where $AVG(i_Q)$ is the averaged value of the input current, i_Q . The averaged current can be determined by:

$$AVG(i_Q) = \frac{\Delta i_L * T_{on}}{2T_{sw}} \quad (8.5)$$

At DCM, the initial value of i_Q is zero before the on-state, the peak-to-peak ripple can be determined by:

$$\Delta i_L = \frac{V_{in} - v_o}{L} T_{ON} \quad (8.6)$$

The constraints of the last 3 equations lead to the standard quadratic equation. The averaged value of the output voltage, v_o , can be determined by solving the equation. The parameters include T_{sw} , T_{on} , and the load resistance, R, besides other constants in steady state. The values of T_{sw} and T_{on} are known from the PWM generation. The output voltage is dependent on load condition at DCM, which is different from voltage determination of CCM.

$$(2T_{sw}L) V_O^2 + (V_{in}RT_{ON}^2) V_O + (-V_{in}^2RT_{ON}^2) = 0 \quad (8.7)$$

8.3 Boundary Conduction Mode

Even though CCM is preferred in most cases for high power density of buck converters, DCM happens when the load current is low enough. Load variation generally causes transition between CCM and DCM. The boundary conduction mode (BCM) is a critical condition to divide DCM and CCM. The waveform of BCM is illustrated in Figure 8.5 which is a special case of CCM since the waveform of i_L reaches the zero level without saturation. Therefore, the voltage conversion ratio in steady state is the same as CCM , BCM happens when the load current in a steady state is equal to the critical value expressed by:

$$i_{crit} = \frac{\Delta I_L}{2} \quad (8.8)$$

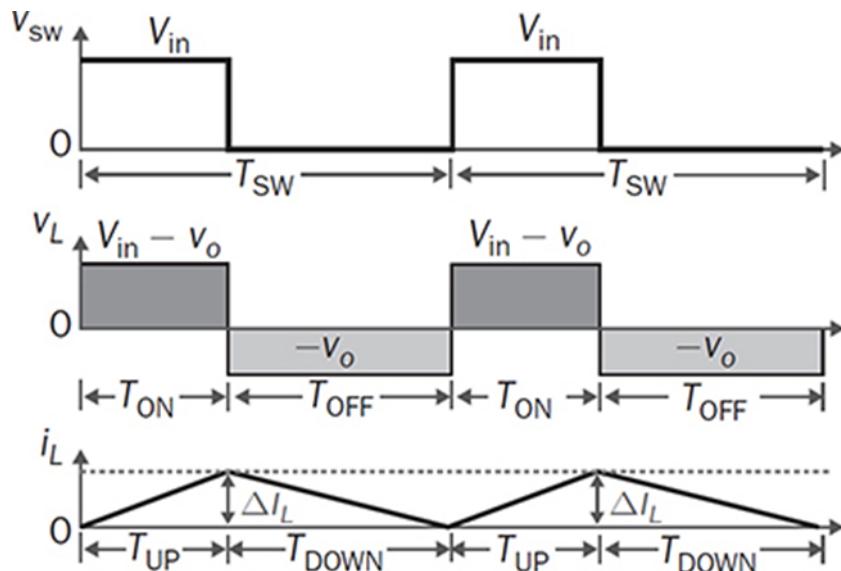


Figure 8.5: Waveform of BCM

When a resistive load is considered, the critical value of the load resistance is computed by $R_{crit} = V_o / I_{crit}$. When the resistive load condition becomes $R > R_{crit}$, the operation enters DCM, where V_o is no longer proportional to the on-state duty ratio, D_{ON} .

8.4 Circuit Design and Calculations

Figure 8.6 shows the basic configuration of a buck converter where the switch is integrated in the selected integrated circuit (IC). Some converters have the diode replaced by a second switch integrated into the converter (synchronous converters). If this is the case, all equations in this document apply besides the power dissipation equation of the diode.

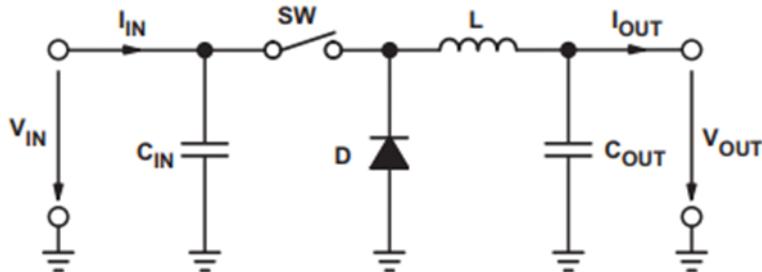


Figure 8.6: Basic configuration of buck converter

- Calculate the Maximum Switch Current The first step to calculate the switch current is to determine the duty cycle, D , for the maximum input voltage. The maximum input voltage is used because this leads to the maximum switch current

$$\text{Maximum Duty Cycle : } D = \frac{V_{\text{OUT}}}{V_{\text{IN(max)}} \times \eta} \quad (8.9)$$

- The next step in calculating the maximum switch current is to determine the inductor ripple current. In the converter's data sheet; normally, a specific inductor or a range of inductors are named for use with the IC. So, use the recommended inductor value to calculate the ripple current, an inductor value in the middle of the recommended range.

$$\text{Inductor Ripple Current : } \Delta L = \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times D}{f_S \times L} \quad (8.10)$$

$$\text{Maximum output current of the selected } I_{\text{maxout}} = I_{\text{min}} - \frac{\Delta I_L}{2}$$

- Inductor Selection Data sheets often give a range of recommended inductor values. If this is the case, choose an inductor from this range. The higher the inductor value, the higher is the maximum output current because of the reduced ripple current. In general, the lower the inductor value, the smaller is the solution size. **Note that** the inductor must always have a higher current rating than the maximum current , this is because the current increases with decreasing inductance.

For parts where no inductor range is given, the following equation is a good estimation for the right inductor:

$$L = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{\Delta I_L \times f_S \times V_{\text{IN}}} \quad (8.11)$$

- Rectifier Diode Selection To reduce losses, use Schottky diodes. The forward current rating needed is equal to the maximum output current:

$$I_F = I_{\text{OUT(max)}} \times (1 - D) \quad (8.12)$$

- Output Capacitor Selection:

To adjust the output capacitor values for a desired output voltage ripple, the following equations can be used:

$$C_{OUT(\min)} = \frac{\Delta L}{8 \times f_S \times \Delta V_{OUT}} \quad (8.13)$$

8.5 Design example and MATLAB Model

Symbol	Description	Value
P_{norm}	Nominal power rating at CCM	5 W
V_{in}	Nominal input voltage	12 V
V_o	Nominal value of output voltage	5 V
f_{sw}	Switching frequency	50 kHz
ΔI_L	Nominal value of peak-to-peak ripple of inductor current	0.2 A
ΔV_o	Nominal peak-to-peak ripple of capacitor voltage	0.05 V

Figure 8.7: Specification of Buck DC/DC Converter

$$\begin{aligned}
 D &= \frac{5}{12 \times 1} = 0.4166 \\
 L &= \frac{5 \times (12 - 5)}{0.2 \times 50k \times 5} = 7e-4 H \\
 C_{OUT(\min)} &= \frac{0.2}{8 \times 50k \times 0.1} = 5e-6 F \\
 I_{crit} &= \frac{\Delta L}{2} = 0.1 A \\
 R_{crit} &= \frac{V_o}{I_{crit}} = 50 \text{ ohm}
 \end{aligned}$$

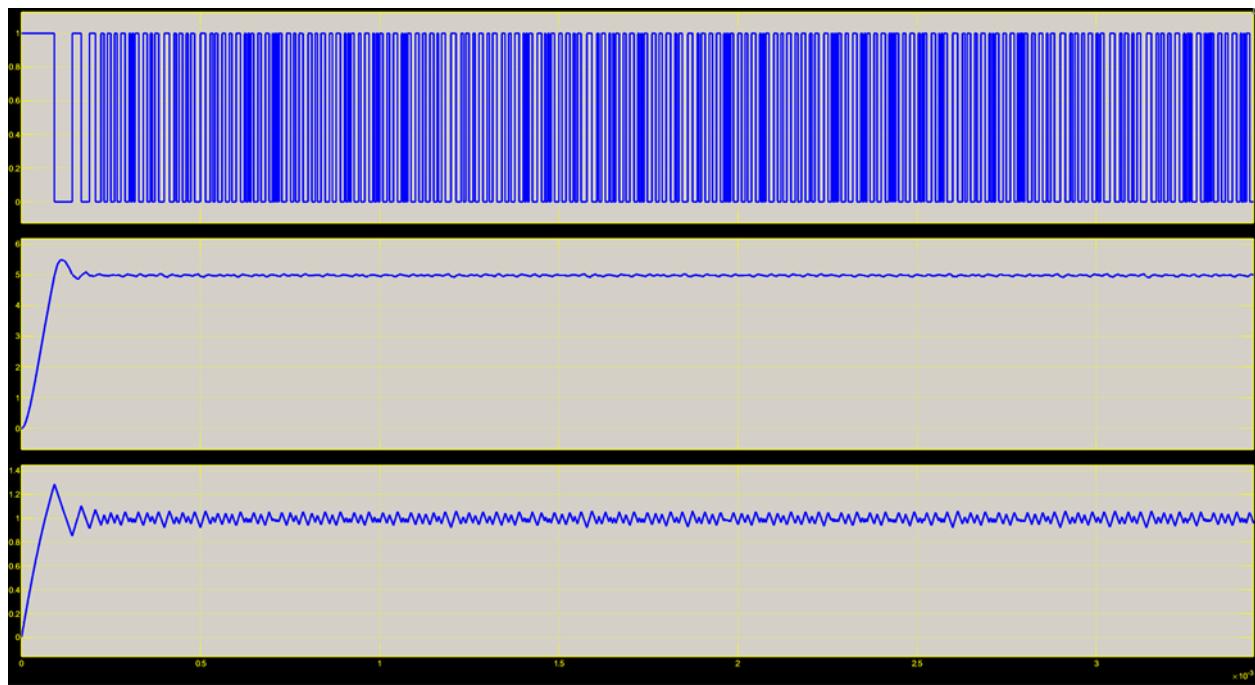


Figure 8.8: Simulation results of the nominal operation ($R = 5 \Omega$).

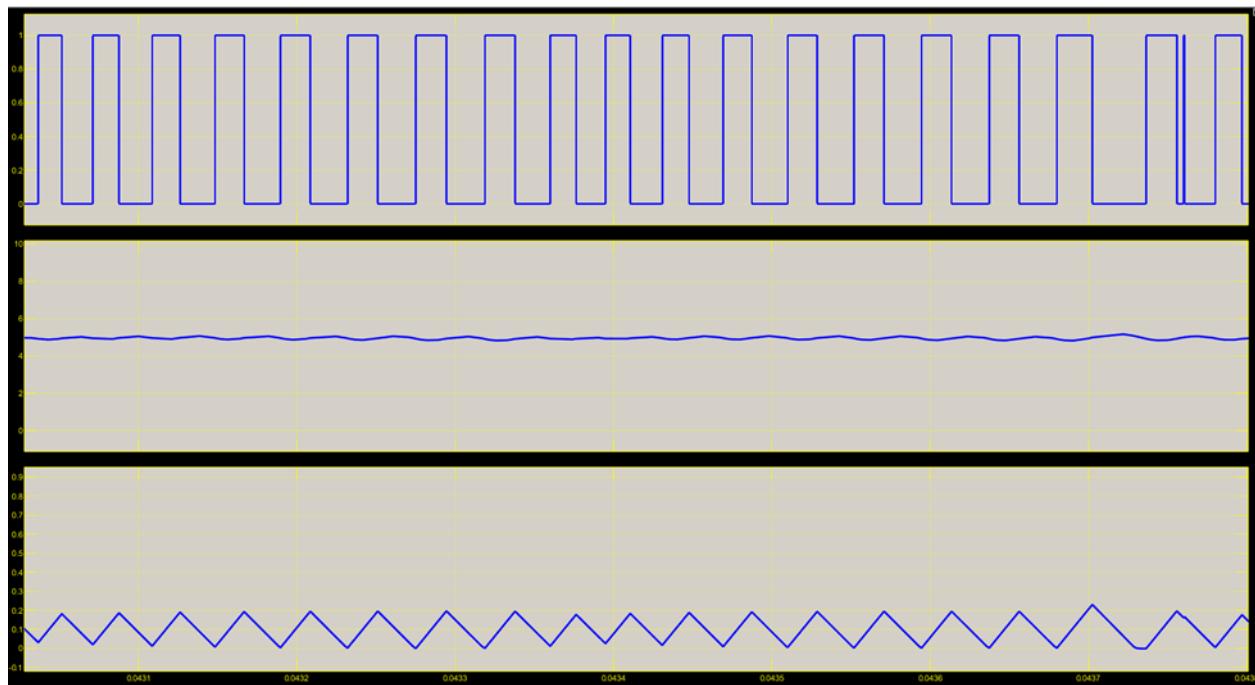


Figure 8.9: Simulation results of the buck converter for BCM ($R = 50 \Omega$).

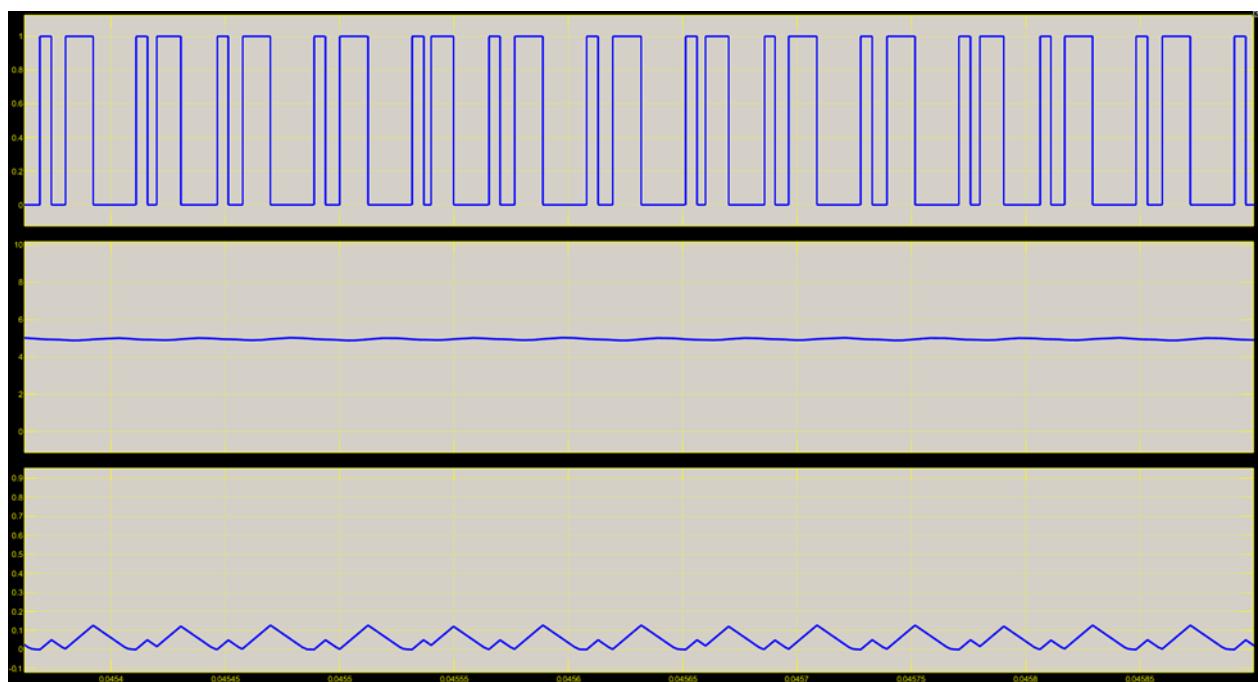


Figure 8.10: Simulation results of the buck converter for DCM ($R = 100 \Omega$).

Chapter 9

Synchronous Buck-Boost Converters

The Synchronous Buck-Boost converters are developed. Unlike the traditional buck-boost converters, the synchronous converter has fast transient response, similar to the behaviour of the buck converter with synchronous rectification. In addition, it has a non-pulsating output current. The synchronous buck-boost converter operates in the Continuous Current Mode (CCM) which, not only reduces the stress on the output capacitor, but also reduces the ripple of the output voltage. Simulation results are provided to demonstrate the effectiveness of the proposed control system.[17]

9.1 Introduction

In many applications such as portable devices, electronic devices in cars, etc., where the output voltage range of the battery is considerably large, buck-boost converters are required. There are numerous types of buck-boost converters such as the non-isolated Cuk converter , the SEPIC converter , the Zeta converter and the Sheppard-Taylor topologies . However, corresponding feedback regulators that would ensure fast close-loop transients as well as high stability are difficult to design. In addition to that, each of these topologies requires two inductors instead of one, increasing thus the cost and bulkiness of the system. Also, their small signal model is a fourth order one, making the control design more difficult and complex. In comparison with these converters mentioned previously, the proposed 2D KY converter has an ultra-fast transient response, similar to the behaviour of the buck converter. Moreover, this converter operates in continuous current mode (CCM) which reduces the stress on the output capacitor and decreases the output ripple. In this paper, the detailed operation of the synchronous buckboost converter is first illustrated, and then a mathematical representation of the converter is developed both in the state-space and the frequency domain. Based on the proposed model, a linear feedback voltage regulator is designed to ensure high transient performance. Simulation results are finally presented to demonstrate the effectiveness of the control system.[17]

9.2 Synchronous Buck-Boost Converter

Fig. 9.1 shows the synchronous buck-boost converters topology. It consists of four power MOSFETs Q1, Q2, Q3 and Q4 with anti parallel diodes. It consists also of a diode D, an output inductor L, an output capacitor C0 and an energy transfer capacitor C which is large enough to maintain a constant voltage across itself, which is equal to the input voltage. Here the output of the converter is controlled

by the PIPWM because of this controller is high accuracy and more reliable compare with other converter.[17]

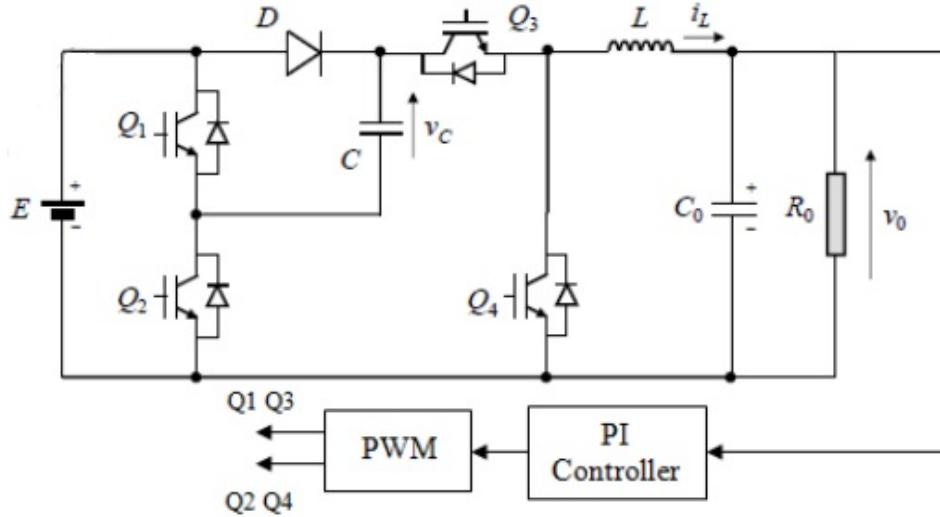


Figure 9.1: Synchronous buck-boost topology with its voltage control circuit

9.3 Principle Of Operation

The converter generates an output voltage v_0 across the load represented by R_0 from an assumed ideal voltage source E . The current flowing through the inductor L is designated by i_L . The pair of switches (Q_1 , Q_3) has a same control signal characterized by a duty cycle d and a switching period T . Similarly, the pair (Q_2 , Q_4) is controlled synchronously. In the Continuous Current Mode (CCM) operation, the converter has the two successive configurations: State 1: $0 < t < dT$. The pair (Q_1 , Q_3) are turned ON and (Q_2 , Q_4) are turned OFF, as illustrated in Figure 9.2. The diode D is not conducting and the intermediate capacitor C is discharging.[17]

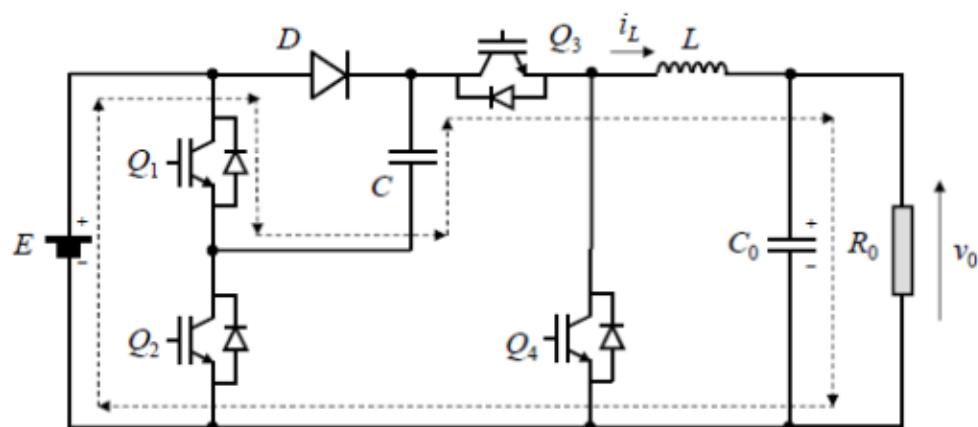


Figure 9.2: Current path in state 1 configuration

In this case, the voltage across L is equal to the input voltage ($E+vc-v_0$), which causes the magnetization of the inductor. The state equations for this configuration are as follows:

$$L \frac{di_L}{dt} = E + V_c - V_o \quad (9.1)$$

$$C_o \frac{dV_o}{dt} = i_L - \frac{V_o}{R_o} \quad (9.2)$$

State 2: $dT < t < T$. The pair (Q2, Q4) are now turned ON and (Q1, Q3) are turned OFF, as depicted in Figure 9.3. The diode D conducts the source current and allows, thus, the instantaneous charging of capacitor C. During this interval, the voltage across C is constantly equal to E, and the voltage across inductor L is equal to ($-v_0$) causing the demagnetization of L. The resulting state equations are as follows:

$$L \frac{di_L}{dt} = -V_o \quad (9.3)$$

$$C_o \frac{dV_o}{dt} = i_L - \frac{V_o}{R_o} \quad (9.4)$$

$$V_c = E \quad (9.5)$$

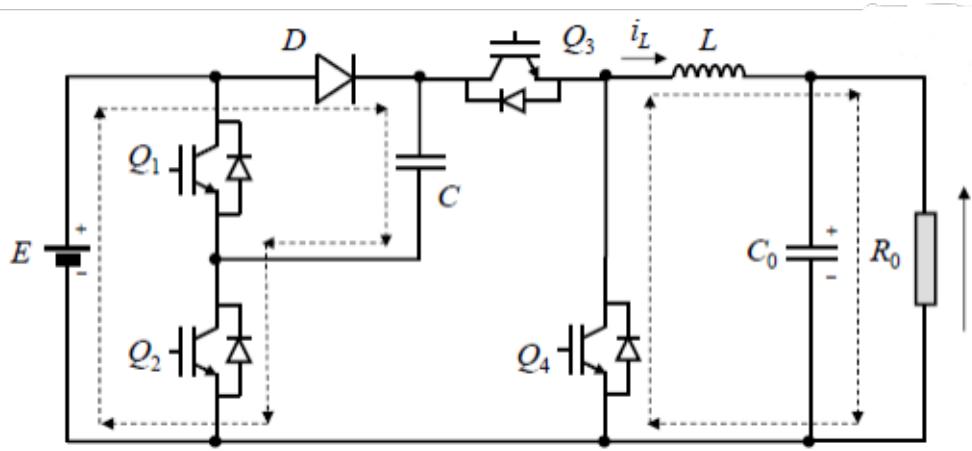


Figure 9.3: Current path in state 2 configurations

By neglecting the switching ripple in the inductor current and the capacitors voltages, we get in the steady state:

$$v_C \cong VC = E \quad (9.6)$$

$$\frac{V_o}{E} = 2D \quad (9.7)$$

$$I_L = \frac{V_o}{R_o} \quad (9.8)$$

Where D, I_L , V_o and V_c are respectively the static values of the duty cycle, the inductor current, the output voltage and the voltage across the intermediate capacitor. In addition, since the duty cycle range is between 0 and 1, the output voltage can increase from 0 to twice the input voltage, which makes this topology pertain to the buck-boost family of converters.[17]

9.4 Design Considerations

The value of the inductor L should be high enough to limit at an acceptable value the switching frequency ripple in the current I_L . It yields:

$$L > L_{min} = \frac{V_o(1 - D)}{F_s \Delta i_{L,max}} \quad (9.9)$$

Where $f_s = \frac{1}{T}$ is the switching frequency, and $\Delta i_{L,max}$ denotes the admissible value of the current ripple. Similarly, the output capacitor C_o should limit the voltage ripple across it and, therefore, should be chosen as follows:

$$C_o > C_{o,min} = \frac{V_o(1 - D)}{4L_s F_s^2 \Delta V_{o,max}} \quad (9.10)$$

Where $\Delta V_{o,max}$ represents the admissible value of the output voltage ripple.[17]

9.5 Averaged Model Of The Synchronous Converter

The converter must be associated to an adequately designed control circuit to maintain a constant output voltage. Any change in the input voltage and/or the load current can cause in open-loop an output voltage different from that desired.

For that, a feedback control law is necessary to compensate the voltage gap and bring quickly the output voltage to the desired level. Modeling plays a key role in revealing the dynamic behavior of the converter and provides a basis in designing the control system.

The adopted modeling approach is known as the state-space average modeling technique. It is based on:

- The formulation of state-space equations for each configuration in a switching cycle.
- Averaging these equations in order to obtain a single state space model.
- If they obtained model is nonlinear, the application of a small-signal linearization around a static point, that yields the computation of the transfer functions on the basis of which the linear voltage regulator would be finally designed.

Referring to section III, the converter presents in the CCM operation two configurations in a switching cycle T. The elementary state models corresponding to each configuration are given respectively by equations of state (1) and (2).

Combining these two elementary mathematical representations of the converter within a whole switching period leads to the following averaged state-model:

$$\begin{cases} L \frac{di_L}{dt} = 2dE - V_o \\ C_o \frac{dV_o}{dt} = i_L - \frac{V_o}{R_o} \end{cases} \quad (9.11)$$

Model (9.11) is purely linear and the required transfer functions can be obtained naturally without the necessity of applying the small-signal linearization process as it is the case for most of the DC-DC converters. The performance of the linear regulator that will be developed later would thus be unaffected by a variation of the setup point within the whole range of operation.[17]

Applying the Laplace transform to model (9.11) yields the following duty-cycle-to-input current and duty-cycle-to-output voltage transfer functions:

$$G_{i_L,d}(s) = \frac{2E}{L} * \frac{s + \frac{1}{R_o C_O}}{s^2 + \frac{s}{R_o C_O} + \frac{1}{L C_O}} \quad (9.12)$$

$$G_{V_o,d}(s) = \frac{2E}{L C_O} * \frac{1}{s^2 + \frac{s}{R_o C_O} + \frac{1}{L C_O}} \quad (9.13)$$

9.6 PIPWM Control Design

The aim of the feedback control circuit is to regulate the output voltage V_o . This voltage is compared with the reference value V_0 , and the resulting error is feed to PI controller output of the PI signal compared to a sawtooth signal using a comparator, as illustrated in Figure 9.4.

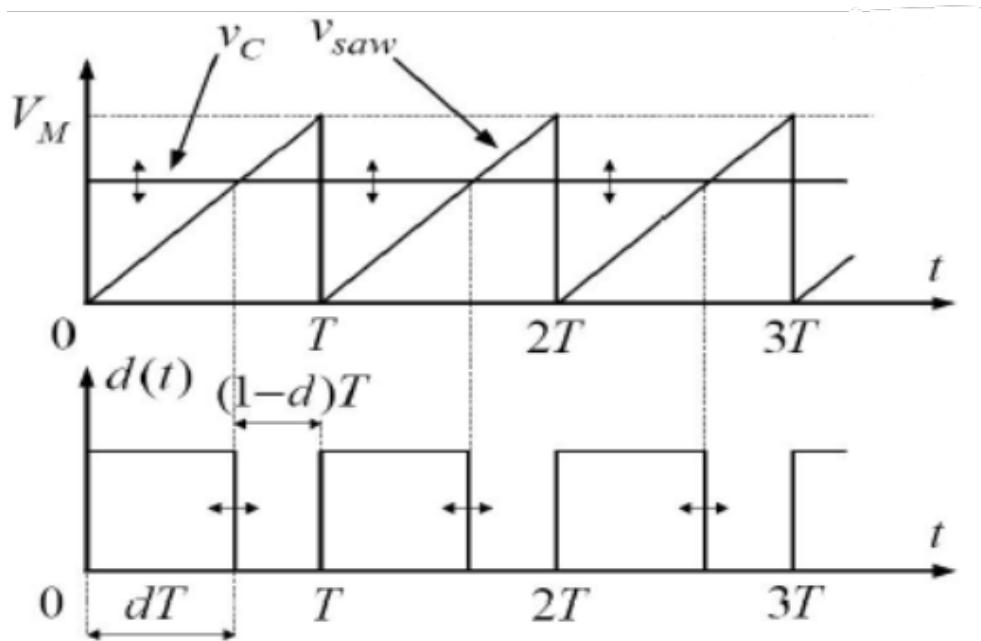


Figure 9.4: Generation of the switches gate signals

This energy harvesting application note describes a simple implementation of a discrete Proportional Integral (PI) controller. When working with applications where control of the system output due to changes in the reference value or state is needed, implementation of a control algorithm may be necessary. Examples of such applications are motor control, control of temperature, pressure, flow rate, speed, force or other variables. The PI controller can be used to control any measurable variable, as long as this variable can be affected by manipulating some other process variables. Many control solutions have been used over the time, but the PI controller has become the industry standard due to its simplicity and good performance.

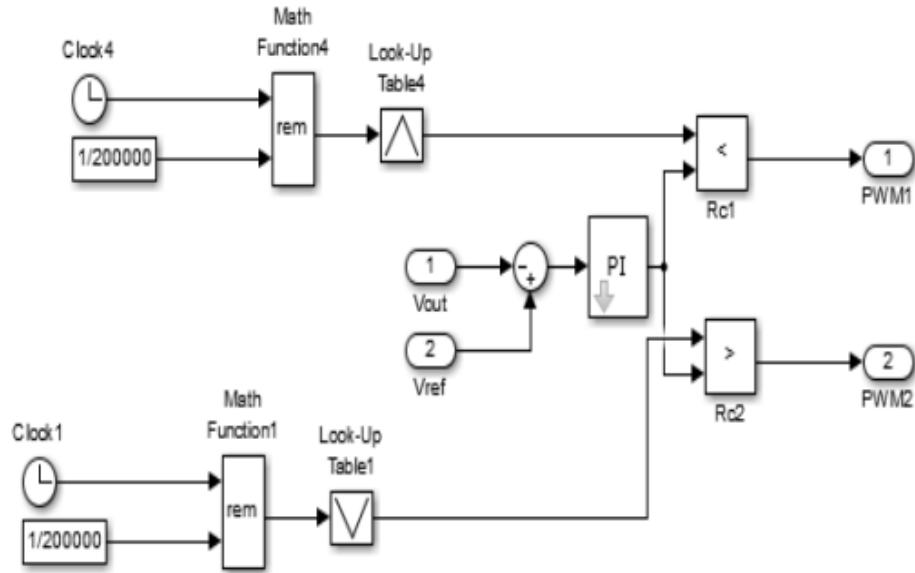


Figure 9.5: Simulink PI-PWM gate signals for switches

In Figure 9.5, a schematic of a system with a PI controller is shown. The PI controller compares the measured process value V with a reference set point value, V_0 . The difference or error, e , is then processed to calculate a new process input, u . This input will try to adjust the measured process value back to the desired setpoint.

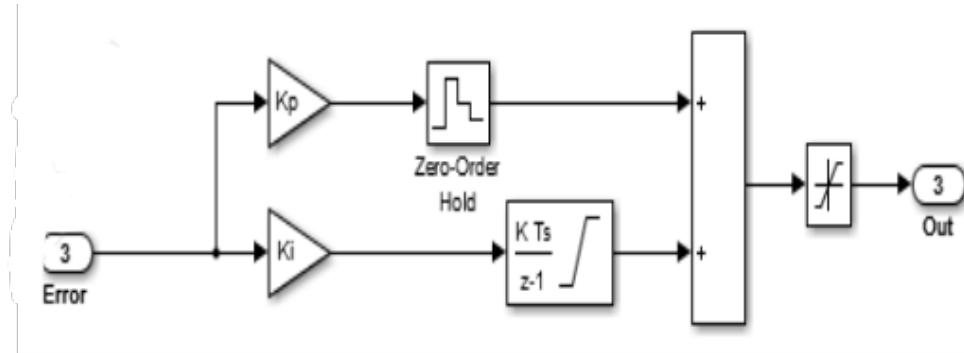


Figure 9.6: Discrete PI Controller

The alternative to a closed loop control scheme such as the PI controller is an open loop controller. Open loop control (no feedback) is in many cases not satisfactory, and is often impossible due to the system properties. By adding feedback from the system output, performance can be improved. Figure 9.6 shows the discrete PI controller.[17]

9.7 Simulation Results

The converter of Figure 9.1 and its control circuit were implemented numerically using the SimPower Blockset of the Matlab/Simulink tool. The adopted parameters and operating conditions are the following:

- The rated input voltage E is 9 to 16V.
- The rated output voltage V₀ is set to 12V.
- The rated output current is equal to 4A, which corresponds to R₀ = 3 ohms.
- The switching frequency f_S is 200kHz.
- The rise time t_m is set to 0.1s.
- L = 14 MicroHenry, C = 470 MicroFarad and C₀ = 470 MicroFarad.

The waveforms of the current in the input inductor and the voltage across the output capacitor at rated operating conditions are represented in Figure 9.5. In addition, in order to test the dynamics of the control system, an input voltage disturbance, a load variation and set point offset have been applied successively. The system's responses are given respectively in Figures from 9.7 to 9.11b. The Figures 9.11a shows zoomed portion of the inductor current, when system start bucking condition in this waveform duty cycle D less the 1-D and Figure 9.11b shows zoomed portion of the inductor current, when system start boosting condition in this waveform duty cycle D is grater then 1-D.[17]

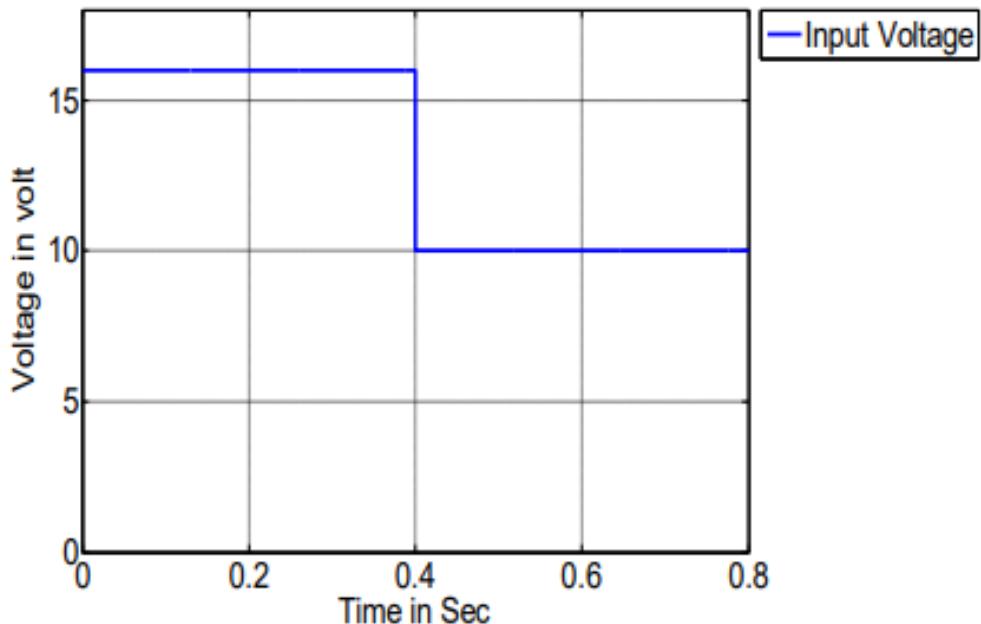


Figure 9.7: Waveform of the Input Voltage Decreased from 16V to 10V

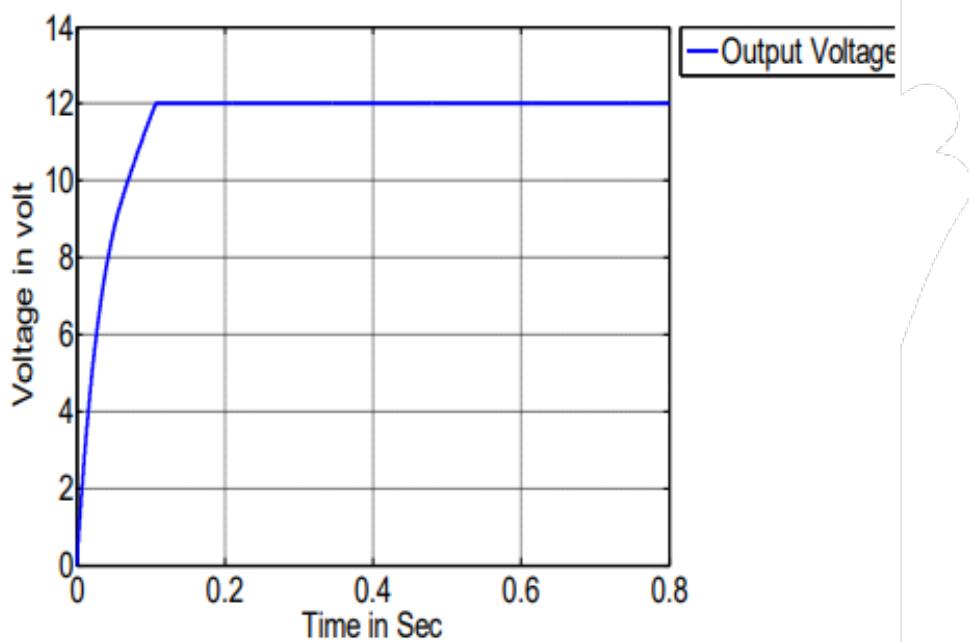


Figure 9.8: Waveform of the Output Voltage ie 12vots

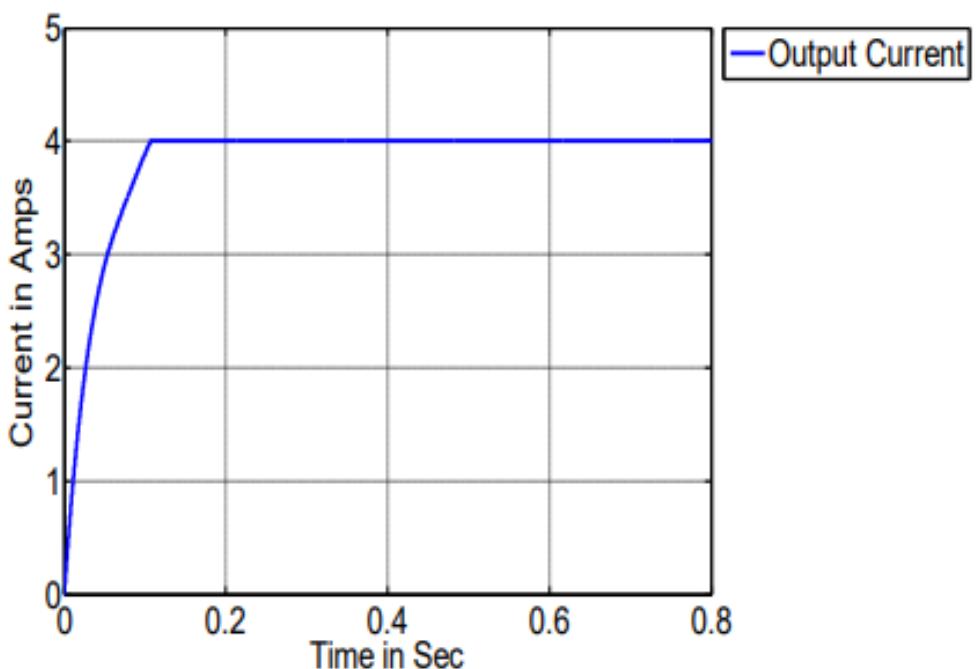


Figure 9.9: System Response of Output Current

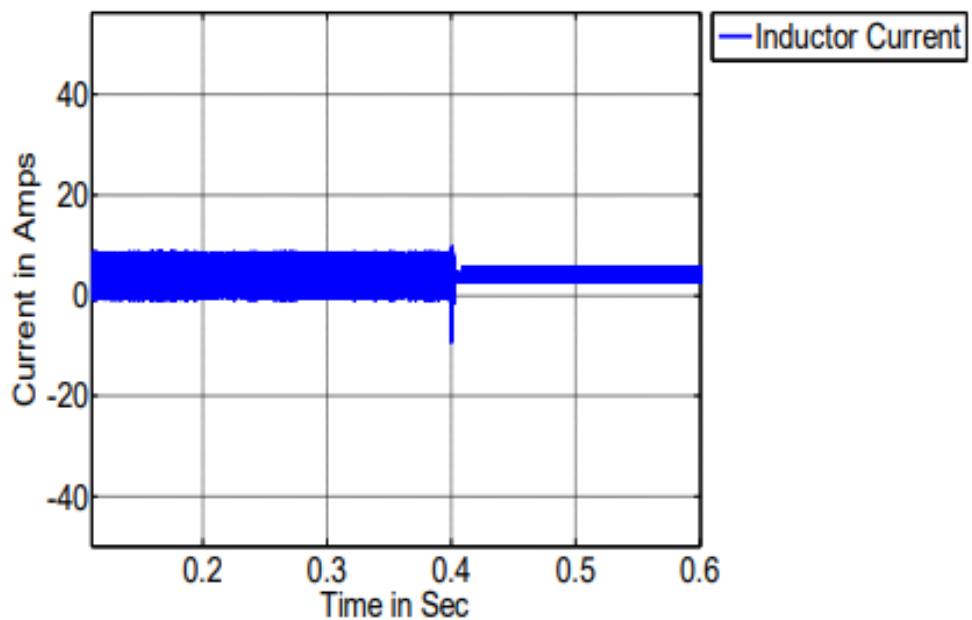


Figure 9.10: System Response of Inductor Current

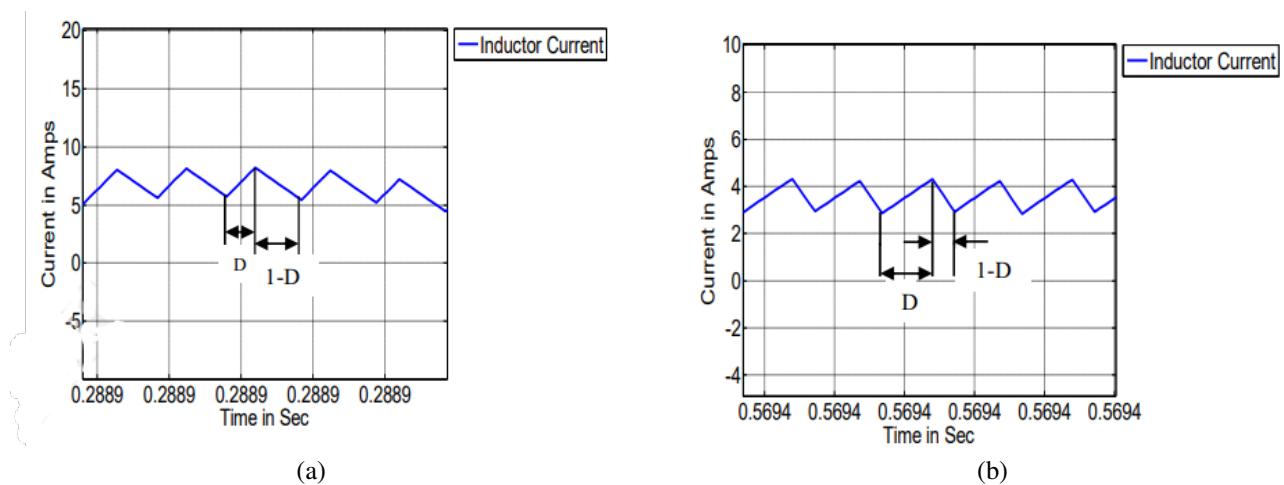


Figure 9.11: Waveforms for Inductor Current

Chapter 10

Dual Active Bridge

The increase demand of an intermediate storage of electrical energy in battery systems, in particular due to the use of renewable energy, has resulted in the need of bidirectional DC/DC power converters with galvanic isolation. Uninterruptible Power Supplies (UPS), battery charging systems, photovoltaic equipment and auxiliary power supplies in traction applications are examples of some fields of application of this kind of converters.

A Dual Active Bridge (DAB) bidirectional DC/DC converter is a topology with the advantages of decreased number of devices, soft-switching commutations, low cost, and high efficiency. The use of this topology is proposed for applications where the power density, cost, weight, and reliability are critical factors. In the chapter the steady-state analysis of the converter has been carried out, giving some guidelines for the design (considering soft switching limits and the amount of reactive current) and a small-signal model of the topology. Simulations and experimental results are also presented.

10.1 Introduction

Global climate change and depleting fossil fuel reserves are driving society's quest for a sustainable energy infrastructure. The incorporation of renewable energy is limited in many ways due to the variable and intermittent nature of its output. Hence, energy storage systems have to be used to compensate the source variations. A bidirectional converter, usually with galvanic isolation, is generally needed to control the power flow between the energy storage and the load. The Dual Active Bridge (DAB, see Figure 7.1), is a bidirectional DC/DC converter based on two active bridges interfaced through a high-frequency transformer (with a great influence of its leakage inductance) enabling power flow in both directions in case of active load.

Each bridge is controlled with constant duty cycle (50%) to generate a high-frequency square-wave voltage at its transformer terminals ($\pm v_i, \pm v_o$). Considering the presence of the leakage inductance of the transformer, with a controlled and known value, the two square waves can be appropriately phase shifted to control the power flow from one dc-source to the other, so bidirectional power transfer can be achieved. Power is delivered from the bridge which generates the leading square wave.

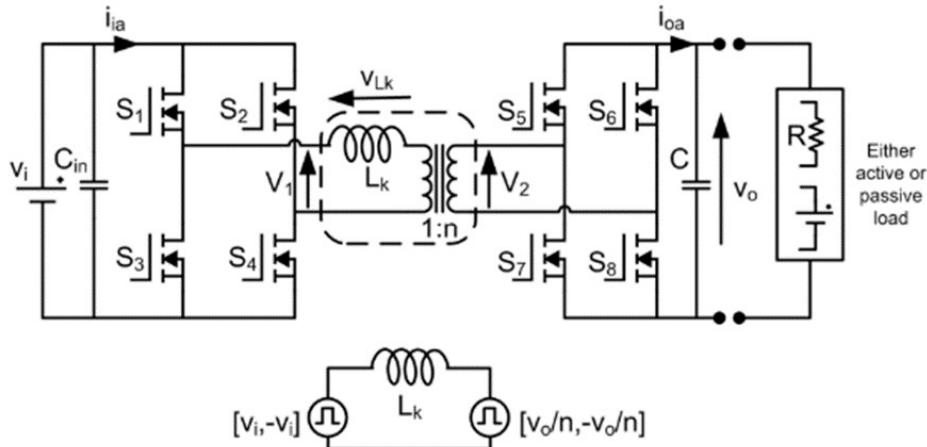
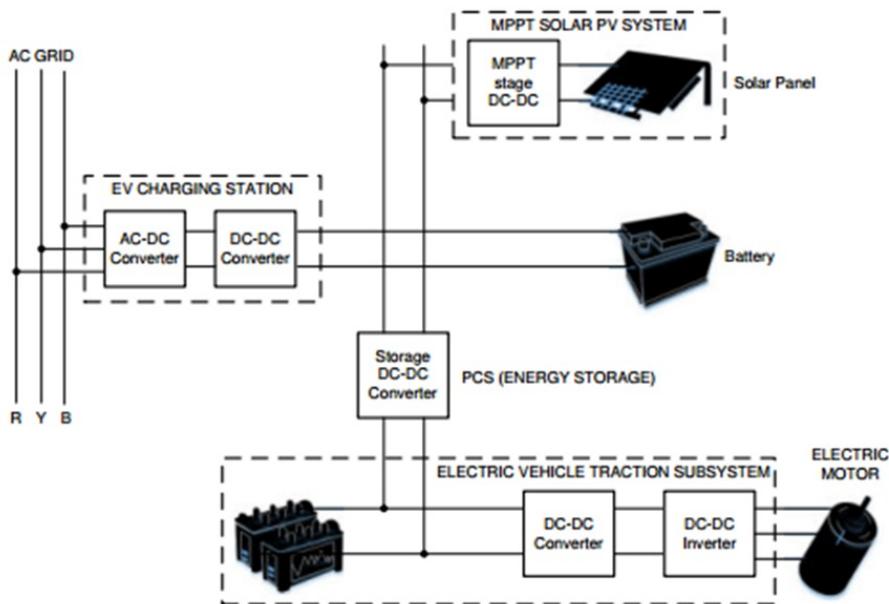


Figure 10.1: Circuit schematic of a DAB converter

10.2 System Description

The DC/DC converter in a charging station must be capable of interfacing with the rectified bus voltage from a three-phase Vienna rectifier at its input and connect with the battery of an electric vehicle at its output, delivering rated power. The DC/DC converter finds important application in a number of end equipment.

The DC/DC converter must be capable of handling high power levels. In addition to this, the converter must be modular, which enables single power stage converter units to be paralleled, whereby the output power throughput can be scaled to higher levels as required by DC charging station standards. Current trends in the charging station are moving toward converters that can handle bidirectional power flow.



New practices, such as Vehicle-to-Grid (V2G), involve power transfer between the battery of an electric vehicle and the AC grid. Bidirectional DC/DC converters enable charging of the battery in the forward mode of operation and facilitate flow of power back to the grid from the battery during reverse mode of operation, which can be used to stabilize the grid during peak load periods.

Power density and system efficiency are two important requirements of a converter in a DC charging station. Operating at high switching frequencies enables reduced size of magnetics. By moving to higher bus voltage to facilitate fast charging, more power can be transferred at the same current level. This helps to reduce the amount of copper, thereby improving power density of the converter. The converter must also be highly efficient as it results in significant cost savings and reduced thermal solution. This reduced thermal solution directly translates into reduced and compact heat sink size, which in turn increases the power density of the converter.

The converter must also be capable of inherent soft switching like ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) without the addition any bulky passive components which might hamper power density.

10.3 Design

Power transfer between the two bridges in a dual-active bridge is analogous to the power flow between two voltage buses in a power system. Consider two voltage sources connected by a line reactance.

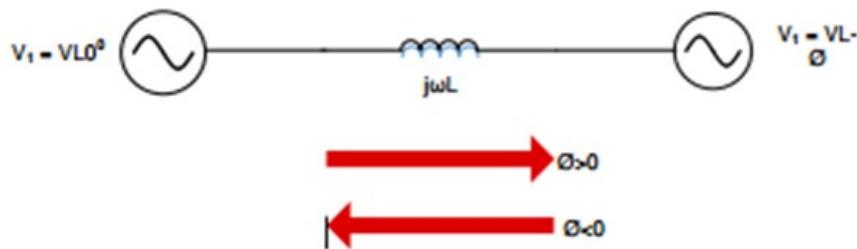
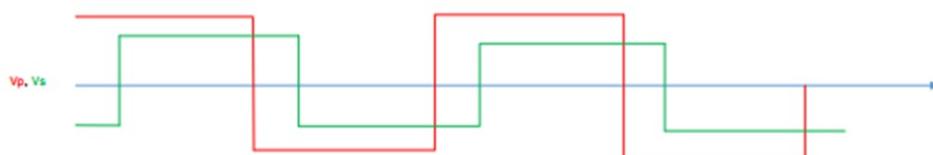


Figure 10.2: Power Transfer Between Voltage Bus

$$P = \frac{V_1 V_2 \sin(\Phi)}{wL} \quad (10.1)$$

Similarly, power transfer happens in a dual-active bridge where two high-frequency square waves are created in the primary and secondary side of the transformer by the switching action of MOSFETs. These high-frequency square waves are phase shifted with respect to each other. Power transfer takes place from the leading bridge to the lagging bridge, and this power flow direction can be easily changed by reversing the phase shift between the two bridges.



10.3.1 Switching Sequence

In a single-phase, dual-active bridge, primary and secondary bridges are controlled simultaneously. All switches operate at 50 percent of duty ratio. The diagonal switches turn on and turn off together so

that the output of each bridge is a square wave. The switching sequence is divided into four intervals based on the inductor current waveform and phase shift between the voltages at the primary and secondary of the transformer.

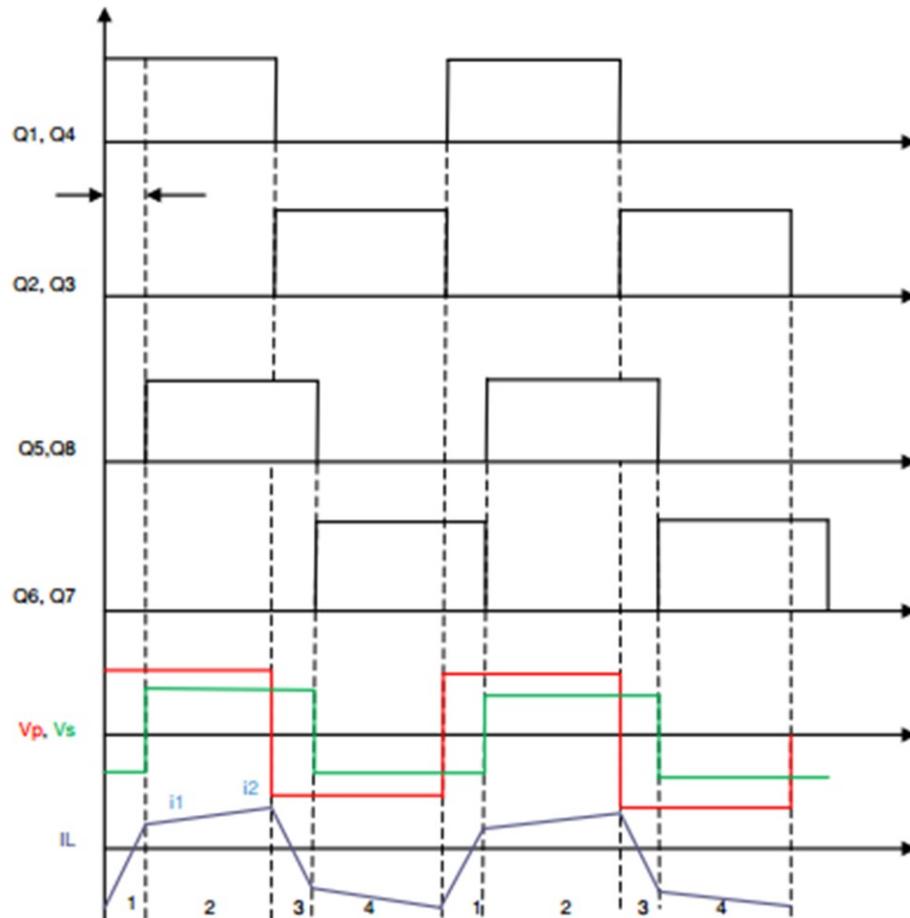


Figure 10.3: Switching Sequence

10.3.2 Zero Voltage Switching (ZVS)

During the transition from interval one to two, there exists a small dead time where the inductor-stored energy discharges the output capacitances of the MOSFETs and holds them close to zero voltage before they are turned on. This phenomenon, where the voltage across the MOSFET is close to zero at turn on, is referred to as zero voltage switching (ZVS). This is a major advantage with this topology, where due to the natural lagging current in one of the bridges, the inductive stored energy causes ZVS of all of the lagging bridge switches and some of the switches of the leading bridge. This depends on the stored inductive energy

$$E_L = \frac{1}{2} L I^2 \quad (10.2)$$

available to charge and discharge the output capacitances of MOSFETs

$$E_c = \frac{1}{2} C V^2 \quad (10.3)$$

When transition happens from interval one to two, the primary side switches Q1 and Q5 continue conduction, whereas in the secondary, Q6 and Q7 turn off and Q5 and Q8 turn on. Initially the voltage across Q6 and Q7 is zero when they are conducting, and Q5 and Q8 block the entire secondary voltage. During dead time, when all of the switches in the secondary are off, the inductor-stored energy circulates current which discharges the capacitor across MOSFETs Q5 and Q8 to zero and charges the capacitor across MOSFETs Q6 and Q7 to the full secondary voltage.

10.3.3 Switching Frequency

Switching frequency is important design parameter which affects the efficiency and power density of power converter. The input and the output voltage levels primarily determine the type of switches used in the power stage. Operating at higher switching frequencies enables reduced size of magnetics which help in improved thermal solution, thereby improving power density of the converter. Therefore, selection of switching frequency is primarily a tradeoff between the allowable heat sink solution and transformer size for a given efficiency target.

parameter	Value
Phase Shift	$-90 < \Phi < 90$
Turns Ratio	1:1
Load Resistance	40Ω
Input voltage	200V
Output voltage	200V
Output Power	1Kw

Table 10.1: Model Electrical Parameters

10.3.4 Design steps

1-Building The Model

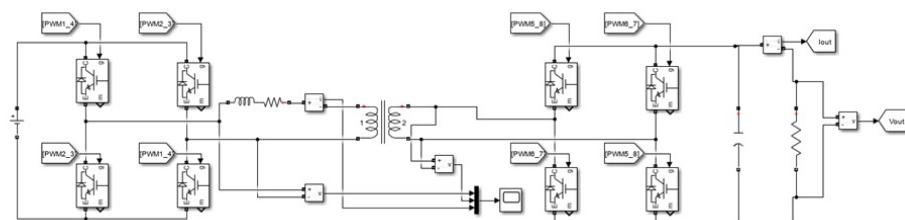


Figure 10.4: simulink module

The 1st bridge is connected to the input DC source, the 2nd bridge is connected to the load and the transformer connects between them.

2-Generating The PWM for The Switches

Firing the 1st bridge diagonal switches (1,4), the NOT go to switches (2,3) and the 2nd bridge diagonal switches (5,8) delayed by the shift from the PI controller, the NOT go to switches (6,7).

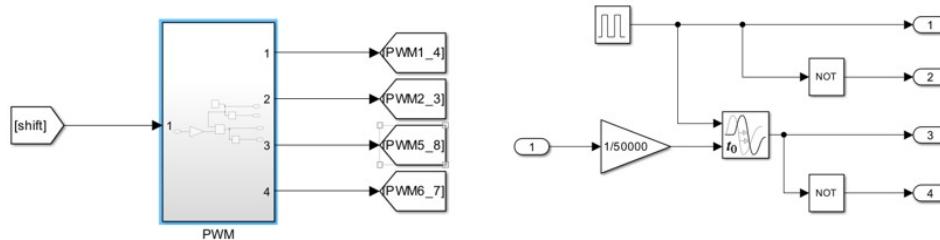


Figure 10.5: PWM generating block

3-Controlling The Shift

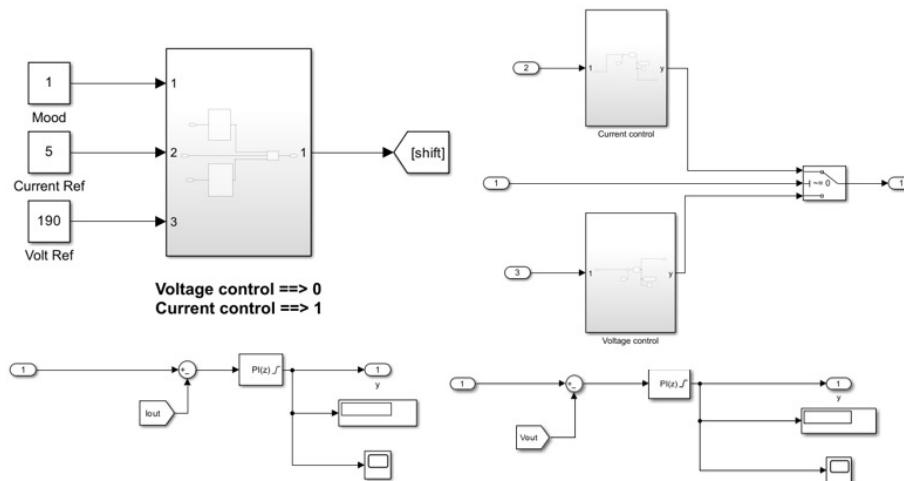


Figure 10.6: Control block

At the first we chose 0 for voltage control and 1 for current control. Then subtracting the reference value from the measured value to get the error and the PI controller makes that error small as possible after we tune it.

4-The Output Current and Voltage

The system has a slow response which we are trying to improve with the PI tuning.

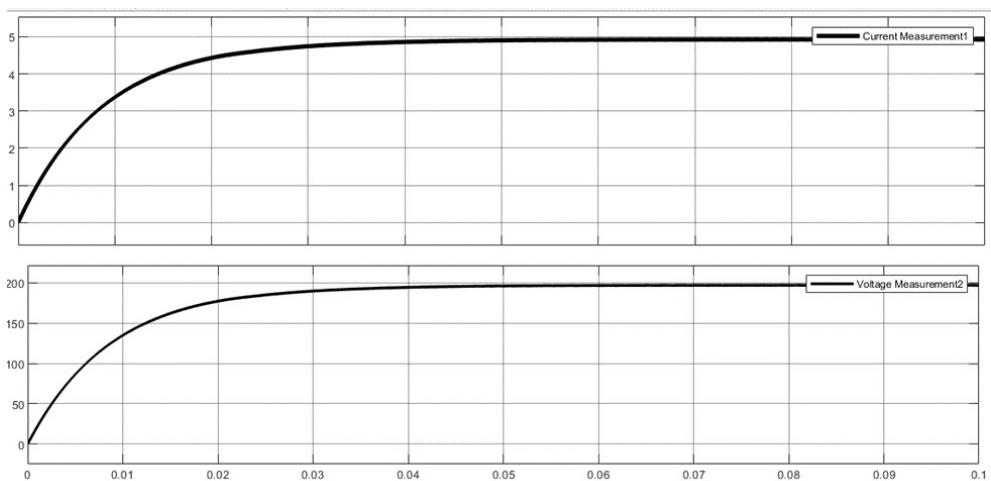


Figure 10.7: The output current and voltage

Chapter 11

LLC Converters

11.1 Introduction

LLC resonant converters have become an important topic in power electronics because they can meet the demanding performance requirements set by modern power supply designs. The LLC is one of a significantly larger family of resonant converter topologies, all of which are based on resonant tanks. Resonant tanks are circuits made up of inductors and capacitors that oscillate at a specific frequency, called the resonant frequency. Because they allow for higher switching frequencies (f_{SW}) and reduce switching losses, these switch-mode DC/DC power converters are often used in high-power, high-efficiency applications.

An LLC converter is made up of 4 blocks: the power switches, resonant tank, transformer, and diode rectifier. First, the MOSFET power switches convert the input DC voltage into a high-frequency square wave. This square wave then enters the resonant tank, which eliminates the square wave's harmonics and outputs a sine wave of the fundamental frequency. The sine wave is transferred to the secondary of the converter through a high-frequency transformer, which scales the voltage up or down, according to the application. Lastly, the diode rectifier converts the sine wave into a stable DC output.

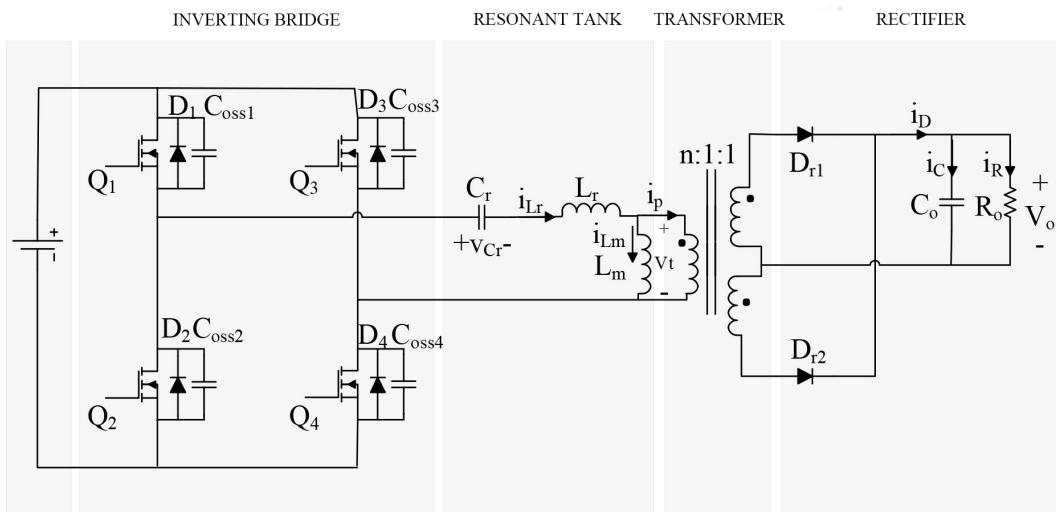


Figure 11.1: LLC Resonant Converter circuit

$$\text{Gain} = \text{bridge gain} * \text{resonant tank gain} * \text{turns ratio } (N_s/N_p) \quad (11.1)$$

Ns: Secondary side turns ratio

Np: Primary side turns ratio

The bridge can be full bridge or half bridge. Full bridge gain = 1 and half bridge gain = 0.5. Full bridge consists of 4 switches but half bridge consists of only two switches. in our design we will use full bridge inverter as shown in Figure 11.1 so the bridge gain equals 11.1.

11.2 Resonant Tank

The resonant tank is made up of a resonant capacitor (CR) and two inductors: the resonant inductor (LR), in series with the capacitor and transformer, and the magnetizing inductor (LM), in parallel. The tank's role is to filter out the square wave's harmonics, outputting a sine wave of the fundamental switching frequency to the input of the transformer.

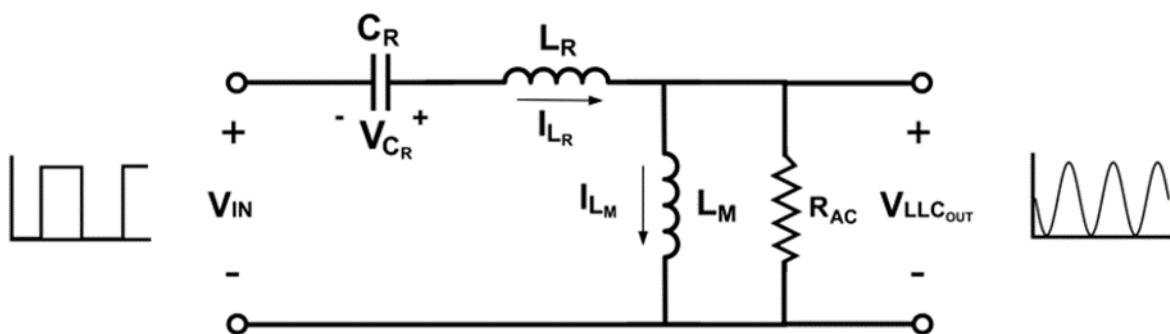


Figure 11.2: resonant tank

The resonant tank has a gain that varies according to the frequency and the load applied to the secondary side and the ratio between L_M and L_R (L_n). Designers must tune these parameters to ensure that the converter efficiently operates across a wide range of loads by designing the tank's gain to exceed 1 for all load values. This Figure shows the resonant tank's gain for a range of loads if the resonant tank were only composed of the resonant capacitor and the magnetizing inductor. At light loads, there is a clear peak in the resonant tank's gain. However, the gain for the heavy load does not peak — instead, it has a damped response and only achieves unity gain at very high frequencies. If the resonant tank is only made up of the resonant inductor (L_R) in series with the resonant capacitor, the behavior is different. The gain does not exceed 1, but when the load is heaviest, the tank reaches unity gain much more quickly than it would with the parallel inductor.

By implementing both inductors in the resonant tank, the resulting frequency gain response ensures that the converter can adequately respond to a much larger range of loads —in addition, it can enable stable control for the entire load range

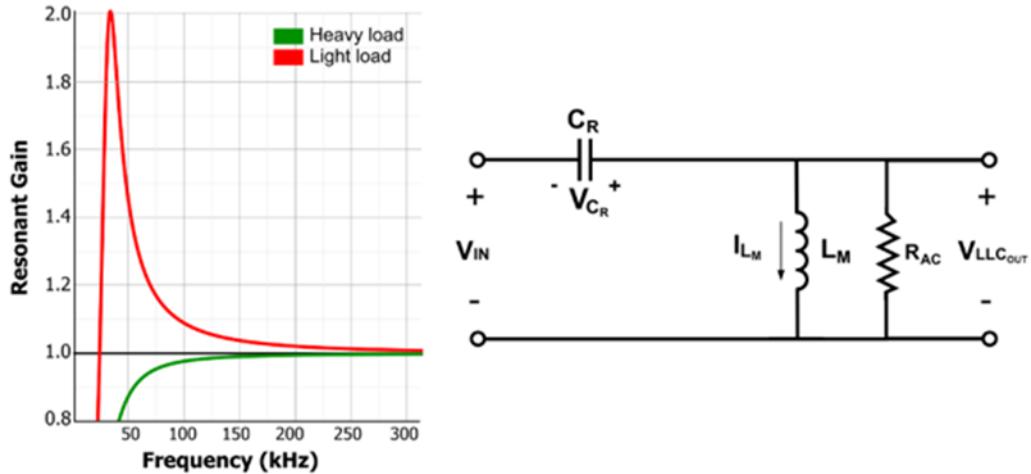


Figure 11.3: parallel resonant tank response

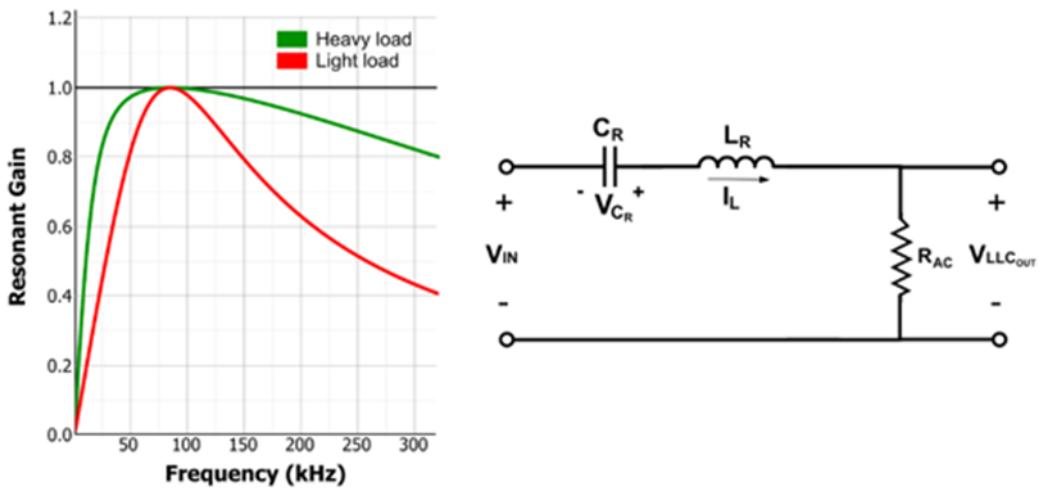


Figure 11.4: series resonant tank response

11.3 Behavior of the Voltage-Gain Function

The voltage-gain function expressed by Equation

$$M_G(Q, L_N, F_N) = \frac{V_{OVT}}{V_{IN}} = \frac{f_N^2 \times (L_N - 1)}{(f_N^2 - 1)^2 + f_N^2 x (f_N^2 - 1) \times (L_N - 1)^2 \times Q^2} \quad (11.2)$$

the quality factor (Q), which is dependent on the load connected to the output. However, using the value of the load is not accurate, since there is a transformer and a rectifier between the output of the resonant tank and the load. Therefore, we must use a primary-referenced value for the load, called RAC. R_{AC} and Q can be estimated with these two equations respectively

$$R_e = \frac{V_{oe}}{I_{oe}} = \frac{8 \times n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8 \times n^2}{\pi^2} \times R_L \quad (11.3)$$

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} \quad (11.4)$$

it is necessary to understand how Mg behaves as a function of the three factors f_n , L_n , and Q . In the gain function, frequency f_n is the control variable. L_n and Q are dummy variables, since they are fixed after their physical parameters are determined Mg is adjusted by f_n after a design is complete. As such, a good way to explain how the gain function behaves is to plot Mg with respect to f_n at given conditions from a family of values for L_n and Q

Regardless of which combination of L_n and Q is used, all curves converge and go through the point

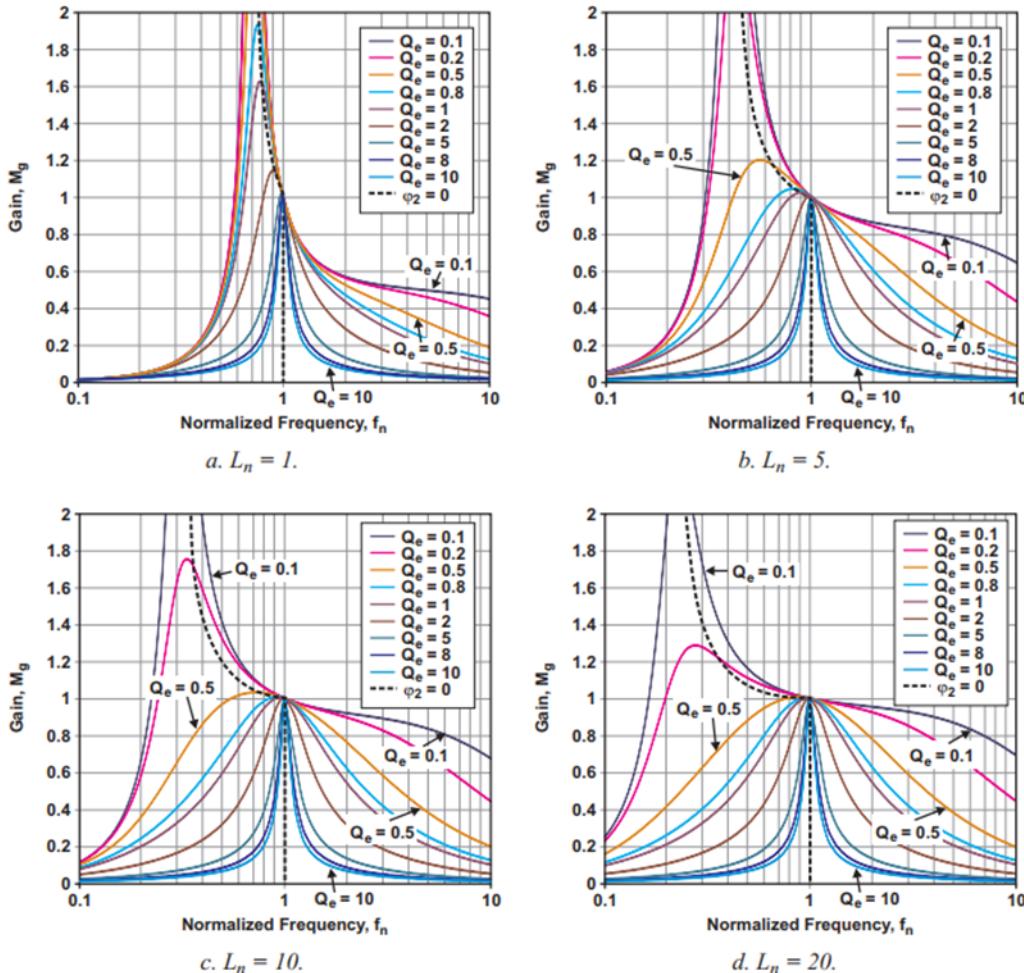


Figure 11.5: Plots of voltage-gain function (M_g) with different values of L_n

of $(f_n, Mg) = (1, 1)$. This point is at $f_n = 1$, or $f_{sw} = f_0$. By definition of series resonance, $XL_r - XC_r = 0$ at f_0 . In other words, the voltage drop across L_r and C_r is zero, so that the input voltage is applied directly to the output load, resulting in a unity voltage gain of $Mg = 1$.

It is obvious that lower values of L_n can achieve higher boost gain, in addition to the narrower range of the frequency modulation, meaning more flexible control and regulation, which is valuable in applications with wide input voltage range. Nevertheless, low values of L_n for the same quality factor Q and resonant frequency f_r means smaller magnetizing inductance L_m , hence, higher magnetizing peak-peak current ripple, causing increased circulating energy and conduction losses.

For summarize, After analysis of the tank circuit, the resonant tank gain equation:

$$K(Q, m, F_x) = \frac{F_x^2(m - 1)}{\sqrt{(m \cdot F_x^2 - 1) + F_x^2(F_x^2 - 1)^2 \cdot (m - 1)^2 \cdot Q^2}} \quad (11.5)$$

where,

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \quad (\text{Quality factor}) \quad (11.6)$$

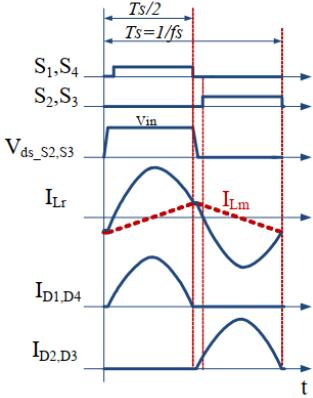
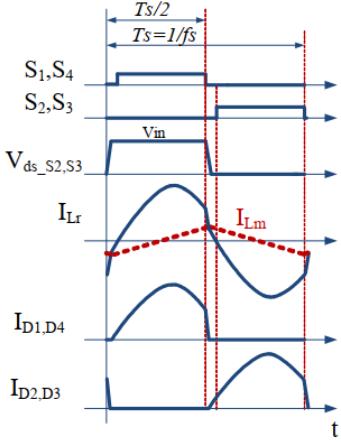
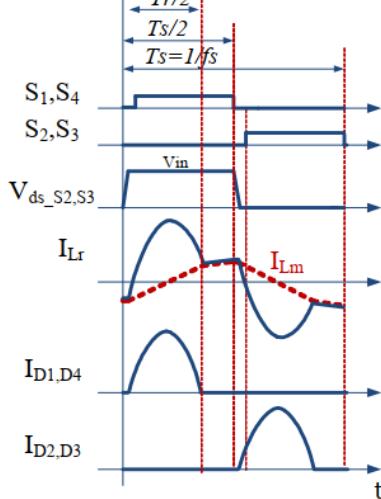
$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot R_o \quad (\text{Reflected load resistance}) \quad (11.7)$$

$$F_x = \frac{f_s}{f_r} \quad (\text{Normalized switching frequency}) \quad (11.8)$$

$$f_r = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \quad (\text{Resonant frequency}) \quad (11.9)$$

$$m = \frac{L_r + L_m}{L_r} \quad (\text{Ratio of total primary inductance to resonant inductance}) \quad (11.10)$$

using previous equations we can design our resonant tank by assuming variable with a constant value then start to calculate other parameters.

At Resonant frequency operation $f_s=f_r$	Above resonant frequency operation $f_s>f_r$	Below resonant frequency operation $f_s<f_r$
<p>Each half of the switching cycle contains a complete power delivery operation (described above), where the resonant half cycle is completed during the switching half cycle. By end of the switching half cycle, the resonant inductor current I_{Lr} reaches the magnetizing current I_{Lm}, and the rectifier current reaches zero. The resonant tank has unity gain and best optimized operation and efficiency, therefore, transformer turns ratio is designed such that the converter operates at this point at nominal input and output voltages</p> 	<p>Each half of the switching cycle contains a partial power delivery operation (described above), similar to the resonant frequency operation, but it differs in that the resonant half cycle is not completed and interrupted by the start of the other half of the switching cycle, hence primary side MOSFETs have increased turn off losses and secondary rectifier diodes have hard commutation. The converter operates in this mode at higher input voltage, where a step down gain or buck operation is required.</p> 	<p>Each half of the switching cycle contains a power delivery operation (described above), at the time when resonant half cycle is completed and resonant inductor current I_{Lr} reaches the magnetizing current, the freewheeling operation (as described above) starts and carries on to the end of the switching half cycle, hence primary side have increased conduction losses due to the circulating energy. The converter operates in this mode at lower input voltage, where a step up gain or boost operation is required.</p> 

11.4 Design Steps and Considerations

Line regulation is a requirement needs to be considered , it is defined as the maximum output voltage variation caused by an input voltage variation over a specified range, at a given output load current.A minimum and maximum output voltage, $V_{o_{min}}$ and $V_{o_{max}}$, respectively, will be assumed. To simplify the discussion, it will also be assumed that all parasitic voltage drops—for example, from PCB traces, the MOSFET's $R_{ds_{on}}$, the diode's forward voltage, etc.—are already converted or lumped into a part of the output-voltage range Mg should be designed to meet the conditions which says that all possible Mg values must contain the value of both Mg_{min} and Mg_{max} within the fn limits.

$$M_{g_min} = \frac{n \times V_{o_min}}{V_{in_max}}, M_{g_max} = \frac{n \times V_{o_max}}{V_{in_min}} \quad (11.11)$$

1. Selecting the Transformer Turns Ratio (n)

Initially the gain can be set at unity ($Mg = 1$) for the output voltage at its middle value between $V_{o_{min}}$ and $V_{o_{max}}$. This middle value can be called the output voltage's nominal value, $V_{o_{nom}}$, Similarly, the input voltage's nominal value can be called $V_{in_{nom}}$. Then the transformer turns ratio.

$$n = \frac{M_g \times V_{in_{nom}}}{V_{o_{nom}}} \quad (11.12)$$

2. Selecting L_n and Q

there is two ways for selecting these values

first method :

first we need to select Q_{max} , it depends on the load current. Heavy load conditions operate at high Q values, while lighter loads have lower Q values. It is important to set a value for the Q_{max} associated with the maximum load point

To illustrate the effect of the Q value on voltage regulation, Figure below shows an example voltage gain plot for different Q values. Let's assume that the resonant tank gain is required to range from 0.8 to 1.2 for example, we can see that the low Q value curve ($Q=0.3$) can reach higher boost gain, but it is less sensitive to frequency modulation in the “above resonance f_s, f_r ” region, hence, switching frequency has to increase much in order to reach the minimum voltage gain ($K=0.8$), causing extra switching losses, while the higher Q value curve ($Q=1$) can reach the minimum gain ($K=0.8$) with less switching frequency increase, but unable to reach the maximum gain ($K=1.2$). Therefore, a moderate Q value of around 0.5 seems to satisfy the voltage gain requirement in this specific case.

and then we can assume a suitable value for L_n which is around 6 and then plot gain curve , Mg_{max} can be plotted to the gain curves to obtain cross point between Q_{max} and Mg_{max} it will define the minimum frequency to operate to make sure that we operate in inductive region Because the gain curves are dependent on L_n and Q, several gain curves may need to be drawn to find a proper point This is certainly one way to make the initial selection of L n and Q, but it is a difficult way and most likely will require some wild guess.

second method : A more desirable approach is to create a common tool to represent the gain curves that can be shared and reused by different designs. Since the attainable peak gain (Mg_{ap}) corresponding to Qg_{max} is the highest gain of concern for a design, gain-curve plots can be created beforehand to show Mg_{ap} with different values of L_n and Q. Then L_n and Q can be selected to achieve $Mg_{ap} > Mg_{max}$ based on a common tool—the Mg_{ap} curves. How this method is used will be described after a discussion of how the Mg_{ap} curves are obtained. the created Mg_{ap} curves are shown in Fig. a The horizontal axis is Q and the vertical axis is Mg_{ap} with

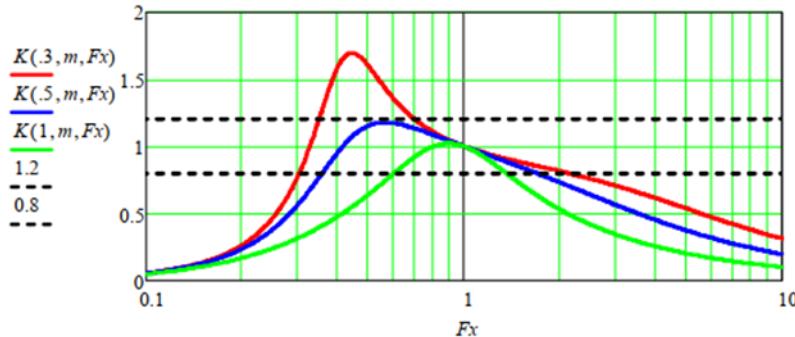
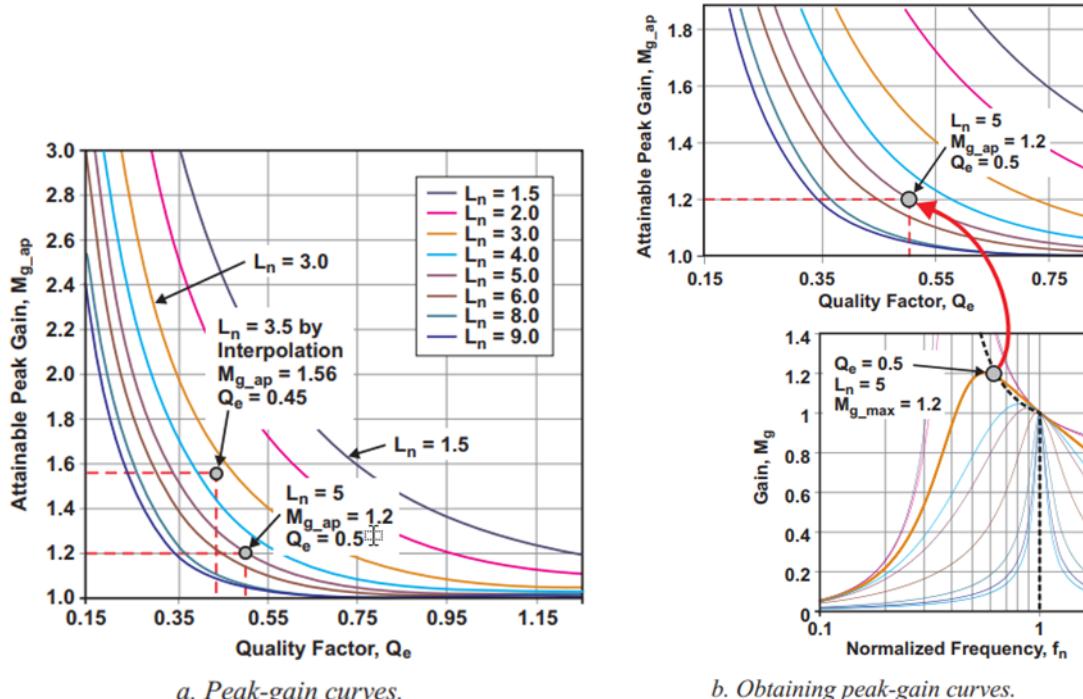


Figure 11.6: voltage gain

Figure 11.7: The created Mg_{ap} curves

respect to a family of fixed values for L_n . Fig. a is used to illustrate how Fig. b is formed. From a plot of gain curves, for example from Fig. b, which is partially copied to the lower half of Fig. b, one attainable peak-gain value, $Mg_{ap} = 1.2$, can be located at the curve with $(L_n, Q) = (5, 0.5)$. This point can be plotted to Fig. a at $(Mg_{ap}, Q) = (1.2, 0.5)$. (Note that $L_n = 5$ at this point.) Because all curves in Fig. b have a fixed $L_n = 5$, that figure can be used to repeat the process with different Q values. Then a peak-gain curve can be formed as a function of Q with a fixed $L_n = 5$.

With Mg_{max} already determined, Mg_{max} can be plotted as a horizontal line on Fig. a. Any Mg_{ap} values above this line are greater than Mg_{max} , so the designed converter should operate in the inductive region. For example, for $Mg_{max} = 1.2$, any values of Mg_{ap} can be selected that are greater than 1.2, as shown in Fig. a. Then the selected value meets the maximum-gain requirement. From the selected Mg_{ap} value, L_n and Q values can then be selected. For example, selecting a value from the curve of $L_n = 5$ provides the L_n value right away. Since a gain value greater than Mg_{max} needs to be selected, Q would have to be less than 0.5, based on Fig. a.

Similarly, a smaller L_n provides more gain and L_n can be selected by interpolating as shown in Fig. a. For example, if a value of 0.45 is selected for Q , the corresponding Mg_{ap} value with $L_n = 3.5$ would be $1.56 > Mg_{max}x = 1.2$, which satisfies the design requirements

3. determining R_e and resonant circuit parameters.

$$C_r = \frac{1}{2\pi \times Q_e \times f_0 \times R_e}, \quad L_r = \frac{1}{(2\pi \times f_0)^2 C_r}, \quad L_m = L_n \times L_r \quad (11.13)$$

11.5 Design Using MATLAB Script

This MATLAB Script used to find the values of components of resonant tank.

```
%----- DC Input -----
Vin = 700; % operating input voltage
Vin_rated = 700; % rated input voltage
Vin_min = 650; % minimum input voltage
Vin_max = 800; % maximum input voltage
%----- Output Load -----
Vo = 450; % operating output voltage
Vo_rated = 450; % rated output voltage
Vo_min = 400; % minimum output voltage
Vo_max = 600; % maximum output voltage
Po_rated = 7000; % rated output power
% load percentage with respect to the rated load
K_load = 1;
Q_rated = 0.3; % Q factor at the rated condition
%----- Operating Conditions -----
f_res = 70000; % resonant frequency
K_ind = 6; % parallel-to-series inductance ratio
% relative frequency factor for open-loop operation
K_rel_freq = 0.75;
%*****
%
% Parameters from Calculation
%
%*****
fsw = f_res*K_rel_freq; % switching frequency fsw
%----- Transformer and Load -----
a_sp = (Vo_max+Vo_min)/(2*Vin_rated); % Ns/Np ratio
a_sp2 = a_sp*a_sp;
% rated load resistance
Ro_rated = Vo_rated*Vo_rated/Po_rated;
% Ro_rated referred to the primary side
Ro_rated_pri = Ro_rated/a_sp2;
% load resistance at the operating conditions
```

```

Ro = Ro_rated / K_load ;
%----- Resonant Circuit -----
% Minimum gain and maximum gain required
G_dc_min = Vo_min/(a_sp*Vin_max); % minimum gain
G_dc_max = Vo_max/(a_sp*Vin_min); % maximum gain
% resonant inductance
Ls = (Q_rated*Ro_rated_pri)/(2*pi*f_res);
% resonant capacitance
Cs = 1/(2*pi*f_res*Q_rated*Ro_rated_pri);
% transformer magnetizing inductance
Lm = K_ind*Ls;
% Q value at the operating conditions
%Q = Zo / R; Zo = sqrt(Ls/Cs);
Q = sqrt(Ls/Cs)/(Ro/a_sp2);

```

11.6 LLC Resonant Converter Closed Loop Control

In any DC-DC converter, it's important to keep the value of the output voltage constant. The change in load leads to a change in output voltage in the case of open-loop control. Using closed-loop control is necessary, so LLC converter closed-loop control can be achieved by the cascaded control loop, as shown in the Figure 11.8.

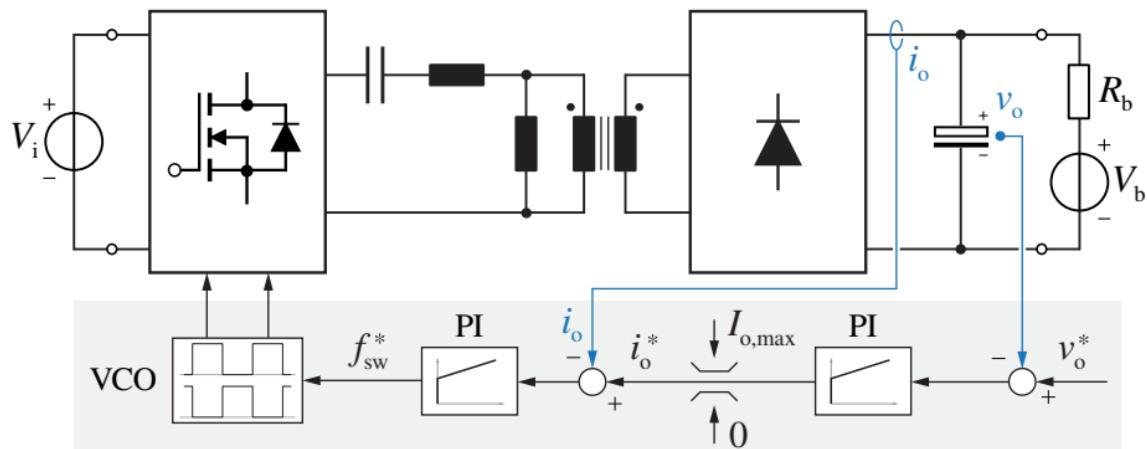


Figure 11.8: Cascaded Closed Loop Control for LLC Resonant Converter

The cascaded control loop is used to control both the output voltage and the current value. If the control loop consisted of a single PI controller that only controls the output voltage, during the transient of the circuit, the current value may become too high, potentially exceeding the rated switch current.

There are two PI controllers used in this setup. The first PI controller's input is the voltage error (the reference value minus the measured value), while the second PI controller's input is the current error (the output of the first PI controller minus the measured current value), as shown in the Figure 11.8.

11.7 Matlab Model

The simulation ratings:

- Input voltage: 650 - 800 volt rated 700 Volt.
- Output voltage: 350 - 500 volt rated 400 Volt.
- Transformer turns ratio $N_p/N_s = 700/400$.
- Frequency 70K Hz.
- Rated power: 7000 watt.
- L_r : 3.8e-05 H.
- L_m : 2.32e-04 H.
- C_r : 1.3e-07 F.

The MATLAB Simulink model:

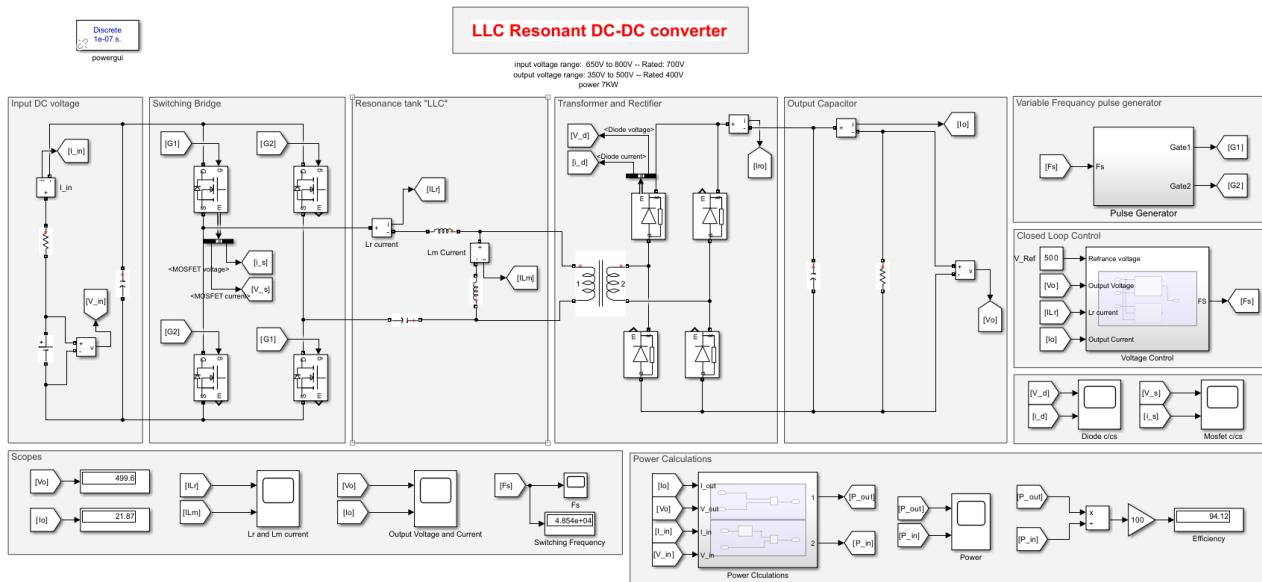


Figure 11.9: MATLAB Simulink Model For LLC Resonant Converter

This model consists of three main sections:

- The power circuit [11.10].
- Voltage controller [11.11].
- Variable frequency pulse generator [11.12].

The power circuit has input DC source, active bridge, resonant tank, transformer, diode bridge and output DC link.

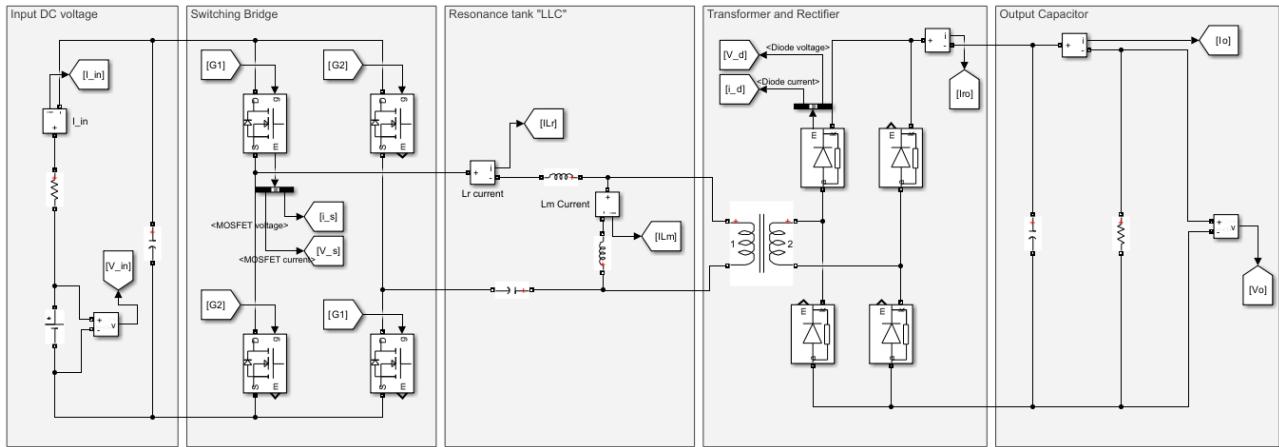


Figure 11.10: LLC Resonant Converter Power Circuit

The voltage controller is a cascaded control "multi loop control" using PI controller. It controls the output voltage and limit the transient current.

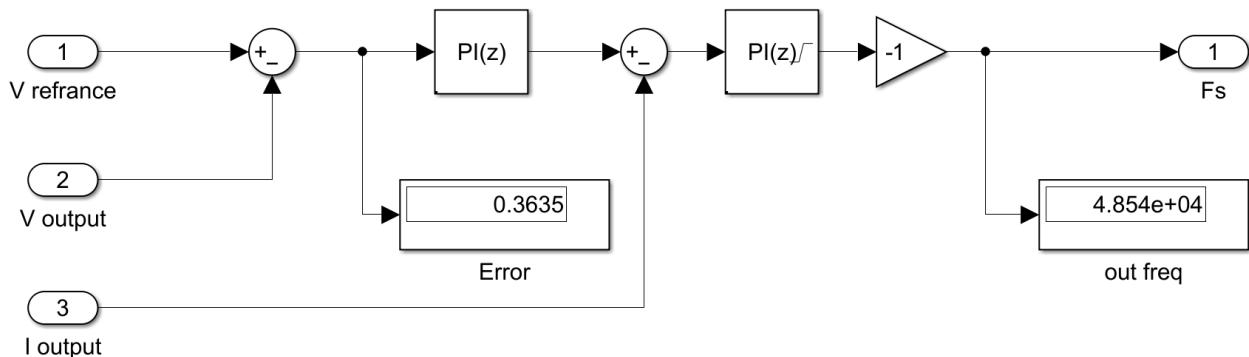


Figure 11.11: Cascaded Control for LLC Resonant Converter

Variable frequency pulse generator is used to generate pulses with specific duty cycle (in this model the duty cycle = 0.5) with variable frequency.

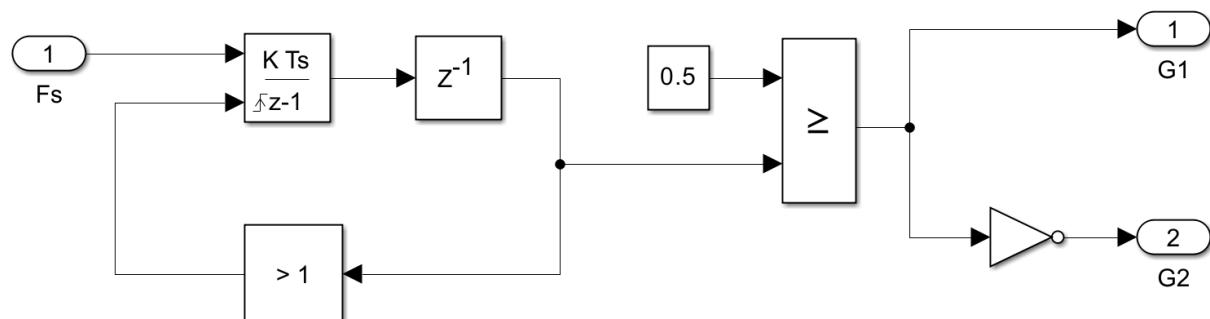


Figure 11.12: Variable Frequency Pulse Generator

This is the result of simulation in case of the reference voltage is 350V so the converter operates as a buck converter.

The figure 11.13 shows the results of simulation and shows the output voltage, the waveform of leakage inductor current and magnetizing inductor current and the change in frequency.

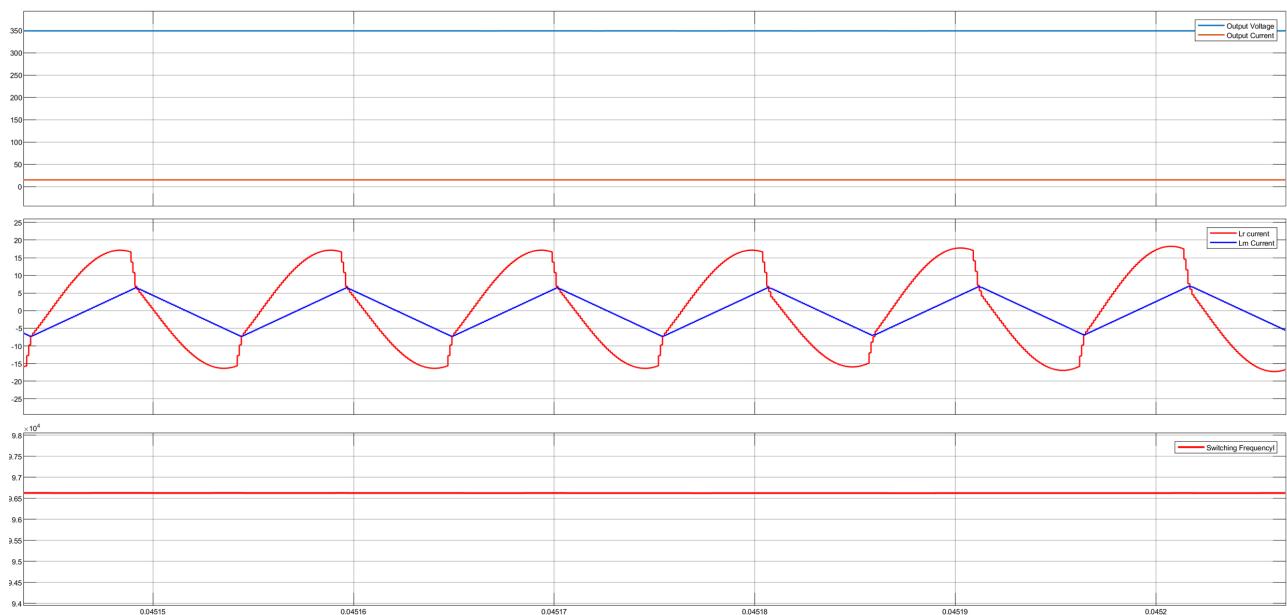
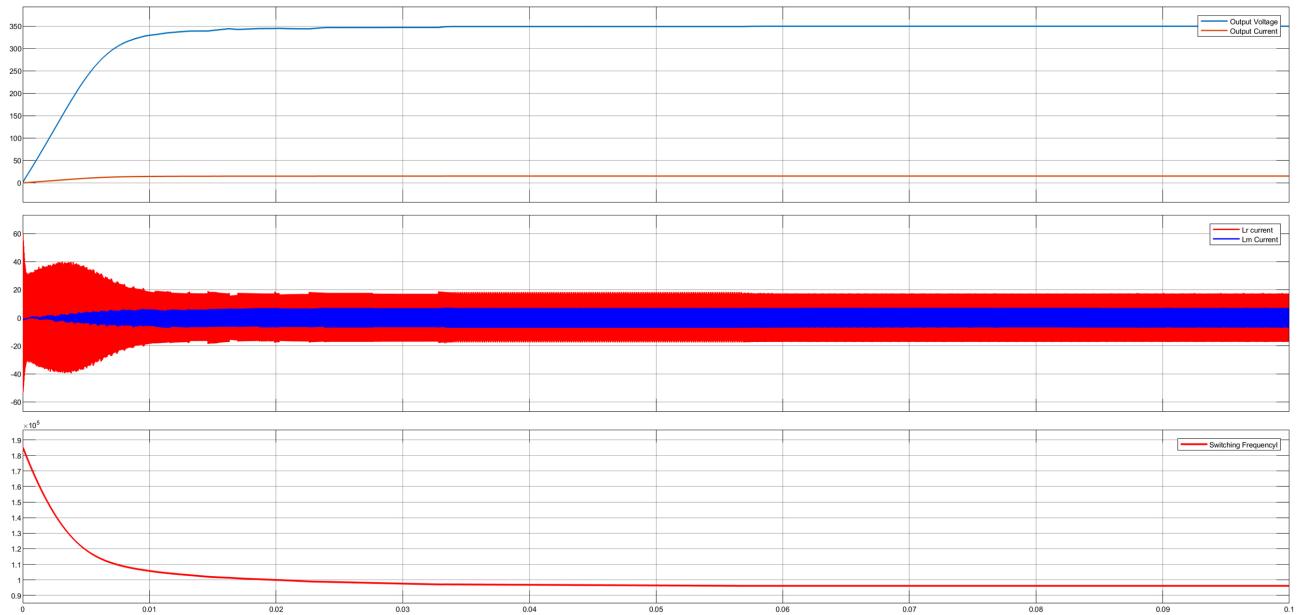


Figure 11.13: Results in case of Reference voltage equal 350V

This is the result of simulation in case of the reference voltage is 400V.

The figure 11.14 shows the results of simulation and shows the output voltage, the waveform of leakage inductor current and magnetizing inductor current and the change in frequency.

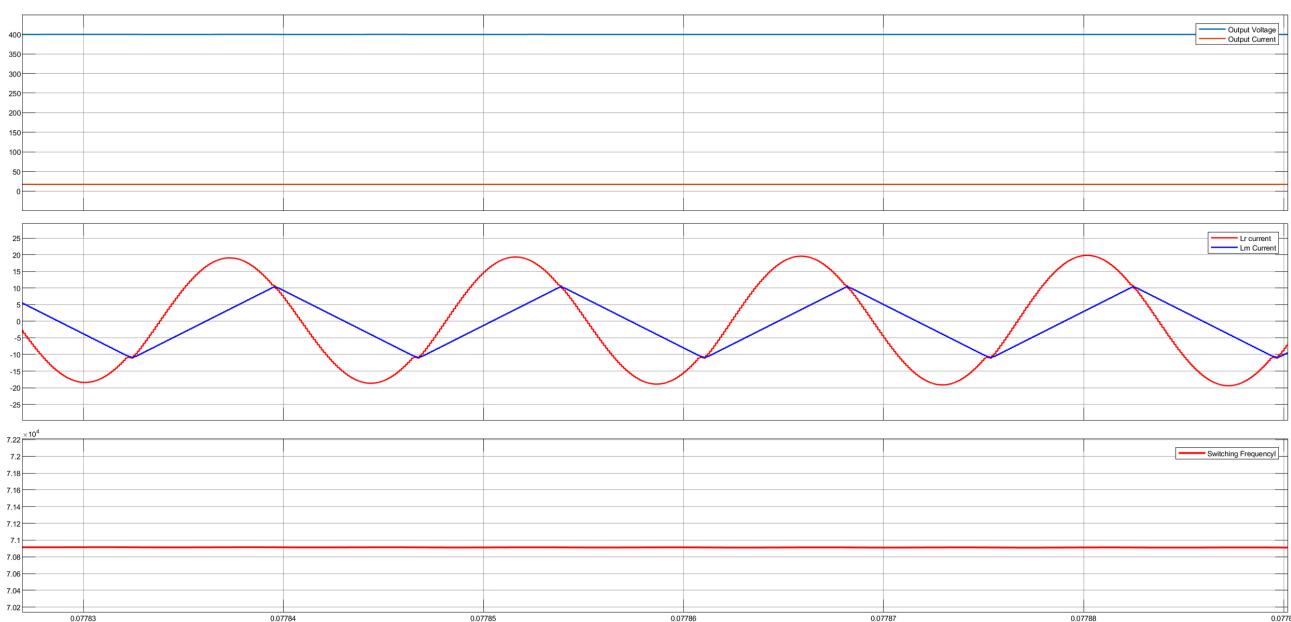
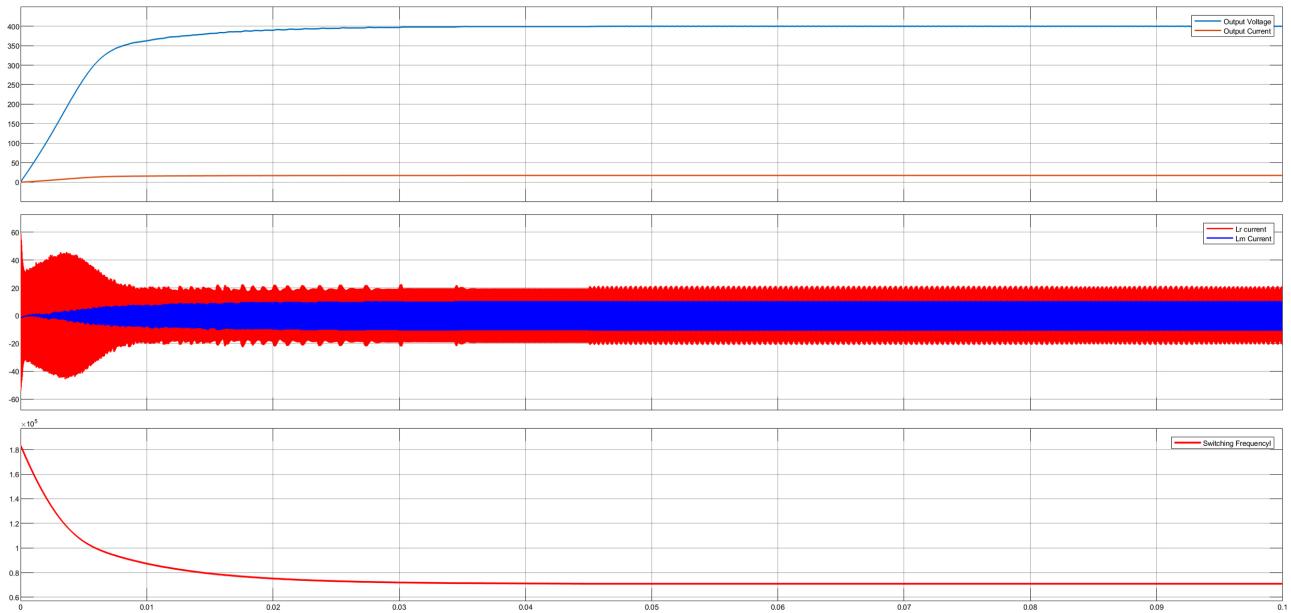
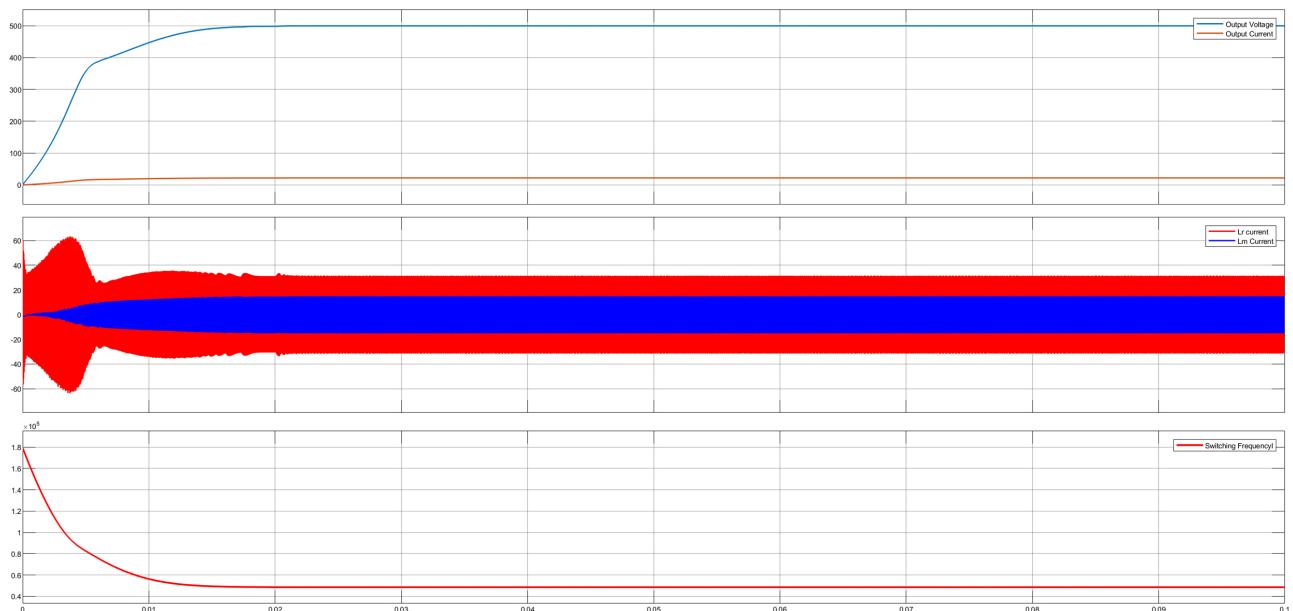


Figure 11.14: Results in case of Reference voltage equal 400V

This is the result of simulation in case of the reference voltage is 350V so the converter operates as a boost converter.

The figure 11.15 shows the results of simulation and shows the output voltage, the waveform of leakage inductor current and magnetizing inductor current and the change in frequency.



At Steady State

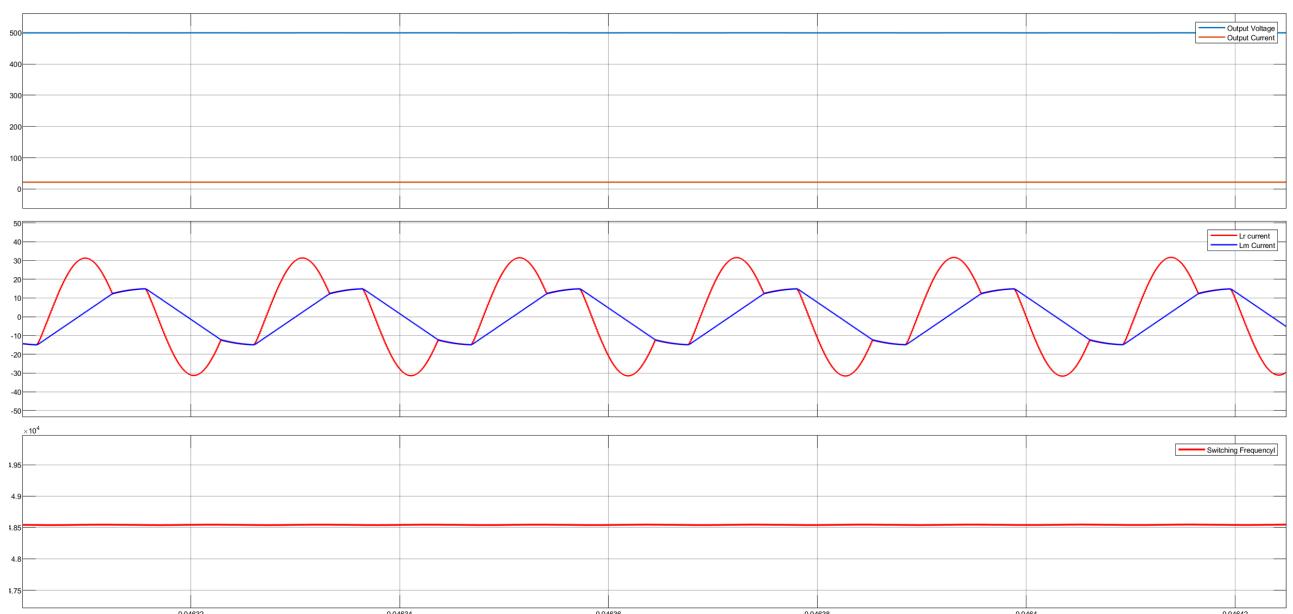


Figure 11.15: Results in case of Reference voltage equal 500V

11.8 Conclusion

The LLC resonant converter is an isolated DC-DC converter with high efficiency, around 96%. It can be used for bucking or boosting the input voltage. The LLC resonant converter can be controlled by adjusting the switching frequency of its inverting bridge, allowing it to operate in three modes. It finds application in various fields such as electrical vehicles, solar panels, and more.

Chapter 12

High Frequency (HF) Transformer Design

12.1 Introduction to HF Transformer

High-frequency transformers are vital components in various electronic systems, especially in power electronics, telecommunications, and high-frequency switching applications. Unlike conventional transformers operating at line frequencies (50 Hz or 60 Hz), high-frequency transformers are designed to operate at frequencies ranging from several kHz to MHz.[18]

12.1.1 Operating Frequency

High-frequency transformers operate at frequencies higher than those of traditional transformers. They are commonly used in applications such as switch-mode power supplies (SMPS), DC-Dc converters (the application used in our project), inverters, and radio frequency (RF) circuits.

12.1.2 Core Materials

High-frequency transformers often use ferrite cores rather than traditional iron cores. Ferrite materials have low losses at high frequencies, making them ideal for high-frequency applications. Other materials like powdered iron, amorphous metals, and some specialty materials are also used based on specific design requirements.

12.1.3 Winding Configurations

Transformers designed for high frequencies may have specialized winding configurations to minimize leakage inductance and inter-winding capacitance. Techniques such as interleaving, layering, and other techniques may be employed to achieve desired electrical characteristics.

12.1.4 Wire and Insulation

High-frequency transformers often use specialized wire types with thin enamel insulation to minimize skin effect losses and maximize packing density. Insulation materials are carefully selected to withstand the high voltages and minimize parasitic capacitances.

12.1.5 Losses and Efficiency

Efficiency is critical in high-frequency transformers due to the increased switching losses at higher frequencies. Design considerations include minimizing core losses (hysteresis and eddy current losses), and copper losses (resistive losses in windings).

12.1.6 Magnetic Design

Magnetic design involves selecting core materials, determining core geometry, calculating the number of turns, and optimizing magnetic flux density to achieve desired performance.

12.1.7 Electromagnetic Interference (EMI)

High-frequency transformers should be designed to minimize electromagnetic interference (EMI) emissions and susceptibility. Techniques such as shielding, grounding, and layout optimization are used to mitigate EMI issues.

12.1.8 Temperature Rise and Cooling

High-frequency transformers may experience significant temperature rise due to increased losses. Cooling methods such as conduction, convection, and liquid cooling may be employed to manage temperature rise.

12.2 HF Transformer Design

High-frequency transformer design requires a deep understanding of core materials, winding configurations, losses, efficiency, electromagnetic properties, and thermal management techniques. The design process involves careful consideration of these factors to meet the performance requirements of modern electronic systems operating at high frequencies.

12.2.1 General Procedures

1. Select system requirements including:
 - Switching Frequency.
 - Power Supply in Watt.

- Output Voltage and Current and Input Voltage.
2. Choose the suitable and most appropriate core material.
 3. Determine number of turns.
 4. Test the obtained output and compare it with the required one to be obtained.
 5. Determine diameter of wire.
 6. Determine number of layers.
 7. Determine length of wire.

12.2.2 Procedures in Detail

Starting with the Primary Side:

- **First:** The Choice of Core Material:

The choice of the core and its material is done through the intersection between the power rating, the switching frequency, and the selected shape from Typical Power Handling Chart shown in Figure 12.1:

Typical Power Handling Chart

Power in Watts				Pot, RS, DS	E Cores	RM, PQ, EP	UU, UI, UR	ETD, EER, EC	EFD, Planar	Toroid
20 kHz	50 kHz	100 kHz	250 kHz							
2	3	4	7	41811 RS DS PC	41205 EE 41707 EE	41313 EP 41812 RM 41912 RM			42107 EE 41805 EE	40907 TC 41406 TC 41303 TC 41435 TC 41304 TC 41206 TC 41506 TC 41407 TC 41405 TC 41305 TC
5	8	11	21	41814 PC 42311 RS DS HS	41808 EE	41717 EP 42013 RM 42016 PQ 42610 PQ			42019 EFD 42216 EI 42214 EI 43208 EI	41306 TC 41607 TC 41450 TC 41410 TC 41605 TC 41610 TC 41606 TC
12	18	27	52		41810 EE 42510 EE	42316 RM				
13	20	29	56	42213 PC		42614 PQ				
15	22	32	62	42318 RS DS HS					42214 EE	
18	28	40	78			42020 PQ			42523 EFD	
19	30	42	83	42616 RS DS HS	42513 EE 42515 EI	42120 EP 43214 PQ	42515 UI		42216 EE 43618 EI 42217 EE 44008 EI	42106 TC 41809 TC
26	42	58	113						43208 EE	42206 TC
28	45	63	122		42520 EE				43030 EFD	
30	49	67	131	42616 RS PC		42620 PQ				42109 TC
33	53	74	144		42515 EE	42819 RM				42207 TC
40	61	90	175		42526 EE 43007 EE					42506 TC
42	70	94	183	43019 HS		42625 PQ			43618 EE	
48	75	108	210	42823 PC 43019 RS DS PC	43009 EE		42512 UU 42515 UU	42929 ETD	44008 EE	42507 TC

Figure 12.1: Typical Power Handling Chart

- **Second:** Checking or Testing the Power:

$$Power = \frac{AP_c * f}{754} \quad (12.1)$$

Where $AP_c = A_e * W_c$,

AP_c is calculated in cm^4 ,

A_e is the effective area of the core (from datasheet) in cm^2 ,

W_c is the winding window of copper.

OR

$$Power = Area * (5.6)^2 \quad (12.2)$$

Where Area is the product of core length and width or total area of core in cm^2 .

- **Third:** Calculating the Number of Turns:

$$N_p = \frac{V_{peak} * 10^8}{4 * B_{MaxGauss} * A_e * f} \quad (12.3)$$

Where, $B_{MaxGauss}$ is the flux density that depends on core material choice in Gauss,

$$1000 \text{ Gauss} = 0.1 \text{ Tesla}$$

V_{Peak} is the peak input voltage to the primary side of transformer in Volt (V),

A_e is the effective area of the chosen core in cm^2 ,

N_p is the required Number of primary side turns,

f is the switching frequency in Hz.

Another Rule:

$$N_p = \frac{V_{in} * D * 10^8}{B_{max\text{ Gauss}} * A_e * f} \quad (12.4)$$

Where, D is the Duty Cycle (Since we are dealing with square wave),

V_{in} is the input voltage.

OR

$$N_p = \frac{V_{in} * t_{on}}{B_{max\text{ Tesla}} * A_e} \quad (12.5)$$

There is an important check to take into account which is:

For the calculated N_p , check the flux density obtained (B) to make sure that it still suited the chosen core material by substituting in the following rule:

$$B_{max\text{ Gauss}} = \frac{V_{peak} * 10^8}{4 * N_p * A_e * f} \quad (12.6)$$

Fourth: Calculating the Diameter of Wire:

We should determine Current in Primary Side by:

- a. Finding output power from the relation: $P_o = V_o * I_o$
- b. Finding input power from the relation: $P_{in} = P_o + 0.05 * P_o$ where $0.05 * P_o$ are some assumed losses.
- c. Finding current in primary side from the relation: $I_p = \frac{P_p}{V_p} = \frac{P_{in}}{V_{in}}$

Using the AWG (American Wire Gauge) and entering with the value of I_p which is approximately the maximum current in such table, we get the suitable diameter of wire.

However, there are well-known diameters like 0.4 mm and 0.6 mm.

So, there are some other checks to determine whether to use the standard diameters or the one obtained from table after calculating I_p :

- a. Check for Max Frequency (Make sure you choose diameter that has maximum frequency greater than the input switching frequency).
- b. Check the resistance from the table (Make sure that the chosen diameter has resistance (ohm/km) that causes an acceptable voltage drop. However, Voltage Drop Calculation is more effective in Secondary than in Primary).
- c. Check for maximum current, max frequency, and resistance per km if you decide to use a standard diameter like 0.4 mm and 0.6 mm.

Fifth: Calculating the Number of Layers:

- a. Calculate the vertical distance of the area subjected to the winding.
- b. Calculate the number of wires: Number of wires = $\frac{\text{Distance Calculated in a}}{\text{Diameter of Wire}}$

Note: There will be a margin to prevent the presence of high voltage at the terminals in the case of E-core for example (The margin is between 1 mm and 2 mm).

- c. Calculate the number of layers from the relation:

$$\text{Number of Layers} = \frac{\text{Number of Turns}}{\text{Number of Wires}}$$

There is another check here which is the guarantee that the area of the chosen core will be enough for or compatible with the winding and number of layers:

This check is done by:

- a. If Number of Layers * diameter of 1 wire < Area occupied by the wires by acceptable value. Therefore, proceed to the next step of design.
- b. If Number of Layers * diameter of 1 wire \geq Area occupied by the wires. Therefore, there should be some suggested modifications either:

1. Change Core to a larger one.
2. Or Increase Switching Frequency to decrease the Number of turns and hence decrease the number of layers.

$$N_p = \frac{V_{\text{peak}} * 10^8}{4 * B_{\text{max Gauss}} * A_c * f} \quad \& \text{ Number of Layers} = \frac{\text{Number of Turns}}{\text{Number of Wires}}$$

As N_p is inversely proportional to Switching Frequency and directly proportional to Number of Layers.

Note: Take into consideration that increasing frequency increases the core losses.

Sixth: Calculating the Length of Wire:

Length of Wire = Number of Turns * Length of Complete Turn + Additional 10 or 20 cm (according to design) for the terminals

Checking the Voltage Drop mentioned in **Fourth** is done by:

(Value from Table) ----- 1000 m

? ----- Length of Wire

After that, the Secondary Side:

Many steps are the same as those done in Primary Side but with some differences.

Calculating Number of Turns:

From the relation: $\frac{V_p}{V_s} = \frac{N_p}{N_s}$ ----- $N_s = \frac{N_p * V_s}{V_p}$

Where, V_p is the primary voltage,

V_s is the secondary voltage,

N_p is the number of turns in the primary side,

N_s is the number of turns in the secondary side.

Some Notes and differences for Secondary Design:

- If N_s is decimal, approximate it to the larger or the smaller value then check for V_s from the relation: $\frac{V_p}{V_s} = \frac{N_p}{N_s}$.
- The value of I_s is the same as output current.
- If there is a problem with the diameter of wire with the max frequency when dealing with the AWG Table (as the current in secondary is in Amperes with max frequencies less than the ones used in switching and diameter of wire which is not standard), stranding, or bundling are used in this case. The Number of wires is calculated from the relation:

$$\text{Number of wires} = \frac{I_s}{I_{\text{chosen from table to achieve a standard diameter}}}$$

For Low Rating (Practical):**Givens:**

Switching Frequency = 50KHz

Input and Output Voltage = 200 V

Output Power = 1Kw = 1000 watt

First: The Choice of Core Material:

20 kHz	50 kHz	100 kHz	250 kHz	Pot, RS, DS	E Cores	RM, PQ, EP	UU, UI, UR	ETD, EER, EC	EFD, Planar	Toroid
220	350	495	962		44721 EE		44119 UR			
230	350	550	1073	44229 RS DS		43535 PQ	44121 UR	44013 EER		
260	400	585	1137							43813 TC
280	430	630	1225	44229 PC	44020 EE			44216 EER		
300	450	675	1312					44444 ETD 44818 EER 45224 EC	45810 EI	43615TC
340	550	765	1487		44033 EE		44125 UR			
360	580	810	1575		44022 EE	44040 PQ		45418 EER		43620 TC
410	650	922	1793		44033 EE 45724 EE		44130 UR	44821 EER 44949 ETD	46410 EI	44416 TC 44419 TC 43825 TC
550	800	1237	2406		46016 EE					44015 TC 44715 TC
650	1000	1462	2843			45050 PQ			45810 EE	
700	1100	1575	3062		45528 EE		45716 UR	45454 ETD	46410 EE	44920 TC 44916 TC
900	1500	2000	3900		45530 EE					44925 TC
1000	1600	2250	4375	43428 UG	47228 EE 46022 EE		45917 UR	45959 ETD 47035 EC		46013 TC 46113 TC
1600	2600	3700	7215				46420 UR			44932 TC 46019 TC
2000	3000	4500	8750		46527 EE 47133 EE 48020 EE					46325 TC 46326 TC 47313 TC
2800	4200	6500	12675				49316 UI		49938 EE	48613 TC 48626 TC

Figure 12.2: Typical Power Handling Chart

But here, we don't want to choose these types of cores. We are searching for E cores. Therefore, we head to a power > 1000 watt from this chart.

Checking Powers for E cores with the intersections of 50 KHz and powers: 1100watt, 1500 watt and 1600 watt:

For 1100 watt: 45528 EE (or 45528 EC)

Typical Power Handling Chart

Power in Watts				Pot, RS, DS	E Cores	RM, PQ, EP	UU, UI, UR	ETD, EER, EC	EFD, Planar	Toroid
20 kHz	50 kHz	100 kHz	250 kHz							
220	350	495	962		44721 EE		44119 UR			
230	350	550	1073	44229 RS DS		43535 PQ	44121 UR	44013 EER		
260	400	585	1137							43813 TC
280	430	630	1225	44229 PC	44020 EE			44216 EER		
300	450	675	1312					44444 ETD 44818 EER 45224 EC	45810 EI	43615TC
340	550	765	1487		44033 EE		44125 UR			
360	580	810	1575		44022 EE	44040 PQ		45418 EER		43620 TC
410	650	922	1793		44033 EE 45724 EE		44130 UR	44821 EER 44949 ETD	46410 EI	44416 TC 44419 TC 43825 TC
550	800	1237	2406		46016 EE					44015 TC 44715 TC
650	1000	1462	2843			45050 PQ			45810 EE	
700	1100	1575	3062		45528 EE		45716 UR	45454 ETD	46410 EE	44920 TC 44916 TC
900	1500	2000	3900		45530 EE					44925 TC

Figure 12.3: Typical Power Handling Chart

For 1500 watt: 45530 EE (or 45530 EC)

Typical Power Handling Chart

Power in Watts				Pot, RS, DS	E Cores	RM, PQ, EP	UU, UI, UR	ETD, EER, EC	EFD, Planar	Toroid
20 kHz	50 kHz	100 kHz	250 kHz							
220	350	495	962		44721 EE		44119 UR			
230	350	550	1073	44229 RS DS		43535 PQ	44121 UR	44013 EER		
260	400	585	1137							43813 TC
280	430	630	1225	44229 PC	44020 EE			44216 EER		
300	450	675	1312					44444 ETD 44818 EER 45224 EC	45810 EI	43615TC
340	550	765	1487		44033 EE		44125 UR			
360	580	810	1575		44022 EE	44040 PQ		45418 EER		43620 TC
410	650	922	1793		44033 EE 45724 EE		44130 UR	44821 EER 44949 ETD	46410 EI	44416 TC 44419 TC 43825 TC
550	800	1237	2406		46016 EE					44015 TC 44715 TC
650	1000	1462	2843			45050 PQ			45810 EE	
700	1100	1575	3062		45528 EE		45716 UR	45454 ETD	46410 EE	44920 TC 44916 TC
900	1500	2000	3900		45530 EE					44925 TC

Figure 12.4: Typical Power Handling Chart

For 1600 watt:47228 EE or 46022 EE

Typical Power Handling Chart

20 kHz	50 kHz	100 kHz	250 kHz	Pot, RS, DS	E Cores	RM, PQ, EP	UU, UI, UR	ETD, EER, EC	EFD, Planar	Toroid
220	350	495	962		44721 EE		44119 UR			
230	350	550	1073	44229 RS DS		43535 PQ	44121 UR	44013 EER		
260	400	585	1137							43813 TC
280	430	630	1225	44229 PC	44020 EE			44216 EER		
300	450	675	1312					44444 ETD 44818 EER 45224 EC	45810 EI	43615 TC
340	550	765	1487		44033 EE		44125 UR			
360	580	810	1575		44022 EE	44040 PQ		45418 EER		43620 TC
410	650	922	1793		44033 EE 45724 EE		44130 UR	44821 EER 44949 ETD	46410 EI	44416 TC 44419 TC 43825 TC
550	800	1237	2406		46016 EE					44015 TC 44715 TC
650	1000	1462	2843			45050 PQ			45810 EE	
700	1100	1575	3062		45528 EE		45716 UR	45454 ETD	46410 EE	44920 TC 44916 TC
900	1500	2000	3900		45530 EE					44925 TC
1000	1600	2250	4375	43428 UG	47228 EE 46022 EE		45917 UR	45959 ETD 47035 EC		46013 TC 46113 TC

Figure 12.5: Typical Power Handling Chart

Second: Checking or Testing the Power:

For 45528 EE (or 45528 EC), 45530 EE (or 45530 EC) & 47228 EE or 46022 EE:

TYPE/SIZE	ORDERING CODE	MAGNETIC DATA						HARDWARE
		I _e (mm)	A _e (mm ²)	A _e min (mm ²)	V _e (mm ³)	WaAc (cm ⁴)	Weight (grams per set)	
E 40/17/11	0_44011EC	76.7	127	114	9,780	1.26	49	
E 42/21/9	0_44016EC	98.4	107	106	10,500	1.65	52	
E 43/21/15	0_44020EC	97.0	178	175	17,300	3.55	87	PCB4020N1
I 43/6/15	0_44020IC	67.1	177	176	11,900	1.36	60	PCB4020N1
E 43/21/20	0_44022EC	97.0	233	233	22,700	4.22	114	PCB4022N1
E 42/33/20	0_44033EC	145	236	234	34,200	6.36	164	
E 41/17/12	0_44317EC	77.0	149	142	11,500	1.88	57	PCB4317M1
E 47/20/16	0_44721EC	88.9	234	226	20,800	3.3	103	PCB4721M1
E 56/28/21	0_45528EC	124	353	345	44,000	9.78	212	PCB5528WC
E 56/28/25	0_45530EC	123	420	411	52,000	12.1	255	PCB5530FA
E 56/24/19	0_45724EC	107	337	337	36,000	6.98	179	PCB5724M1
E 60/22/16	0_46016EC	110	248	240	27,200	5.74	135	
E 60/31/22	0_46022EC	139	402	401	55,900	21.0	200	
E 65/32/27	0_46527EC	147	540	530	79,000	23.5	410	00B652701
E 70/33/32	0_47133EC	149	683	676	102,000	23.3	495	
E 72/28/19	0_47228EC	137	368	363	50,300	15.0	250	00B722801
E 80/38/20	0_48020EC	184	392	392	72,300	31.6	357	00B802081
E 100/59/27	0_49928EC	274	738	692	202,000	90.6	980	

Refer to page 62 for additional hardware information.

Figure 12.6: Typical Power Handling Chart

For 1100 watt: 45528 EE (or 45528 EC):

$$\text{Power} = \frac{AP_c * f}{754} = \frac{9.78 * 50 * 10^3}{754} = 648.5411141 \text{ watt} < 1000 \text{ watt}$$

Then, Search in the chart for a core with a higher power (>1100watt)

For 1500 watt: 45530 EE (or 45530 EC):

$$\text{Power} = \frac{AP_c * f}{754} = \frac{12.1 * 50 * 10^3}{754} = 802.3872679 \text{ watt} < 1000 \text{ watt}$$

Then, Search in the chart for a core with a higher power (>1500watt)

For 1600 watt: 47228 EE:

$$\text{Power} = \frac{AP_c * f}{754} = \frac{15 * 50 * 10^3}{754} = 994.6949602 \text{ watt}$$

For 1600 watt: 46022 EE:

$$\text{Power} = \frac{AP_c * f}{754} = \frac{21 * 50 * 10^3}{754} = 1392.572944 \text{ watt}$$

Then we can choose either **47228 EE** or **46022 EE**. We chose **46022 EE**.

Third: Calculating the Number of Turns:

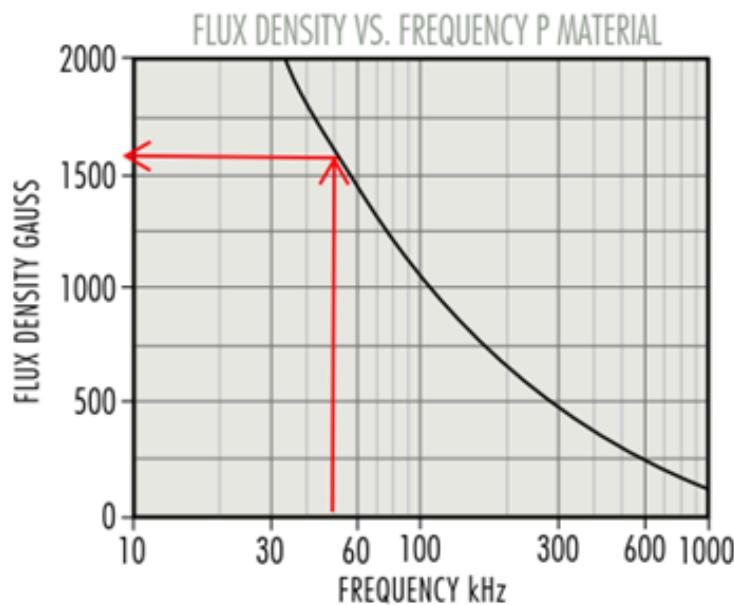


Figure 12.7: Flux Density Vs Frequency (P-Material)

$$N_p = \frac{V_{\text{peak}} * 10^8}{4 * B_{\max} \text{Gauss} * A_e * f} = \frac{200 * 10^8}{4 * 1580 * 402 * 10^{-2} * 50 * 10^3} = 15.74406449 \text{ turns} \approx 16 \text{ turns}$$

Fourth: Calculating the Diameter of Wire:

We should determine Current in Primary Side by:

$$P_o = V_o * I_o = 1000 \text{ watt} = 1\text{Kw}$$

$$P_{\text{in}} = P_o + 0.05 * P_o = 1000 + 0.05 * 1000 = 1050 \text{ watt} = 1.05\text{Kw}$$

$$I_p = \frac{P_p}{V_p} = \frac{P_{\text{in}}}{V_{\text{in}}} = \frac{1050}{200} = 5.25\text{A}$$

From AWG Table: $I_p = 5.25\text{A}$ (I_{max}). However, for 50KHz or 53KHz, the maximum current is 0.729A. So, parallel wires or bundling will be used:

$$\text{Number of parallel wires} = \frac{I_p}{I_{\text{max}}} = \frac{5.25}{0.729} = 7.201646091 \text{ wires} \approx 8 \text{ wires}$$

AWG	Diameter [inches]	Diameter [mm]	Area [mm ²]	Resistance [Ohms / 1000 ft]	Resistance [Ohms / km]	Max Current [Amperes]	Max Frequency for 100% skin depth
0000 (4/0)	0.46	11.684	107	0.049	0.16072	302	125 Hz
000 (3/0)	0.4096	10.40384	85	0.0618	0.202704	239	160 Hz
00 (2/0)	0.3648	9.26592	67.4	0.0779	0.255512	190	200 Hz
0 (1/0)	0.3249	8.25246	53.5	0.0983	0.322424	150	250 Hz
1	0.2893	7.34822	42.4	0.1239	0.406392	119	325 Hz
2	0.2576	6.54304	33.6	0.1563	0.512664	94	410 Hz
3	0.2294	5.82676	26.7	0.197	0.64616	75	500 Hz
4	0.2043	5.18922	21.2	0.2485	0.81508	60	650 Hz
5	0.1819	4.62026	16.8	0.3133	1.027624	47	810 Hz
6	0.162	4.1148	13.3	0.3951	1.295928	37	1100 Hz
7	0.1443	3.66522	10.5	0.4982	1.634096	30	1300 Hz
8	0.1285	3.2639	8.37	0.6282	2.060496	24	1650 Hz
9	0.1144	2.90576	6.63	0.7921	2.598088	19	2050 Hz
10	0.1019	2.58826	5.26	0.9989	3.276392	15	2600 Hz
11	0.0907	2.30378	4.17	1.26	4.1328	12	3200 Hz
12	0.0808	2.05232	3.31	1.588	5.20864	9.3	4150 Hz
13	0.072	1.8288	2.62	2.003	6.56984	7.4	5300 Hz
14	0.0641	1.62814	2.08	2.525	8.282	5.9	6700 Hz
15	0.0571	1.45034	1.65	3.184	10.44352	4.7	8250 Hz
16	0.0508	1.29032	1.31	4.016	13.17248	3.7	11 kHz
17	0.0453	1.15062	1.04	5.064	16.60992	2.9	13 kHz
18	0.0403	1.02362	0.823	6.385	20.9428	2.3	17 kHz
19	0.0359	0.91186	0.653	8.051	26.40728	1.8	21 kHz
20	0.032	0.8128	0.518	10.15	33.292	1.5	27 kHz
21	0.0285	0.7239	0.41	12.8	41.984	1.2	33 kHz
22	0.0254	0.64516	0.326	16.14	52.9392	0.92	42 kHz
23	0.0226	0.57404	0.258	20.36	66.7808	0.729	53 kHz

Table 12.1: AWG Table

Fifth: Calculating the Number of Layers:

The vertical distance of the area subjected to the winding = D dimension = 21.6mm

The number of wires: Number of wires = $\frac{21.6 - 2}{8 * 0.57404} = 4.267995262$ wires ≈ 5 wires

Note: There will be a margin to prevent the presence of high voltage at the terminals in the case of E-core for example (The margin is between 1 mm and 2 mm).

$$\text{Number of Layers} = \frac{\text{Number of Turns}}{\text{Number of Wires}} = \frac{16}{5} = 3.2 \text{ Layers} \approx 4 \text{ Layers}$$

TYPE/SIZE	ORDERING CODE	DIMENSIONS (mm)							
		A	B	C	D	E	F	L	M
E 40/17/11	0_44011EC	40.0 ± 0.51	17.0 ± 0.31	10.69 ± 0.31	10.0 min	27.6 min	10.7 ± 0.31	5.99 ± 0.25	8.86 nom
E 42/21/9	0_44016EC	42.15 ± 0.85	21.1 ± 0.2	9.0 ± 0.25	14.9 min	29.5 min	11.95 ± 0.25	5.94 ± 0.13	8.9 ± 0.25
E 43/21/15	0_44020EC	43.0 +0/-1.7	21.0 ± 0.2	15.2 +0/-0.6	14.8 +0.6/-0	29.5 +1.4/-0	12.2 +0/-0.5	6.75 nom	8.65 nom
I 43/6/15	0_44020IC	43.0 +0/-1.7	5.9 ± 0.2	15.2 +0/-0.6					
E 43/21/20	0_44022EC	43.0 +0/-1.7	21.0 ± 0.2	20.0 +0/-0.8	14.8 +0.6/-0	29.5 +1.4/-0	12.2 +0/-0.5	6.75 nom	8.65 nom
E 42/33/20	0_44033EC	42.0 +1/-0.7	32.8 +0/-0.4	20.0 +1/-0.8	26.0 +1/-0	29.5 +1.4/-0	12.2 +0/-0.5	5.98 ref	9.13 ref
E 41/17/12	0_44317EC	40.6 ± 0.65	16.6 ± 0.2	12.4 ± 0.3	10.4 min	28.6 min	12.45 ± 0.25	6.33 max	7.95 min
E 47/20/16	0_44721EC	46.9 ± 0.8	19.6 ± 0.2	15.6 ± 0.25	12.1 min	32.4 ± 0.65	15.6 ± 0.25	7.54 nom	7.87 min
E 56/28/21	0_45528EC	56.2 +0/-2.1	27.5 ± 0.3	21.0 +0/-0.8	18.5 +0.8/-0	37.5 +1.5/-0	17.2 +0/-0.5	9.35 ref	10.15 ref
E 56/28/25	0_45530EC	56.2 +0/-2.1	27.6 ± 0.38	24.61 ± 0.38	18.5 min	37.5 min	17.2 +0/-0.5	9.35 ref	10.15 ref
E 56/24/19	0_45724EC	56.1 ± 1	23.6 ± 0.25	18.8 ± 0.25	14.6 ± 0.13	38.1 min	18.8 ± 0.25	9.5 nom	9.03 nom
E 60/22/16	0_46016EC	59.99 ± 0.78	22.3 ± 0.3	15.62 ± 0.38	13.8 min	44.0 min	15.62 ± 0.38	7.7 ± 0.25	14.49 ± 0.25
E 60/31/22	0_46022EC	60.3 ± 0.9	30.6 ± 0.3	22.3 ± 0.38	21.6 ± 0.3	42.3 ± 0.78	18.1 ± 0.25	9.0 ref	12.1 ref
E 65/32/27	0_46527EC	65.0 +1.5/-1.2	32.8 +0/-0.6	27.4 +0/-0.8	22.0 +0.8/-0	44.2 +1.8/-0	20.0 +0/-0.7	9.95 ref	12.72 ref
E 70/33/32	0_47133EC	70.5 ± 1	33.2 +0/-0.5	32.0 +0/-0.8	21.9 +0.7/-0	48.0 +1.5/-0	22.0 +0/-0.7	11.25 nom	13.0 nom
E 72/28/19	0_47228EC	72.4 ± 0.76	27.9 ± 0.33	19.0 ± 0.33	17.8 min	52.6 min	19.0 ± 0.38	9.53 ± 0.38	16.9 min
E 80/38/20	0_48020EC	80.0 ± 1.6	38.1 ± 0.3	19.8 ± 0.4	28.2 ± 0.3	59.1 min	19.8 ± 0.4	11.25 nom	19.45 min
E 100/59/27	0_49928EC	100.3 ± 2.0	59.4 ± 0.47	27.5 ± 0.5	46.85 ± 0.38	72.0 min	27.5 ± 0.5	13.75 ± 0.38	22.65 ± 0.5

Table 12.2: Core Dimension

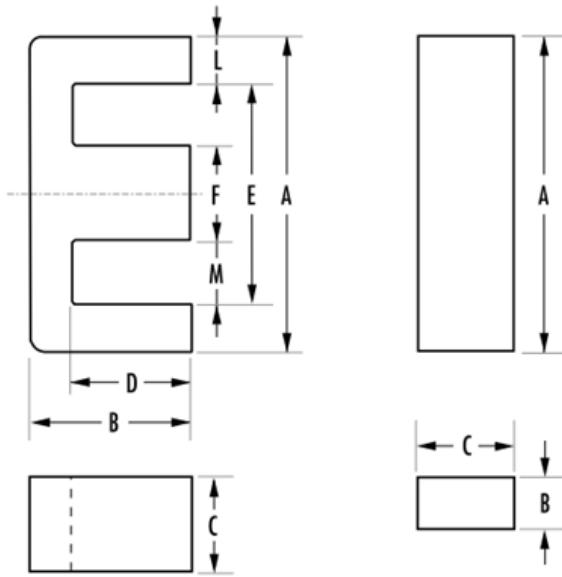
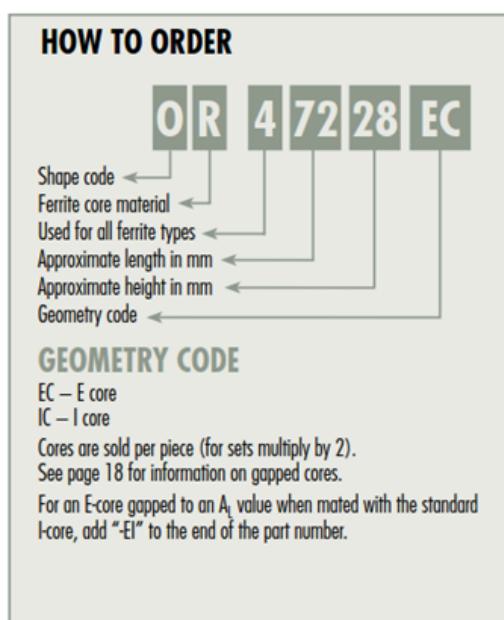


Figure 12.8: Core OR47228EC

Sixth: Calculating the Length of Wire:

Length of Wire = Number of Turns * Length of Complete Turn + Additional 10 or 20 cm (according to design) for the terminals = $16 * (2 * c + 2 * F) + 10 * 10$

$$\begin{aligned} &= 16 * [2 * (22.3 + 0.38) + 2 * (18.1 + 0.25)] + 100 \\ &= 1412.96 \text{ mm} \\ &= 1.41296 \text{ m} \end{aligned}$$

Checking the Voltage Drop mentioned in **Fourth** is done by

$$\begin{array}{rcl} 66.7808 & \text{-----} & 1000 \text{ m} \\ ? & \text{-----} & 1.41296 \end{array}$$

Therefore $R = \frac{66.7808 * 1.41296}{1000} = 0.09435859912 \text{ ohm}$

Therefore $V.D = I_p * R = 5.25 * 0.09435859912 = 0.495382656 \text{ V} \approx 0.5\text{V}$

Voltage Drop % = $\frac{0.5}{200} * 100 = 0.25\% < (5\%)$

Therefore, this voltage drop is **accepted**.

After that, the Secondary Side:

Many steps are the same as those done in Primary Side but with some differences.

Calculating Number of Turns:

From the relation: $\frac{V_p}{V_s} = \frac{N_p}{N_s}$

$$N_s = \frac{N_p * V_s}{V_p} = \frac{16 * 200}{200} = 16 \text{ turns (Same as primary)}$$

$$I_s = \frac{P_s}{V_s} = \frac{P_o}{V_o} = \frac{1000}{200} = 5\text{A}$$

From AWG Table: $I_s = 5\text{A}$ (I_{\max}). However, for 50KHz or 53KHz, the maximum current is 0.729A. So, parallel wires or bundling will be used:

$$\text{Number of parallel wires} = \frac{I_s}{I_{\max}} = \frac{5}{0.729} = 6.858710562 \text{ wires} \approx 7 \text{ wires}$$

The wire used in both primary and secondary is: **AWG 23, 0.57404mm, 0.729A, 53KHz**

- The vertical distance of the area subjected to the winding = D dimension = 21.6mm
- The number of wires: Number of wires = $\frac{21.6 - 2}{7 * 0.57404} = 4.87770887 \text{ wires} \approx 5 \text{ wires}$

Note: There will be a margin to prevent the presence of high voltage at the terminals in the case of E-core for example (The margin is between 1 mm and 2 mm).

- Number of Layers = $\frac{\text{Number of Turns}}{\text{Number of Wires}} = \frac{16}{5} = 3.2 \text{ Layers} \approx 4 \text{ Layers}$

- Length of Wire = Number of Turns * Length of Complete Turn + Additional 10 or 20 cm (according to design) for the terminals = $16 * (2 * c + 2 * F) + 10 * 10$
 $= 16 * [2 * (22.3 + 0.38) + 2 * (18.1 + 0.25)] + 100$
 $= 1412.96 \text{ mm}$
 $= 1.41296 \text{ m}$

- No need to check for voltage drop because $I_s < I_p$ so voltage drop for I_s is less than that of I_p

Same steps will be done for another high ratings:

Givens:

Switching Frequency = 100KHz

Input and Output Voltage = 800 V

Output Power = 10Kw = 10000 watt

Results for both high and low ratings:

<i>POC</i>	<i>Low Rating</i>	<i>High Rating</i>
Core Type and Material	EI Ferrite (P-Material) 46022 EE or 46022 EC	EI Ferrite (P-Material) 49928EE or 49928EC
Effective Area of Core	402 mm ²	738 mm ²
Core Dimension	60/31/22	100/59/27
Number of Turns	16 Turns	26 Turns
Diameter of Wire for Both Sides	0.57404 mm	0.40386 mm
Number of Parallel Wires in Primary Side	8	37
Number of Parallel Wires in Secondary Side	7	34
Number of Layers in Primary Side	4	9
Number of Layers in Secondary Side	4	7
Length of Wire	1.41296 m	3.012 m

Table 12.3: Comparison Between the Results for High and Low Rating

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