Si474x Antenna, Schematic, Layout, and Design Guidelines

1. Introduction

This document provides general Si474x design guidelines and AM/LW/SW/FM/WB antenna selections, which include schematic, BOM, layout, and design checklist.

Users should follow the Si474x design guidelines presented in Section “2. Si474x 4x4 mm QFN Schematic and Layout” and proceed to the appropriate antenna selections according to the application and device used presented in Sections 3 through 6.

Table 1. Supported Devices and Antennas

P/N	General Description	Function				FM Antenna	WB Antenna	AM/LW/SW Antenna
		FM Receiver	AM Receiver	SW/LW Receiver	WB Receiver	Whip	Whip	Whip
Si4740	High-Performance AM/FM Receiver	✓	✓			✓		AM/LW
Si4741	High-Performance AM/FM Receiver with RDS	✓	✓			✓		AM/LW
Si4742	High-Performance AM/LW/SW/FM/WB Receiver	✓	✓	✓	✓	✓	✓	✓
Si4743	High-Performance AM/LW/SW/FM/WB Receiver with RDS	✓	✓	✓	✓	✓	✓	✓
Si4744	High-Performance AM/LW/SW/FM Receiver	✓	✓	✓		✓		✓
Si4745	High-Performance AM/LW/SW/FM Receiver with RDS	✓	✓	✓		✓		✓
Si4749	High-Performance RDS-only Receiver	✓				✓		

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2. Si474x 4x4 mm QFN Schematic and Layout

This section describes the minimum schematic and layout options required for optimal Si474x performance. Population options are provided to support layouts for different audio output options and mitigation of system noise.

2.1. Si474x 4x4 mm Design

C1 (22 nF) is a required bypass capacitor for VDD supply pin 13. Place C1 as close as possible to VDD pin 13 and GND pin 14. Place a VIA connecting C1 VDD supply to the power rail such that the cap is closer to the Si474x than the VIA. Route C1 GND directly and only to GND pin 14 with a wide, low-inductance trace. These recommendations are made to reduce the size of the current loop created by the bypass cap and routing, minimize bypass cap impedance, and return all currents to the GND pad.

C13 (22 nF), C17 (100 µF), and C19 (0.1 µF) are optional bypass capacitors for the VIO supply pin 12 and may be placed to mitigate supply noise. Place C13, C17, and C19 as close as possible to the VIO pin 12 and the GND pin 14. Place VIAs connecting C13, C17, and C19 VIO supply to the power rail such that the capacitors are closer to the Si474x than the VIAs. Route C13, C17, and C19 GND directly and only to GND pin 14 with wide, low-inductance traces. These recommendations are made to reduce the size of the current loop created by the bypass capacitors and routing, minimize bypass cap impedance, and return all currents to the GND pad.

C2 (2 pF) is a required shunt capacitor from the DFS pin to ground when using digital audio output (Si4741/43/45 only), and is used to prevent degradation of audio quality. Place the capacitor as close as possible to the DFS pin.

C6 (0.1 µF) and C18 (100 µF) are optional bypass capacitors to mitigate system noise in AM and FM frequencies. Route them the same way as C1.

C8 and C9 (0.39 µF) are ac coupling capacitors for analog audio output from ROUT pin 15 and LOUT pin 16. The input resistance of the amplifier and the capacitor will set the high-pass pole given by Equation 1. Placement location is not critical.

$$f_c = \frac{1}{2\pi RC}$$

Equation 1. High-Pass Pole Calculation

R12, R14, R26, R29, and R30 (25 Ω to 2 kΩ) are optional series termination resistors used to mitigate system noise. The recommended value of the resistors is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place the series termination resistors, R12, R14, R21, R24, R26, R29, and R30, as close to the host controller as possible.

R21 and R24 (25 Ω to 2 kΩ) are optional series termination resistors used to mitigate system noise. The recommended value of the resistors is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place the series termination resistors, R21 and R24 as close to the chip input as possible.

R17 and R20 (22 kΩ) are optional pull-up resistors for the RSTB and SENB lines. The size of pull-up resistor value will vary based on the number of devices, capacitance, and speed of the bus. Placement location is not critical.

R27 and R28 (22 kΩ) are optional pull-up resistors for the SCLK and SDIO lines required only when using an I2C bus. The size of pull-up resistor value will vary based on the number of devices, capacitance, and speed of the bus. Placement location is not critical. Refer to the I2C specification for additional design information.

R16 (25 Ω to 2 kΩ) is a required series termination resistor when using digital audio output (Si4741/43/45 only) and is used to mitigate noise from the digital data routed from DOUT pin 17. The recommended value of the resistor is 604 Ω for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R16 as close to pin 17 as possible.

R15 (25 Ω to 2 kΩ) is a required series termination resistor when using digital audio (Si4741/43/45 only) and is used to mitigate noise from the digital clock routed to GPO3/DCLK pin 19. The recommended value of the resistor is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R15 as close to the host controller as possible. Choosing a DCLK frequency that is above the AM band reduces the chances of having DCLK harmonics that fall in the AM band and create digital noise.

R11 (25 Ω to 2 kΩ) is a required series termination resistor when using digital audio output (Si4741/43/45 only) and is used to mitigate noise from the digital frame clock routed to DFS pin 18. The recommended value of the resistor is 1.4 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R11 as close to the host controller as possible.

R22 and R23 (4.02 kΩ) are optional pull-up and pull-down resistors for the RCLK line to reduce the energy in harmonics of RCLK that might fall in the AM band. The recommended value is chosen such that RCLK will still meet the voltage requirements of Si474x. Place R22 and R23 as close as possible to RCLK pin 11. If the RCLK frequency is higher than the maximum frequency in the AM band, this will eliminate harmonics of RCLK that fall in the AM band. Refer to “AN332: Si47xx Programming Guide” and “AN344: Si4706/07/4x Programming Guide” for recommended RCLK and prescalar values.

R2 (24.3 kΩ) and R13 (4.53 kΩ) are optional pull-up and pull-down resistors for the DFS line when using digital audio output (Si4741/43/45 only.) They are used to reduce the energy in harmonics of DFS that might fall in the AM band. The recommended value is chosen such that DFS will still meet the voltage and timing requirements of I2S. Place R2 and R13 as close as possible to DFS pin 18.

2.2. Si474x 4x4 mm Schematic

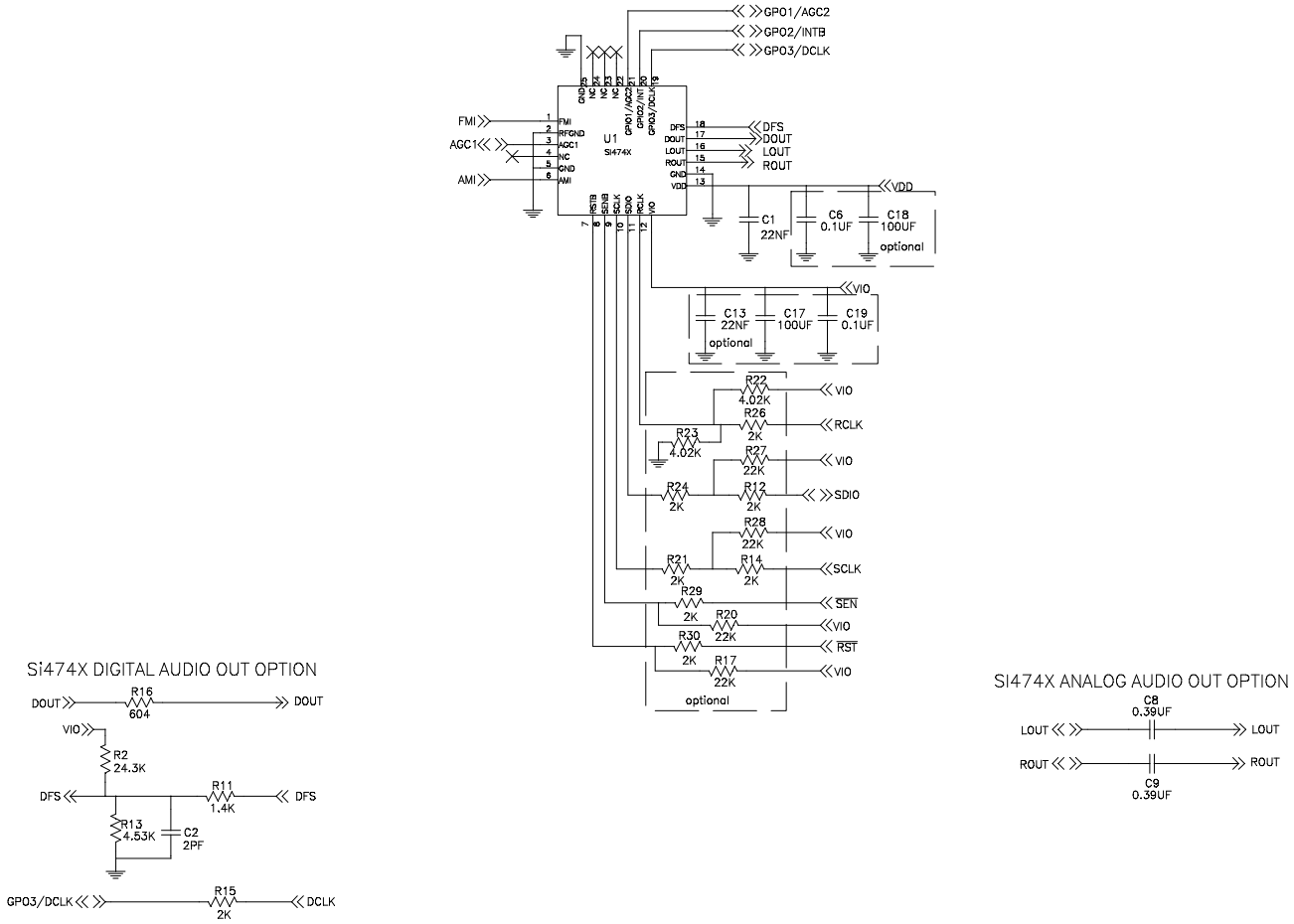


Figure 1. Si474x 4x4 mm QFN Schematic

2.3. Si474x 4x4 mm Bill of Materials

The required bill of materials for Figure 1 is shown in Table 2.

The optional bill of materials for Figure 1 is shown in Table 3.

Table 2. Required Bill of Materials

Designator	Description	Note
C1	VDD Supply bypass capacitor, 22 nF, 10%, Z5U/X7R	
C2	Shunt cap from DFS to gnd to prevent degradation of audio quality, 2 pF, COG, ±0.25 pF	For digital audio output (Si4741/43/45 only)
R11	DFS current limiting resistor, 25 Ω to 2 kΩ	For digital audio output (Si4741/43/45 only)
R15	DCLK current limiting resistor, 25 Ω to 2 kΩ	For digital audio output (Si4741/43/45 only)
R16	DOUT current limiting resistor, 604 Ω	For digital audio output (Si4741/43/45 only)
U1	Silicon Laboratories Si474x, 4 x 4 mm, 24-pin, QFN	

Table 3. Optional Bill of Materials

Designator	Description	Note
C6, C19	VDD and VIO Supply bypass capacitors, 0.1 µF, 10%, X7R/X5R	For supply noise mitigation
C13	VIO Supply bypass capacitor, 22 nF, 10%, X7R/X5R	For supply noise mitigation
C17, C18	VIO and VDD Supply bypass capacitors, 100 µF, 10%, X7R/X5R	For supply noise mitigation
C8, C9	AC coupling capacitor, 0.39 µF, X7R/X5R	For analog audio output
R12, R14, R21, R24, R26, R29, R30	Current limiting resistor, 25 Ω to 2 kΩ	For digital system noise mitigation
R27, R28	Pull-up resistor, 22 kΩ	For I2C bus mode communication
R17, R20	Pull-up resistor, 22 kΩ	For control bus communication
R22, R23	Pull-up/Pull-down resistors, 4.02 kΩ	For reducing energy in RCLK harmonics
R2	Pull-up resistor, 24.3 kΩ	For reducing energy in DFS harmonics
R13	Pull-down resistor, 4.53 kΩ	For reducing energy in DFS harmonics

2.4. Si474x 4x4 mm Layout

The following layout example selector guide provides guidance for selecting the proper example based on audio options.

Table 4. Layout Example Selector Guide by Option

Feature	Layout Example	
	1	2
Analog Output	X	X
Digital Output		X

The following layout rules are used:

- Layer 1 top side placement and routing (shown)
- Layer 2 GND
- Power routed by trace (not shown)
- 0402 component size or larger
- 12 mil traces for power, 8 mil traces for all other signals
- 8 mil trace spacing
- 15 mil component spacing

Figure 2 shows critical component layout with top side placement, top and bottom side routing, and analog output support. In this example, a 2-layer board is used where components are all placed on the top side. RF signals are routed on the top layer, and digital lines are routed on the bottom layer. As an example, only two of the capacitors on each supply pin are shown.

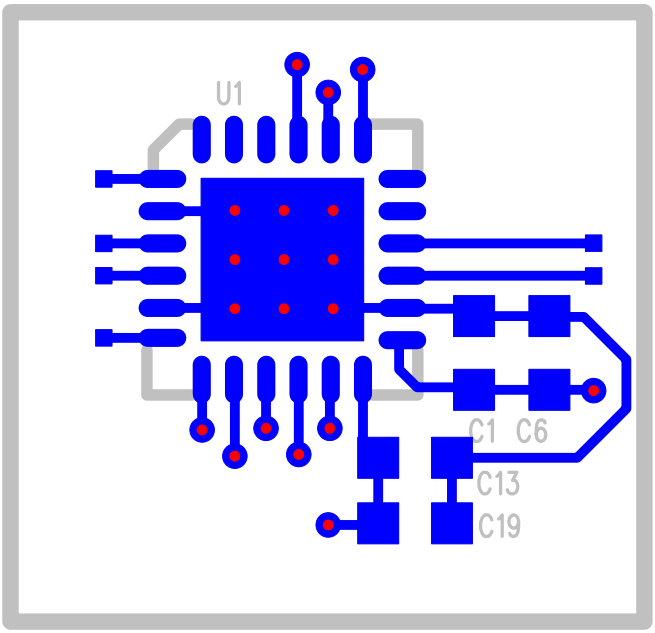


Figure 2. Layout Example 1

Figure 3 shows critical component layout with top side placement, top and bottom side routing, analog and digital output support. Layout example 2 shares the same placement and routing as the first example and adds digital audio support. Digital lines are routed to the bottom side through vias. These vias are placed as close as possible to the digital pins.

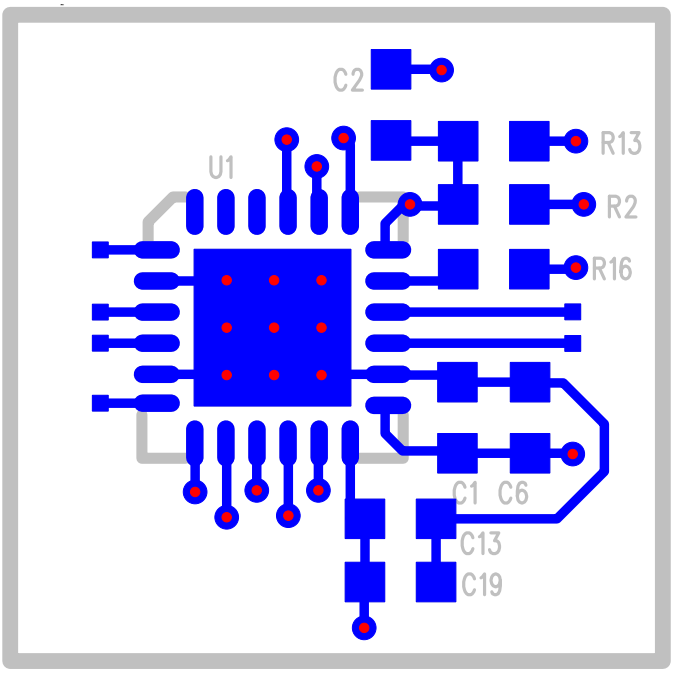


Figure 3. Layout Example 2

Place a ground plane under the Si474x as shown in Figure 4. For designs in which a continuous ground plane is not possible, place a local ground plane directly under the Si474x. Do not route signal traces on the ground layer under the Si474x. Flood the primary layer with ground, and place stitching VIAs to create a low-impedance connection between planes. If the design is sufficiently flexible to have more than two layers, put the GND plane between RF signals and digital signals. Another improvement would be to put the digital signals between two GND planes.

Do not route digital or RF traces over breaks in the ground plane. Route all traces to minimize inductive and capacitive coupling by keeping digital traces away from analog and RF traces, minimizing trace length, minimizing parallel trace runs, and keeping current loops small. In particular, care should be taken to avoid routing digital signals or reference clock traces near or parallel to VCO pins 22 and 23 or LOUT/ROUT pins 15 and 16. Route digital traces on the opposite side of the chip. This means that, for a two-sided board, all RF signals should be routed on layer 1, and all digital signals should be routed on layer 2.

Route digital traces including I2C and digital audio away and orthogonal to the RF traces to avoid coupling of digital noise to RF traces. This is especially important for the AM band where digital noise frequencies can easily occur.

Route all GND (including RFGND) pins to the ground pad. The ground pad should be connected to the ground plane using multiple vias to minimize ground potential differences.

Route power to the Si474x by trace, ensuring that each trace is rated to handle the required current. Some trace impedance is preferable so that the decoupling currents are forced to flow through decoupling caps C1, C6, C13, C17, C18, and C19 directly to the ground pins and not by alternate pathways.

Place the Si474x close to the antenna(s) to minimize antenna trace length and capacitance and inductive and capacitive coupling. This recommendation must be followed for optimal device performance. Route the antenna trace over an unobstructed ground plane to minimize antenna loop area and inductive coupling. Design, place, and route other circuits such that radiation in the band of interest is minimized.

Figure 4. Two-Layer Stackup

2.5. Si474x 4x4 mm Design Checklist

The following design checklist summarizes the guidelines presented in this section:

- ☐ Place bypass caps C1, C6, and C18 (for VDD) and C13, C17, and C19 (for VIO) as close as possible to the supply and ground pins.
- ☐ Place a VIA connecting C1, C6, and C18 (for VDD) and C13, C17, and C19 (for VIO) such that the cap is between the Si47xx and the VIA.
- ☐ Route a wide, low-inductance return current path from the C1, C6, C13, C17, C18, and C19 to the Si47xx GND pins.
- ☐ Place resistor R16 as close to DOUT pin 17 as possible.
- ☐ Place the series termination resistors, R12, R14, R21, R24, R26, R29, and R30 as close to the host controller as possible.
- ☐ Place the pull-up/pull-down resistors, R2, R13, R22, and R23, as close to the DFS (pin 18) and RCLK (pin 11) as possible.
- ☐ Place shunt cap C2 from DFS to gnd and as close to DFS (pin 18) as possible.
- ☐ Place a ground plane under the device as shown in Figure 4, “Two-Layer Stackup”.
- ☐ Place a local ground plane directly under the device for designs in which a continuous ground plane is not possible.
- ☐ Route all traces to minimize inductive and capacitive coupling by keeping digital traces away from analog and RF traces, minimizing trace length, minimizing parallel trace runs, and keeping current loops small.
- ☐ Route digital traces on the opposite side of the chip. Place stitching VIAs around digital traces to minimize current loop areas.
- ☐ Route digital traces RSTb, SENb, SCLK, SDIO, RCLK, DOUT, DFS, and DCLK away from and orthogonal to RF traces to minimize digital noise coupling onto RF traces.
- ☐ Choose DCLK and RCLK frequencies that fall above the AM band. Ensure that timing requirements are met for both RCLK and DCLK with higher frequencies. Refer to “AN332: Si47xx Programming Guide” for timing requirements.
- ☐ Route all GND (including RFGND) pins to the ground pad. The ground pad should be connected to the ground plane using multiple VIAs to minimize ground potential differences.
- ☐ Route power to the Si474x by trace, ensuring that each trace is rated to handle the required current.
- ☐ Do not route signal traces on the ground layer directly under the Si474x.
- ☐ Do not route signal traces under the Si474x without a ground plane between the Si474x and signal trace.
- ☐ Do not route digital or RF traces over breaks in the ground plane.
- ☐ If the design is flexible to have more than two layers, put the GND plane between RF signals and digital signals. Another improvement would be to put the digital signals between two GND planes.
- ☐ Do not route digital signals or reference clock traces near VCO pins 22 and 23 or LOUT/ROUT output pins 15 and 16.
- ☐ Do not route VCO pins 22 and 23 (NC). These pins must be left floating to guarantee proper operation.
- ☐ Do not route pin 24 (NC). This pin must be left floating to guarantee proper operation.
- ☐ Do not route pin 4 (NC). This pin must be left floating to guarantee proper operation.
- ☐ Flood the primary and secondary layers with ground and place stitching VIAs.
- ☐ Place the Si474x close to the antenna(s) to minimize antenna trace length and capacitance and inductive and capacitive coupling. This recommendation must be followed for optimal device performance.
- ☐ Route the antenna trace over an unobstructed ground plane to minimize antenna loop area and inductive coupling.
- ☐ Design, Place, and Route other circuits such that radiation in the band of interest is minimized.
- ☐ Tie unused pin(s) to GND, but do not tie No Connect (NC) or unused GPO pins to GND.

3. Whip Antenna for FM/WB Receiver (Si4740/41/42/43/44/45 Only)

A whip antenna is a typical monopole antenna used in AM/LW/SW/FM/WB/RDS receivers. The AM/LW application is covered in Section "5. Whip Antenna for AM/LW Receiver (Si4740/41/42/43/44/45 Only)" on page 15. The AM/LW/SW application is covered in "6. Whip Antenna for AM/LW/SW Receiver (Si4742/43/44/45 only)" on page 18. The whip antenna for FM is also used for Si4749. The front-end circuits differ considerably between Si4740-43 and Si4749; so, the whip antenna for Si4749 will be covered in Section "4. Whip Antenna for RDS Receiver (Si4749 Only)" on page 13.

3.1. FM/WB Whip Antenna Design

A whip antenna is a monopole antenna with a stiff but flexible wire mounted vertically and one end adjacent to the ground plane.

There are various types of whip antennas including long, non-telescopic metal whip antennas, telescopic metal whip antennas, and rubber whip antennas. Figure 5 shows the telescopic whip antenna.

Figure 5. Typical Telescopic Whip Antenna Application

The whip antenna is capacitive, and its output capacitance depends on the length of the antenna (maximum length ~56 cm). At 56 cm length, the capacitance of the whip antenna ranges from 18 to 32 pF for the U.S. FM band. The antenna capacitance is about 22 pF in the center of the U.S. FM band (98 MHz).

3.2. FM/WB Whip Antenna Schematic

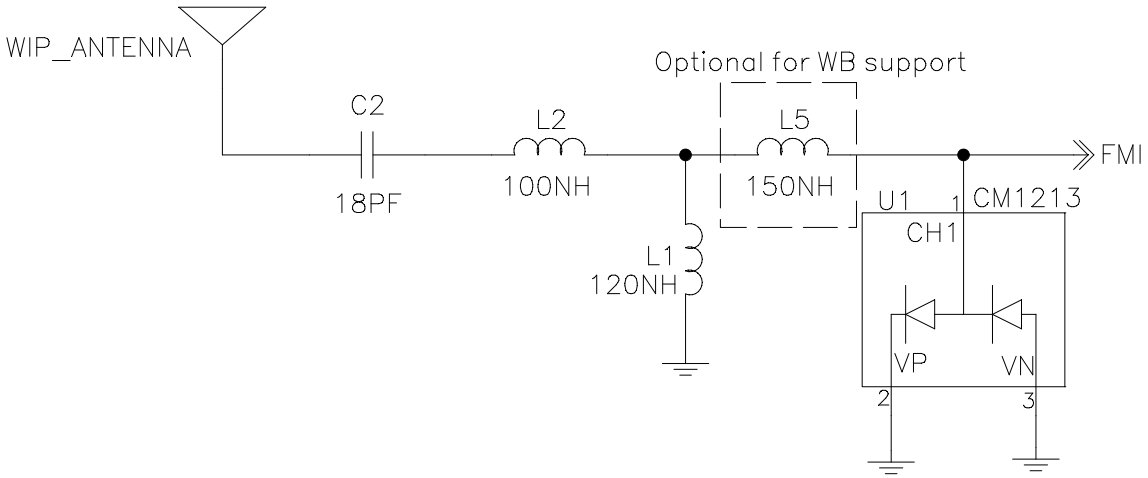


Figure 6. FM/WB Whip Antenna Schematic

C2 (18 pF) is the ac coupling capacitor going to the FMI pin.

L2 (100 nH), L1 (120 nH), and L5 (150 nH) are the tuning inductors that provide dual peaking for FM and Weather band. These inductors, together with the whip antenna capacitance (~22 pF at the center of FM band), 18 pF ac coupling cap (C2), and 5 pF typical FMI pin input capacitance (C_FMI), resonate in the FM band as well as Weather band. If either of the capacitance values changes, the inductor values have to be adjusted to achieve peaking in both bands (desired peaking at 100 MHz and 162 MHz). The equivalent schematic model is shown below. Si4740/41/44/45 do not support weather band. L5 can be replaced by a 0 Ω resistor, and the value of L2 can be changed to 33 nH to support FM band only for Si4740/41/44/45.

U1 is a required ESD diode since the antenna is exposed. The diode should be chosen with no more than 1 pF parasitic capacitance, such as the California Micro Device CM1213.

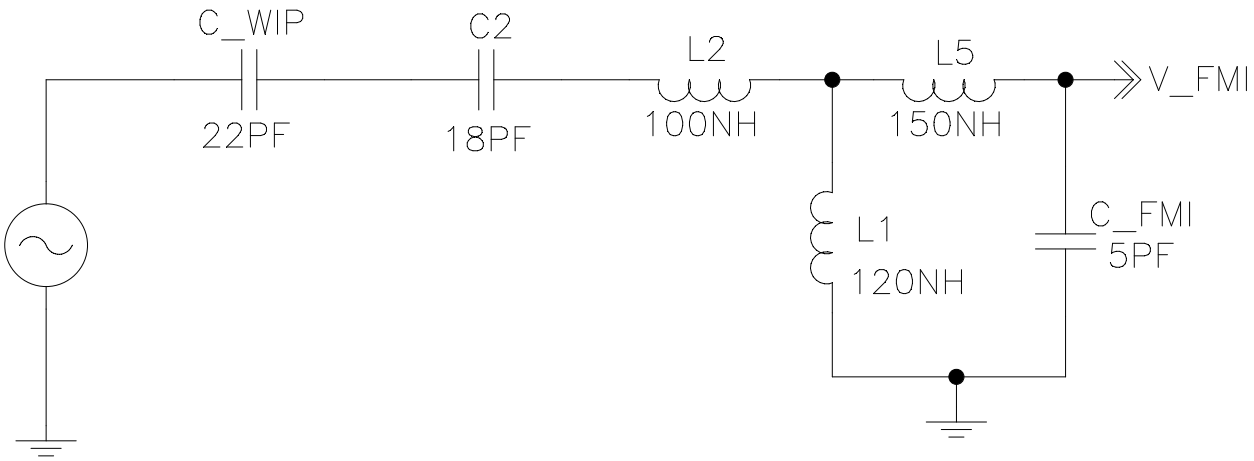


Figure 7. FM/WB Whip Antenna Schematic Model

3.3. FM/WB Whip Antenna Bill of Materials

Table 5. FM/WB Whip Antenna Bill of Materials

Designator	Description
WIP_ANTENNA	Whip antenna
C2	Capacitor, 18 pF, 5%, COG
L1	Inductor, 0603, SM, 120 nH, MURATA, LQW18ANR12J00D
L2	Inductor, 0603, SM, 100 nH, MURATA, LQW18ANR10J00D
L5	Inductor, 0603, SM, 150 nH, MURATA, LQW18ANR15J00D
U2	IC, SM, ESD DIODE, SOT23-3, California Micro Devices, CM1213-01ST

3.4. FM/WB Whip Antenna Layout

Place the chip as close as possible to the whip antenna. This will minimize the trace length between the device and whip antenna, which, in turn, will minimize parasitic capacitance and the possibility of noise coupling. Place inductors L1, L2, and L5 and the antenna connector together and as far from potential noise sources as possible and away from the I/O signals of the Si474x. ESD diode is placed near the FMI pin in order to prevent strong input signals from clipping by the diode.

3.5. FM/WB Whip Antenna Design Checklist

- ☐ Maximize whip antenna length for optimal performance.
- ☐ Select L1, L2, and L5 inductor values to maximize signal strength across the FM and weather band.
- ☐ Place L1, L2, L5, and the whip antenna close together and as far from potential noise sources as possible to reduce capacitive and inductive coupling.
- ☐ Place the chip as close as possible to the whip antenna to minimize the antenna trace length. This reduces parasitic capacitance and hence reduces coupling into the antenna by noise sources. This recommendation must be followed for optimal device performance.
- ☐ Select ESD diode U1 with minimum capacitance.
- ☐ Place the ac coupling capacitor, C2, as close to the FMI pin as possible.

4. Whip Antenna for RDS Receiver (Si4749 Only)

4.1. Whip Antenna Schematic for RDS Receiver

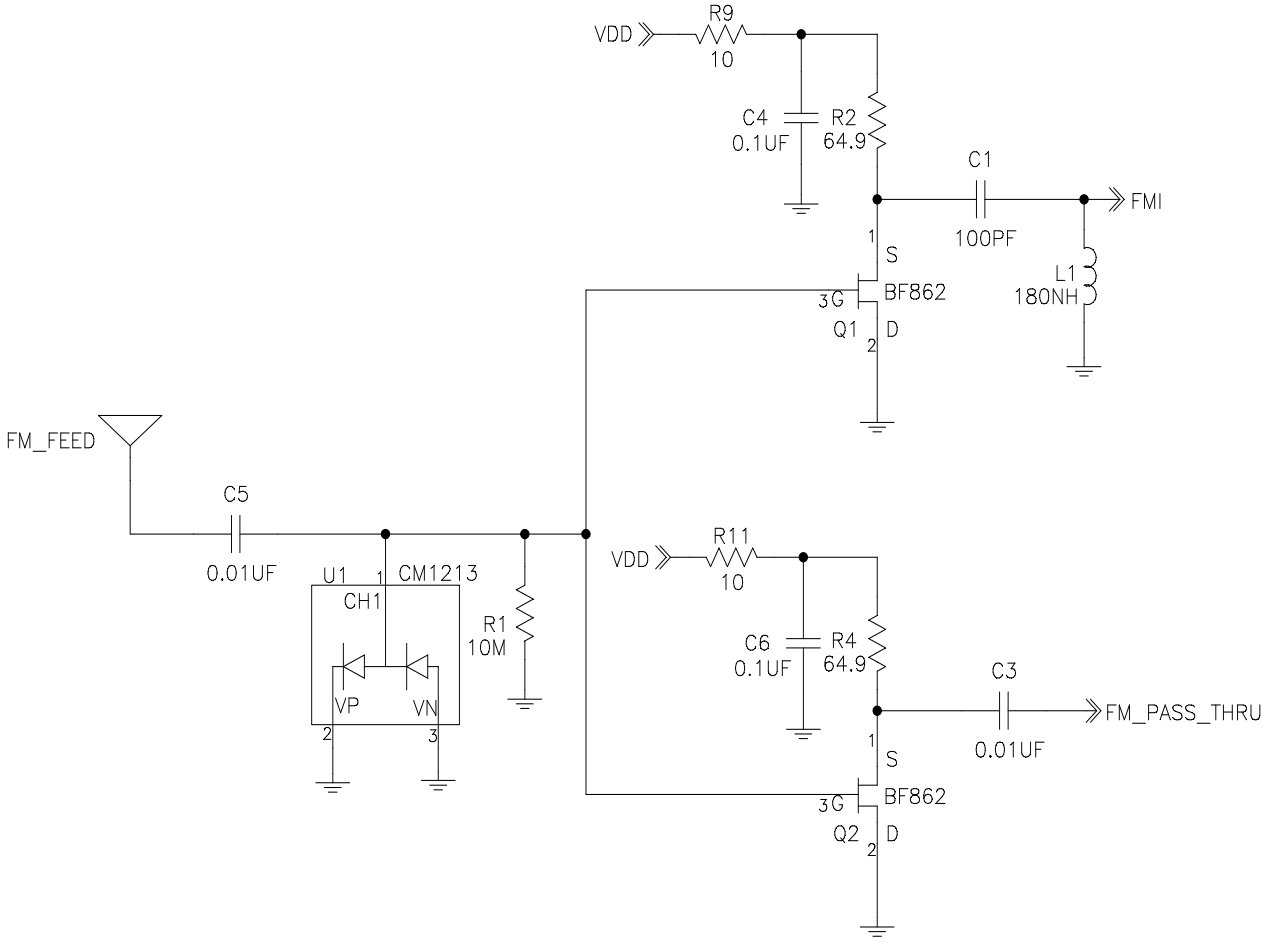


Figure 8. Whip Antenna Schematic for RDS Receiver

Si4749 is used as an RDS companion tuner. Customers will have another tuner in their design that will act as the main tuner for AM and FM. In most of these applications, the same antenna is used to feed AM and FM inputs. Figure 8 assumes that the customer has already split the antenna feed for AM and FM; so, it only demonstrates the circuit necessary for FM inputs to the main tuner and Si4749.

An active splitter circuit is used to isolate the two tuner front-ends that are fed by the same antenna feed. FM pass-through connection is intended to feed the FM input of the main tuner.

U1 is a required ESD diode since the antenna is exposed. A diode with no more than 1 pF parasitic capacitance should be chosen, such as the California Micro Devices CM1213.

Q1, Q2, R1, R2, and R4 make up the splitter circuit. R2 and R4 values can be changed to achieve more voltage gain in the FM band. This kind of circuit is needed to prevent any changes caused by each tuner's tracking filter or attenuators from affecting the other tuner's FM front-end.

Two filters, made up of R11/C6 and R9/C4, are needed to suppress any noise coupling through the power supply.

C1 (100 pF), C3 (0.01 µF), and C5 (0.01 µF) are the ac-coupling caps going to the FMI pin and the FM pass through connection.

L1 (180 nH) is the tuning inductor that combines with the antenna impedance and the FMI impedance to resonate in the FM band. Select an inductor with minimal dc resistance and a Q > 25 in the FM band.

4.2. Whip Antenna for RDS receiver Bill of Materials

Table 6. Whip Antenna for RDS Receiver Bill of Materials

Designator	Description
WIP_ANTENNA	Whip antenna
C1	Capacitor, 100 pF, COG
C3, C5	Capacitor, 0.01 µF, COG
C4, C6	Capacitor 0.1 µF, COG
R1	Resistor, 0603, SM, 10 MΩ
R2, R4	Resistor, 0402, SM, 64.9 Ω
R9, R11	Resistor, 0402, SM, 10 Ω
L1	Inductor, 0603, SM, 180 nH, MURATA, LQW18ANR18J00D
Q1, Q2	FET,SM,SOT-23, BF862
U1	IC, SM, ESD DIODE, SOT23-3, California Micro Devices, CM1213-01ST

4.3. Whip Antenna Layout for RDS Receiver

Place the chip as close as possible to the antenna feed. This will minimize the trace length between the device and whip antenna, which, in turn, will minimize parasitic capacitance and the possibility of noise coupling. Place the antenna connector as far from potential noise sources as possible and away from the I/O signals of the Si4749. Place ESD diode U1 as close as possible to the whip antenna input connector for maximum effectiveness.

4.4. Whip Antenna Design Checklist for RDS Receiver

- ☐ Maximize whip antenna length for optimal performance.
- ☐ Select matching inductor L1 with a Q of 25 or greater at 100 MHz and minimal dc resistance.
- ☐ Select the L1 inductor value to maximize signal strength across the FM band.
- ☐ Place the chip as close as possible to the whip antenna to minimize the antenna trace length. This reduces parasitic capacitance and hence reduces coupling into the antenna by noise sources. This recommendation must be followed for optimal device performance.
- ☐ Place ESD diode U1 as close as possible to the whip antenna for maximum effectiveness.
- ☐ Select ESD diode U1 with minimum capacitance.

5. Whip Antenna for AM/LW Receiver (Si4740/41/42/43/44/45 Only)

A whip antenna is a typical monopole antenna used in AM/LW/SW/FM/WB/RDS receivers. This section covers the whip antenna for AM/LW applications. See sections "3. Whip Antenna for FM/WB Receiver (Si4740/41/42/43/44/45 Only)" on page 10, "4. Whip Antenna for RDS Receiver (Si4749 Only)" on page 13, and "6. Whip Antenna for AM/LW/SW Receiver (Si4742/43/44/45 only)" on page 18.

5.1. AM/LW Whip Antenna Schematic

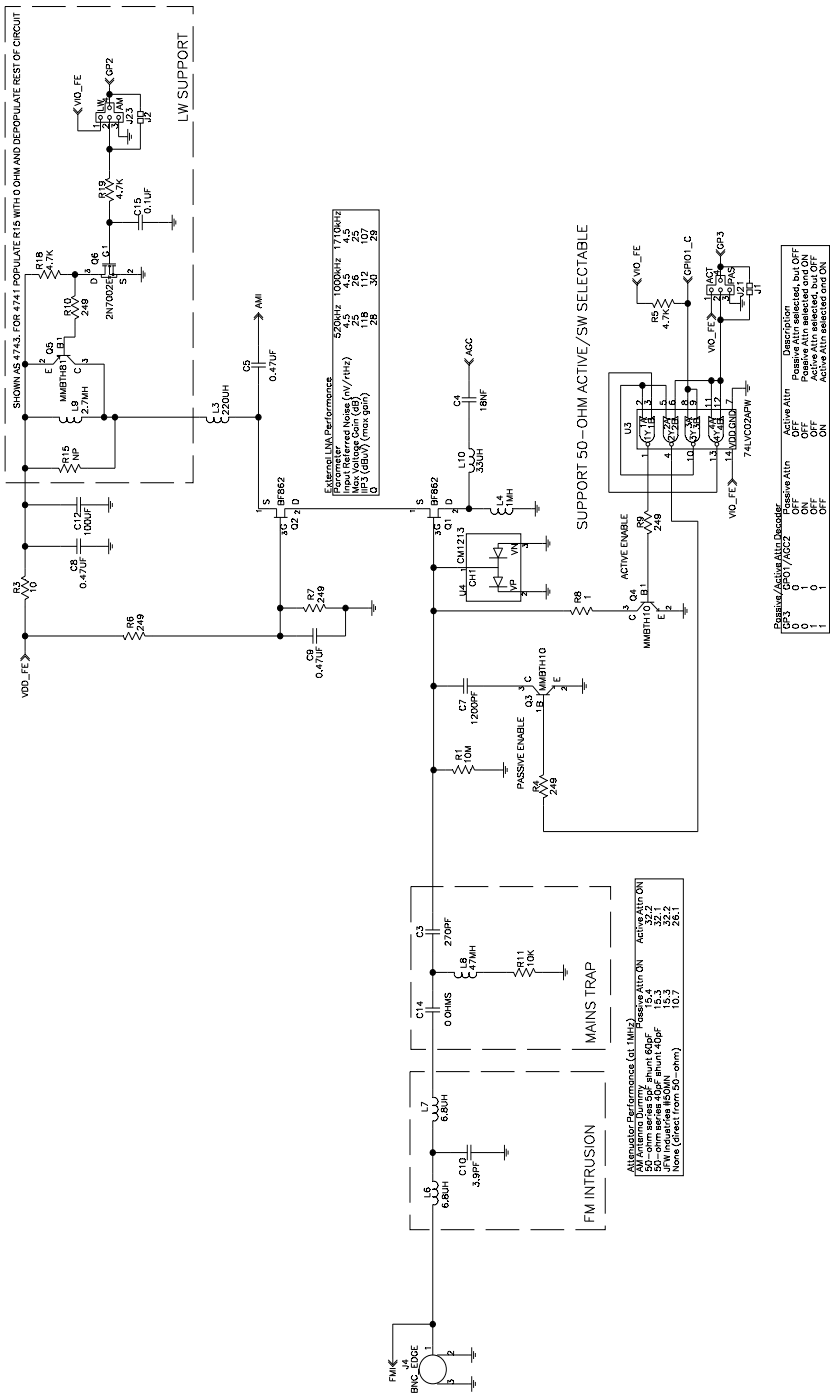


Figure 9. AM/LW Whip Antenna Schematic

L6 (6.8 µH), C10 (3.9 pF), and L7 (6.8 µH) function as a filter for the FM frequency.

C14 (0 Ω, currently not used), L8 (47 mH), and R13 (10 kΩ) act as a filter trap for the ac main line.

C3 (270 pF) provides dc isolation from the ac main line trap as well as a minimum capacitance (in series with the antenna capacitance) for the switched attenuator. This minimum capacitance improves the "Passive" attenuator performance with lower impedance sources (even a direct 50 Ω), and, if max signal with active source (50 Ω) is below ~95 dBµV, the "Active" attenuator option is no longer required.

R1 (10 MΩ) is the bias resistor for transistor Q1.

C7 (1200 pF) is used for the passive whip antenna by turning on Q3.

R8 (1 Ω) is used for the active whip antenna by turning on Q4. The R8 value is chosen to meet and exceed 40 dB SINAD at 120 dBµV AM input from an active (50 Ω) antenna. Different designs might have active antenna AGCs that keep the peak signal level below ~95 dBµV. In these cases, the passive-only option is adequate. If the design requirements are such that peak signal will be between 95 and 120 dBµV, R8 should be increased until the SINAD requirement at max signal level is met. The ATTN_BACKUP field in the AM_FRONTEND_AGC_CONTROL can then be optimized against the new value of R8 per the procedure described in AM_FRONTEND_AGC_CONTROL property in “AN344: Si4706/07/4x Programming Guide”.

Q3 and Q4 (MMBTH10), R4 and R9 (249 Ω) along with U3 (74LVC02) and R5 (4.7 kΩ) are the circuits to switch C7 for a passive whip antenna or R8 for an active whip antenna by using the GPIO1 signal.

U4 is a required ESD diode since the antenna is exposed. The diode should be chosen with no more than 1 pF of parasitic capacitance, such as the California Micro Devices CM1213.

Q1 and Q2 (BF862 N-FET transistors) are configured in a cascode architecture to amplify the input signal coming from the whip antenna.

L4 (1 mH) provides dc bias for the cascode amplifier and has a high impedance at AM/LW.

L10 (33 µH), C4 (18 nF), and Si474x AGC provide AM/LW gain control via cascode source degeneration.

R15 is Not Populated for the standard Si4743 board build that supports LW. Replace R15 with a 0 Ω resistor for the Si4741 board that does not have LW support.

L3 (220 µH) sets the gain of the amplifier along with the source degeneration load. L3, combined with the on-chip varactor, also functions as the AM tracking filter. Q > 55 at 1 MHz is required.

R6 (249 Ω), R7 (249 Ω), and C9 (0.47 µF) provide the bias voltage for the cascode transistor.

R3 (10 Ω), C8 (0.47 µF), and C12(100 µF) filter the power supply noise.

C5 (0.47 µF) is an ac-coupling capacitor going to the AMI pin.

L9 (2.7 mH) sets the gain of the amplifier along with the source degeneration load when the LW option is selected. L9, combined with the on-chip varactor, also functions as the LW tracking filter.

Q5 (MMBTH81 pnp transistor) is a transistor to bypass L9 if the dual AM or LW support option is selected.

R10 (249 Ω), R18 (4.7 kΩ), Q6 (2N7002 N-FET), C15 (0.1 µF), and R19 (4.7 kΩ) are circuits to drive the Q5 switch if the LW support option is selected.

5.2. AM/LW Whip Antenna Bill of Materials

Table 7. AM/LW Whip Antenna Bill of Materials

Designator	Description	Note
WIP_ANTENNA	Whip antenna	
L6	FM signal filter, 6.8 µH inductor, 0805PS-682KB	
C10	FM signal filter, 3.9 pF, COG capacitor	
L7	FM signal filter, 6.8 µH inductor, 0805PS-682KB	
C14	AC main line filter, 0 Ω (currently not used)	
L8	AC main line filter, 47 mH inductor, 388BN-1211Z	
R13	AC main line filter, 10 kΩ	
C3	AC main line filter, 270 pF, COG capacitor	
R1	Transistor bias resistor, 10 MΩ	
C7	Passive whip antenna load, 1200 pF, X7R, X5R capacitor	
R8	Active whip antenna load, 1 Ω resistor	
Q3, Q4	Passive/active whip antenna load switch, MMBTH10, NPN transistor	
R4, R9	Bias resistor to drive the transistor switch, 249 Ω	
U3	Logic driver, 74LVC02APW, 4 NOR gates	
R5	Pullup resistor, 4.7 kΩ	
U4	ESD protection diode, SOT23-3, California Micro Devices, CM1213-01ST	
Q1, Q2	N-FET in cascode architecture, BF862	
L4	Source degeneration load, 1 mH inductor, LPS4018-105ML	
L10	Source degeneration load, 33 µH, 1008PS-333KLB	
C4	Source degeneration load, 18 nF	
L3	Output load and part of tracking filter for AM. 220 µH, Q>55@1 MHz, 1008PS-224KLB	
C5	AC coupling capacitor, 0.47 µF	
R6, R7	Bias resistor, 249 Ω	
C9	Bypass cap for bias voltage, 0.47 µF	
R3	Resistor to filter VDD line, 10 Ω	
C8	Bypass cap, 0.47 µF, X7R/X5R capacitor	

Table 7. AM/LW Whip Antenna Bill of Materials (Continued)

Designator	Description	Note
C12	Bypass cap, 100 µF, X7R/X5R	
R15	0 Ω resistor, removed for dual AM/LW operation	Optional for LW
L9	Output load and part of tracking filter for LW. 2.7 mH inductor, RFB0807-272L	Optional for LW
Q5	Switch for AM/LW operation, MMBTH81	Optional for LW
R10	Bias resistor to drive the switch transistor, 249 Ω	Optional for LW
Q6	Driver transistor, N-FET, 2N7002	Optional for LW
R18	Bias resistor, 4.7 kΩ	Optional for LW
C15	Bypass cap, 0.1 µF, X7R/X5R capacitor	Optional for LW
R19	Bias resistor, 4.7 kΩ	Optional for LW

5.3. AM/LW Whip Antenna Layout

Place the LNA amplifier (Q1 and Q2) as close as possible to the whip antenna. This minimizes the trace length between the LNA and whip antenna, which, in turn, minimizes parasitic capacitance and the potential for noise coupling.

Place the chip as close to the LNA amplifier (Q2) as possible. This minimizes parasitic capacitance and the potential for noise coupling.

Place the Q3 collector directly next to C7, and place the Q4 collector directly next to R8.

5.4. AM/LW Whip Antenna Design Checklist

The following design checklist summarizes the guidelines presented in this section:

- ☐ Maximize whip antenna length for optimal performance.
- ☐ Place the LNA amplifier as close as possible to the whip antenna.
- ☐ Place the chip as close as possible to the LNA amplifier.
- ☐ Insure that AM signals are routed away/orthogonal (if possible) from the digital lines, RSTb, SENb, SCLK, SDIO, RCLK, GPO3/DCLK, DFS, and DOUT.

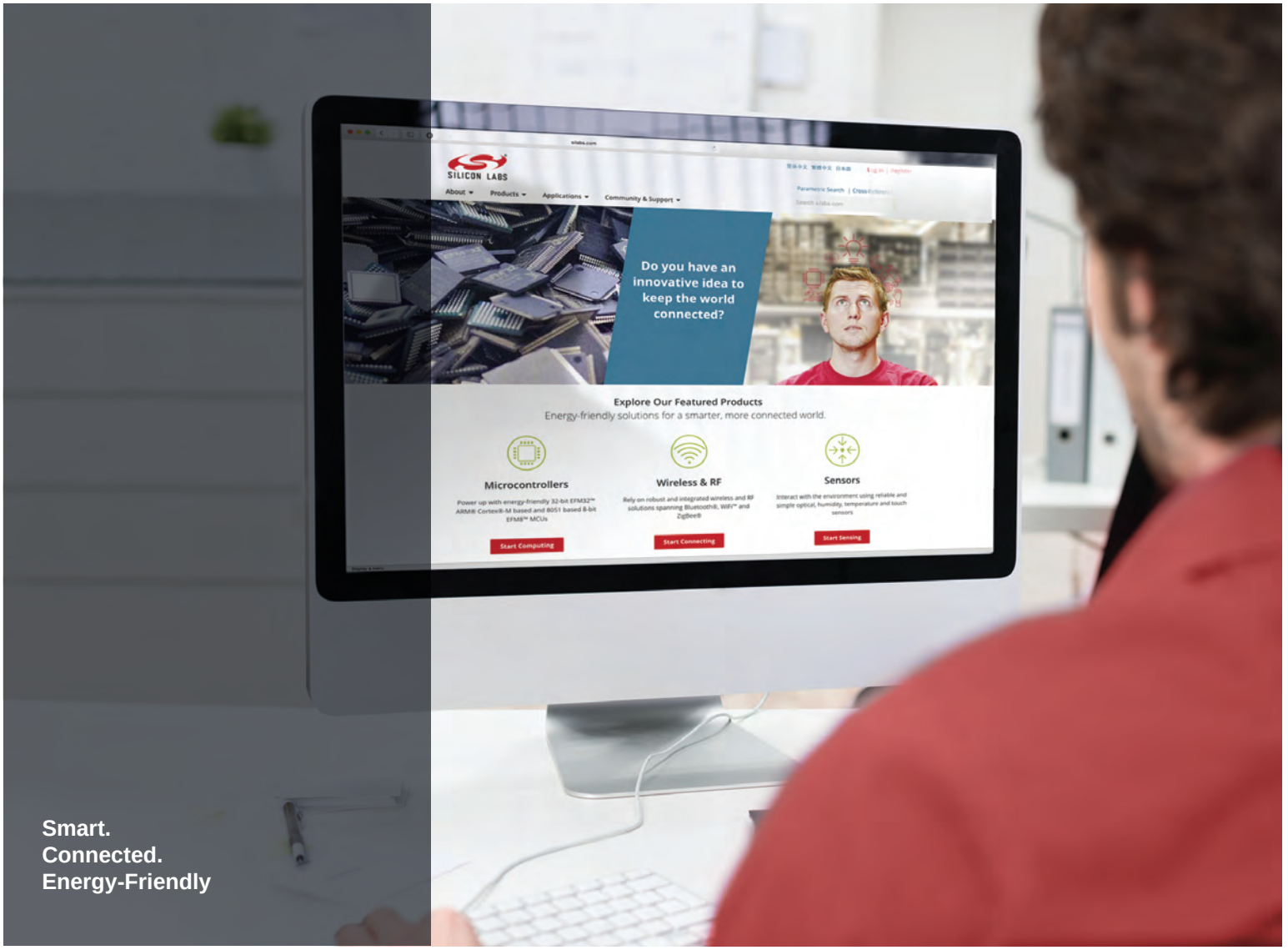
6. Whip Antenna for AM/LW/SW Receiver (Si4742/43/44/45 only)

Please contact Silicon Labs Application Support for the recommended schematic and antenna layout.

Document Change List

Revision 0.4 to Revision 0.5

- Updated Table 1, “Supported Devices and Antennas,” on page 1.
- Added Section “6. Whip Antenna for AM/LW/SW Receiver (Si4742/43/44/45 only)”.
- Made the schematic reference designators to be the same as the EVB schematic.
- Added shunt capacitor C2 from DFS to ground to prevent degradation of audio quality when in digital mode.
- Recommended values for R2, R13, R11,R16 changed.
- Recommended leaving unused GPO pins floating.



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