Some of the Big Ideas in Electronics

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There is a built-in potential across the junction:

$$\phi_0 = \phi_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$$

where ϕ_T is the thermal voltage

$$\phi_T = \frac{kT}{q} = 26\,\mathrm{mV} \qquad \text{at room temperature.}$$

9.2.1 Static behaviour: a simple model

Ideal diode equation

$$I_D = I_S(e^{V_D/\phi_T} - 1)$$

9.2.2 Dynamic, or transient, behaviour

9.2.2.1 Depletion-region capacitance

Abrupt junction

$$Q_j = A_D \sqrt{\left(2\epsilon_{si} q \frac{N_A N_D}{N_A + N_D}\right)(\phi_0 - V_D)}$$

Width

$$W_j = W_2 - W_1 = A_D \sqrt{\left(\frac{2\epsilon_{si}}{q} \frac{N_A + N_D}{N_A N_D}\right)(\phi_0 - V_D)}$$

$$\frac{W_2}{-W_1} = \frac{N_A}{N_D}$$

$$E_j = A_D \sqrt{\left(\frac{2q}{\epsilon_{si}} \frac{N_A N_D}{N_A + N_D}\right)(\phi_0 - V_D)}$$

$$
\begin{aligned}
C_j = \tfrac{\mathrm{d}Q_j}{\mathrm{d}V_D} &= A_D\sqrt{\left(\frac{\epsilon_{si}q}{2}\frac{N_A N_D}{N_A+N_D}\right)(\phi_0 - V_D)^{-1}} \\
&= \frac{C_{j0}}{\sqrt{1 - V_D/\phi_0}}
\end{aligned}
$$

Linearly graded junction

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

where m is the grading coefficient.

Large-signal depletion-region capacitance.

9.2.2.2 Excess minority carrier charge

9.2.3 Secondary effect: a more accurate model

9.2.3.1 Breakdown

Avalanche breakdown. This occurs when carriers crossing the depletion-region are accelerated enough to create electron-hole pairs when they collide with silicon atoms.

Zener breakdown.

9.2.3.2 Emission coefficient

9.3 Thyristors and triacs

9.4 Bipolar transistors (BJTs)

9.5 Junction field effect transistors (FETs)

9.6 Metal oxide field effect transistors (MOSFETs)

Advantages:

- Few parasitic effects
- Simple planar manufacturing process

9.6.1 Static behaviour

9.6.1.1 Cut-off region

If we apply a positive voltage to the gate, a depletion region forms

$$W_d = \sqrt{\frac{2\epsilon_{si}\phi}{qN_A}}$$

$$Q_d = \sqrt{2qN_A\epsilon_{si}\phi}$$

When the voltage equals twice the Fermi potential

$$\phi_F = \phi_T \ln\left(\frac{N_A}{n_i}\right) \approx -0.3\,\mathrm{V}$$

strong inversion occurs. The depletion layer no longer grows, but a layer of electrons forms.

$$Q_B = \sqrt{2qN_A\epsilon_{si}(|-2\phi_F + V_{SB}|)}$$

We determine the threshold voltage empirically and use

$$V_T = V_{T0} + \gamma(\sqrt{|V_{SB} - 2\phi_F|} - \sqrt{|2\phi_F|})$$

with γ the body effect coefficient.

9.6.1.2 Ohmic region

Charge per unit area

$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T]$$

Current flow:

$$I_D = -v_n(x)Q_i(x)W$$

where the electron velocity is related to the mobility μ_n

$$v_n = -\mu_n\xi(x) = \mu_n\frac{\mathrm{d}V}{\mathrm{d}x}$$

Combining we get

$$I_D\,\mathrm{d}x = \mu_n C_{ox} W(V_{GS} - V - V_T)\,\mathrm{d}V$$

Integrating over length of channel L:

$$\begin{aligned} I_D &= k_n'\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \\ &= k_n\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \end{aligned}$$

For small V_{DS} we can ignore the quadratic term. Then the relation between V_{DS} and I_D is linear.

9.6.1.3 Saturation region

When

$$V_{GS} - V_{DS} \le V_T$$

$$I_D = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

9.6.2 Some secondary effects

9.6.2.1 Channel length modulation

$$I_D = I_D'(1 + \lambda V_{DS})$$

9.6.2.2 Velocity saturation

$$v = \begin{cases} \frac{\mu_n \xi}{1+\xi/\xi_c} & (\xi \leq \xi_c) \\ v_{sat} & (\xi \geq \xi_c) \end{cases}$$

More time in saturation for short devices.
I_{DSAT} depends linearly on $V_G S$.

A simpler model

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Designing digital integrated circuits

Divide-and-conquor: hierarchy, but clocks and power defy hierarchy -¿ global and external issues
die, wafer, masks

19.1 Design parameters

19.1.1 Cost

The cost of an integrated circuit can be split into fixed costs, such as the cost of designing the IC, indirect costs for general company overhead and variable costs which is the cost directly attributable to the manufactured product:

$$\text{cost per IC} = \text{variable cost per IC} + \left(\frac{\text{fixed cost} + \text{indirect cost}}{volume}\right)$$

The fixed cost is strongly dependent on complexity and its impact is much more pronounced for small-volume products.
The variable cost is made up of the cost of the die plus the cost of testing and packaging, where the cost of the die is given by

$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}.$$

The die yield gives the proportion of dies that do not have a defect and, assuming defects are randomly distributed, can be expressed as

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

where α is a parameter that depends on the complexity of the manufacturing process and is roughly proportional to the number of masks. For modern CMOS processes $\alpha \approx 3$. One can expect about 0.5 to 1 defects per cm^2, but this depends strongly on the maturity of the process. Using $\alpha = 3$, we see that

$$\text{cost of die} \sim (\text{die area})^4$$

so the die area is a prime metric for the cost.

19.1.2 Performance

Obviously we want our ICs to be as fast as possible.
For processors the speed depends on both the architecture of the processor (e.g. how many commands it can execute in parallel) and its clock speed.
For individual gates the performance is determined by the **propagation delay** t_p which is how quickly the output responds to changes in input. In other words it is the delay experienced by a signal traveling through the gate. This delay actually also depends on the input signal. In particular its slope (see figure TODO). For that reason we introduce the quantities t_r and t_f which are the rise and fall times.

19.1.2.1 Ring oscillators

The de facto way to measure delays for a given circuit technology is with a ring oscillator, which is an odd number (usually at least five are needed) of inverters put back-to-back in a loop. This configuration has no stable state and thus will oscillate. The frequency of the oscillation is proportional to the propagation delay.
This method is primarily useful to compare different technologies, not to determine actual values for t_p. The situation is fairly ideal with minimal load. In actual circuits t_p may be expected to be 50 to 100 times slower.

19.1.3 Functionality and robustness

In real life nothing is perfect, but the output of an integrated circuits must be within an acceptable range, even if the conditions it is deployed in are not ideal.
A good design accounts for variations in the manufacturing process and must also be able to deal with *noise*, which is unexpected variation in the signal. Noise can also easily be generated within the IC if the input is rapidly changing for example. A good design will not introduce too much noise itself.

Noise margins are the ranges that the input voltage has to be in to be interpreted as either low or high. Ideally these are as large as possible.

Noise immunity refers to the ability to function correctly in the presence of noise. Many digital circuits with low noise margins have very good noise immunity because the reject the noise.

Regenerative property. If every gate adds a bit of noise, the signal will eventually be lost. Thus an important property of gates is the ability to bring back the signal to nominal levels after a disturbance.

Directivity. We in general want gates to be *unidirectional*: changes in output should not impact the input. In practice there will always be some capacitive coupling for instance.

Fan-out refers to the number of gates attached to the output. With large fan-out, the added load can reduce performance. For this reason library components often specify a maximum fan-out.
The added load can also affect the logic output levels. In order to minimise this effect, the input resistance is made as large as possible while keeping the output resistance small.

Fan-in is the number of inputs. More inputs means more complexity.

19.1.4 Power and energy consumption

Power considerations are very important. This was the main limiting factor for vacuum tube and bipolar technologies. It is also the reason CMOS is much more popular than pure NMOS (TODO ?), although now even CMOS is reaching its limits in this regard.
Power and energy consumption can be measured with different metrics. Obviously we can measure peak and average power dissipation, P_{peak} and P_{av}. It is also useful to decompose power consumption into *static* and *dynamic* components. The higher the number of switching events, the higher the dynamic power consumption.
The propagation delay and power consumption of a gate are related: the propagation delay is mostly determined by the speed at which a given amount of energy can be stored in the gate capacitors. For a given technology and gate topology, the product of the power consumption and propagation delay is generally a constant, called the power-delay product (PDP). This is simply the energy consumed per switching event and is a good quality measure for a switching device.

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27.2 Oscilloscopes

The main function of an oscilloscope is the measure voltage in function of time. Time is on the horizontal axis.
If the signal is periodic, it is easiest if one point in the cycle is fixed on the horizontal axis. This is achieved with triggering: every time the signal does something specific (the trigger event), the plot is shifted so that time is at a designated point on the screen. Typically a trigger event is when the signal passes a certain threshold and is either rising or falling.

27.2.1 Probes

Usually BNC connector on one end and other end has measuring tip and alligator clip for reference.

27.2.1.1 Isolation

It is important that the circuit being measured is completely isolated from the oscilloscope. If this is not the case and the ground clip is connected to a part of the circuit that is not ground, then this will complete a low resistance path to ground, causing much current to flow.
Usually oscilloscopes probes are connected to the ground of the grid. So the circuit being tested should be isolated from the grid! It is done this way round for a couple of reasons: as soon as the scope is connected to something else, e.g. to a computer via USB, then it is no longer floating. Also floating a scope may leave it with charge that will discharge through the next user.
If the circuit being measured cannot be isolated, then differential probes can be used. There are also devices for galvanically isolating USB connections. Remember that a circuit connected by USB is not isolated!

27.2.1.2 Types

There are three basic types: 1X, 10X and 100X.

27.2.2 Controls

Most oscilloscopes have the following controls:

- Moving vertical position up and down.
- Change scale of time and voltage axis. This is often labelled as seconds / division and volts / division. Some scopes have a button or a sensing device (Tektronix) to know whether the probe is 1X or 10X. All this does is change the label on the voltage axis.
- Coupling: DC, AC and ground. DC shows the signal as is, AC translates the signal vertically such that the average is zero and ground disconnects the signal.
- Setting trigger type.
- Autoset tries to find settings that show something of the signal. Very useful if you don't know why a signal is not showing up.

Appendix A

Symbols and constants

Appendix B

Formula reference

Appendix C

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