

Some of the Big Ideas in Electronics

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	tie inputs high / low: good practice	
	capacitors at input / output to reduce noise	
	timing with RC and Schmidt trigger	
	chopping optics	
	Kron reduction (from Schur complement)	

Part I

The circuit formalism

Chapter 1

Circuits and circuit topologies

A circuit is a symmetric digraph (C, N) .

- The vertices in C are called components.
- The edges in N are called nets.

A complex network is a circuit (C, N) together with a pair of functions

- $V : N \rightarrow \mathbb{C}$ such that $V(n) = -V(n^t)$ for all $n \in N$;
- $I : N \rightarrow \mathbb{C}$ such that $I(n) = -I(n^t)$ for all $n \in N$.

A timedependent network is a circuit (C, N) together with a pair of functions

- $V : N \rightarrow (\mathbb{R} \rightarrow \mathbb{R})$ such that $V(n) = -V(n^t)$ for all $n \in N$;
- $I : N \rightarrow (\mathbb{R} \rightarrow \mathbb{R})$ such that $I(n) = -I(n^t)$ for all $n \in N$.

Chapter 2

Part II

Introducing some basic ideas

heat conduction / thermal resistance
ground
decibels

Chapter 3

Different types of circuits

3.1 Basic circuits

3.1.1 Wires

3.1.2 Series circuits

3.1.3 Parallel circuits

3.2 Integrated circuits

3.3 Circuit boards

3.4 Inside actual electronic devices

Chapter 4

Describing sources: AC / DC

Chapter 5

Transients

Chapter 6

The bare minimum of practical tips

6.1 Measuring with a multimeter

6.2 Mains power

Part III

Analog electronics

Chapter 7

Ideal linear components

7.1 Voltage and current sources

RMS / peak

7.2 Resistors

7.2.1 Ohm's law

7.2.2 Potentiometers

7.2.3 Resistors in circuits

7.2.3.1 Resistors in parallel

7.2.3.2 Resistors in series

Voltage divider 10 percent rule (of total load current when multiload)

7.3 Capacitors

7.3.1 Capacitors in circuits

7.3.1.1 Capacitors in parallel

7.3.1.2 Capacitors in series

Capacitive divider

7.3.2 Capacitive reactance

7.3.3 Quality factor

7.4 Inductors

7.4.1 Inductors in circuits

7.4.1.1 Inductors in parallel

7.4.1.2 Inductors in series

7.4.2 Inductive reactance

7.4.3 Quality factor

7.4.4 Unwanted coupling: spikes

7.5 Transformers

7.6 Crystals and resonators

Chapter 8

Analysis of linear circuits

Miller effect??

8.1 Kirchhoff's laws

8.1.1 Voltage law *or* loop rule

8.1.2 Current law *or* junction rule

8.1.3 Result: systems of linear equations

8.2 Superposition principle

8.3 Thévenin's and Norton's theorems

8.3.1 Thévenin's theorem

8.3.2 Norton's theorem

8.3.3 Nodal analysis

8.3.4 Mesh analysis

8.4 Power in AC circuits

Apparent power, real power, reactive power

8.4.1 Power factor

8.5 Circuits with sinusoidal sources

8.6 Circuits with periodic non-sinusoidal sources

Chapter 9

Elements of circuits

9.1 Resonance

9.1.1 Series-resonant circuits

9.1.1.1 LC

9.1.1.2 LRC

9.1.1.3 Bandwidth

9.1.1.4 Quality factor

9.1.2 Parallel-resonant (antiresonant) circuits

More common

9.1.2.1 LC

9.1.2.2 LRC

9.1.2.3 Bandwidth

9.1.2.4 Quality factor

9.2 Input and output impedance

9.3 Filters

9.3.1 Passive filter

9.3.1.1 Low-pass filters

9.3.1.2 High-pass filters

9.3.1.3 Bandpass filters

9.3.1.4 Notch filters

9.3.1.5 Speaker crossover network

9.3.2 Active filters

9.3.2.1 Low-pass RC active audio filter

9.3.2.2 High-pass RC active audio filter

9.4 RC ripple filter

9.5 Attenuators

9.6 Coupling and DC blocking

9.7 Bypassing

9.8 Arc suppression

9.9 Switching regulators

Chapter 10

Non-ideal components and models

10.1 Wires

- Not breaking
- Not overheating
- Clean signal

Wire vs cable

10.1.1 Non-ideal behaviour

10.1.1.1 Wire resistance

10.1.1.2 Wire inductance

10.1.1.3 Skin effect

10.1.1.4 Cable impedance

Inductance

Capacitance

Impedance matching

Circuit solutions

10.1.2 Forms of wire

10.1.2.1 Solid core wire

TODO table of wire gauges.

10.1.2.2 Stranded wire

10.1.2.3 Braided wire

10.1.3 Kinds of wires

- Pretinned solid bus wire
- Speaker wire
- Magnet wire

10.1.4 Kinds of cables

- Paired cable
- Twisted pair
- Unbalanced coaxial
- Dual coaxial
- Balanced coaxial
- Shielded twin lead
- Ribbon
- Multiple conductor
- Fiberoptic
- 300Ω

10.1.5 Kinds of connectors

10.1.6 Symbols

10.1.6.1 Wiring

10.1.6.2 Connectors

10.2 Switches

- Wear: depends on speed (arcing)

10.2.1 Kinds of switch

10.2.2 Relays

10.2.2.1 Kinds of relays

10.2.2.2 Relay driver circuit

10.2.3 Symbols for switches

10.3 Resistors

10.3.1 Realistic model

10.3.2 Characteristics of real capacitors

10.3.2.1 Tolerance

10.3.2.2 Power rating

power rating twice maximum

10.3.2.3 Temperature coefficient of resistance

10.3.3 Resistor labels

10.3.4 Types of resistors

Groups:

- General purpose
- Precision
- Semiprecision
- Power resistors

10.3.5 Variable resistors

Rheostats, potentiometers, trimmers

10.3.5.1 Resistance taper

10.3.5.2 Types

10.4 Capacitors

10.4.1 Realistic model

Leakage, equivalent series resistance, equivalent series inductance, dielectric absorption

10.4.2 Characteristics of real capacitors

10.4.2.1 Dissipation factor

10.4.2.2 Insulation resistance

10.4.2.3 Dissipation factor or tangent delta ($\tan \delta$)

10.4.3 Types of capacitors

10.5 Inductors

10.5.1 Geometries of inductor configurations

10.5.1.1 Simple coil

10.5.1.2 Multilayer coil

10.5.1.3 Spiral coil

10.5.1.4 Toroidal coil

10.5.2 Realistic model

10.5.3 Inductor specifications

10.5.4 Types of inductors

10.5.5 Reading inductor labels

10.5.5.1 5-band inductor codes

10.5.5.2 4-band inductor codes

10.5.5.3 SMD inductance codes

10.6 Transformers

10.7 Batteries

- Size
- Power
- Voltage
- Current capacity
- Rechargeability

- 10.7.1 Battery capacity**
- 10.7.2 Internal resistance**
- 10.7.3 Combining batteries**
- 10.7.4 Battery packages**
- 10.7.5 Primary batteries**
- 10.7.6 Secondary batteries**

10.8 Ground

Symbols for ground

Ground loops (and single-point ground; ground bus)
separate digital and analog grounds

10.9 Power supplies

10.10 Fuses and circuit breakers

Chapter 11

Active components

11.1 Semiconductor physics

11.2 Diodes

There is a built-in potential across the junction:

$$\phi_0 = \phi_T \ln \left[\frac{N_A N_D}{n_i^2} \right]$$

where ϕ_T is the thermal voltage

$$\phi_T = \frac{kT}{q} = 26 \text{ mV} \quad \text{at room temperature.}$$

11.2.1 Static behaviour: a simple model

Ideal diode equation

$$I_D = I_S (e^{V_D/\phi_T} - 1)$$

11.2.2 Dynamic, or transient, behaviour

11.2.2.1 Depletion-region capacitance

Abrupt junction

$$Q_j = A_D \sqrt{\left(2\epsilon_{si} q \frac{N_A N_D}{N_A + N_D} \right) (\phi_0 - V_D)}$$

Width

$$W_j = W_2 - W_1 = A_D \sqrt{\left(\frac{2\epsilon_{si}}{q} \frac{N_A + N_D}{N_A N_D} \right) (\phi_0 - V_D)}$$

$$\frac{W_2}{-W_1} = \frac{N_A}{N_D}$$

$$E_j = A_D \sqrt{\left(\frac{2q}{\epsilon_{si}} \frac{N_A N_D}{N_A + N_D} \right) (\phi_0 - V_D)}$$

$$C_j = \frac{dQ_j}{dV_D} = A_D \sqrt{\left(\frac{\epsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \right) (\phi_0 - V_D)^{-1}}$$

$$= \frac{C_{j0}}{\sqrt{1 - V_D/\phi_0}}$$

Linearly graded junction

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

where m is the grading coefficient.

Large-signal depletion-region capacitance.

11.2.2.2 Excess minority carrier charge

11.2.3 Secondary effect: a more accurate model

11.2.3.1 Breakdown

Avalanche breakdown. This occurs when carriers crossing the depletion-region are accelerated enough to create electron-hole pairs when they collide with silicon atoms.

Zener breakdown.

11.2.3.2 Emission coefficient

11.3 Thyristors and triacs

11.4 Bipolar transistors (BJTs)

11.5 Junction field effect transistors (FETs)

11.6 Metal oxide field effect transistors (MOSFETs)

Advantages:

- Few parasitic effects
- Simple planar manufacturing process

11.6.1 Static behaviour

11.6.1.1 Cut-off region

If we apply a positive voltage to the gate, a depletion region forms

$$W_d = \sqrt{\frac{2\epsilon_{si}\phi}{qN_A}}$$

$$Q_d = \sqrt{2qN_A\epsilon_{si}\phi}$$

When the voltage equals twice the Fermi potential

$$\phi_F = \phi_T \ln \left(\frac{N_A}{n_i} \right) \approx -0.3 \text{ V}$$

strong inversion occurs. The depletion layer no longer grows, but a layer of electrons forms.

$$Q_B = \sqrt{2qN_A\epsilon_{si}(|-2\phi_F + V_{SB}|)}$$

We determine the threshold voltage empirically and use

$$V_T = V_{T0} + \gamma(\sqrt{|V_{SB} - 2\phi_F|} - \sqrt{|2\phi_F|})$$

with γ the body effect coefficient.

11.6.1.2 Ohmic region

Charge per unit area

$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T]$$

Current flow:

$$I_D = -v_n(x)Q_i(x)W$$

where the electron velocity is related to the mobility μ_n

$$v_n = -\mu_n \xi(x) = \mu_n \frac{dV}{dx}$$

Combining we get

$$I_D dx = \mu_n C_{ox} W (V_{GS} - V - V_T) dV$$

Integrating over length of channel L :

$$\begin{aligned} I_D &= k'_n \frac{W}{L} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \\ &= k_n \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \end{aligned}$$

For small V_{DS} we can ignore the quadratic term. Then the relation between V_{DS} and I_D is linear.

11.6.1.3 Saturation region

When

$$\begin{aligned} V_{GS} - V_{DS} &\leq V_T \\ I_D &= \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2 \end{aligned}$$

11.6.2 Some secondary effects

11.6.2.1 Channel length modulation

$$I_D = I'_D(1 + \lambda V_{DS})$$

11.6.2.2 Velocity saturation

$$v = \begin{cases} \frac{\mu_n \xi}{1 + \xi / \xi_c} & (\xi \leq \xi_c) \\ v_{sat} & (\xi \geq \xi_c) \end{cases}$$

More time in saturation for short devices.

I_{DSAT} depends linearly on $V_G S$.

A simpler model

11.6.2.3 Threshold variations

11.6.2.4 Hot-carrier effects

11.6.2.5 CMOS latchup

11.6.3 Dynamic behaviour

11.6.3.1 Capacitive device model

MOS structure capacitances

Channel capacitances

Junction capacitances

11.6.3.2 Source-drain resistance

11.6.4 Comparison NMOS and PMOS

- Velocity saturation less pronounced in PMOS.

11.6.5 SPICE models

11.6.6 Process variations

11.6.7 Technology scaling

11.7 Insulated-gate bipolar transistors (IGBTs)

Chapter 12

Analogue integrated circuits

large analog ICs not very abstractable

12.1 The ideal op-amp

12.2 The practical op-amp

12.3 Comparators

12.4 Voltage references

Chapter 13

Classic circuits

13.1 Rectifiers

13.2 Switching regulators

13.2.1 Buck converter

13.2.2 Boost converter

13.2.3 Buck-boost converter

13.3 Oscillators

13.3.1 Simple relaxation oscillator

13.3.2 Op-amp oscillator

13.3.3 Colpits oscillator

13.3.4 Hartley oscillator

13.4 Radio circuits

13.4.1 Short-wave receiver

13.4.2 RF oscillator / transmitter

Chapter 14

Filters

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20.1.1 Carry-ripple adders

20.1.2 Carry-look-ahead adders

20.1.3 Adders and subtractors

20.1.4 Logic unit and arithmetic-logic unit

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20.1.12 Programmable logic arrays

20.2 Sequential logic components

20.2.1 Latches

20.2.1.1 SR-latch

20.2.1.2 Gated SR-latch

20.2.1.3 Gated D-latch

20.2.2 Flip-flops

Flip-flop types

20.2.3 Analysis of sequential logic

20.3 Storage components

20.3.1 Registers

20.3.1.1 Shift registers

20.3.2 Counters

20.3.2.1 BCD counter

20.3.2.2 Asynchronous counter

20.3.3 Random-access memories (RAMs)

Chapter 21

Designing digital integrated circuits

Divide-and-conquer: hierarchy, but clocks and power defy hierarchy - global and external issues

die, wafer, masks

21.1 Design parameters

21.1.1 Cost

The cost of an integrated circuit can be split into fixed costs, such as the cost of designing the IC, indirect costs for general company overhead and variable costs which is the cost directly attributable to the manufactured product:

$$\text{cost per IC} = \text{variable cost per IC} + \left(\frac{\text{fixed cost} + \text{indirect cost}}{\text{volume}} \right)$$

The fixed cost is strongly dependent on complexity and its impact is much more pronounced for small-volume products.

The variable cost is made up of the cost of the die plus the cost of testing and packaging, where the cost of the die is given by

$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}.$$

The die yield gives the proportion of dies that do not have a defect and, assuming defects are randomly distributed, can be expressed as

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}$$

where α is a parameter that depends on the complexity of the manufacturing process and is roughly proportional to the number of masks. For modern CMOS processes $\alpha \approx 3$. One can expect about 0.5 to 1 defects per cm^2 , but this depends strongly on the maturity of the process. Using $\alpha = 3$, we see that

$$\text{cost of die} \sim (\text{die area})^4$$

so the die area is a prime metric for the cost.

21.1.2 Performance

Obviously we want our ICs to be as fast as possible.

For processors the speed depends on both the architecture of the processor (e.g. how many commands it can execute in parallel) and its clock speed.

For individual gates the performance is determined by the **propagation delay** t_p which is how quickly the output responds to changes in input. In other words it is the delay experienced by a signal travelling through the gate. This delay actually also depends on the input signal. In particular its slope (see figure TODO). For that reason we introduce the quantities t_r and t_f which are the rise and fall times.

21.1.2.1 Ring oscillators

The de facto way to measure delays for a given circuit technology is with a ring oscillator, which is an odd number (usually at least five are needed) of inverters put back-to-back in a loop. This configuration has no stable state and thus will oscillate. The frequency of the oscillation is proportional to the propagation delay.

This method is primarily useful to compare different technologies, not to determine actual values for t_p . The situation is fairly ideal with minimal load. In actual circuits t_p may be expected to be 50 to 100 times slower.

21.1.3 Functionality and robustness

In real life nothing is perfect, but the output of an integrated circuits must be within an acceptable range, even if the conditions it is deployed in are not ideal.

A good design accounts for variations in the manufacturing process and must also be able to deal with *noise*, which is unexpected variation in the signal. Noise can also easily be generated within the IC if the input is rapidly changing for example. A good design will not introduce too much noise itself.

Noise margins are the ranges that the input voltage has to be in to be interpreted as either low or high. Ideally these are as large as possible.

Noise immunity refers to the ability to function correctly in the presence of noise. Many digital circuits with low noise margins have very good noise immunity because they reject the noise.

Regenerative property. If every gate adds a bit of noise, the signal will eventually be lost. Thus an important property of gates is the ability to bring back the signal to nominal levels after a disturbance.

Directivity. We in general want gates to be *unidirectional*: changes in output should not impact the input. In practice there will always be some capacitive coupling for instance.

Fan-out refers to the number of gates attached to the output. With large fan-out, the added load can reduce performance. For this reason library components often specify a maximum fan-out.

The added load can also affect the logic output levels. In order to minimise this effect, the input resistance is made as large as possible while keeping the output resistance small.

Fan-in is the number of inputs. More inputs means more complexity.

21.1.4 Power and energy consumption

Power considerations are very important. This was the main limiting factor for vacuum tube and bipolar technologies. It is also the reason CMOS is much more popular than pure NMOS (TODO ?), although now even CMOS is reaching its limits in this regard.

Power and energy consumption can be measured with different metrics. Obviously we can measure peak and average power dissipation, P_{peak} and P_{av} . It is also useful to decompose power consumption into *static* and *dynamic* components. The higher the number of switching events, the higher the dynamic power consumption.

The propagation delay and power consumption of a gate are related: the propagation delay is mostly determined by the speed at which a given amount of energy can be stored in the gate capacitors. For a given technology and gate topology, the product of the power consumption and propagation delay is generally a constant, called the power-delay product (PDP). This is simply the energy consumed per switching event and is a good quality measure for a switching device.

21.2 Design methodologies

21.2.1 Custom circuit design

21.2.2 Cell-based

21.2.2.1 Standard cell

21.2.2.2 Compiled cell

21.2.2.3 Macro cells

21.2.3 Array-based

21.2.3.1 Prediffused (or mask-programmable) arrays

21.2.3.2 Prewired arrays (FPGAs)

21.3 Coping with interconnect

21.4 Timing issues

21.4.1 Timing classification

Chapter 22

Designing gates and components

22.1 Transistor-transistor logic (TTL)

22.2 CMOS technology

22.2.1 The CMOS inverter

22.2.2 Combinational logic in CMOS

22.2.3 Sequential logic in CMOS

Chapter 23

Processors and microcontrollers

Intel 4004 in 1972 and 8080 in 1974 (IBM computers? Instruction set)

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Electric devices

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Motors and actuators

Chapter 25

Audioelectronics

Chapter 26

Optoelectronics

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Radio engineering

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Part VII

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27.1 Precision and low noise

Part VIII

Simulation

27.2 Spice

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Part IX

Tools and accessories

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Hardware

28.1 Screws

Chapter 29

Devices

29.1 Power supplies

29.1.1 Bench power supply

Output: three terminals: positive, negative and ground. Ground should be isolated from other terminals.

29.2 Oscilloscopes

The main function of an oscilloscope is the measure voltage in function of time. Time is on the horizontal axis.

The scope will sweep along the time axis. Triggering resets the horizontal sweep at a particular location each time a particular event, the trigger event, occurs. Typically a trigger event is when the signal passes a certain threshold and is either rising or falling.

29.2.1 Probes

Usually BNC connector on one end and other end has measuring tip and alligator clip for reference.

29.2.1.1 Isolation

It is important that the circuit being measured is completely isolated from the oscilloscope. If this is not the case and the ground clip is connected to a part of the circuit that is not ground, then this will complete a low resistance path to ground, causing much current to flow.

Usually oscilloscopes probes are connected to the ground of the grid. So the circuit being tested should be isolated from the grid! It is done this way round for a couple of reasons: as soon as the scope is connected to something else, e.g. to a computer via USB, then it is no longer floating. Also floating a scope may leave it with charge that will discharge through the next user.

If the circuit being measured cannot be isolated, then isolated probes can be used. There are also devices for galvanically isolating USB connections. Remember that a circuit connected by USB is not isolated!

29.2.1.2 Types

There exist many types of probes. These include passive probes, active probes, differential probes, current probes, logic probes, high voltage probes, optical probes and isolated. Most common are passive probes.

Passive probes Passive are distinguished by their attenuation factor: usually 1X, 10X or 100X. Probes may be switchable: it can be both 1X and 10X or 10X and 100X.

The attenuation is achieved by connecting a resistor in series inside the probe, such that the oscilloscope is measuring over a voltage divider.

WHY?

29.2.2 Controls

Most oscilloscopes have the following controls:

- Moving vertical position up and down.
- Change scale of time and voltage axis. This is often labelled as seconds / division and volts / division. Some scopes have a button or a sensing device (Tektronix) to know whether the probe is 1X or 10X. All this does is change the label on the voltage axis.
- Coupling: DC, AC and ground. DC shows the signal as is, AC translates the signal vertically such that the average is zero and ground disconnects the signal.
- Setting trigger type.
- XY mode: displays a second channel along the horizontal axis instead of time.
- Autoset tries to find settings that show something of the signal. Very useful if you don't know why a signal is not showing up.

There will also be a square wave output to calibrate probes with compensation.

Appendix A

Symbols and constants

Appendix B

Formula reference

Appendix C

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