The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design
HW # 2: *Due on Thursday 2/15/2024 - 11:59 pm (US CST)*

When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

Consider the following three circuits shown in Figures 3.23, 3.34, 3.37 in your textbook:

1. Exactly as they are (with no change to an equivalent topology), apply the three steps of fault analysis iteratively similar to the example shown at the end of "4.fault_simulation_2". Basically, you apply: (i) fault collapsing using checkpoint theorem (or by level-by-level dropping) and then iteratively apply (ii) D-algorithm (or PODEM) to find test pattern(s) for a selected fault and (iii) critical path tracing (or other fault simulation methods) to find a subset of faults detectable by the same pattern chosen in (ii).

2. Without changing/optimizing the above circuits:

   (i) Use **SYNOPSYS** toolset to model and implement the circuits at the gate level.

   (ii) Find all stuck-at faults, the test vectors and the fault coverage. If fault coverage is not 100% show the undetected faults reported by the tool.

   (iii) Verify the results reported by the tool with your hand-work analysis.

   Note 1: Check the course webpage for some guidelines on how to use SYNOPSYS.

   Note 2: Your report should include HDL (VHDL or Verilog) description, schematic of the circuit, some simulations to show the correct behavior, test analysis by Tetramax (e.g. faults, test patterns) and any other interesting observations.

3. Considering the set of collapsed faults for circuit of Figure 3.37 above and for test vector $x_1x_2x_3x_4x_5 = 11011$:

   (i) Demonstrate **parallel** fault simulation.

   (ii) Demonstrate **deductive** fault simulation.

   (iii) Demonstrate **concurrent** fault simulation.

   (iv) Demonstrate **critical path tracing** fault simulation