EEDG/CE 6303: Testing and Testable Design

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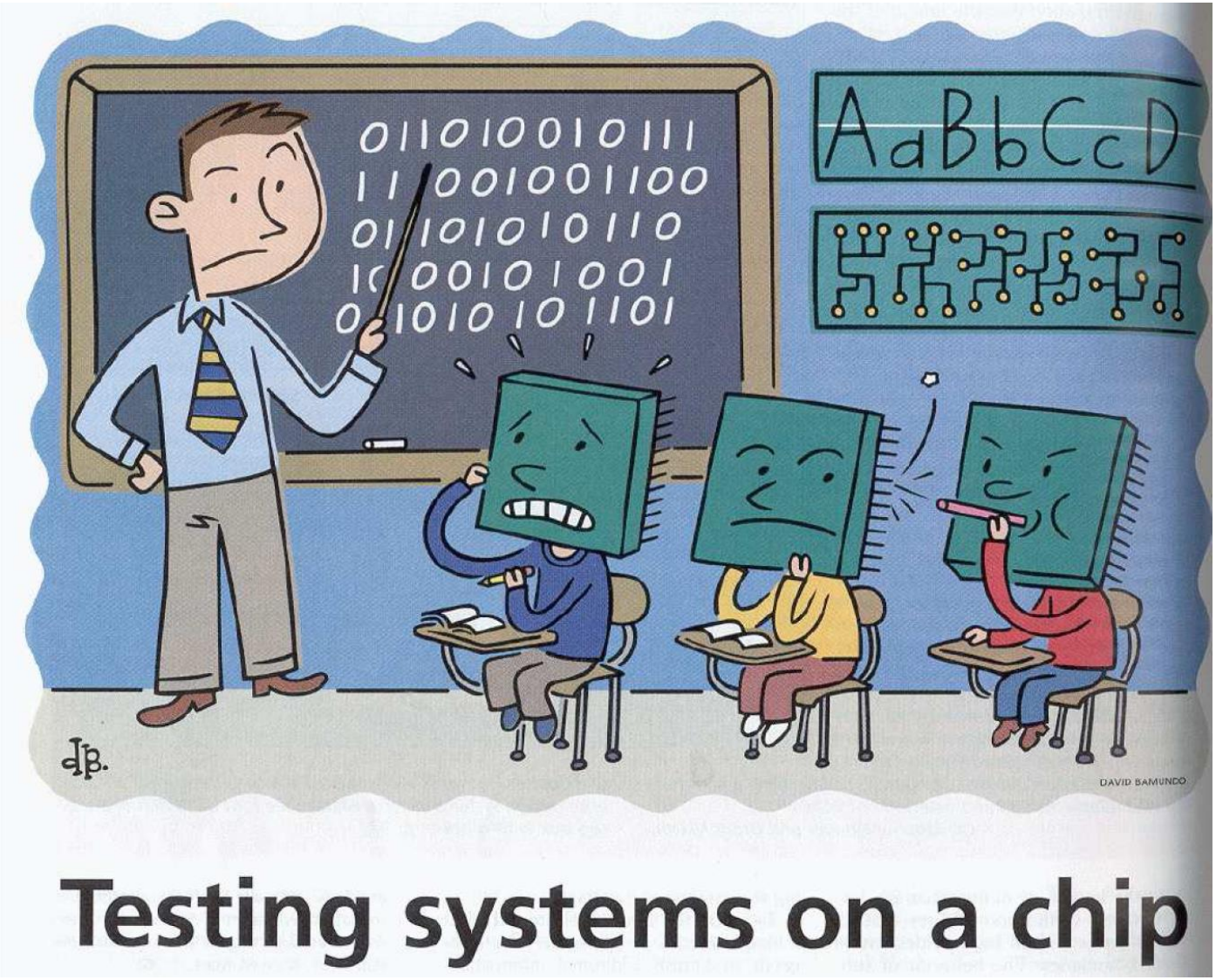
Session 01

Introduction

VLSI Test Philosophy

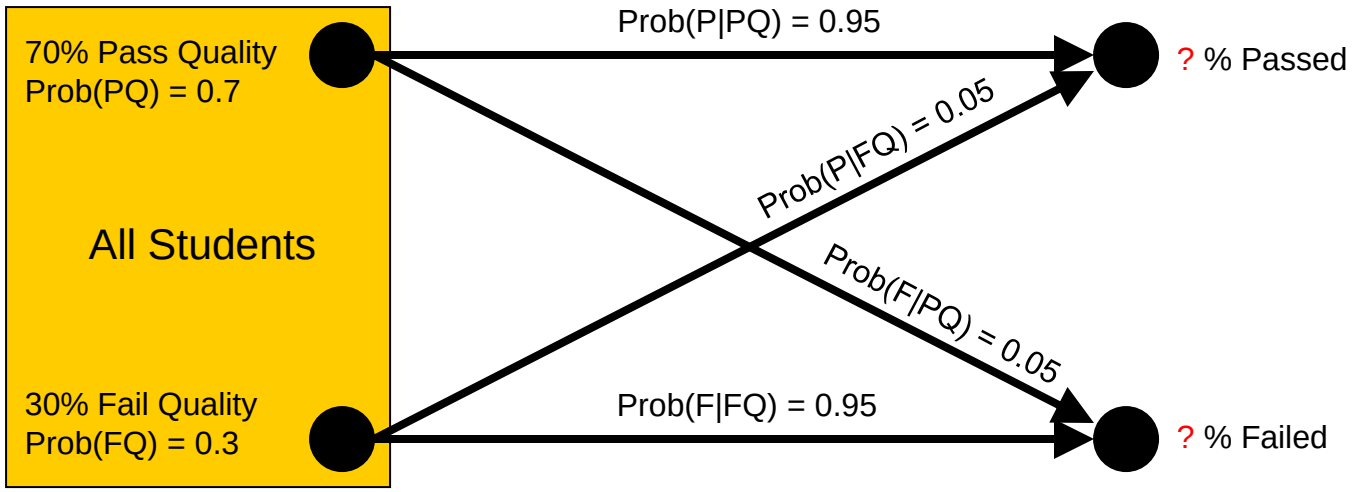
Testing



Source: IEEE Spectrum

Test Philosophy

- A Pass/Fail test:



PQ: student is pass quality
FQ: student is fail quality

P: student passes the test
F: student fails the test

Test Philosophy (cont'd)

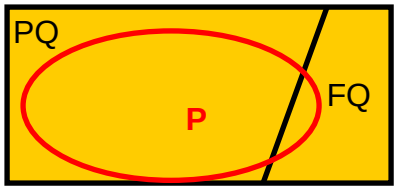
- Conditional Probability: $P[A|B]=P[AB]/P[B]$
  - Rewrite the relation: $P[AB]=P[A|B].P[B]=P[B|A].P[A]=P[BA]$
  - If A and B are independent: $P[A|B]=P[A]$ or $P[AB]=P[A].P[B]$

- Bay's Theorem:
  - Simple form: $P[A|B]=P[B|A].P[A]/P[B]$
  - General Form for mutually exclusive & exhaustive events E_i's:
    - $P[A]=\sum_{i=1}^{n} P[A|E_i].P[E_i]$ or
    - $P[E_i|A]=P[E_iA]/P[A]=P[A|E_i].P[E_i]/\sum_{i=1}^{n} P[A|E_i].P[E_i]$

- Probability of Passing/Failing the Exam:

$$Prob(P) = Prob(P|PQ)*Prob(PQ)+Prob(P|FQ)*Prob(FQ)$$
$$= 0.95*0.70+0.05*0.30=0.68$$

$$\Pr ob(F)=1-\Pr ob(P)=1-0.68=0.32$$



Test Philosophy (cont'd)

- Student's risk (manufacturer's risk or yield loss):

$$\Rightarrow \text{Prob}(PQ \mid F) = \frac{\text{Prob}(F \mid PQ) * \text{Prob}(PQ)}{\text{Prob}(F)} = \frac{0.05 * 0.7}{0.32} = 0.11$$

11% of failed students (chips) should have passed

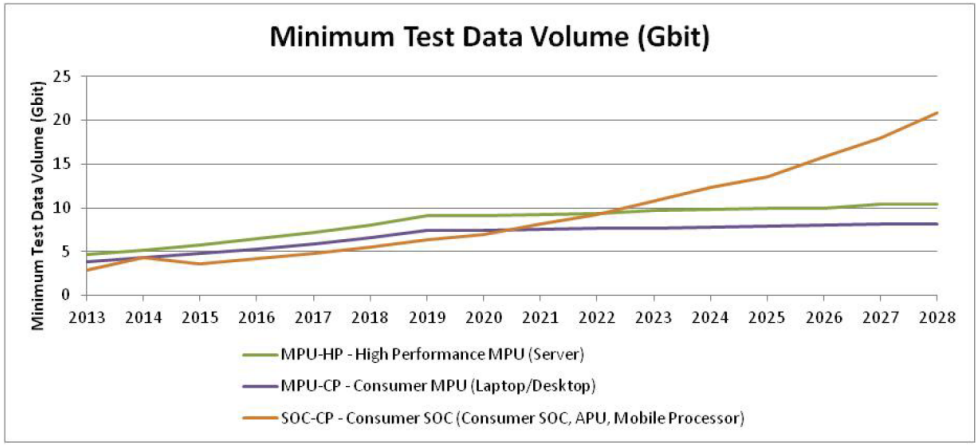
- Teacher's risk (consumer's risk):

$$\Rightarrow \text{Prob}(FQ \mid P) = \frac{\text{Prob}(P \mid FQ) * \text{Prob}(FQ)}{\text{Prob}(P)} = \frac{0.05 * 0.3}{0.68} = 0.022$$

2.2% of students (chips) passed the tests should have failed

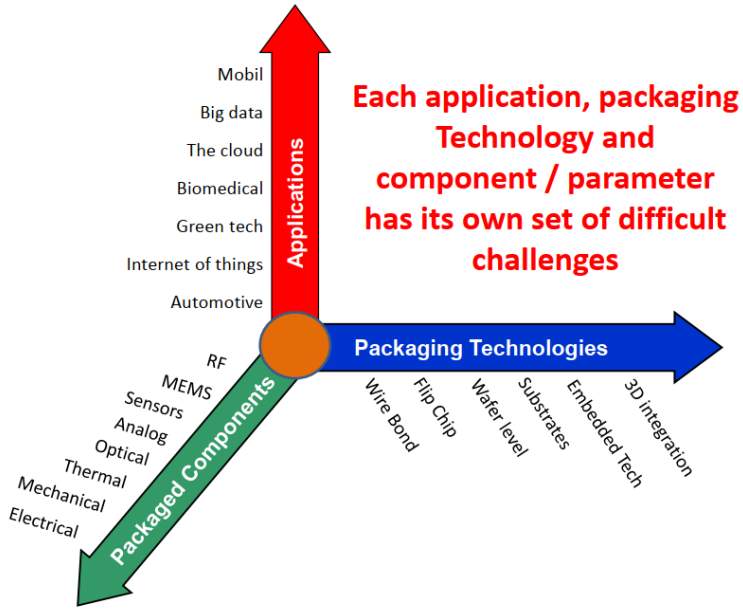
VLSI Chips – Past, Present and Future

Year	1997-2001	2003-2006	2009-2012
Feature Size, μm	0.25 – 0.15	0.13 – 0.10	0.07 – 0.05
Millions of Transistors/cm^2	4 – 10	18 – 39	84 – 180
Number of wiring layers	6 – 7	7 – 8	8 – 9
Die Size, mm^2	50 – 385	60 – 520	70 – 750
Pin count ($\alpha\sqrt{N_{tran}}$)	100 – 900	160 – 1475	260 – 2690
Clock Rate, MHz	200 – 730	530 – 1100	840 – 1830
Voltage, V	1.2 – 2.5	0.9 – 1.5	0.5 – 0.9
Power, W	1.2 – 61	2 – 96	2.8 – 109



IoE

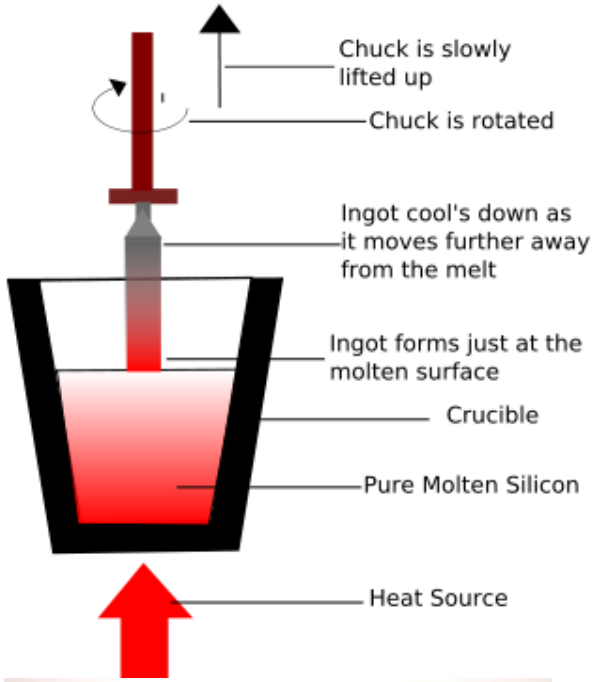
Categories	Year	2015	2017	2019	2021	2023	2025	2027	2029
Power	Energy source (B = battery; H = energy harvesting)	B	B	B + H	B + H	B + H	B + H	B + H	B + H
	Lowest VDD Used By Components (V)	0.8	0.75	0.7	0.65	0.65	0.55	0.45	0.45
	Deep suspend current of MCU (nA)	100	72	52	38	27	20	14	10
	Conversion efficiency of DC-to-DC Conversion (%)	80%	82%	86%	88%	89%	91%	93%	95%
	Spatial Power Density of DC Converter (W/mm^2)	1	1.17	1.36	1.59	1.85	2.16	2.52	2.94
	Peak Current Consumed by Connectivity Interface (mA)	50	19.28	7.44	2.87	1.11	0.43	0.16	0.06
	Transmission Power per bit (μW/bit)	2.48	0.972	0.381	0.149	0.058	0.023	0.009	0.004
Form factor	Module footprint (mm2)	500	500	280	179	115	73	47	30
Performance	MCU Number of Cores	1	1	1	1	1	1	1	1
	MCU Current / Operation frequency (mA/MHz)	30	21.7	15.7	11.3	8.9	7.7	6.7	5.8
	Max MCU Frequency (MHz)	200	235	277	306	316	327	338	350
	MCU Flash Size (KB)	1024	1024	2048	4096	4096	8192	8192	8192
	MCU Dhrystone MIPS (DMIPS)	200	242	293	354	429	519	628	759
Peripheral	Number of Sensors Integrated to System	4	8	10	12	12	13	13	13
	Max Sensor Power (μW)	2850	1397	1009	729	617	522	442	374



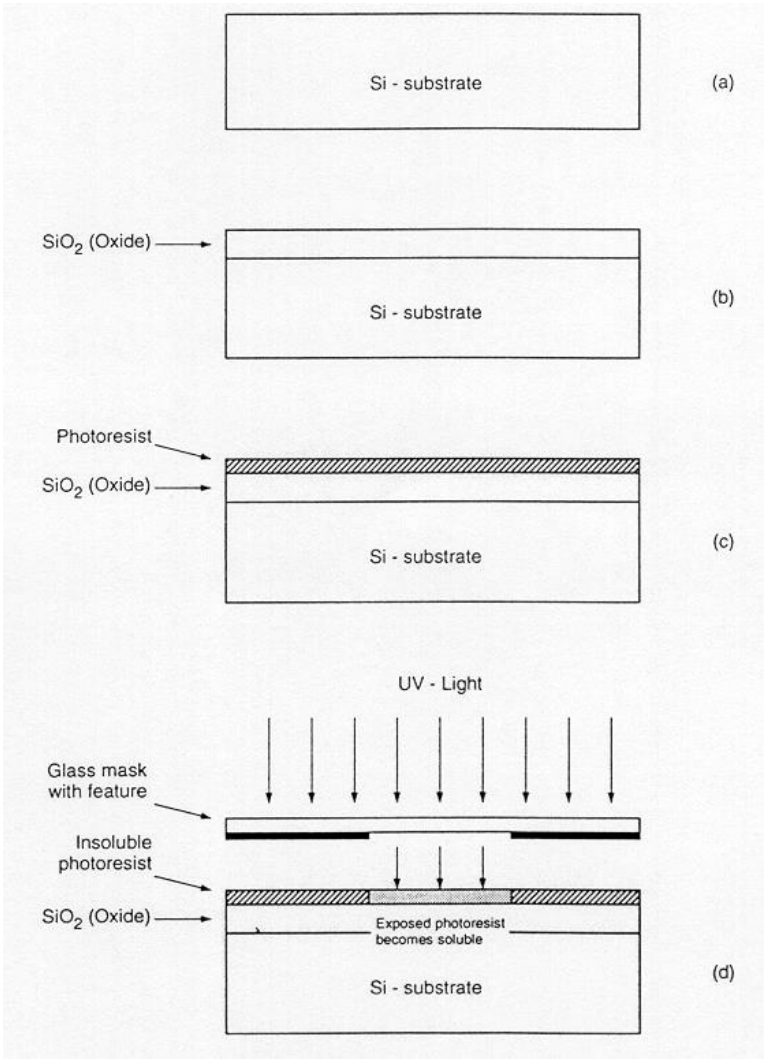
https://www.semiconductors.org/

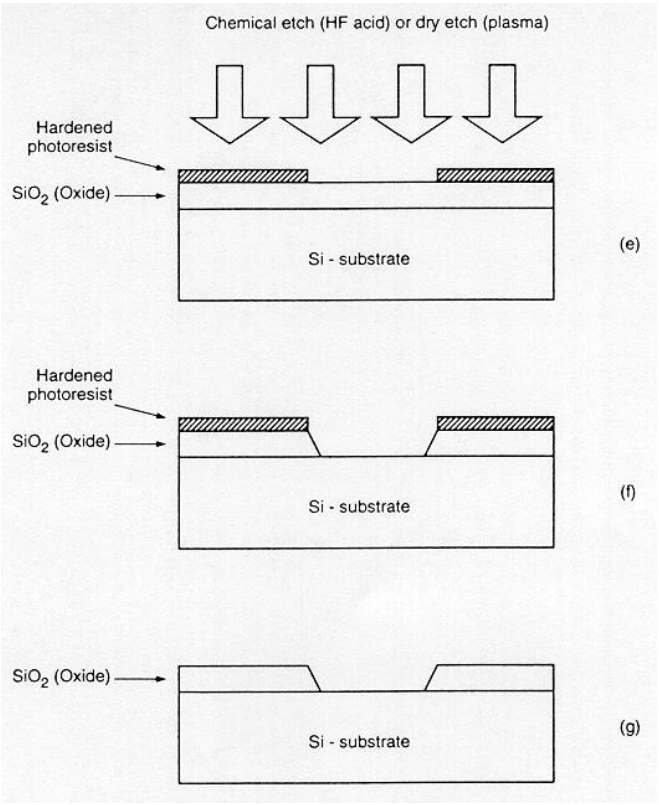
VLSI Fabrication Process

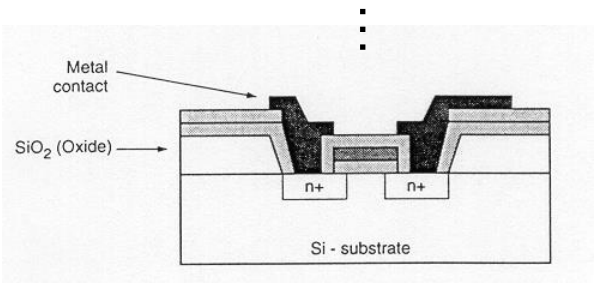
- A seed crystal is dipped into the melted silicon to initiate single-crystal growth
- Diameter: 75 – 230 mm
- Growth rate: 30 – 180 mm/hour
- The output is a silicon ingot
- Using diamond blades, the wafers are produced (thickness = 0.25 – 1 mm)
- At least one surface is polished to a flat, scratch-free mirror finish



VLSI Fabrication Process (cont'd)

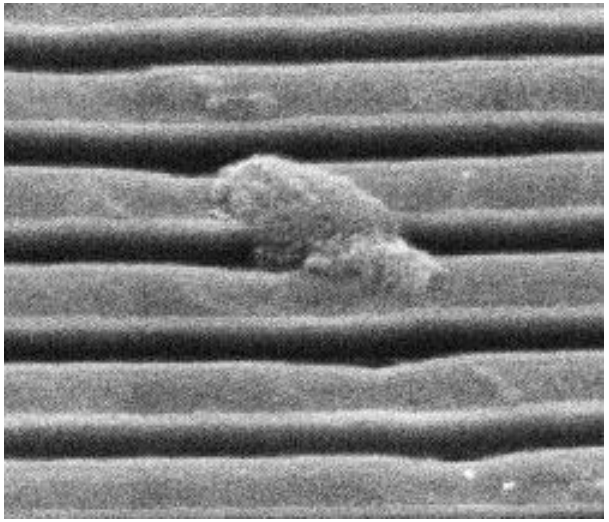


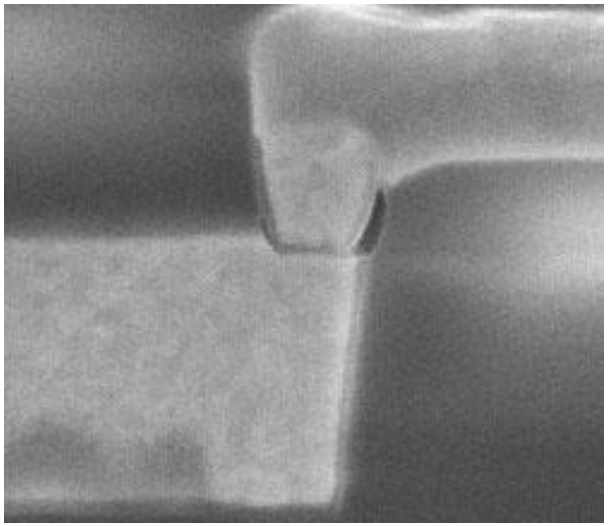




What May Go Wrong?

- Shorts between two points (bridges)
- Open in a line
- Improper doping
- Masking error
- Improper thickness of a line
- Particles on surface
- Electron migration due to heat
- Corrosion
- …





What Can be Done?

1. Wafer probe testing.
2. Use microscope to find faulty dices. Mark with a small ink. Reject after separation. Package the unmarked dies.
3. Test for electrical and mechanical characteristics.
4. Final inspection for cosmetic defects.
5. Pack and ship.

Test Definition

- "Testing" of a system is an experiment in which the system is exercised and its resulting responses are analyzed to ascertain whether it behaved correctly
  - How to send input data (test patterns)?
  - How to collect output results (test signatures)?
  - How long the system should run?
  - How to make the conclusion?
  - How to locate the cause of misbehavior (diagnosis)?
  - What causes misbehavior?
  - What test equipment are needed?
  - …

Test Importance

- Test is an integral part of any manufacturing process.
  - Production Cost = Fabrication & Packaging + Testing
  - According to Semiconductor Industry Association (SIA) roadmap, the cost of testing a die will surpass its manufacturing cost in the near future.

- Each VLSI chip needs to be tested. Sampling is not adequate. Why?

When and Where to Test

- Try to detect defects at the earliest point possible.
- Costs increases dramatically (typically by an order of magnitude) as faulty components find their way to the higher level of integration
- Rule of 10:
  - —$1 to detect a faulty chip. Throw it out!
  - —$10 to find (and replace) a bad IC on a board.
  - —$100 to find a bad PC board in a system.
  - —$1000 to find a bad component in the fielded system

Taxonomy of Testing

- **Defect**: Physical problems due to imperfect manufacturing process.
  - Defects are not directly attributable to a human error.
  - Examples: shorts, opens, improper doping, etc.
- **Fault**: the failure mechanism.
  - Fault effect: the logical effect of a fault on a signal or carrying net.
  - Fault model: the simplification of the real problem
- **Error**:
  - The condition (or state) of a system containing a fault, i.e. deviation from correct state (e.g. wrong component, incorrect wiring, …).
  - An error does not necessarily lead to a failure (e.g. wrong tire pressure (error) versus a flat tire (failure)).
- **Failure**: Incorrect operation of a system.

Taxonomy of Testing (cont'd)

- Fault model: the basic assumptions regarding the nature of the logical (malignant) fault.
- A fault is "detected" by observing an error caused by it.

- Briefly:

Defect → Fault → Error → Failure

(e.g. dust particle → stuck-at-1 → erroneous logic value → circuit failing)

Taxonomy of Testing (cont'd)

- Yield (Y): the probability (usually expressed as percent) that items (e.g. ICs) will not be defective (fraction of manufactured parts that is defect-free).
  - For VLSI chips yields range from 10% to 90% depending on the process, circuit complexity, VLSI technology size/feature lambda (λ), etc.
  - Y=1 (100%) means defect-free production.
  - Y=0 (0%) means all circuits are faulty.

Taxonomy of Testing (cont'd)

- Fault coverage (FC) is a measure to grade the quality of a test:
  - $FC = \frac{\text{Number of faults detected}}{\text{Total number of faults}} * 100\%$
  - FC=1 (100%) : all possible faults detected
  - FC=0 (0%) : no fault detected.
- Defect level (DL): the probability of shipping a defective product (the fraction of bad parts that pass all tests).
  - An empirical/analytical equation: $DL = \left[1 - Y^{(1-FC)}\right] * 100\%$
  - Both Y and FC must be continually improved to maintain reliability of shipped products

Defect Level Formula

- Because tests may not be complete, a defective chip may pass the tests.
- Assumptions:
  - a chip has exactly n faults (e.g. stuck-at faults).
  - Let m be the number of detected faults ($m \leq n$)
  - the probability of a fault occurrence is independent of the occurrence of another fault (i.e., there is no fault clustering) and that all faults are equally likely with probability p
  - A is the event that a part is free of faults, and B that a part has been tested for m faults while none were found.

Defect Level Formula (cont.)

- The Fault Coverage of a test is: $FC = m/n$
- The Process Yield is defined as: $Y = (1-p)^n = P(A)$
- Considering: $P(A \cap B) = P(A) = (1-p)^n$

  $P(B) = (1-p)^m$

We will get:

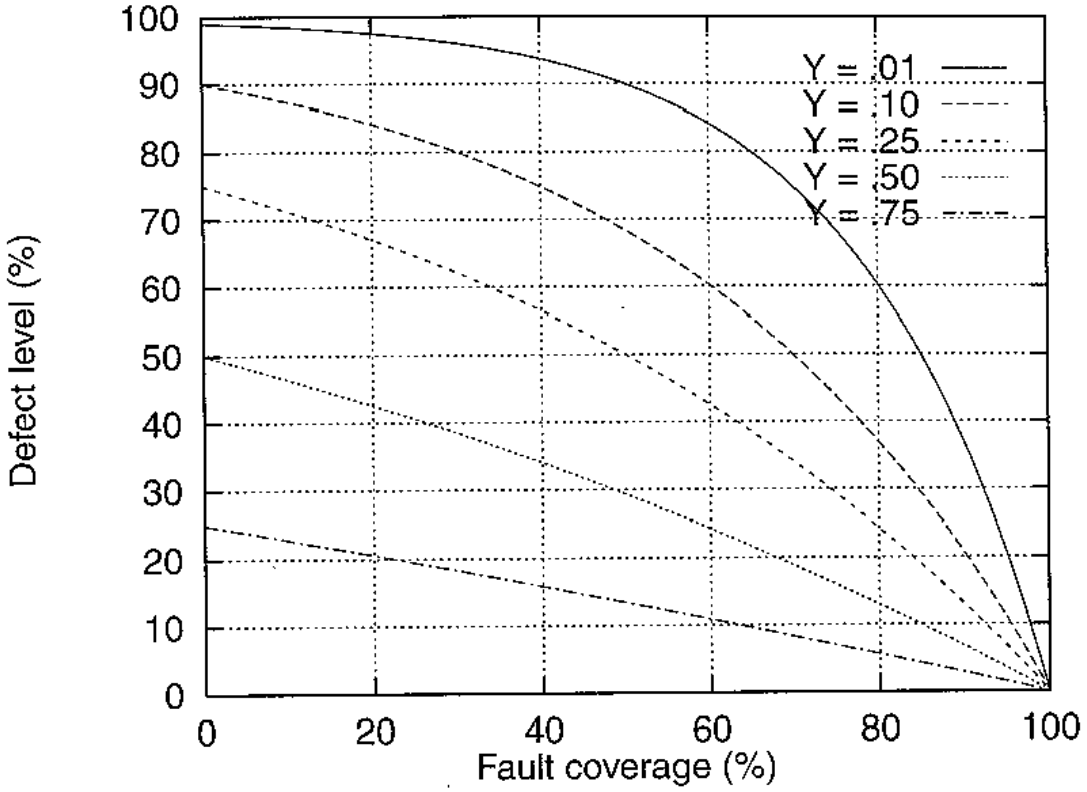
$$P(A|B) = P(A \cap B)/P(B) = (1-p)^n/(1-p)^m = (1-p)^{n-m} = (1-p)^{n(1-m/n)}$$

- *DL* can now be expressed as:

$$DL = 1 - P(A|B) = 1 - Y^{(1-FC)}$$

Defect Level (cont.)

- *DL* is expressed as: $DL = 1 - P(A|B) = 1 - Y^{(1-FC)}$
- For large values of *Y* (i.e., a manufacturing process with a high yield), it approaches a straight line



Defect Level (cont.)

- Example: Assume a manufacturing process with *Y = 0.5* and a *FC = 0.8*, then:

$$DL = 1 - 0.5^{(1-0.8)} = 0.1295$$

This means that 12.95% of the shipped parts are defective!

- If a DL=200 PPM (i.e., *DL = 0.0002*) is required, given *Y = 0.5*, then:

$$FC = 1 - (\log(1 - DL) / \log Y) = 0.99971$$

This is a *FC* of 99.971%

Type of Faults

- **Permanent fault**: always being present after their occurrence (in existence long enough to be observed at test time).
- **Intermittent fault**: existing only during some intervals (appears and disappears at regular intervals).
- **Transient fault**: a one-time occurrence, e.g. caused by a temporary change in some environmental factors (appears and disappears in short time intervals). These faults are crucial for real-time systems.

Failure Mechanisms

- Failure mechanisms describe the physical and electrical causes for faults. They can be divided into 3 classes:

1. Electrical stress

   Poor design leading to electrical overstress, or careless handling causing static damage

2. Intrinsic failure mechanisms

   Inherent to the semiconductor material itself.

   Examples: Crystal defects, dislocations and processing defects

3. Extrinsic failure mechanisms

   Originate in the packaging and interconnection process

   Examples: Poor bonding, corrosion, etc.

Failure Mechanisms