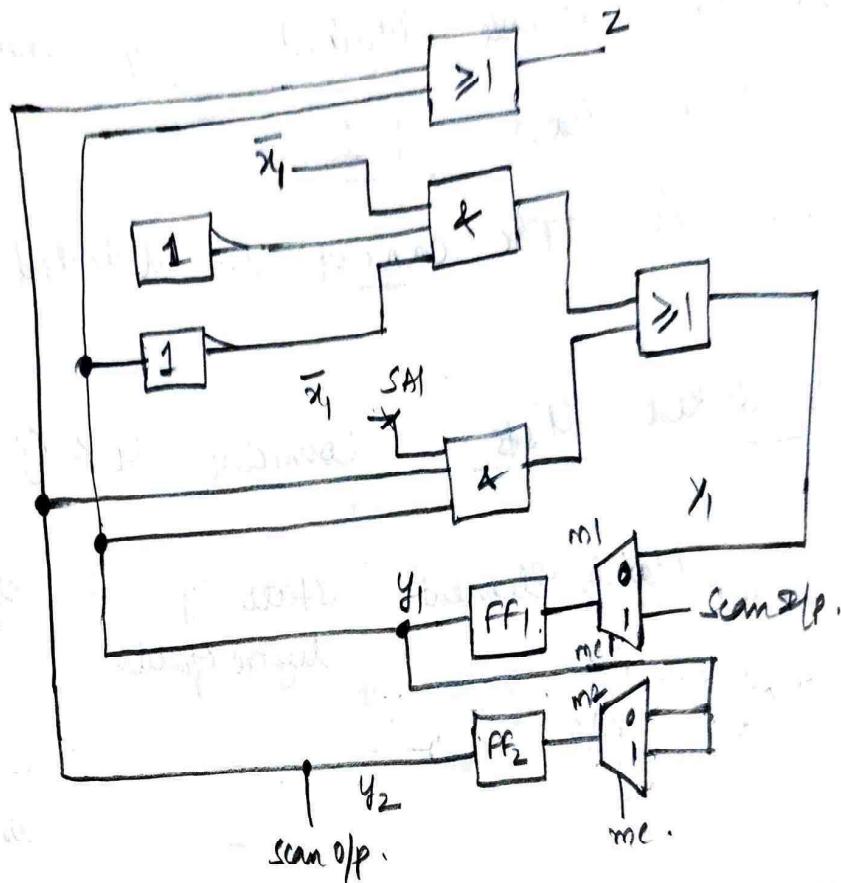


16.04.2024

## Homework - 5 - Solutions

Solution 1:

H.5. Given circuit:



@.

Given: Gatt delay of each gate is  $\alpha$  units for each gate with  $2^k$  inputs.

Critical path: It's through  $G_1$  (inv) ;  $G_3$  (and) ;  $G_5$  (OR).

and  $m_1$  ( $32/p_2$ ) (mux  $2:1$ ).

$2^k/p_1$  & select line.

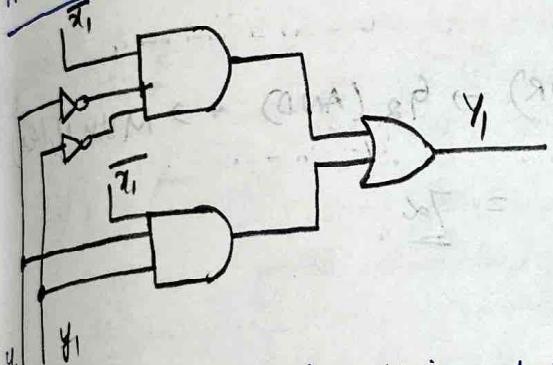
$$\therefore \text{Critical Path Delay} = 1\alpha + 3\alpha + 2\alpha + 3\alpha = 9\alpha$$

for full scan version : Minimum clock period =  $9\alpha$ .

In the non-scan mode, mux's will not be a part of the active circuit. Thus, the o/p is directly fed into the flip-flop.  
 Hence, the performance penalty = 3x.

Q. To redesign the combinational ckt; we use boolean reduction logic.

Actual combinational circuits:



$$Y_1 = \bar{x}_1 y_1 \bar{y}_2 + \bar{x}_1 y_1 y_2$$

$$= \bar{x}_1 (y_1 y_2 + \bar{y}_1 \bar{y}_2)$$

$$= \bar{x}_1 (y_1 \oplus y_2)$$

We can also do this using K-maps and truth table;

	Y1Y2	00	01	11	10
X1	1	1			
X2	0	1			

$$Y_1' = \underline{\bar{x}_1 (y_1 \oplus y_2)}$$

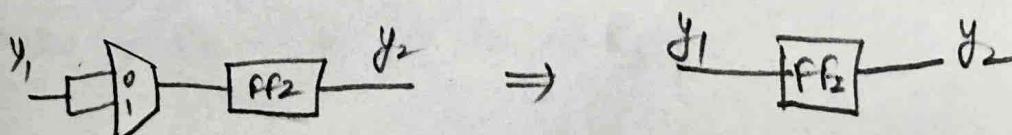
Truth table:

<u>X1</u>	<u>Y1</u>	<u>Y2</u>	<u>Y1'</u>
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

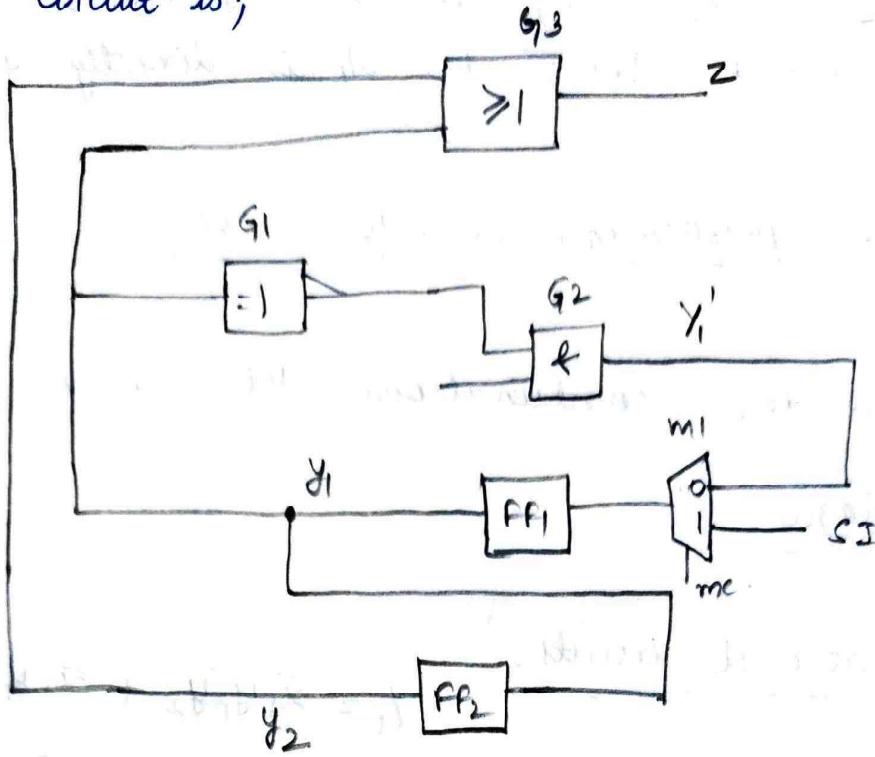
From the above boolean reduction



In F/F optimization, we can see that both the F/F's of  $MUX_{2 \times 1}$  ( $M_2$ ) connected to the same fan-in. So, we can eliminate  $MUX_2$ .



Redesigned circuit is,



The new critical path is :  $G_1$  (XOR)  $\rightarrow G_2$  (AND)  $\rightarrow \text{MUX } M_1(2\times 1)$

Critical Path Delay :  $2d + 2d + 3d = \underline{7d}$ .

Minimum Clock Period =  $\underline{7d}$ .

Performance Penalty of using full scan is ' $3d$ '. as mux  $2\times 1$  is still a part of critical path.

### c) Comparing Area Overheads:

Area of original full scan circuit

= 8 combinational elements (including mux).

= 2 PPs

= 10 elements

Area of reduced full scan circuit = 4 combinational elements  
 + 2 FF's (1 mux)  
 = 6 elements.

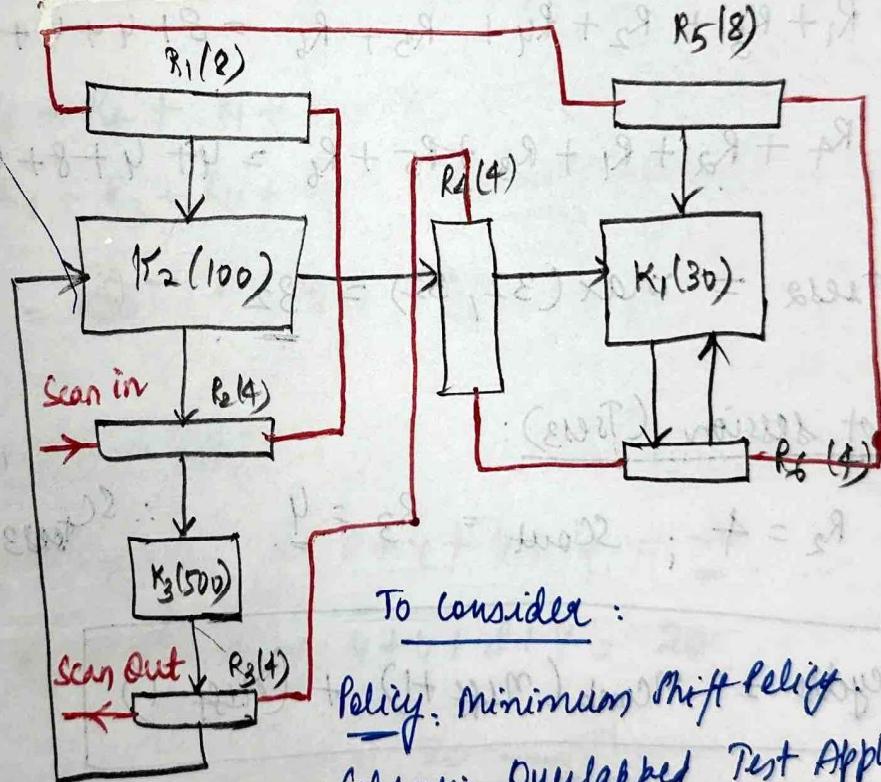
Area overhead = (-f) gate elements for the new circuit.

Performance of original circuit =  $9\alpha$

Performance of reduced circuit =  $7\alpha$

Performance penalty =  $(-\underline{2\alpha})$  for new circuit.

Solution 11.14:



To consider :

Policy: Minimum Shift Policy.

Scheme: Overlapped Test Application scheme

+ The best way to have the scan chain designed based on rules for minimum application time is;

$$R_2 \rightarrow R_1 \rightarrow R_5 \rightarrow R_6 \rightarrow R_4 \rightarrow R_3$$

For the 1<sup>st</sup> test session ( $T_{\text{sess}1}$ ):

$$SC_{\text{Test}} = \max (SC_{\text{in}}, SC_{\text{out}})$$

$$SC_{\text{in}} = R_5 + R_6 + R_4 + R_1 + R_2 + R_3 = 8 + 4 + 4 + 8 + 4 + 4 = 32$$

$$SC_{\text{out}} = R_6 + R_4 + R_3 = 4 + 4 + 4 = \underline{\underline{12}}$$

$$\therefore SC_{T_{\text{sess}1}} = \max (32, 12) = \underline{\underline{32}} \quad - ①$$

For 2<sup>nd</sup> test session ( $T_{\text{sess}2}$ ):

$$SC_{\text{in}} = R_1 + R_3 + R_2 + R_4 + R_5 + R_6 = 8 + 4 + 4 + 4 + 8 + 4 = \underline{\underline{32}}$$

$$SC_{\text{out}} = R_4 + R_2 + R_1 + R_3 + R_5 + R_6 = 4 + 4 + 8 + 4 + 8 + 4 = \underline{\underline{32}}$$

$$\therefore SC_{T_{\text{sess}2}} = \max (32, 32) = \underline{\underline{32}} \quad - ②$$

For 3<sup>rd</sup> test session ( $T_{\text{sess}3}$ ):

$$SC_{\text{in}} = R_2 = 4; SC_{\text{out}} = R_3 = 4. \quad \therefore SC_{T_{\text{sess}3}} = \max (4, 4) = \underline{\underline{4}}$$

$$\therefore \text{No. of cycles} = m_{\text{comb}} (m_{\text{eff}} + 1) + (m_{\text{eff}} - 1)$$

$$\therefore SC_{\text{Test}} = \max (32, 32, 4) = \underline{\underline{32}}$$

$$\therefore \text{Time} = \text{No. of cycles} = 30(32+1) + (100-30)(32+1) +$$

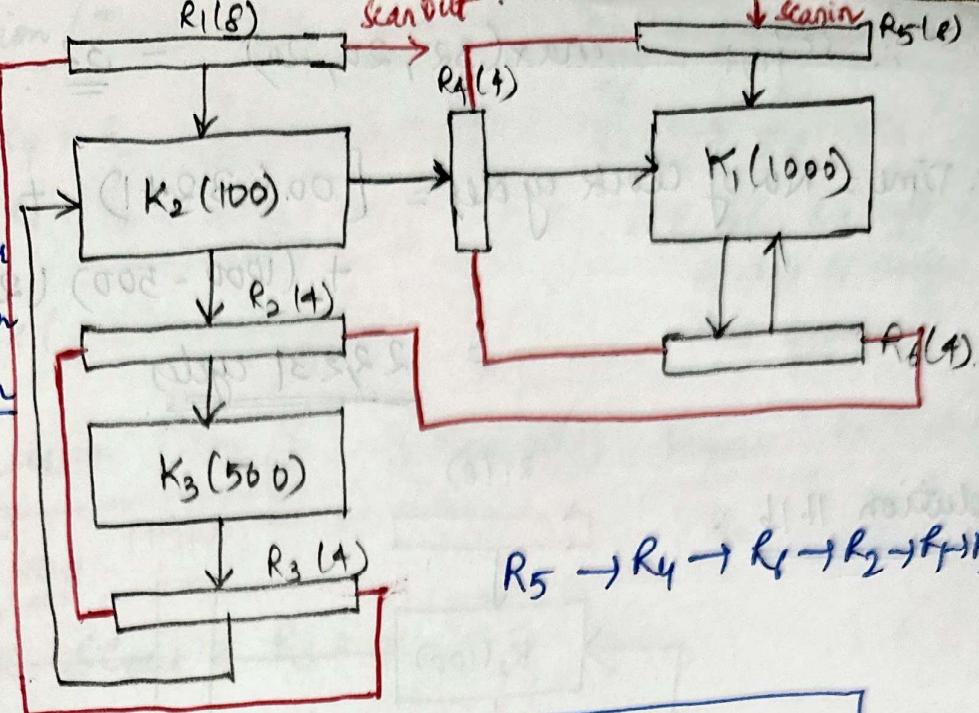
$$\begin{aligned} & (500-100)(4+1) + (32-1) \\ &= (30 \times 33) + (70 \times 33) + 5(400) + 31 \\ &= \underline{\underline{5331}} \text{ cycles} \end{aligned}$$

Solution 11.15:

To minimize the test application time under the overlapped test approach scheme & minimum shift policy, we have to rearrange the registers into single chain.

for 1<sup>st</sup> test session ( $T_{\text{test}}$ ):

$$SCT_{\text{test}} = \max(S_{\text{chain}}, S_{\text{carry}})$$



$$R_5 \rightarrow R_4 \rightarrow R_1 \rightarrow R_2 \rightarrow R_3$$

$$\begin{aligned} S_{\text{chain}} &= R_5 + R_6 + R_4 + R_1 + R_2 + R_3 = 8 + 4 + 8 + 4 + 4 + 4 = 32. \\ S_{\text{carry}} &= R_2 + R_1 + R_3 + R_4 + R_6 = 4 + 8 + 4 + 4 + 4 = 24. \\ \therefore SCT_{\text{test}} &= \max(32, 24) = 32. \quad \text{--- ①} \end{aligned}$$

For 2<sup>nd</sup> test session ( $T_{\text{test2}}$ ):

$$\begin{aligned} S_{\text{chain}} &= R_5 + R_6 + R_4 + R_2 = 8 + 4 + 4 + 4 = 20. \\ S_{\text{carry}} &= R_3 + R_6 + R_1 + R_2 = 4 + 4 + 8 + 4 = 20. \\ \therefore SCT_{\text{test2}} &= \max(20, 20) = 20. \quad \text{--- ②} \end{aligned}$$

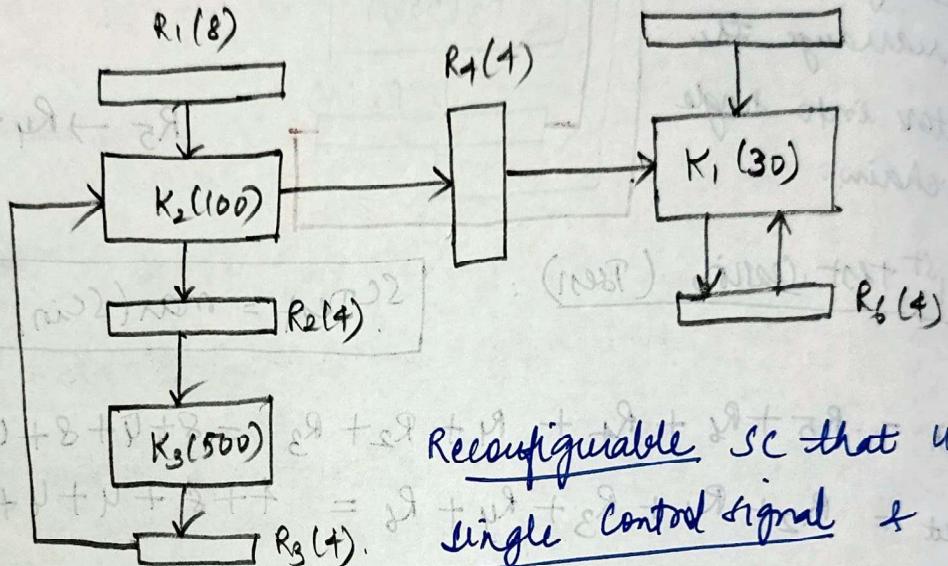
For 3<sup>rd</sup> test session ( $T_{\text{test3}}$ ):

$$\begin{aligned} S_{\text{chain}} &= R_5 + R_4 + R_6 = 8 + 4 + 4 = 16. \\ S_{\text{carry}} &= R_6 + R_3 + R_1 + R_2 = 4 + 4 + 8 + 4 = 20. \\ \therefore SCT_{\text{test3}} &= \max(16, 20) = 20. \quad \text{--- ③} \end{aligned}$$

$$\therefore S_{C_{\text{test}}} = \max(32, 20, 20) = \underline{\underline{32}}$$

$$\begin{aligned} \therefore \text{Time} &= \text{No. of clock cycles} = [100(32+1) + (500-100)(20+1) \\ &\quad + (1000-500)(20+1)] + [(32-1)] \\ &= \underline{\underline{23231 \text{ cycles}}}. \end{aligned}$$

Solution 11.1b :



Reconfigurable SC that uses single control signal &

minimizes the test application scheme and minimum Rift policy

The register arrangement is :   $R_2 \rightarrow R_1 \rightarrow R_5 \rightarrow R_6 \rightarrow R_9 \rightarrow R_3$ .

Reconfigurable chain is :  $R_2 \rightarrow R_1 \rightarrow R_5 \rightarrow R_6 \rightarrow R_9 \rightarrow R_3$

For the 1<sup>st</sup> test session ( $T_{\text{ses1}}$ ) :

$(K_1 = 30)$  :

Drivers	Receivers
$R_5$	$R_6$
$R_6$	
$R_1$	

$$S_{C_{in}} = R_5 + R_6 + R_4 + R_1 + R_2 + R_3 = 8 + 4 + 4 + 8 + 4 + 4 = \underline{\underline{32}}$$

$$S_{C_{out}} = R_6 + R_4 + R_3 = 4 + 4 + 4 = \underline{\underline{12}}$$

$$\therefore S_{C_{T_{\text{ses1}}}} = \max(32, 12) = \underline{\underline{32}}$$

For the 2nd test session ( $T_{test2}$ ): ( $K_2 = 100$ )

Drivers	Receivers
$R_1$	$R_2$
$R_3$	$R_4$

$$S_{in} = R_1 + R_3 + R_4 + K_2 = 8 + 4 + 4 + 100 = 120.$$

$$S_{out} = R_2 + R_4 + R_1 + R_3 = 4 + 4 + 8 + 4 = 20.$$

$$S_{CTest2} = \max(120, 20) = 120.$$

( $R_5$  &  $R_6$  are not needed as they are bypassed).

For the 3rd test session ( $T_{test3}$ ): ( $K_3 = 500$ )

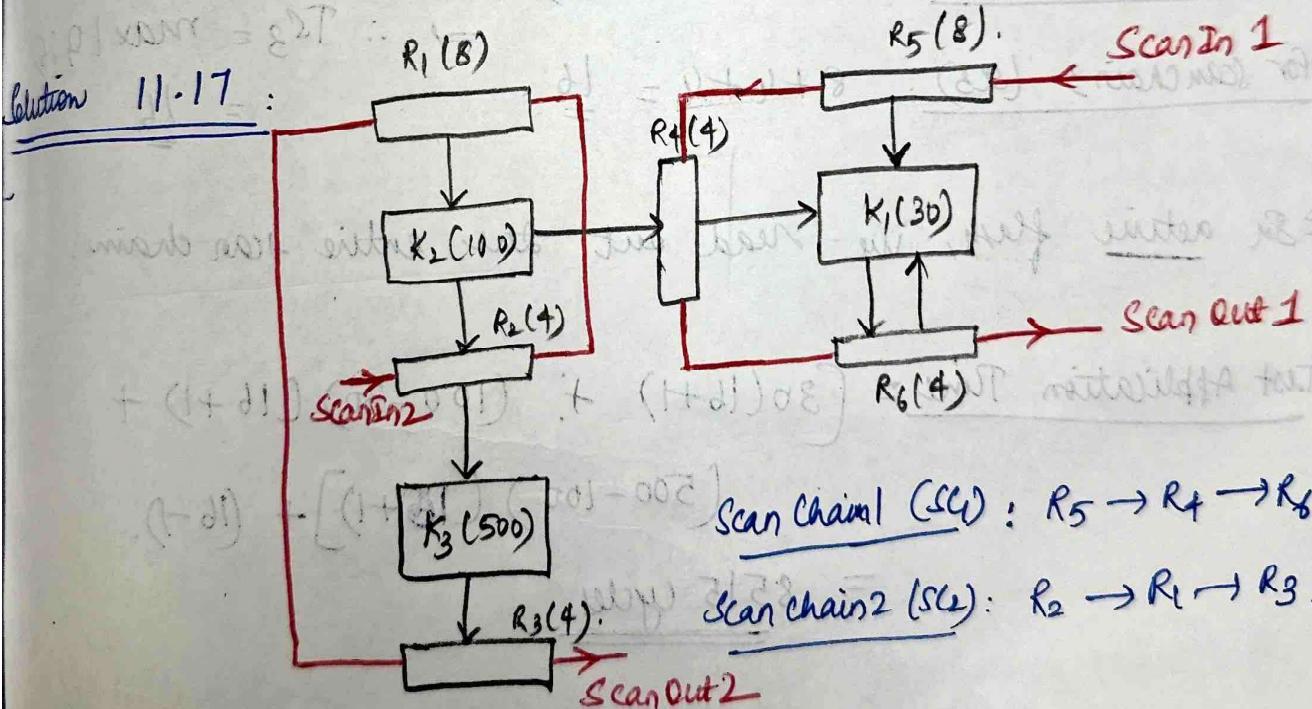
Drivers	Receivers
$R_2$	$R_3$

$$N_T = 500 - 100 = 400.$$

$$S_{in} = R_2 = 4 \quad ; \quad S_{out} = R_3 = 4.$$

$$S_{CTest3} = \max(4, 4) = 4.$$

Time = No. of clock cycles =  $\left[ 30(32+1) + 70(20+1) + 400(4+1) \right] + (32-1)$   
 $= 4491$  cycles



There are 3 Test Sessions and 2 Scanchains here.

Consider 2 approaches and check which is better with minimal time taken. (min. cycles).

For the 1<sup>st</sup> test session (TS<sub>1</sub>):

For ScanChain 1 (SC<sub>1</sub>):  $8+4+4 = \underline{\underline{16}}$ .  $\Rightarrow TS_1 = \max(1b, 1b) = \underline{\underline{1b}}$ .

For ScanChain 2 (SC<sub>2</sub>):  $8+4+4 = \underline{\underline{16}}$ .

For the 2<sup>nd</sup> test session (TS<sub>2</sub>):

For ScanChain 1 (SC<sub>1</sub>):  $8+4+4 = \underline{\underline{16}}$ .  $\Rightarrow TS_2 = \max(1b, 1b) = \underline{\underline{1b}}$ .

For ScanChain 2 (SC<sub>2</sub>):  $8+4+4 = \underline{\underline{16}}$ .

For the 3<sup>rd</sup> test session (TS<sub>3</sub>):

For ScanChain 1 (SC<sub>1</sub>): 0 (Not Active)

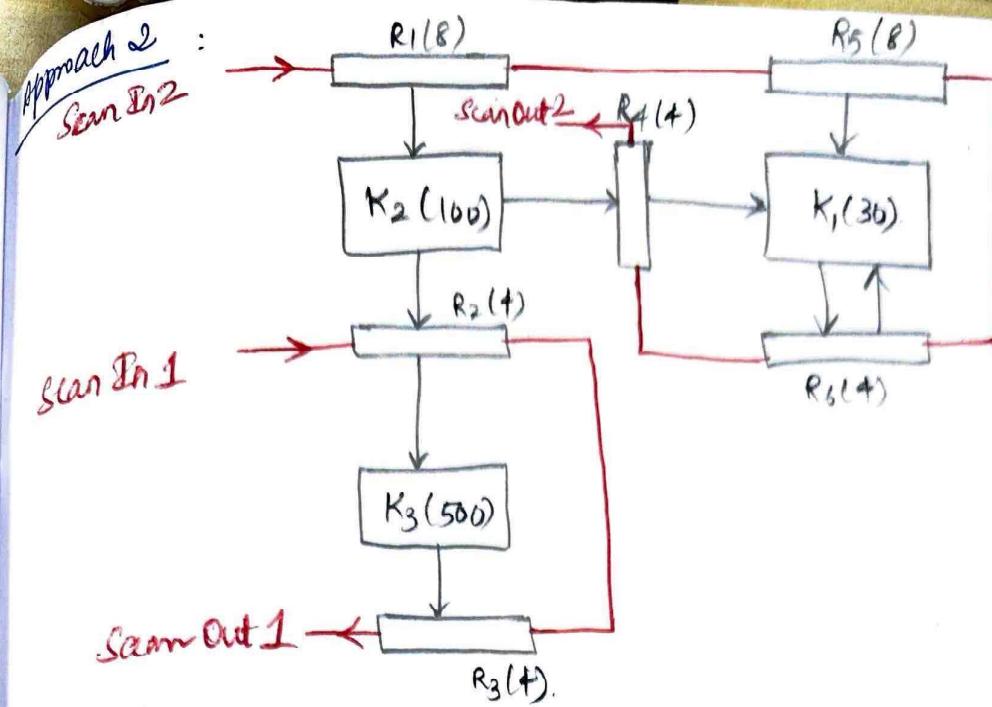
$\Rightarrow TS_3 = \max(0, 16) = \underline{\underline{16}}$ .

For ScanChain 3 (SC<sub>3</sub>):  $8+4+4 = \underline{\underline{16}}$ .

\* In active flash, we read out the entire scan chain.

$$\text{Test Application Time} = [30(16+1) + (100-30)(16+1) + (500-100)(16+1)] + (16-1).$$

$$= \underline{\underline{8515 \text{ cycles}}}$$



for the 1<sup>st</sup> test session ( $T_{\text{sess1}}$ ) :

for scanchain 1 (SC1) :  $SCL_1 = 8 + 4 = 12 \Rightarrow \max(8, 24) = \underline{\underline{24}}$ .

for scan chain 2 (SC2) :  $SCL_2 = 8 + 8 + 4 + 4 = 24$ .

for the 2<sup>nd</sup> test session ( $T_{\text{sess2}}$ ) :

for scanchain 1 (SC1) :  $SCL_1 = 4 + 4 = 8 \Rightarrow \max(8, 24) = \underline{\underline{24}}$ .

for scanchain 2 (SC2) :  $SCL_2 = 8 + 8 + 4 + 4 = 24$ .

for the 3<sup>rd</sup> test session ( $T_{\text{sess3}}$ ) :

for scanchain 1 (SC1) :  $SCL_1 = 4 + 4 = 8 \Rightarrow \max(8, 0) = \underline{\underline{8}}$ .

for scanchain 2 (SC2) :  $SCL_2 = 0$

∴ Test Application Time =  $\left[ 30(24+1) + (100-30)(24+1) + (500-100)(8+1) + (24-1) \right]$

$$= 750 + 1750 + 3600 + 23$$

$$= \underline{\underline{6123 \text{ cycles}}}$$