THE UNIVERSITY OF TEXAS AT DALLAS
Erik Jonsson School of Engineering and Computer Science
Department of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design

(Spring 2024, Tuesday and Thursday: 1:00 pm – 2:15 pm, ECSW 3.250)

1 General Information

Instructor:	Mehrdad Nourani
Office & Phone:	ECSN 4.924, 972-883-4391
E-mail (Webpage):	nourani@utdallas.edu (http://www.utdallas.edu/~nourani)
Office Hours:	Tuesday and Thursday 11:00 am – 12:00 pm, or by appointment;
Required Texts:	*Testing of Digital Systems*, Niraj Jha and Sandeep Gupta, Cambridge University Press, 2003.
Other References:	*VLSI Test Principles and Architectures*, L-T Wang, C-W Wu and X. Wen, Morgan Kaufmann, 2006. *Essentials of Electronic Testing*, Michael Bushnell and Vishwani Agrawal, Kluwer Academic Publishers, 2000.
Course Modality:	Traditional classroom/laboratory in-person instruction
Course Web Page:	http://elearning.utdallas.edu/
Teaching Assistant:	To be announced.

2 Catalog Description

EEDG/CE 6303 Testing and Testable Design (3 semester hours).
Testing and Testable Design (3 semester credit hours) Techniques for detection of failures in digital circuits and systems. Fault modeling and detection. Functional testing and algorithms for automatic test pattern generation (ATPG). Design of easily testable digital systems. Techniques for introducing built-in self test (BIST) capability. Test of various digital modules, such as PLA's, memory circuits, datapath, etc.
Prerequisites: EE 3320 or equivalent and background in VHDL/Verilog. (3-0) Y

3 Course Objective

The objective of this graduate level course is to introduce the testing methodologies for VLSI circuits and digital systems. We provide students with access to the CAD tools to use hardware description language to model, and perform fault simulation/analysis and test insertion for various digital circuits/systems. It is expected that the students will acquire a clear understanding of the main test strategies and the optimizations techniques for fault modeling, structural analysis, test pattern generation and design for testability. In particular, the following are the course learning objectives:

- **CLO1**: Understand the basic process and economics of VLSI testing and be able to work with failure mechanisms, fault models and fault simulations.
- **CLO2**: Ability to apply test pattern generation algorithms to combinational and sequential circuits.
- **CLO3**: Ability to apply algorithms for delay fault testing and memory test.
- **CLO4**: Understand the concepts and be able to apply design-for-test methodologies (scan and built-in-self test).
- **CLO5**: Ability to use hardware description languages and CAD tools for fault simulation, test pattern generation and test analysis

4 Grading

Grading will be based on three tests and several homeworks/projects as follows:

HWs/Projects:	25%	
Test 1:	25%	(Tues. 2/20/2024, 1:00 pm)
Test 2:	25%	(Thurs. 3/28/2024, 1:00 pm)
Test 3:	25%	(Thurs. 5/2/2024, 1:00 pm)

$85 \leq A- < 93$	$93 \leq A \leq 100$	
$70 \leq B- < 75$	$75 \leq B < 80$	$80 \leq B+ < 85$
$60 \leq C < 65$	$65 \leq C+ < 70$	
$0 \leq F < 60$		

Note: For M.S. degrees, a minimum grade of $B-$ in each and a minimum GPA of 3.0 for all "core" courses are required.

5 Course Policies

- Homeworks/projects will be assigned throughout the semester, and will be due approximately once every 2 weeks. All reports should be submitted through elearning.
- A homework/project is considered **late** if it is turned in after the due date/time. There will be 20% per day penalty for late homeworks up to 3 days excluding weekends and holidays. Late homeworks and reports won't be accepted after 3 days.
- No makeup tests/homeworks/projects will be offered in this course. Any graded work can be disputed in writing within one week of the return of that work. In such cases, the entire work will be regraded.
- Some of the homeworks are mini-projects and require programming or using CAD tools (mainly Synopsys toolset) for implementation, simulation and analysis. These tools are available remotely through remote login (e.g. using NX Client or Xmanager or NoMachine) to UTD servers. To have enough time start as early as possible.
- Copying on examinations, assignments and projects is cheating and is prohibited. Any instances of cheating or plagiarism is considered academic dishonesty and will be subject to disciplinary penalties according to the UT Dallas policy on scholastic dishonesty. The penalties include the possibility of failure in the course and/or dismissal from the University. Since such dishonesty harms the individual, all students and the integrity of the University, policies on scholastic dishonesty will be strictly enforced. Please read carefully this policy in **http://www.utdallas.edu/deanofstudents/dishonesty/**.
- There is no make-up test or homework in this course. Under exceptional circumstances (e.g. hospitalization), official documentation is required and the University policies and procedures will be followed.
- Announcements and complementary materials will be posted on the course web page. However, regular attendance and taking notes are highly recommended.

6 Syllabus & Tentative Lecture Plan

Weeks		*Readings*	*Topics Coverage*
Tues.	*Thur.*		
1/16		Ch 1	Introduction: course introduction; test technology evolution; cost of testing;
	1/18		linking design and test.IC testing: VLSI fabrication; testing at the IC level.
1/23		Ch 1	VLSI testing process: test process; automatic test equipment;
	1/25		Test economics: cost analysis; rule of ten; test data analysis; quality measure.
1/30*		Ch 2	Fault modeling: failure mechanisms and characteristics; fault detection
	2/1		and redundancy; fault equivalence and dominance; fault models.
2/6		Ch 4	Test generation for combinational circuits: boolean difference;
	2/8		D-algorithm; PODEM algorithm; testability measures.
2/13		Ch 3	Fault simulation techniques: serial, parallel, deductive and concurrent
	2/15*		fault simulations; fault sampling; statistical fault analysis.
2/20			**TEST 1** (selected topics of Ch 1–4).
	2/22	Ch 5	Test generation for sequential circuits: single clock synchronous model;
2/27			time-frame expansion method; difficulties in sequential circuit testing.
	2/29	Ch 8	Delay test: path delay testing; transition faults; at-speed testing.
3/5		Ch 14	Memory test: memory density and defects;
	3/7*		memory fault modeling;
3/12			**Spring Break – University Holiday**
	3/14		
3/19		Ch 14	March algorithms; testing RAM, ROM and cache.
	3/21		
3/26*		Ch 11	Design for testability: controllability and observability metrics;
	3/28		**TEST 2** (selected topics of Ch 5, 8, 14)
4/2		Ch 11	Boundary scan: full and partial scan;
	4/4		boundary scan standard; ad-hoc methods; variations of scan;
4/9			TAP Controller; test instructions BSD Language;
	4/11	Ch 12	Built-in self-test: BIST concept; test pattern generation for BIST;
4/16*		Ch 12	compression techniques; various BIST architectures; test point selection;
	4/18		memory BIST; delay fault BIST;
4/23		Ch 6	IDDQ test: target faults; testing methods; fault coverage metrics; current limit setting;
	4/25	Ch 16	System test and core based design: using embedded microprocessor in testing;
4/30*		literature	core-based design and test; SoC test architecture; test for signal integrity;
	5/2		**TEST 3** (selected topics of Ch 6, 11, 12, 16 and literature).

Notes: Some topics in this course syllabus are not fully covered in any text book. Dates with "*" indicate likely due dates of homework.

7 Comet Creed

This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same: **"As a Comet, I pledge honesty, integrity, and service in all that I do."**

8 UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus. Please go to **http://go.utdallas.edu/syllabus-policies** for these policies.

The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.