The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design

HW # 6: *Due on Tuesday 4/30/2024 - 11:59 pm (US CST)*

(To prepare for Test 3, the solutions will be posted on 4/31/2024. **No late homework will be accepted.***)*

When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

1. Chapter 12: 1, 8, 13, 22, 24.

2. Draw the circuits of the following six 8-bit designs using the primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$: [1] Internal-XOR LFSR, [2] External-XOR LFSR, [3] Complete LFSR (that produces also zero-state), [4] Weighted LFSR (that produces weights of 0.875, 0.75, 0.625, 0.5, 0.375, 0.25, 0.125), [5] MISR and [6] BILBO. In a table summarize characteristics of these circuits (e.g. estimate of components count/cost, worst case delay). Implementing these circuits using Synopsys is optional and not required.

3. Analyze circuit [1] above and show the first 10 pseudo-random patterns generated assuming the initial value of LFSR is all-1. You have an option to use either Synopsys or matrix/vector MOD 2 calculations (hand-driven or a short script/program) as explained in the slides. Explain your approach and include the details.

4. Consider the circuit under test (CUT) is a 4-bit unsigned multiplier unit that receives $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$ as inputs and produces $Z = z_7z_6z_5z_4z_3z_2z_1z_0$ as outputs such that $Z = X * Y$. For uniformity, assume that $x_3x_2x_1x_0y_3y_2y_1y_0$ are connected in order to $e_7e_6e_5e_4e_3e_2e_1e_0$ the outputs of 8-bit LFSR, respectively. Similarly, assume that eight outputs $z_7z_6z_5z_4z_3z_2z_1z_0$ are connected in order to $d_7d_6d_5d_4d_3d_2d_1d_0$ of the 8-bit MISR (circuit [5] above), respectively.

   Suppose the first 10 pseudo-random patterns that you found in previous part are used to test the CUT. Find the fault-free 8-bit signature assuming the initial value of MISR is all-0.

   Note: You need to first apply 10 8-bit patterns to the CUT and find 10 8-bit outputs. Then, find the result of compacting the outputs using the MISR. The final signature will be 8-bit content of MISR at the end. You have an option to use either an implementation in Synopsys or matrix/vector MOD 2 calculations (hand-driven or a short script/program) as explained in the slides. Explain your approach and include the details.