The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design
HW # 5: *Due on Tuesday 4/16/2024 - 11:59 pm (US CST)*

When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

1. Chapter 11: 5, 14, 15, 16, 17.

2. This problem is for working on a design-for-testability (scan) method using **Synopsys**.

   (i) Design the circuit shown in Figure 11.58 using three D Flip-Flops without set/reset.

   (ii) Isolate only the combinational part(s) of the circuit and use Synopsys tool to generate a set of test vectors that detect all single SAFs in the combinational part(s). Note that the isolated combinational part will have 4 inputs (primary input x and three briken feedback lines y_1, y_2, y_3) and 4 outputs (primary output z and three broken feedback lines Y_1, Y_2, Y_3). Show Synopsys reports including synthesis, schematic and the patterns found by ATPG.

   (iii) Use Synopsys Design Compiler to design the complete circuit (combinational plus flips-flops). Then, use Synopsys to automatically replace flip-flops with the scan flip-flops to build one scan chain. Report schematic, simulation results and design characteristics (e.g., area and delay) before and after scan insertion.

   (iv) Use Synopsys Tetramax to perform ATPG on both variants of the circuit, i.e. one with regular flip-flops and the other with scan flip-flops. Comment on the differences in results. Show Synopsys reports.