EEDG/CE 6303: Testing and Testable Design

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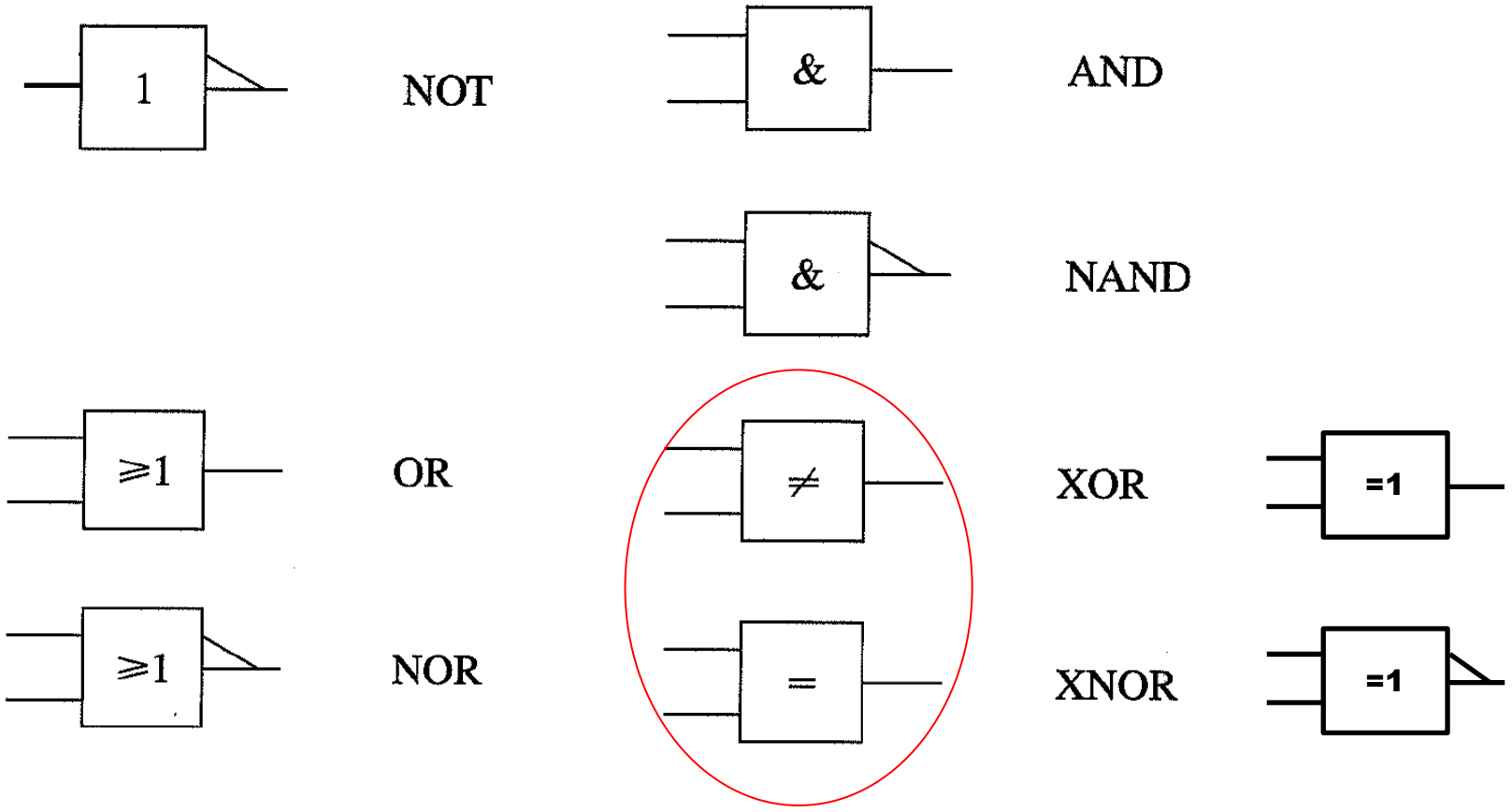
Session 02

Fault Modeling

Main Fault Models

IEEE Gate Symbols

- In some of the examples, the standard IEEE symbols of the logic gates will be used



Goals of Fault Modeling

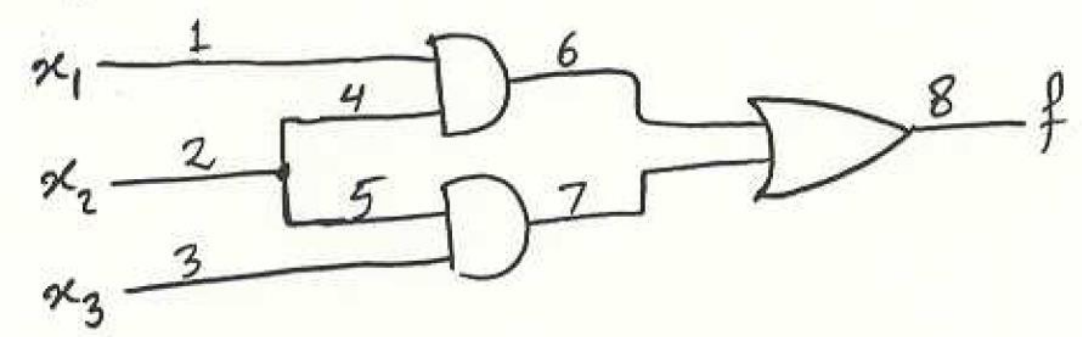
- To model physical defects in the circuit at high level of abstraction.
- To allow test generation and fault/coverage analysis to be done early in the design process.
- To model high percentage of the actual physical defects that can occur in components:
  - —To reduce number of individual defects that have to be considered (e.g. find equivalent or dominant faults).
  - —To reduce the complexity of the component/circuit description for test generation/analysis.

Stuck-at Fault Model

- Most commonly used fault model.
- May consider "single" or "multiple" stuck-at faults.
- The components are assumed to be (internally) fault-free.
- The effect of faults is modeled by having a line segment tied to either:
  - Vcc (s-a-1)
  - GND (s-a-0)

Stuck-at Fault Model (cont'd)

- Example:



- Fault-free function: $f = x_1x_2 + x_2x_3$
- Faulty functions:
  - Fault 1@0 → $f^* = x_2x_3$
  - Fault 2@1 → $f^* = x_1 + x_3$
  - Fault 6@0 → $f^* = x_2x_3$

Line Segment

Stuck-at Value

Features of Single s-a-f Model

- Can be applied at the logic/RTL/system levels.
- Reasonable and manageable number of faults (i.e. less or equal 2 * # of line segments ≈ 2 * # of circuit nodes). So, is computationally feasible to deal with.
- Well-developed algorithms exist for automatic test patter generation (ATPG)
- Other useful fault models like stuck-open, bridging, etc. can be applied into (sequence of) stuck-at faults

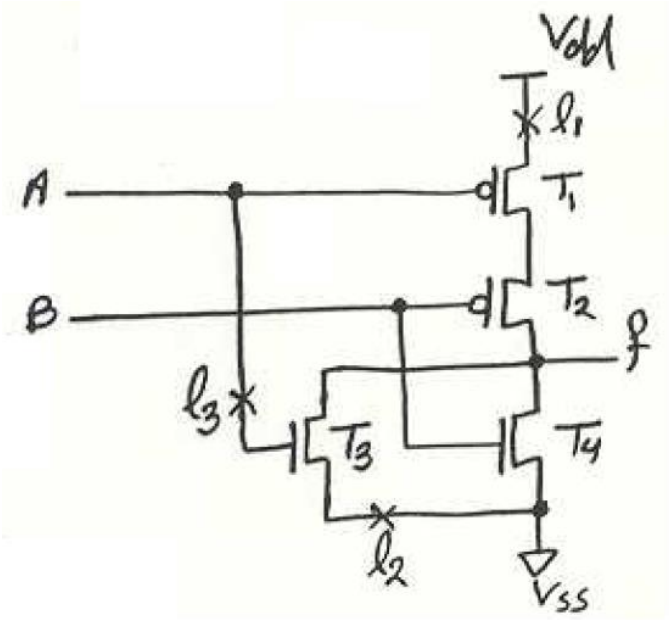
Features of Single s-a-f Model (cont'd)

- Empirical evidence shows that single stuck-at fault model covers the majority (about 90%) of the possible manufacturing defects in circuits such as:
  - Source-drain shorts
  - Oxide pinholes
  - Diffusion contaminants
  - Metallization shorts
  - …

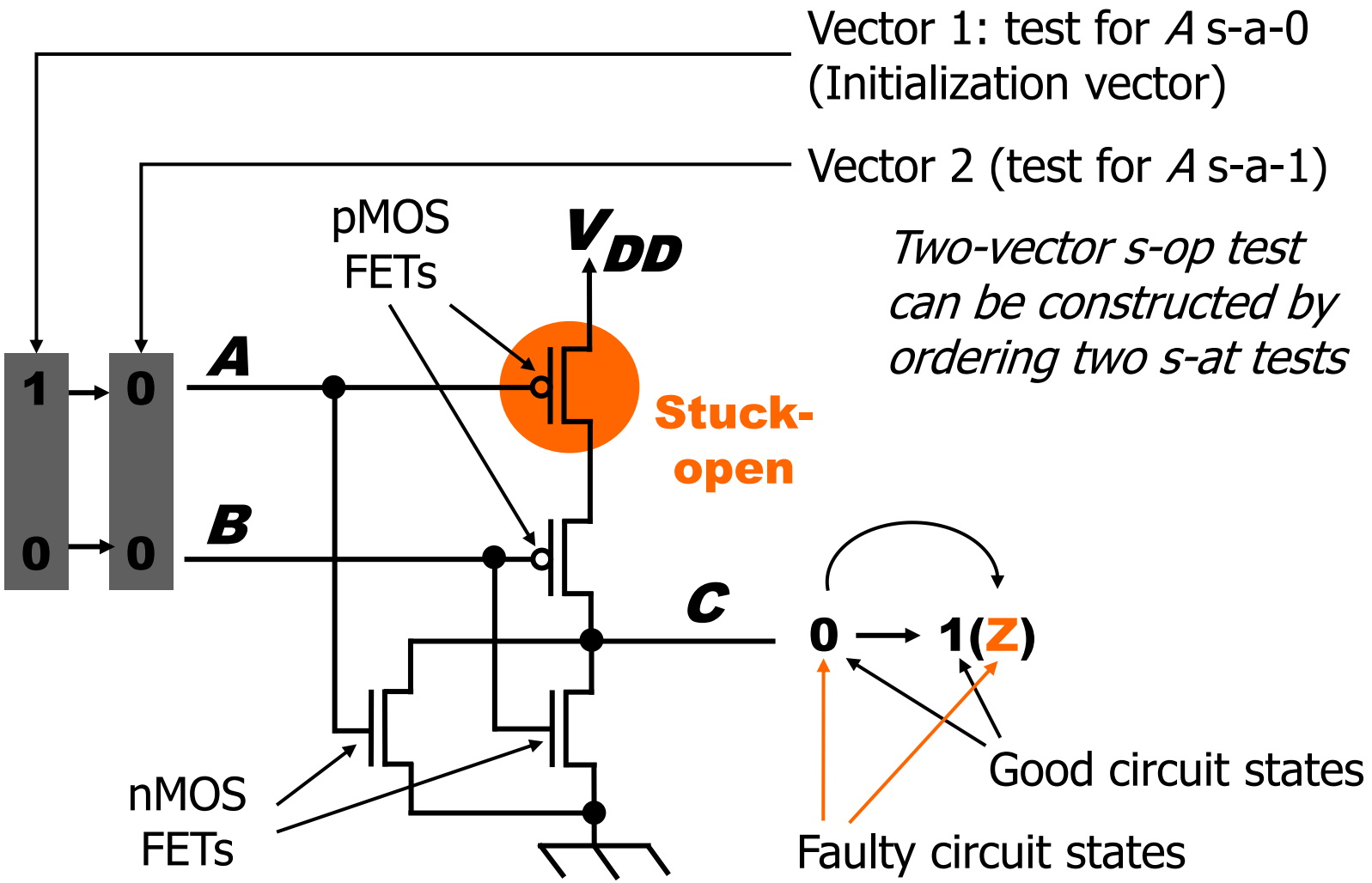
Stuck-Open Fault Model

- The main assumption in this model is that a single physical line in the circuit is broken (usually internal to gates).
- In CMOS circuit, a broken line may result in a "memory effect".
- Example:

  A CMOS NOR gate



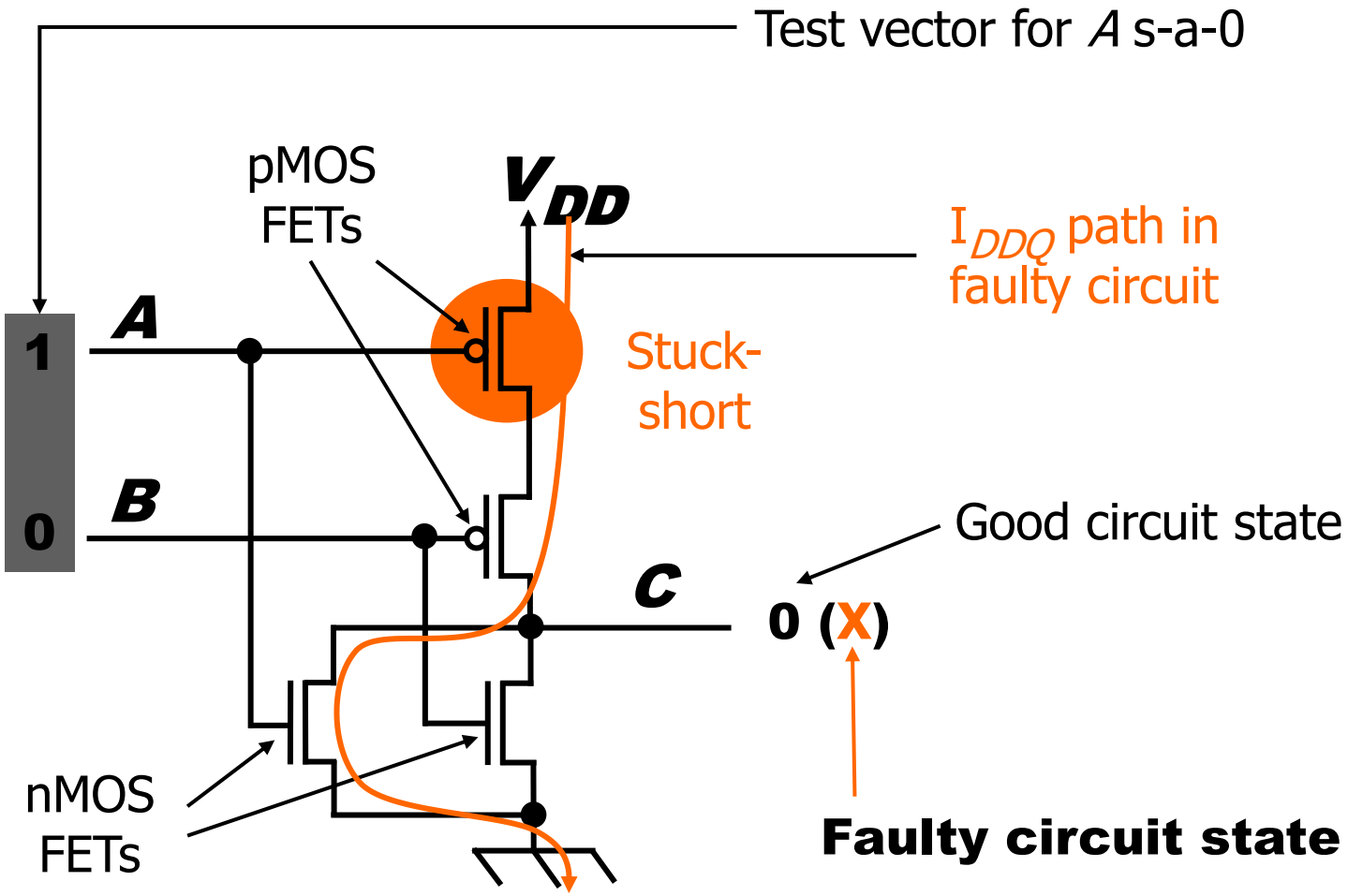
Stuck-Open Example (cont'd)



Stuck-Open Fault Model (cont'd)

- This model covers physical defects not covered by stuck-at fault model
- These faults can be tested with sequences of stuck-at fault tests. In previous example we used "10"-"00" sequence on AB to detect stuck-open.
- This model requires a larger number of tests compared to s-a-f model.
- Algorithms for ATPG and fault simulation are complex
- Transistor-level description is needed to generate the fault list.

Stuck-Short Example

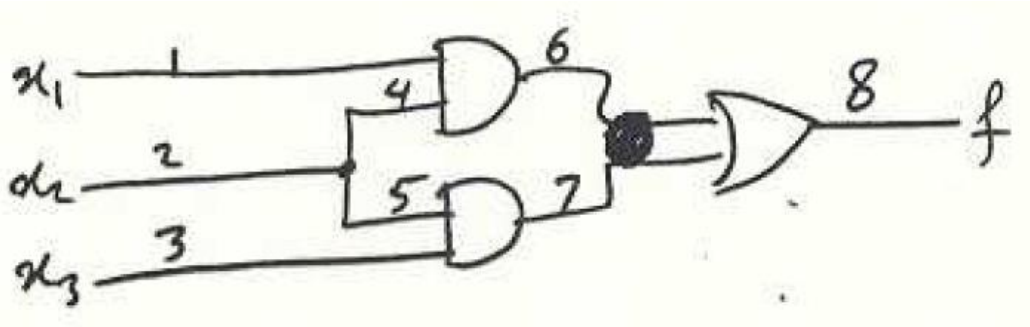


Bridging Fault Model

- Occurs when two (or more) lines are shorted together.
- The functional effect (on the logic nodes) is of a wired logic AND or OR depending on the technology
- Example:
  - Fault-free:

    $f = x_1x_2 + x_2x_3$
  - Faulty:

    $f = x_1x_2x_3$



Bridging Fault Model (cont'd)

- Three classes of bridging faults:
  1. Within a logic gate (e.g. transistor gate, drain, source shorted)
  2. Between logic nodes (e.g. inputs or outputs of logic elements)
  3. Between logic nodes with feedback
- The focus is usually on stuck-at "neighbor" faults between adjacent lines only to reduce complexity
- Requires a lower level (e.g. layout) information to produce the fault list or to analyze them

Bridging Fault Model (cont'd)

- Some research indicates up to 30% of all faults could be bridges.
- Single s-a-f methods can capture some of bridging faults.
- Testing requires setting the two bridged nodes to opposite values and observing the effect. This makes ATPG more complex.

Delay Fault Model

- Basic assumptions:
  - The logic function of the circuit-under-test is error-free.
  - Some physical defects (developed during fabrication) makes some delays in the circuit greater than some predefined bonds.

- Two delay fault models:
  1. Transitional delay fault (a single gate delay violates the bound)
  2. Path delay fault (certain path is too long)

Delay Fault Model (cont'd)

- Transitional delay fault:
  - A logical model for defects that delays either "slow-to-rise" or "slow-to-fall".
  - If a delay fault is large enough, it behaves as a temporary stuck-at fault and single s-a-f techniques can be applied.
  - The minimum delay fault size that can be detected is difficult to determine, especially when hazards are also present.
  - Two patterns are required for fault detection:
    1. For initialization
    2. For detection

Delay Fault Model (cont'd)

- Path delay fault:
  - —Total delays in a path from primary inputs (PI) to primary outputs (PO) is checked to see if it exceeds some predefined maximum value.
  - —Detects more delay faults than transitional delay.
  - —In transitional delay fault model, the delay of a faulty gate maybe compensated for by other faster gates in the path.
  - —It is consistent with a statistical design philosophy that recognizes that gate delays are not usually all "worst case" but they all fall within a range
  - —It deals with large number of paths and thus is a complex/slow process.

Fault Analysis System