# The University of Texas at Dallas
# Dept. of Electrical and Computer Engineering

## EEDG/CE 6303: Testing and Testable Design
**HW # 3:** *Due on Thursday 3/7/2024 - 11:59 pm (US CST)*

*When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:*

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

1. Consider Figure 5.5 in your book. Assume FF is a D flip-flop without any set/reset line. Analyze this sequential circuit for 4 stuck-at faults: (i) $x_1$ s-a-0, (ii) $x_1$ s-a-1, (iii) $x_2$ s-a-0, (iv) $x_2$ s-a-1.

2. Consider Figure 5.27 in your book. Assume FF is a D flip-flop without any set/reset line. Analyze this sequential circuit for 4 stuck-at faults: (i) $x_1$ s-a-0, (ii) $x_1$ s-a-1, (iii) $x_2$ s-a-0, (iv) $x_2$ s-a-1.

3. Consider Figure 5.5 in your book. Use Synopsys toolset to implement two versions of it: (i) with D-FF without any set/reset, and (ii) with D-FF with set/reset. Run ATPG for sequential circuits in Tetramax on both versions and report and discuss the results.

   **Note 1:** Gate library gtech_lib.v file has different types of DFFs. As problems ask, select appropriate DFF with and without set and reset pins.

   **Note 2:** Your report should include HDL (VHDL or Verilog) description, schematic of the circuit, some simulations to show the correct behavior, test analysis by Tetramax (e.g. faults, test patterns) and any other interesting observations.

4. Consider Figure 8.13 in your book. Find the (a) robust and (b) non-robust test patterns for the following **path delay** faults: (i) $\uparrow x_3c_2c_3z$, (ii) $\downarrow x_3c_2c_3z$, Total of 4 cases need to be considered.

5. Consider Figure 8.20 in your book. Find the (a) robust and (b) non-robust test patterns for the following **path delay** faults: (i) $\uparrow x_3c_2c_3c_4c_6z$, (ii) $\downarrow x_3c_2c_3c_4c_6z$, Total of 4 cases need to be considered.

6. Consider the circuit of Figure 8.13 and path delay faults. Use Synopsys toolset to implement the circuit and find robust and non-robust test patterns. A short guide for path delay fault testing is at the end of Test Tutorial in the course webpage. Report and discuss the results.