

台科大

PA1

Computer Organization

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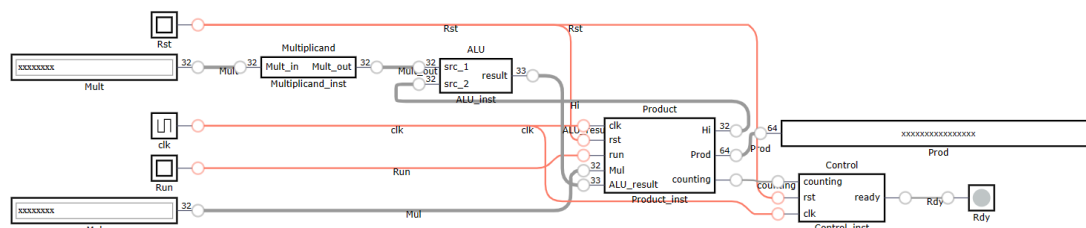
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# Multiplier

## CompMultiplier

```
1  module CompMultiplier (  
2      output [63:0] Prod,  
3      output Rdy,  
4      input [31:0] Mult,  
5      input [31:0] Mul,  
6      input Run,  
7      input Rst,  
8      input clk  
9  );  
10  
11      wire [31:0] Hi;  
12      wire [32:0] ALU_result;  
13      wire [31:0] Mult_out;  
14      wire counting;  
15  
16      ALU ALU_inst (  
17          .src_1(Mult_out),  
18          .src_2(Hi),  
19          .result(ALU_result)  
20      );  
21  
22      Multiplicand Multiplicand_inst (  
23          .Mult_in(Mult),  
24          .Mult_out(Mult_out)  
25      );  
26  
27      Control Control_inst (  
28          .counting(counting),  
29          .rst(Rst),  
30          .clk(clk),  
31          .ready(Rdy)  
32      );  
33  
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45  endmodule
```



## Description

This module is to connect all the small components to form a functional multiplier.

## Details

Line 1~9

I/O Interface.

Signal Symbol	Signal Name	Signal Description
<b>Prod</b>	64-bit calculation result	This signal is set as an output before the <a href="#">Rdy</a> signal is activated to forbid the testbench to read the previous calculation result.
<b>Rdy</b>	completion signal	The “high” level represents the system has completed multiplication and maintained the result.
<b>Mult</b>	32-bit multiplicand	The signal is generated by the testbench and updated when the <a href="#">Rst</a> signal is “high”.
<b>Mul</b>	32-bit multiplier	The signal is generated by the testbench and updated when the <a href="#">Rst</a> signal is “high”.
<b>Run</b>	execution signal	The system performs multiplication as the Run signal is “high” level.
<b>Rst</b>	initialization signal	The “high” level indicates that the system is initialized before multiplication, and the output results are set to zero. This signal has the highest priority and is generated by the testbench.

<b>clk</b>	clock signal	Periodic square waves are generated by the testbench for synchronizing each signal with the drive system.
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Line 11~14

Wires used in this module.

Wire Symbol	Wire Name	Wire Description
<b>Hi</b>	HI register	Upper 32 bits of the product. Used to pass data to ALU.
<b>ALU_result</b>	33 bits ALU result. This sees overflow as the 33th bit.	The computation result of ALU.
<b>Mult_out</b>	32-bit multiplicand	The signal is generated by the testbench and updated when the <a href="#">Rst</a> signal is “high”.
<b>counting</b>	Counting flag	Tell Control to start. This will avoid racing condition.

Line 16~43

Component instances.

Instance Name	Component Name	Instance Description
<b>ALU_inst</b>	<a href="#">ALU</a> instance	src_1 gets data from <a href="#">Mult_out</a> , src_2 gets data from <a href="#">Hi</a> , result is the output of this ALU, connected to <a href="#">ALU_result</a> .
<b>Multiplicand_inst</b>	<a href="#">Multiplicand</a> instance	Mult_in gets data from <a href="#">Mult</a> , Mult_out sets output to <a href="#">Mult_out</a> .
<b>Control_inst</b>	<a href="#">Control</a> instance	counting gets data from Product, rst gets data from <a href="#">Rst</a> , clk gets data from <a href="#">clk</a> , ready sets output to <a href="#">Rdy</a> .

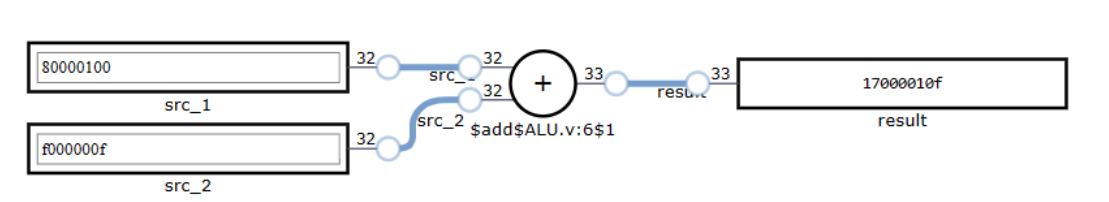
<b>Product_inst</b>	<a href="#">Product</a> instance	<p>clk gets data from <a href="#">clk</a>, rst gets data from <a href="#">Rst</a>, run gets data from <a href="#">Run</a>, Mul gets data from <a href="#">Mul</a> on the posedge of <a href="#">Run</a>, ALU_result gets data from <a href="#">ALU_result</a>, Hi outputs data to <a href="#">Hi</a>, Prod generates output to <a href="#">Prod</a>. And last but not least it gives counting to Control.</p>
---------------------	----------------------------------	---

# ALU

```

1  module ALU (
2      input [31:0] src_1,
3      input [31:0] src_2,
4      output [32:0] result
5  );
6      assign result = src_1 + src_2;
7  endmodule

```



## Description

This module provides basic arithmetic functions that fulfills multiplier’s needs.

## Detail

Line 1~5

I/O Interface.

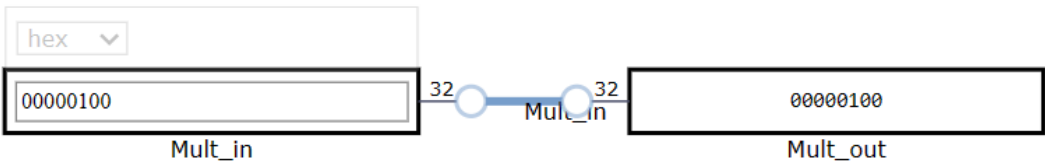
Signal Symbol	Signal Name	Signal Description
<b>src_1</b>	32-bits Source 1	addend
<b>src_2</b>	32-bits Source 2	augend
<b>result</b>	33-bits addition result	Sum with 1 overflow bit

Line 6

Wire connection that represents  $\text{result} = \text{src\_1} + \text{src\_2}$ .

# Multiplicand

```
1 module Multiplicand (  
2     ✦ input [31:0] Mult_in,  
3     output [31:0] Mult_out  
4 );  
5     assign Mult_out = Mult_in;  
6  
7 endmodule
```



## Description

Dummy module. Mult signal is given all along between the 2 posedge of Rst. There is no need to do any other operation.

## Detail

Line 1~4

I/O Interface.

Signal Symbol	Signal Name	Signal Description
<b>Mult_in</b>	In direction of Mult	In
<b>Mult_out</b>	Out direction of Mult	out

Line 5

Wire connection that denotes  $\text{Mult\_out} = \text{Mult\_in}$ .

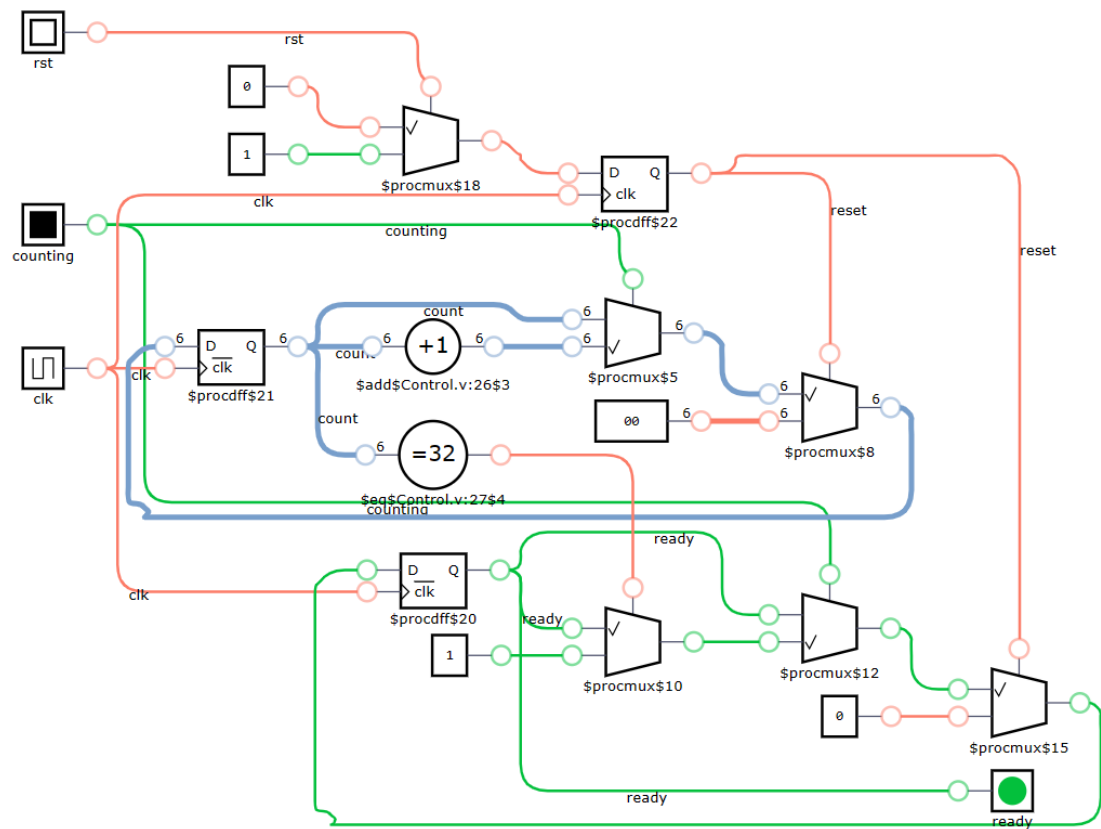


# Control

```

1  module Control (
2      input counting,
3      input rst,
4      input clk,
5      output reg ready
6  );
7
8      reg [5:0] count;
9      reg reset;
10
11     always @(posedge clk) begin
12         if (rst) begin
13             reset <= 1;
14         end
15         else begin
16             reset <= 0;
17         end
18     end
19
20     always @(negedge clk) begin
21         if (reset) begin
22             count <= 0;
23             ready <= 0;
24         end
25         else if (counting) begin
26             count <= count + 1;
27             if (count == 32) begin
28                 ready <= 1;
29             end
30         end
31     end
32
33 endmodule

```



## Description

A counter with a flag.

## Detail

Line 1~6

I/O Interface.

Signal Symbol	Signal Name	Signal Description
<b>counting</b>	Counting flag	The flag telling Control to count.
<b>rst</b>	initialization signal	The “high” level indicates that the system is initialized before multiplication, and the output results are set to zero. This signal has the highest priority and is generated by the testbench.
<b>clk</b>		Periodic square waves are generated by the testbench for synchronizing each signal with the drive system.
<b>ready</b>	Ready flag	Signify the end of the sequence of operation.

Line 11~18

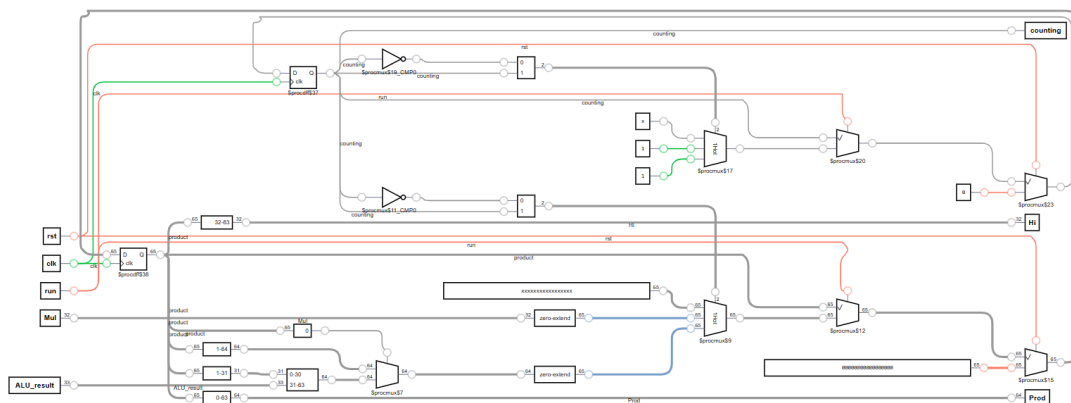
Use reset register to hold rst signal between 2 posedge clk to avoid racing.

Line 20~31

When running count 32 negedges of clk then set ready flag to notify other component to stop or fetch data.

# Product

```
1  module Product (  
2      input clk,  
3      input rst,  
4      input run,  
5      input [31:0] Mul,  
6      input [32:0] ALU_result,  
7      output [31:0] Hi,  
8      output [63:0] Prod,  
9      output counting  
10 );  
11     reg state;  
12     reg [64:0] product;  
13  
14     assign Hi = product[63:32];  
15     assign Prod = product[63:0];  
16     assign counting = state;  
17  
18     always @(posedge clk) begin  
19         if (rst) begin  
20             state <= 0;  
21             product <= 0;  
22         end  
23         else if (run) begin  
24             case (state)  
25                 0: begin // init state: Load Mul into product  
26                     product <= {33'b0, Mul};  
27                     state <= 1;  
28                 end  
29                 1: begin // run state: Multiply  
30                     if (product[0]) begin  
31                         product <= {1'b0, ALU_result, product[31:1]};  
32                     end  
33                     else begin  
34                         product <= {1'b0, product[64:1]};  
35                     end  
36                     state <= 1;  
37                 end  
38             endcase  
39         end  
end
```



## Description

Main module. I use 65 bits representing product in order to handle overflowing result from [ALU](#). The computation is executed on posedge clk to avoid racing condition. And I use counting, which is a flag to tell Control to count. This flag will effective avoid racing.

## Detail

Line 1~10

I/O Interface.

Signal Symbol	Signal Name	Signal Description
clk	clock	Clock
rst	reset	Reset the init state
run	Execution signal	Run operations when high
Mul	32-bits multiplicand	Init will put this to LO
ALU_result	33-bits ALU result	With 1 more carry bit
Hi	HI	Upper 32 bits
Prod	production	64-bits result
counting	Counting flag	Used to avoid racing

Line 11~12

Registers

Register Symbol	Register Name	Register Description
state	state	FSM state
product	65-bits product	1 more bit for overflow result generated by <a href="#">ALU</a> .

Line 14~16

Wire connection of [Hi](#), [Prod](#) and counting.

Line 19~22

Reset.

Line 24~38

FSM

State Symbol	State Name	State Description
0	Init	HI = 0, LO = <a href="#">Mul</a>
1	run	Examine LSB to do predefined <a href="#">operations</a> .

Line 30~36

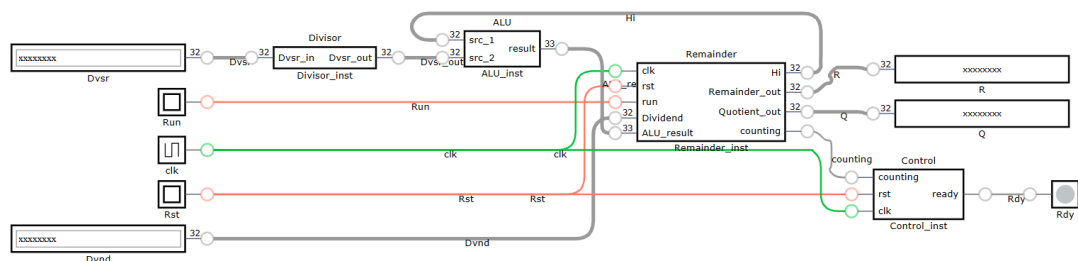
If LSB is set, write ALU\_result to HI and shift right 1 bit.

Else, shift right 1 bit.

# Divider

## CompDivider

```
1  module CompDivider (  
2      output [31:0] Q,  
3      output [31:0] R,  
4      output Rdy,  
5      input [31:0] Dvnd,  
6      input [31:0] Dvsr,  
7      input Run,  
8      input Rst,  
9      input clk  
10 );  
11 wire [32:0] ALU_result;  
12 wire [31:0] Dvsr_out;  
13 wire [31:0] Hi;  
14 wire counting;  
15  
16 ALU ALU_inst (  
17     .src_1(Hi),  
18     .src_2(Dvsr_out),  
19     .result(ALU_result)  
20 );  
21  
22 Divisor Divisor_inst (  
23     .Dvsr_in(Dvsr),  
24     .Dvsr_out(Dvsr_out)  
25 );  
26  
27 Control Control_inst (  
28     .counting(counting),  
29     .rst(Rst),  
30     .clk(clk),  
31     .ready(Rdy)  
32 );  
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995  
996  
997  
998  
999  
1000
```



## Description

This module is to connect all the small components to form a functional divider.

## Detail

Line 1~10

I/O Interface.

Signal Symbol	Signal Name	Signal Description
<b>Q</b>	32-bit Quotient	Quotient result
<b>R</b>	32-bit Remainder	Remainder result
<b>Rdy</b>	completion signal	Iff it's set the, result is valid
<b>Dvnd</b>	32-bit Dividend	Input
<b>Dvsr</b>	32-bit Divisor	Input
<b>Run</b>	execution signal	Start execute when high
<b>Rst</b>	initialization signal	Reset
<b>clk</b>	clock signal	clock

Line 11~14

Wires used in this module.

Wire Symbol	Wire Name	Wire Description
<b>ALU_result</b>	33-bits ALU out	With 1 carry bit
<b>Dvsr_out</b>	Divisor out	Dummy connection
<b>Hi</b>	HI register	Upper 32 bits
<b>counting</b>	Counting flag	Used to avoid racing.

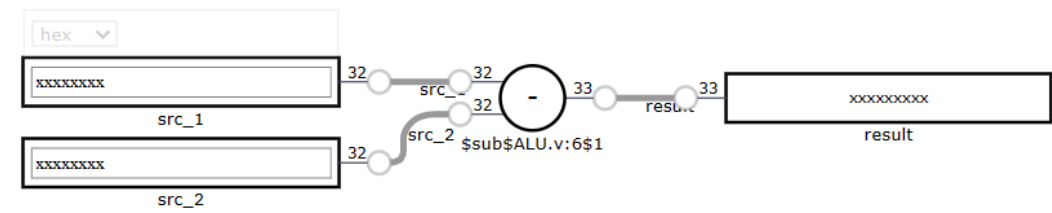
Line 16~44

Component instances.

Instance Symbol	Instance Name	Instance Description
<b>ALU_inst</b>	<a href="#">ALU</a> instance	Output to <a href="#">ALU_result</a> considering <a href="#">R</a> , <a href="#">Dvsr_out</a>
<b>Divisor_inst</b>	<a href="#">Divisor</a> instance	Dummy
<b>Control_inst</b>	<a href="#">Control</a> instance	Counter with <a href="#">Rdy</a> flag.
<b>Remainder_inst</b>	<a href="#">Remainder</a> instance	1 clk, 2 flags, 2 in, 4 out. For more detail <a href="#">click me</a> .

# ALU

```
1 module ALU (  
2     input [31:0] src_1,  
3     input [31:0] src_2,  
4     output [32:0] result  
5 );  
6     assign result = src_1 - src_2;  
7 endmodule
```



## Description

This module provides basic arithmetic functions that fulfills divider’s needs.

## Detail

Line 1~5

I/O Interface.

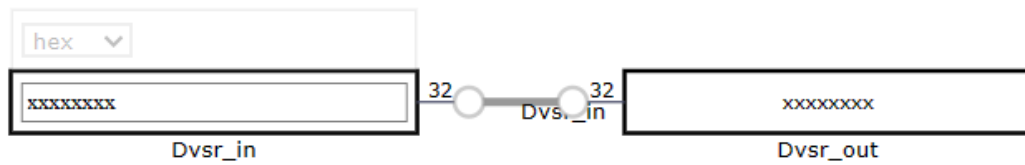
Signal Symbol	Signal Name	Signal Description
src_1	32-bits source 1	Minuend
src_2	32-bits source 2	subtrahend
result	33-bits result	Difference, 1 more borrow bit

Line 6

Wire connection symbolize  $\text{result} = \text{src\_1} - \text{src2}$ .

## Divisor

```
1 module Divisor (  
2     input [31:0] Dvsr_in,  
3     output [31:0] Dvsr_out  
4 );  
5     assign Dvsr_out = Dvsr_in;  
6 endmodule
```



## Description

Dummy

## Detail

Line 1~4

I/O Interface.

Signal Symbol	Signal Name	Signal Description
<b>Dvsr_in</b>	Divisor in	In
<b>Dvsr_out</b>	Divisor out	out

Line 5

Wire connection to make out = in.

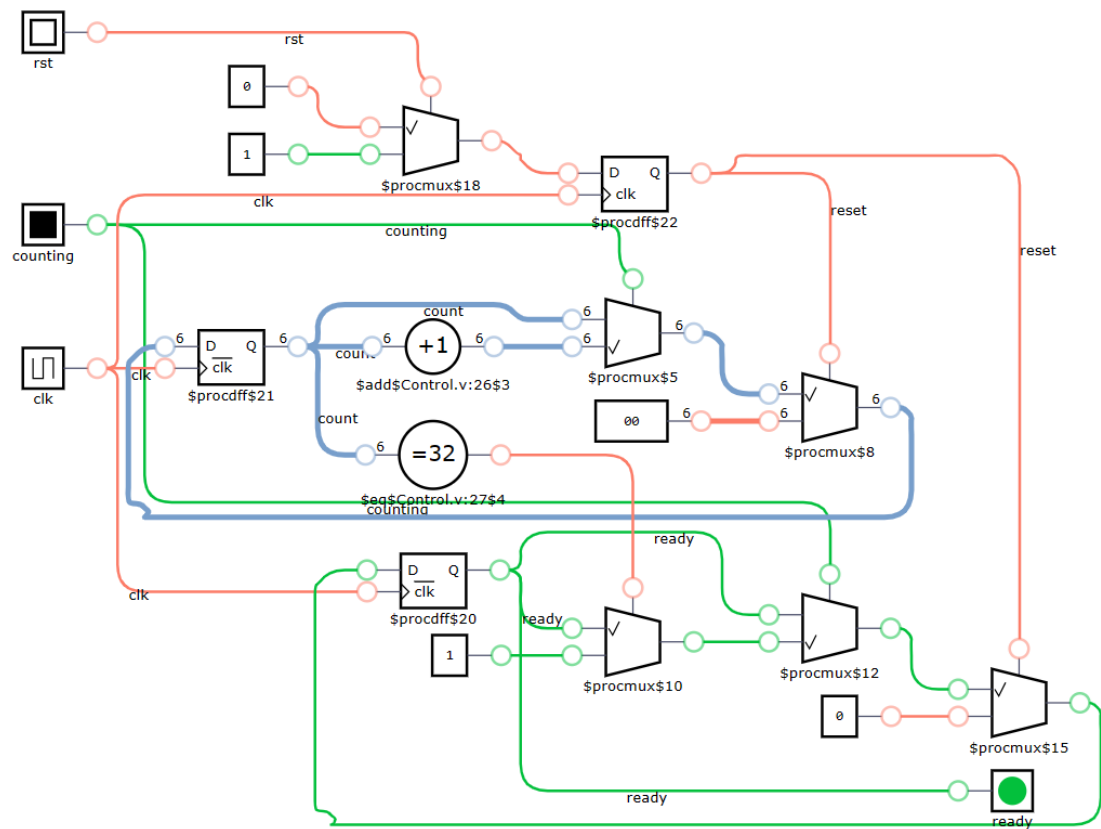


# Control

```

1  module Control (
2      input counting,
3      input rst,
4      input clk,
5      output reg ready
6  );
7
8      reg [5:0] count;
9      reg reset;
10
11     always @(posedge clk) begin
12         if (rst) begin
13             reset <= 1;
14         end
15         else begin
16             reset <= 0;
17         end
18     end
19
20     always @(negedge clk) begin
21         if (reset) begin
22             count <= 0;
23             ready <= 0;
24         end
25         else if (counting) begin
26             count <= count + 1;
27             if (count == 32) begin
28                 ready <= 1;
29             end
30         end
31     end
32
33 endmodule

```



# Description

A counter with 2 in flags, 1 out flag.

## Detail

Line 1~6

I/O Interface.

Signal Symbol	Signal Name	Signal Description
counting	Counting flag	Input flag represent start
rst	Reset flag	Input flag represent reset
clk	Clock	Clock
ready	Ready flag	Signify the end of operation.

Line 8~9

Registers

Line 11~18

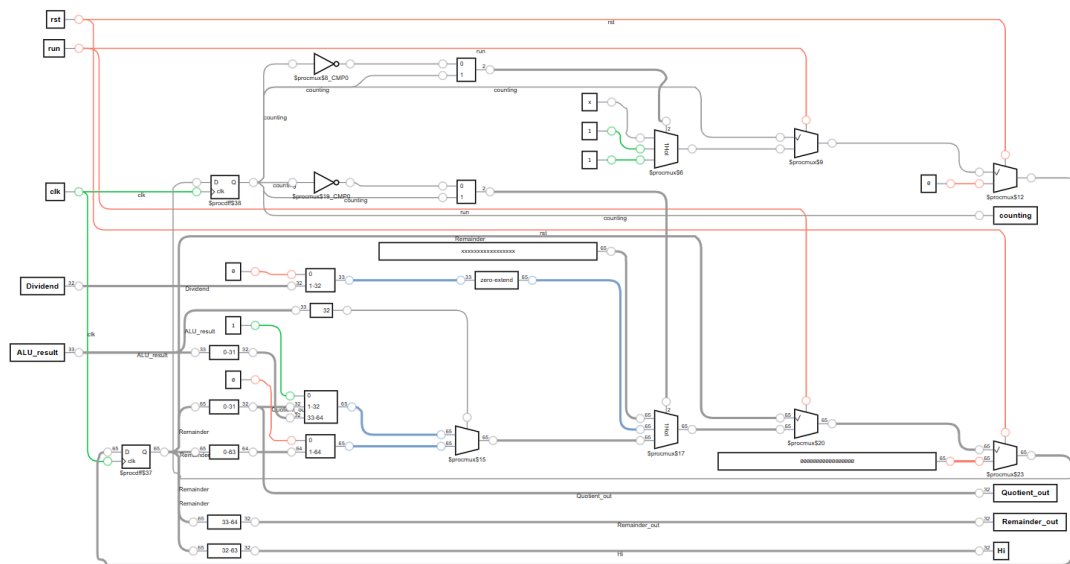
Use reset register to hold rst signal between 2 posedge clk to avoid racing.

Line 20~31

When running count 32 negedges of clk then set ready flag to notify other component to stop or fetch data.

# Remainder

```
1 module Remainder (  
2     input clk,  
3     input rst,  
4     input run,  
5     input [31:0] Dividend,  
6     input [32:0] ALU_result,  
7     output [31:0] Hi,  
8     output [31:0] Remainder_out,  
9     output [31:0] Quotient_out,  
10    output counting  
11 );  
12 reg state;  
13 reg [64:0] Remainder;  
14  
15 assign Hi = Remainder[63:32];  
16 assign Remainder_out = Remainder[64:33];  
17 assign Quotient_out = Remainder[31:0];  
18 assign counting = state;  
19  
20 always @(posedge clk) begin  
21     if (rst) begin  
22         state <= 0;  
23         Remainder <= 0;  
24     end  
25     else if (run) begin  
26         case (state)  
27             0: begin // init state: Load Dividend into Remainder  
28                 Remainder <= {32'b0, Dividend, 1'b0};  
29                 state <= 1;  
30             end  
31             1: begin // run state: Divide  
32                 if (ALU_result[32]) begin  
33                     Remainder <= {Remainder[63:32], Remainder[31:0], 1'b0};  
34                 end  
35                 else begin  
36                     Remainder <= {ALU_result[31:0], Remainder[31:0], 1'b1};  
37                 end  
38                 state <= 1;  
39             end  
40         end  
41     end  
42 end
```



## Description

Main module. I use 65 bits representing product in order to handle overflowing

result from [ALU](#). The computation is executed on posedge clk to avoid racing condition.

## Detail

Line 1~11

I/O Interface.

Signal Symbol	Signal Name	Signal Description
clk	Clock	Clock
rst	Reset flag	Reset to init state
run	Run flag	Run when high
Dividend	32-bits dividend	In when init
ALU_result	33-bits <a href="#">ALU</a> result	With 1 more borrow bit
Hi	Hi register	Upper 32 bits
Remainder_out	32-bits Remainder	34 <sup>th</sup> bit to 65 <sup>th</sup> bit to avoid the right shifting in last iteration
Quotient_out	32-bits Quotient	Output
counting	Counting flag	To avoid racing

Line 12~13

Registers.

Register Symbol	Register Name	Register Description
state	State	For FSM
Remainder	65-bits remainder	1 more bit to handle borrow bit from <a href="#">ALU</a>

Line 15~18

Wire connection to [Remainder\\_out](#), [Quotient\\_out](#), HI, and counting.

Line 21~24

Reset.

Line 26~40

FSM

State Symbol	State Name	State Description
0	Init	Init Remainer by put Dividend to LO and shift left 1 bit.
1	run	Try to divide.

Line 31~39

If ALU\_result is negative, shift left 1 bit.

Else, HI = ALU\_result, then shift left 1 bit. Finally set Remainder[0] to 1.

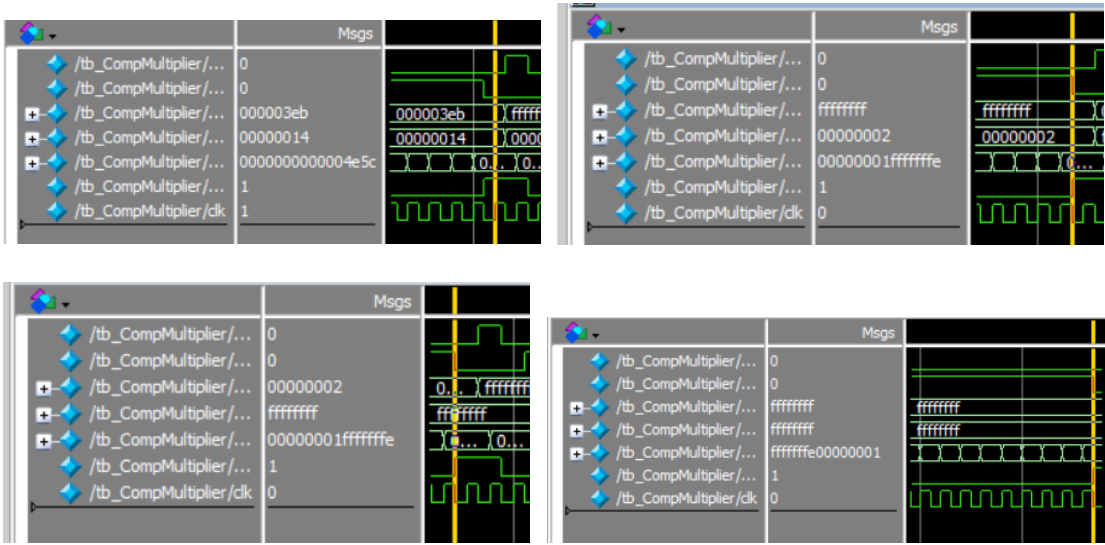
# Test

## Multiplier

### tb\_CompMultiplier

product.v		≡ tb_CompMultiplier.in X		...		≡ tb_CompMultiplier.out X			
testbench >		≡ tb_CompMultiplier.in				testbench >		≡ tb_CompMultiplier.out	
1	000003EB_00000014					1	710,0000000000004e5c		
2	FFFFFFFF_00000002					2	1430,00000001fffffffe		
3	00000002_FFFFFFFF					3	2150,00000001fffffffe		
4	FFFFFFFF_FFFFFFFF					4	2870,fffffffe00000001		
						5			

Multiplicand	Multiplier	Description
000003EB	00000014	Common case
FFFFFFFF	00000002	Multiplicand is extreme value.
00000002	FFFFFFFF	Multiplier is extreme value.
FFFFFFFF	FFFFFFFF	Both are extreme value.



## tb\_ALU

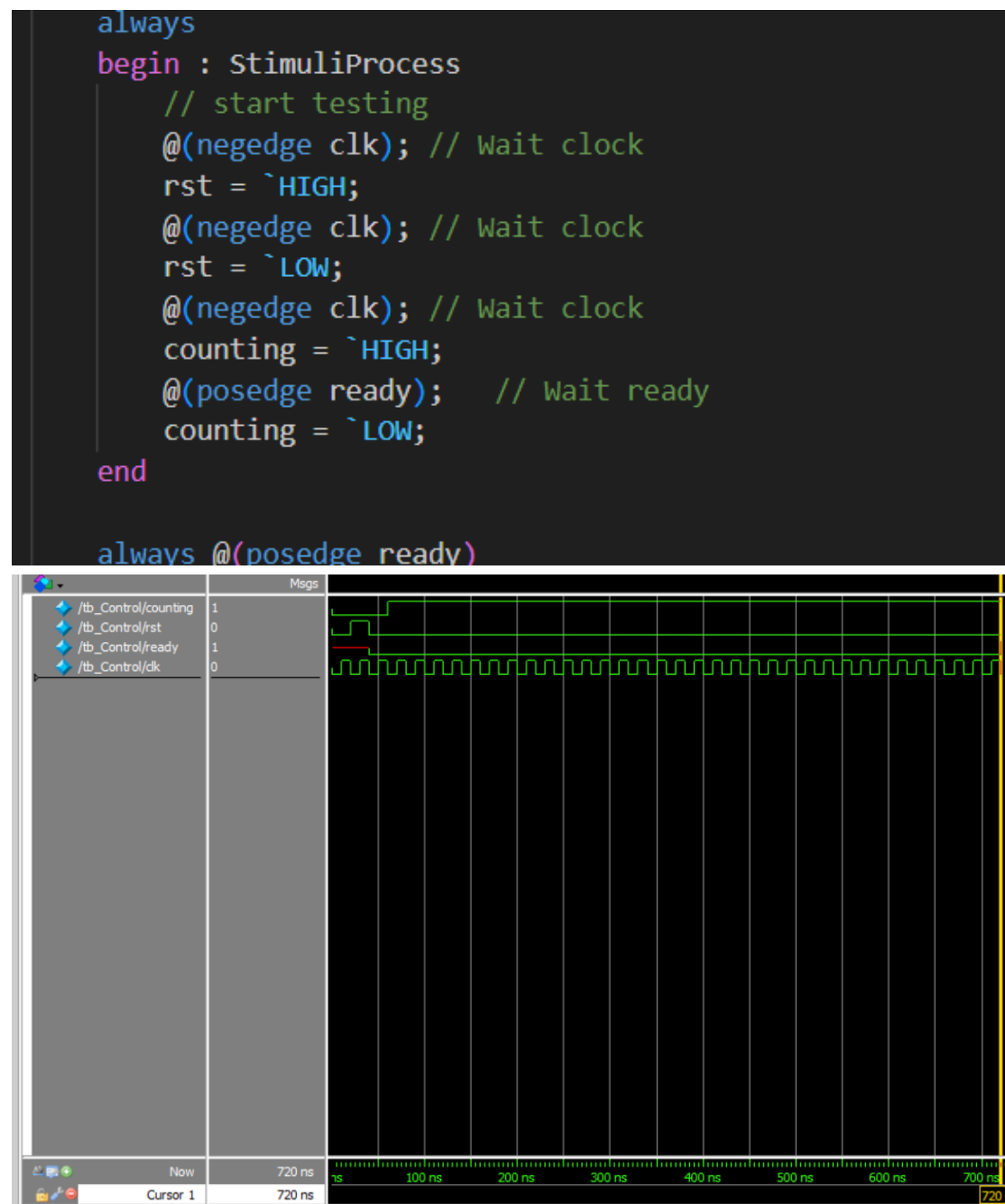
```
58     always
59     begin : StimuliProcess
60         // startt testing
61         while (!$feof(input_file))
62             begin
63                 $fscanf(input_file, "%x\n", read_data);
64                 @ (posedge clk);
65                 {src_1, src_2} = read_data;
66                 @ (negedge clk);
67                 $display("src_1 = %x, src_2 = %x", src_1, src_2);
68                 $display("result = %x", result);
69                 $fdisplay(output_file, "%t, %x, %x, %x", $time, src_1, src_2, result);
70             end
71
72         #`DELAY;
73
74         // Close files
75         $fclose(output_file);
76
77         // Stop simulation
78         $stop;
79     end
```

		Msgs								
/tb_ALU/src_1 /tb_ALU/src_2 /tb_ALU/result /tb_ALU/clk	000003eb		00000000	000003eb	ffffff	00000002	ffffff			
	00000014		00000000	00000014	00000002	ffffff				
	0000003ff		00000000	0000003ff	100000001		1ffffffe			
	1									

tb_ALU.in		tb_ALU.out	
testbench > tb_ALU.in		testbench > tb_ALU.out	
1 000003EB_00000014		1 20, 000003eb, 00000014, 0000003ff	
2 FFFFFFFF_00000002		2 40, ffffffff, 00000002, 100000001	
3 00000002_FFFFFFFF		3 60, 00000002, ffffffff, 100000001	
4 FFFFFFFF_FFFFFFFF		4 80, ffffffff, ffffffff, 1ffffffe	
		5	

Test for functionality of ALU(only addition).

## tb\_Control



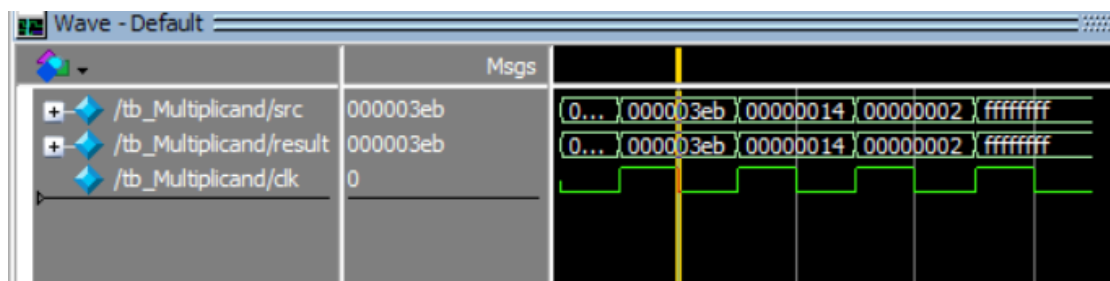
Test for functionality of Control.

$(720-60)/20 = 33$ , 0.5 more for start and 0.5 more for end to avoid racing.

## tb\_Multiplicand

```
55 always
56 begin : StimuliProcess
57     // startt testing
58     while (!$feof(input_file))
59     begin
60         $fscanf(input_file, "%x\n", read_data);
61         @ (posedge clk);
62         src = read_data;
63         @ (negedge clk);
64         $display("src = %x", src);
65         $display("result = %x", result);
66         $fdisplay(output_file, "%t, %x, %x", $time, src, result);
67     end
68
69     #`DELAY;
```

Test for the functionality of Multiplicand.



## tb\_Product

```
70 always
71 begin : StimuliProcess
72     // Start testing
73     while (!$feof(input_file))
74     begin
75         $fscanf(input_file, "%x\n", read_data);
76         @(negedge clk); // Wait clock
77         {ALU_result, Mul} = read_data;
78         rst = `HIGH;
79         @(negedge clk); // Wait clock
80         rst = `LOW;
81         @(negedge clk); // Wait clock
82         run = `HIGH;
83         @(posedge clk); // Wait ready
84         @(posedge clk); // Wait ready
85         run = `LOW;
86         $fdisplay(output_file, "%t, %x, %x, %x", $time, Mul, ALU_result, Product_out);
87     end
88
89     #`DELAY; // Wait for result stable
90
91     // Close output file for safety
92     $fclose(output_file);
93
```

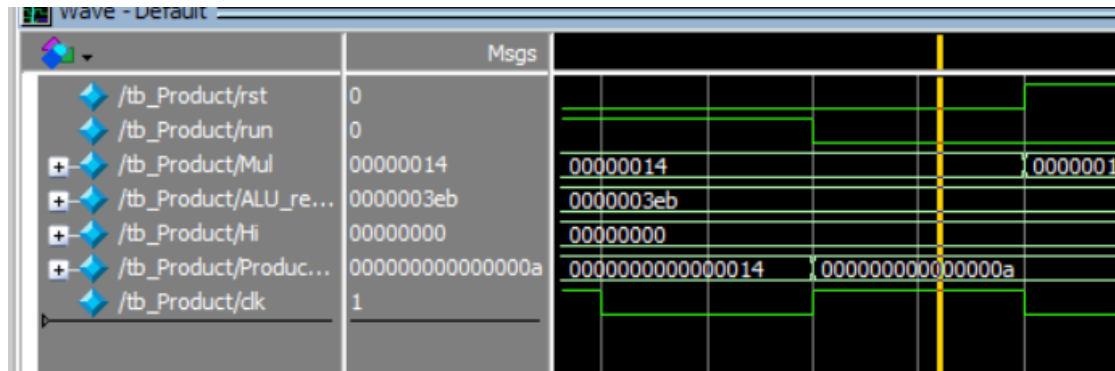
Test for functionality.



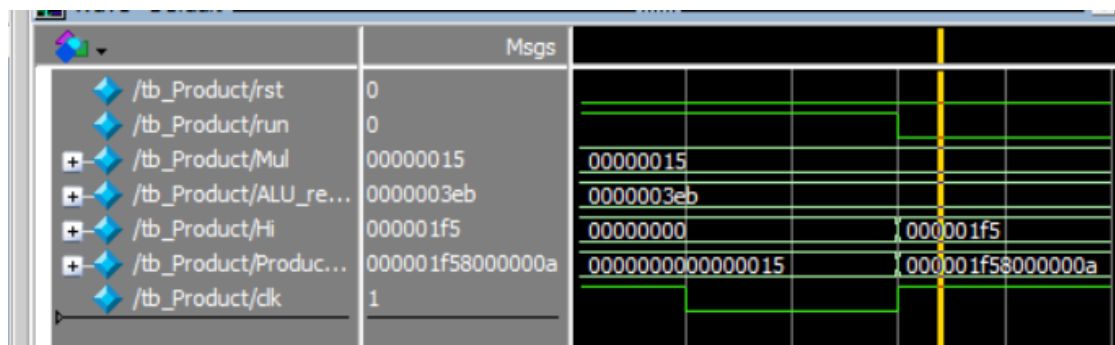
```

ct.out
80, 00000014, 0000003eb, 0000000000000000a
160, 00000015, 0000003eb, 000001f58000000a

```



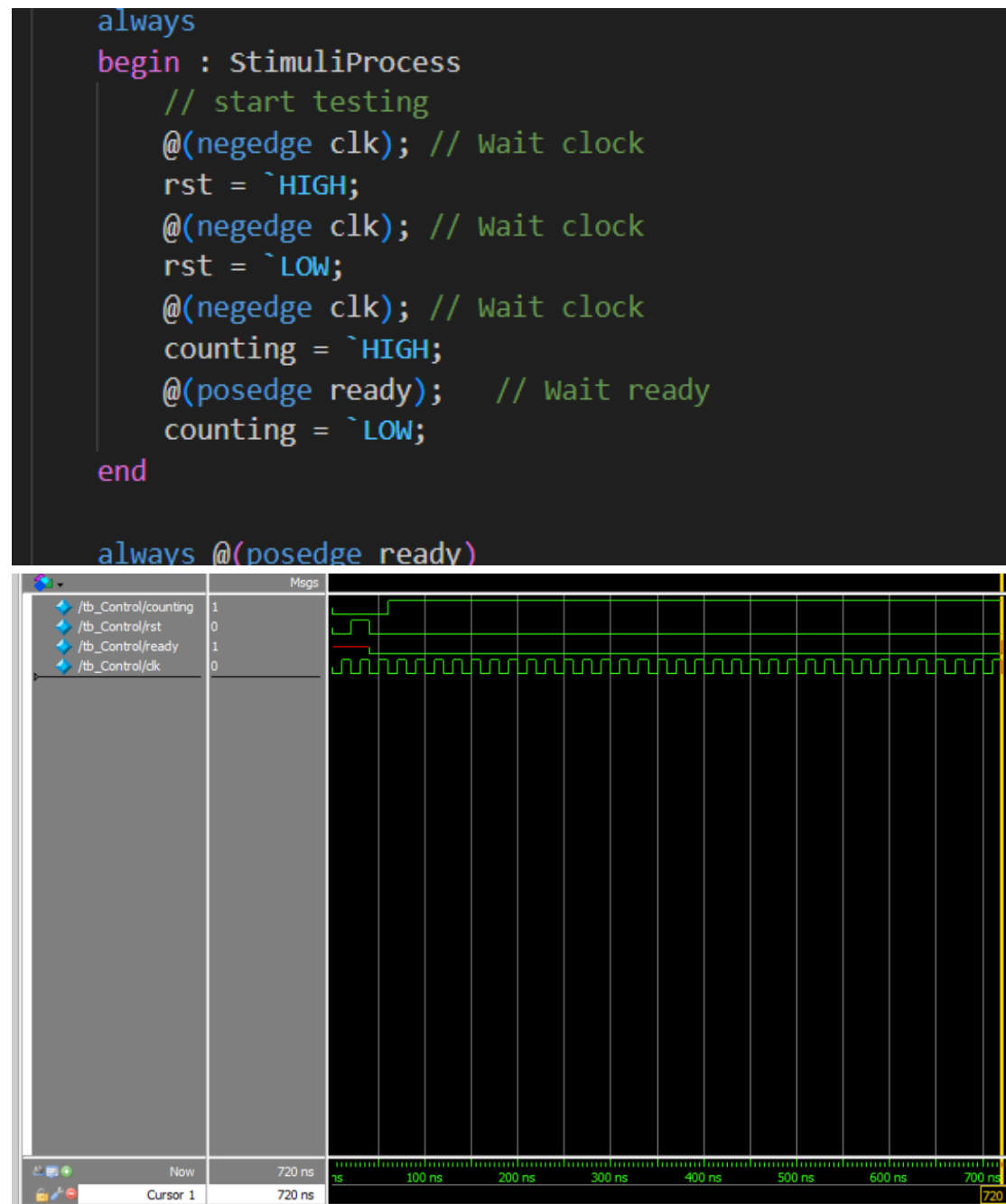
14h LSB is not 1, shift right.



15h LSB is 1, add to HI, then shift right.

# Divider

tb\_Control



Test for functionality of Control.

$(720-60)/20 = 33$ , 0.5 more for start and 0.5 more for end to avoid racing.

## tb\_ALU

```
57
58     always
59     begin : StimuliProcess
60         // startt testing
61         while (!$feof(input_file))
62             begin
63                 $fscanf(input_file, "%x\n", read_data);
64                 @ (posedge clk);
65                 {src_1, src_2} = read_data;
66                 @ (negedge clk);
67                 $display("src_1 = %x, src_2 = %x", src_1, src_2);
68                 $display("result = %x", result);
69                 $fdisplay(output_file, "%t, %x, %x, %x", $time, src_1, src_2, result);
70             end
71
72         #`DELAY;
73
74         // Close files
75         $fclose(output_file);
76
77         // Stop simulation
```

Test for functionality

```
20, 000003eb, 00000014, 0000003d7
40, 00000014, 000003eb, 1ffffffc29
60, ffffffff, 00000002, 0fffffffd
80, 00000002, ffffffff, 100000003
100, ffffffff, ffffffff, 000000000
```

Msgs									
/tb_ALU/src_1	00000014	00000...	000003eb	00000014	fffffff	00000002	fffffff		
/tb_ALU/src_2	000003eb	00000...	00000014	000003eb	00000002	fffffff			
/tb_ALU/result	1ffffffc29	00000...	0000003d7	1ffffffc29	0fffffffd	100000003	000000000		
/tb_ALU/clk	0								

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程式設計人員  
14 - 3EB =  
FFFF FFFF FFFF FC29

Note that result is 33-bits.

## tb\_Divisor

```
53     end
54
55     always
56     begin : StimuliProcess
57         // startt testing
58         while (!$feof(input_file))
59         begin
60             $fscanf(input_file, "%x\n", read_data);
61             @ (posedge clk);
62             src = read_data;
63             @ (negedge clk);
64             $display("src = %x", src);
65             $display("result = %x", result);
66             $fdisplay(output_file, "%t, %x, %x", $time, src, result);
67         end
68
69         #`DELAY;
70
71         // Close files
72         $fclose(output_file);
73
74         // Stop simulation
75         $stop;
76     end
```

Test for functionality.

20,	000003eb,	000003eb
40,	00000014,	00000014
60,	00000002,	00000002
80,	ffffffff,	ffffffff

		Msgs							
+ /tb_Divisor/src	ffffffffff	00000...	000003eb	00000014	00000002	ffffffffff			
	ffffffffff	00000...	000003eb	00000014	00000002	ffffffffff			
+ /tb_Divisor/result									
+ /tb_Divisor/clock									

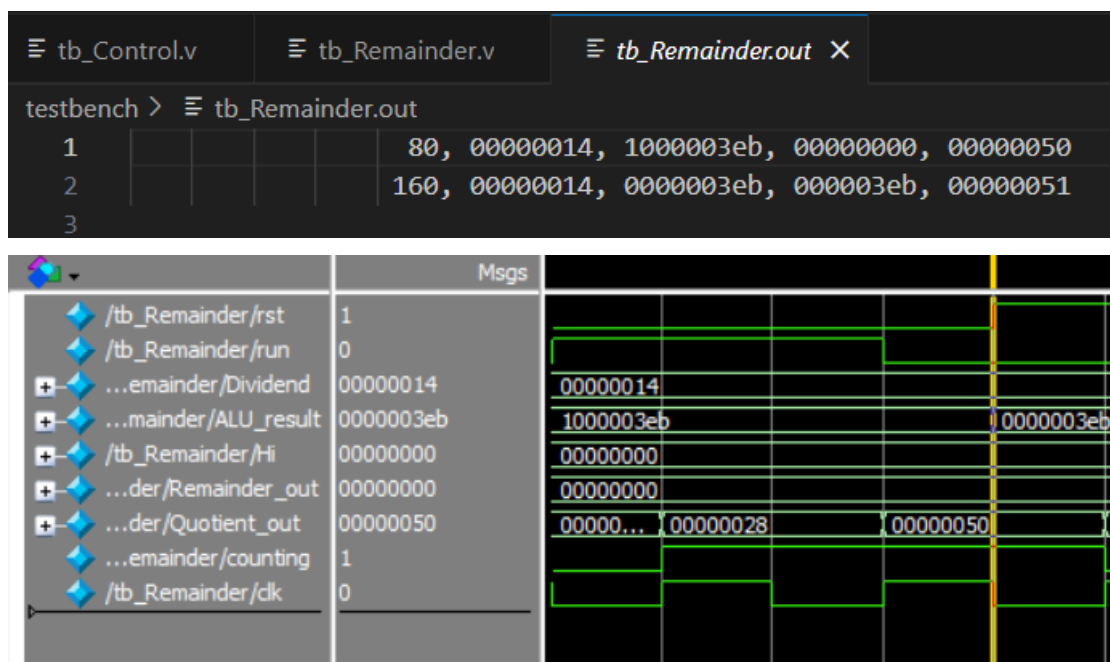
## tb\_Remainder

```

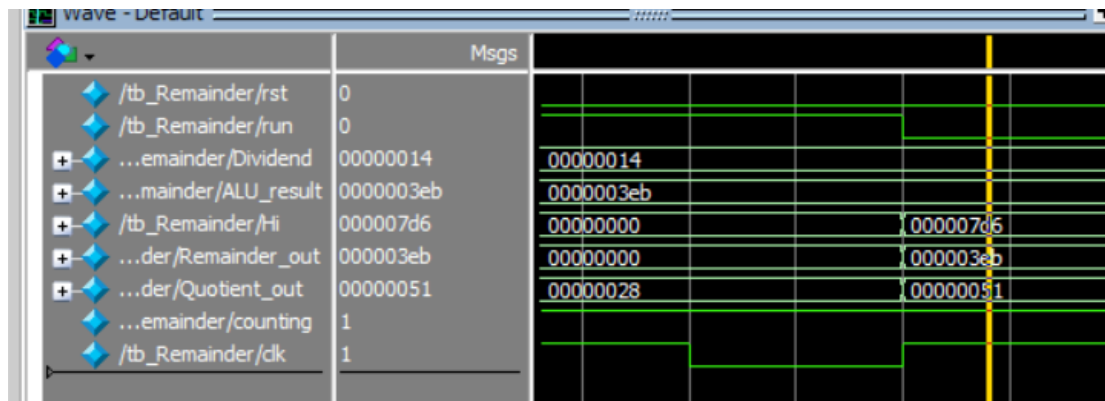
75     while (!$feof(input_file))
76     begin
77         $fscanf(input_file, "%x\n", read_data);
78         @(negedge clk); // Wait clock
79         {ALU_result, Dividend} = {1'b1, read_data};
80         rst = `HIGH;
81         @(negedge clk); // Wait clock
82         rst = `LOW;
83         @(negedge clk); // Wait clock
84         run = `HIGH;
85         @(posedge clk); // Wait ready
86         @(posedge clk); // Wait ready
87         run = `LOW;
88         $fdisplay(output_file, "%t, %x, %x, %x, %x", $time, Dividend, ALU_result, Remainder_out, Quotient_out);
89         @(negedge clk); // Wait clock
90         {ALU_result, Dividend} = {1'b0, read_data};
91         rst = `HIGH;
92         @(negedge clk); // Wait clock
93         rst = `LOW;
94         @(negedge clk); // Wait clock
95         run = `HIGH;
96         @(posedge clk); // Wait ready
97         @(posedge clk); // Wait ready
98         run = `LOW;
99         $fdisplay(output_file, "%t, %x, %x, %x, %x", $time, Dividend, ALU_result, Remainder_out, Quotient_out);
100    end
101

```

Test for functionality.



The first time ALU\_result[32] = 0 -> 28h \* 2h = 50h

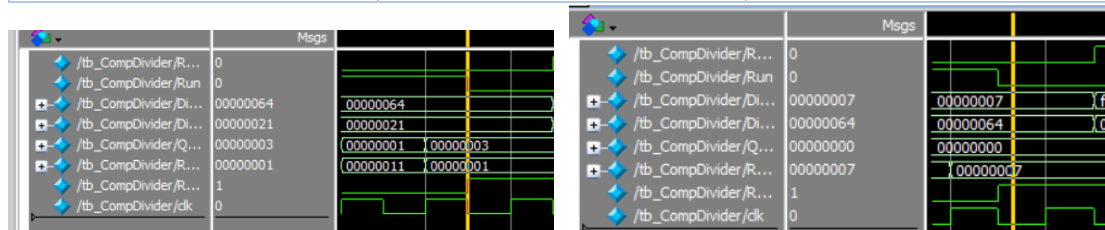


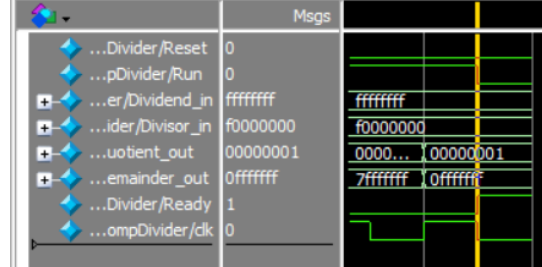
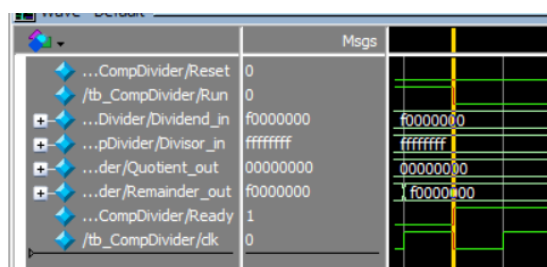
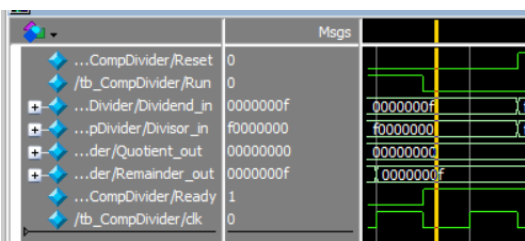
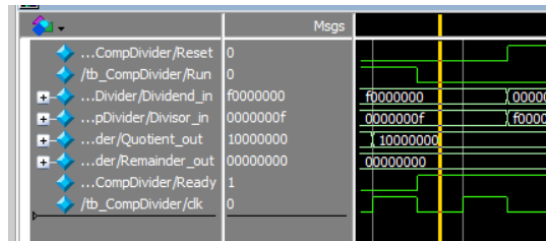
The first time  $ALU\_result[32] = 1 \rightarrow 28h * 2h + 1h = 51h$

## tb\_CompDivider

tb_CompDivider.in	tb_CompDivider.out
testbench > tb_CompDivider.in	testbench > tb_CompDivider.out
1 00000064_00000021	1 00000003_00000001
2 00000007_00000064	2 00000000_00000007
3 F0000000_0000000F	3 10000000_00000000
4 0000000F_F0000000	4 00000000_0000000f
5 F0000000_FFFFFFFF	5 00000000_f0000000
6 FFFFFFFF_F0000000	6 00000001_0ffffff
	7

Dividend	Divisor	Description
00000064	00000021	Common case
00000007	00000064	Common case
F0000000	0000000F	Dividend is extreme value
0000000F	F0000000	Divisor is extreme value
F0000000	FFFFFFF	Both are extreme
FFFFFFF	F0000000	Both are extreme





# Conclusion and Insights

The most valuable lesson I learnt from this assignment is making report is the most tedious thing in the world. I think whom it may concern will feel the same when reading our naïve reports.

Since Run flag will be set on negedge of clk, it'll be better if the mul/div operation is on posedge of clk because of the racing problem. Also, because of the counter should be count on negedge to make the last iteration's output stable (setup time constraint,) this will require 1 more clk to make this happen. Considering the above observation, I make Product/Remainder to tell the control when to start counting.

**This will 100% make no racing.** My structure is not the best in performance, but I think it'll be relative stabler among all the other students' structures in this assignment.

During the implementation, I found out that control can just sit there doing nothing but counting, so I did. It'll need modification if considering merge multiplication and division or even merge all component to a complete ALU, but whatever. The requirement of this assignment doesn't forbid us to do this.

And there is one more trick I used. I make multiplication/division specific ALU to further simplify the control path. As a result, the control just sitting there waiting for set up flags.