## REVISION HISTORY

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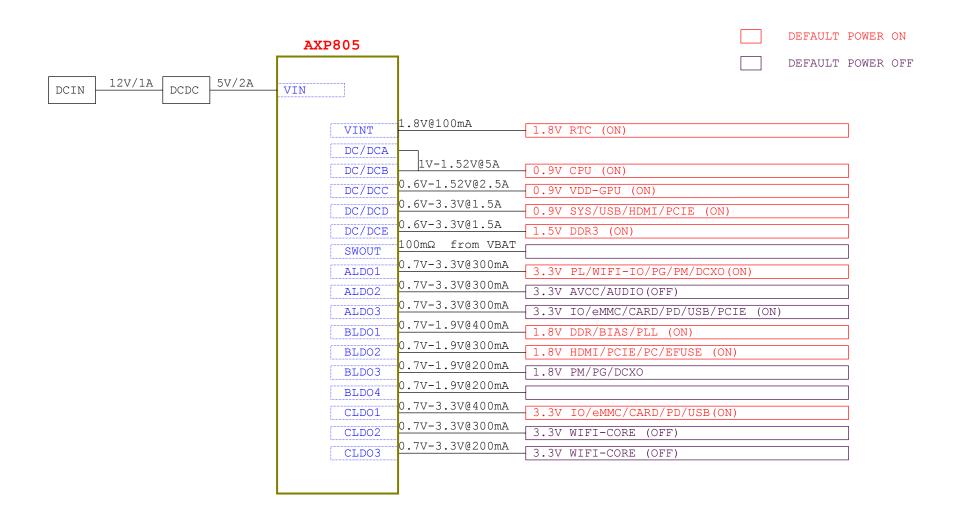
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Revision	Description	Date	Drawn	Checked
Ver 0.5	Initial Version	2016-12-26	НJ	
Ver 0.8		2017-02-23	НЈ	
Ver 1.0		2017-03-22	НЈ	







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GPIO ASSIGNMENT

PIN	Define	CFG	Function
PC0	NAND_WE	2	
PC1	NAND_ALE/SDC2_DS	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE0	2	
PC4	NAND_RE/SDC2_CLK	2/3	
PC5	NAND_RB0/SDC2_CMD	2/3	
PC6	NAND_DQ0/SDC2_D0	2/3	
PC7	NAND_DQ1/SDC2_D1	2/3	NAND/eMMC
PC8	NAND_DQ2/SDC2_D2	2/3	
PC9	NAND_DQ3/SDC2_D3	2/3	
PC10	NAND_DQ4/SDC2_D4	2/3	
PC11	NAND_DQ5/SDC2_D5	2/3	
PC12	NAND_DQ6/SDC2_D6	2/3	
PC13	NAND_DQ7/SDC2_D7	2/3	
PC14	NAND_DQS/SDC2_RST	2/3	
PC15	NAND_CE1	2	
PC16	NAND_RB1	2	

PIN	Define	CFG	Function
PD0			
PD1			
PD2			
PD3			
PD4			
PD5			
PD6			
PD7			
PD8			
PD9			
PD10			
PD11			
PD12			
PD13			
PD14			

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22			
PD23			
PD24			
PD25			
PD26			1

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	WIFI+BT
PG7	UART1_RX	2	WILITEL
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	
PG13	PCM2_DIN	2	
PG14	1		

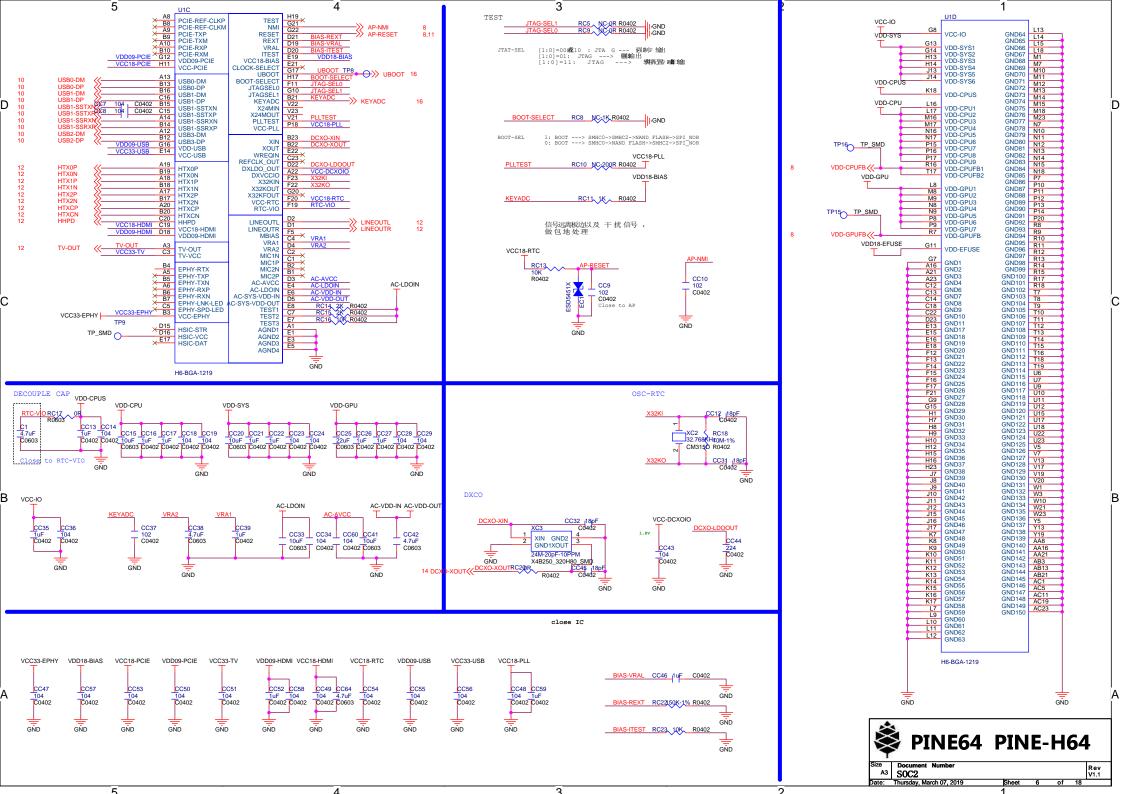
PIN	Define	CFG	Function
PF0	SDC0_D1	2	
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	CARD0
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

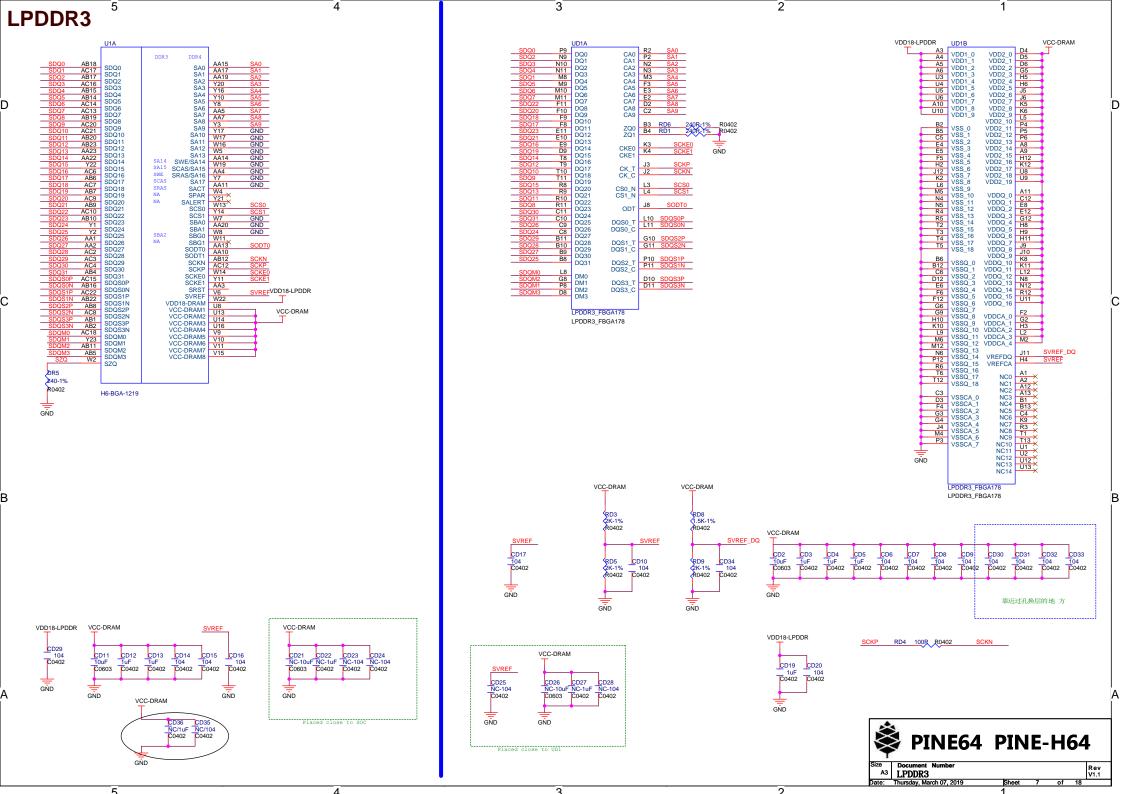
PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	1
PH2			
PH3			
PH4			
PH5			
PH6			
PH7	SPDIF_OUT	3	
PH8	HSCL	2	
PH9	HSDA	2	HDMI
PH10	HCEC	2	

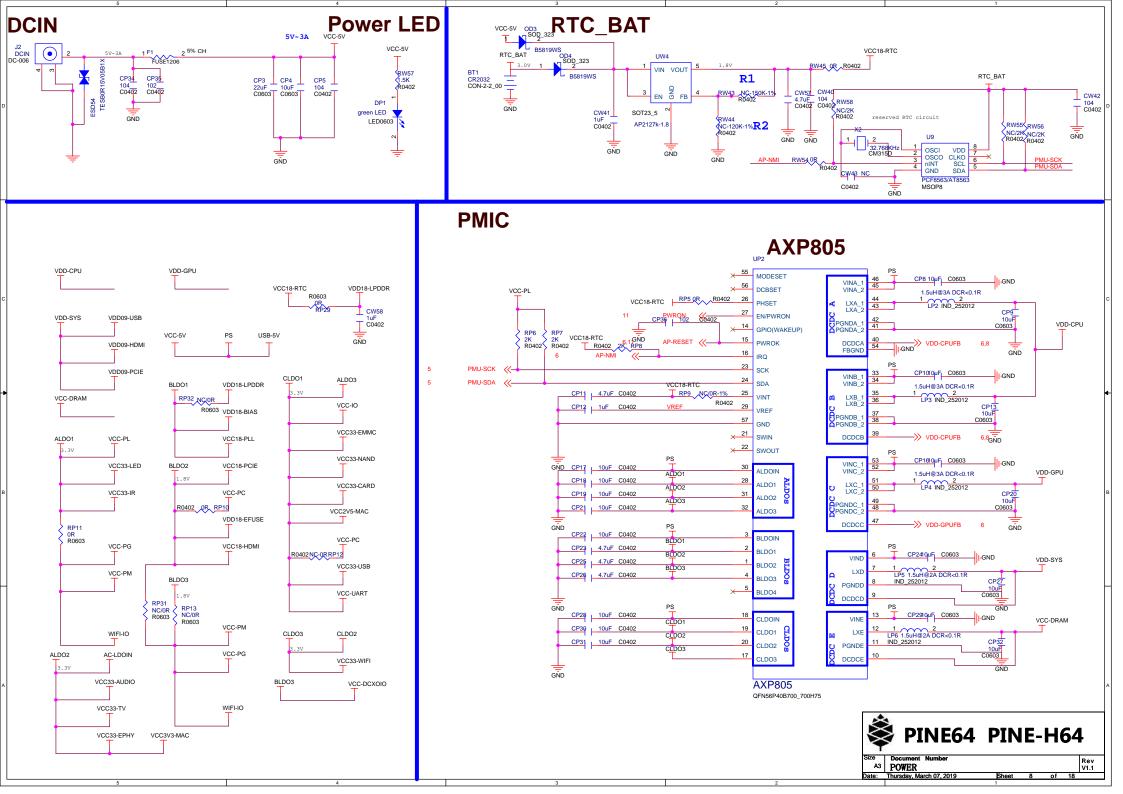
Define	CFG	Function
PMU-SCK	3	
PMU-SDA	3	
RECOVERY	2	
LINK-LED	1	
PWR-LED	1	
USB0-DRVVBUS	1	
MUTE	1	
STATUS-LED	1	
IR-RX	2	
BT-WIFI-ON	1	
WL-WAKE-AP	0	
BT-WAKE-AP	0	
AP-WAKE-BT	1	WIFI+BT
WL-REG-ON	1	WILITDI
BT-REG-ON	1	
	PMU-SCK PMU-SDA RECOVERY LINK-LED PWR-LED USBO-DRVVBUS MUTE STATUS-LED IR-RX BT-WIFI-ON WL-WAKE-AP BT-WAKE-AP AP-WAKE-BT WL-REG-ON	PMU-SCK       3         PMU-SDA       3         RECOVERY       2         LINK-LED       1         PWR-LED       1         USBO-DRVVBUS       1         MUTE       1         STATUS-LED       1         IR-RX       2         BT-WIFI-ON       1         WL-WAKE-AP       0         BT-WAKE-AP       0         AP-WAKE-BT       1         WL-REG-ON       1



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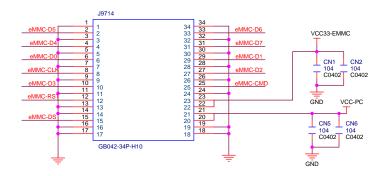


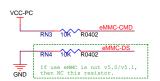


## eMMC module/SIP Flash



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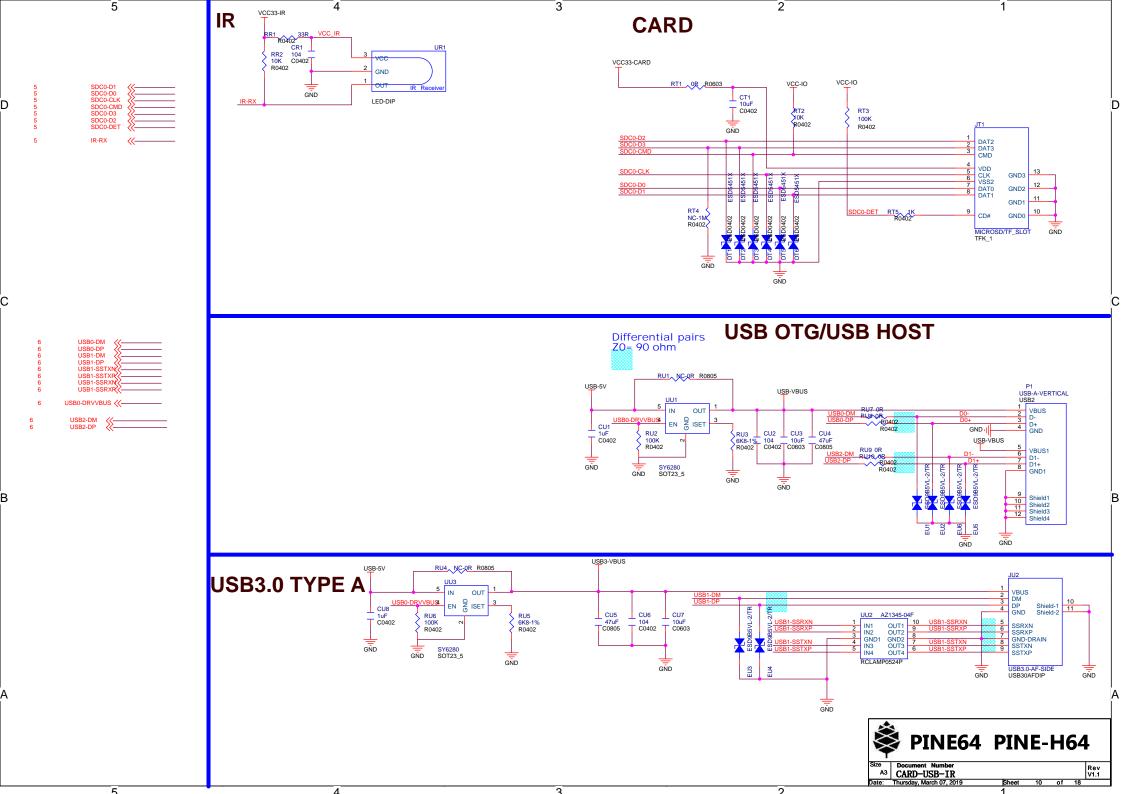


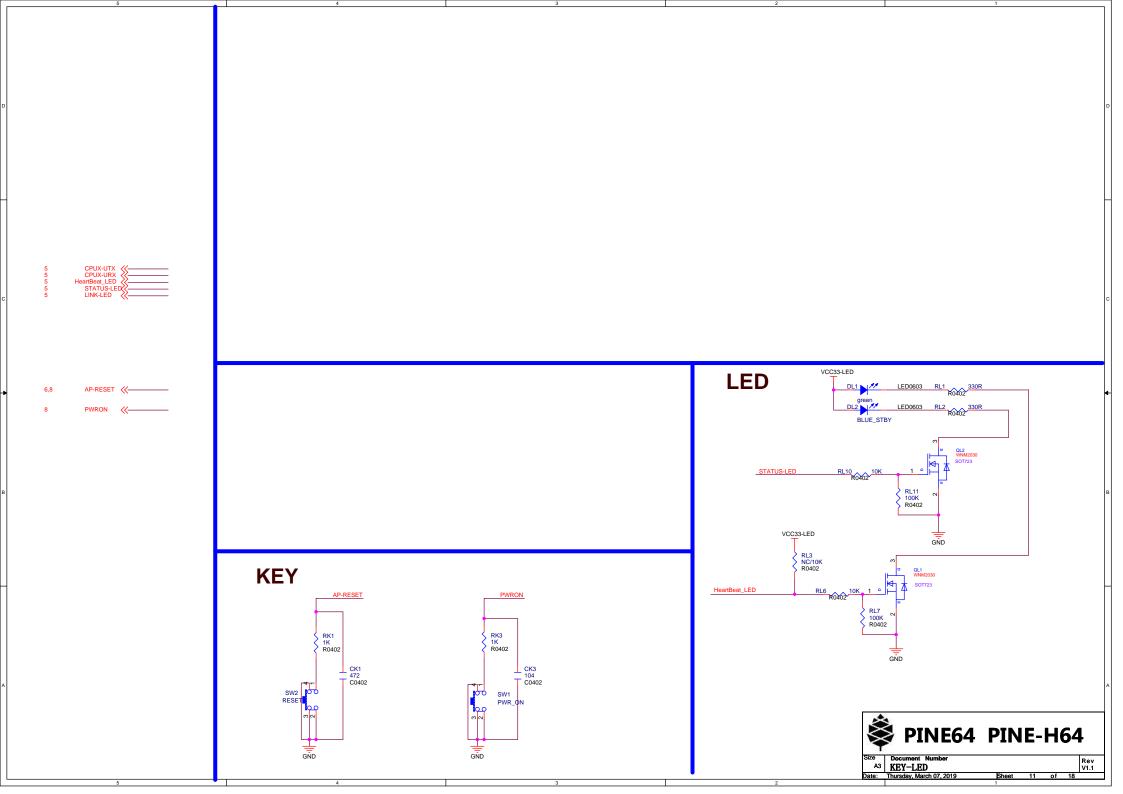
Placed close to SOC

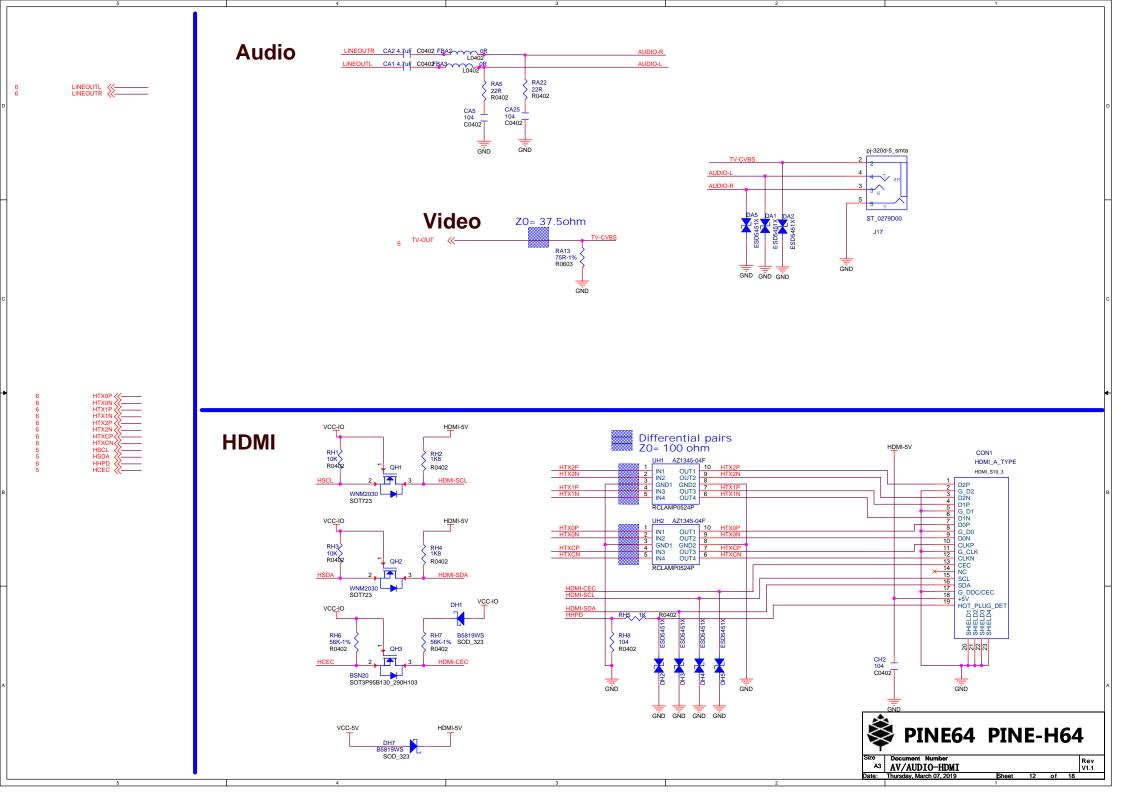
Use spi IC voltage of 3V3 ADD RN6 OOHM, NC RN5. VCC-IO VCC-SPI RN6 NC/0R R0402 VCC-PC VCC-SPI RN5 0R R0402 VCC-SPI SPI\_FLASH \_\_\_\_\_C272\_\_\_C273 10uF 0.1uF C0402 C0402 GND GND PC5-SPIO\_CS VCC  $HOL\overline{D}$ U3500 NC/W25Q128FV/QFN6x5 PC0-SPIO\_CLK VCC-SPI SCLK PC2-SPIO\_MOSI GND SDI VCC-SPI W25Q128FV/W25Q256FV 5 PC2-SPIO\_MOSI 2 PC3-SPIO\_MISO DI/IO0 DO/IO1 PC0-SPIO\_CLK6 WP\*/IO2 3 HOLD\*/IO3 7 VCC-SPI VCC-SPI 4 GND 9 E\_PAD

GND

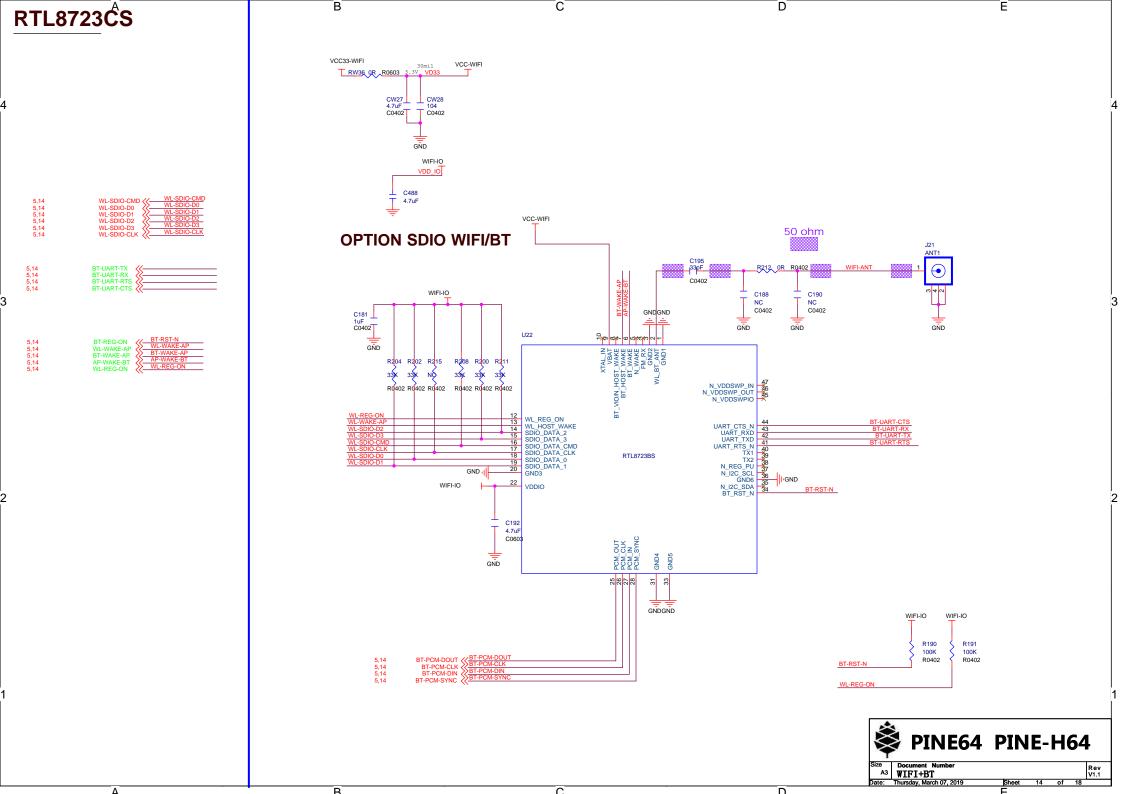
NOTE:Use spi IC voltage of 1V8 ADD RN5 00HM,NC RN6.



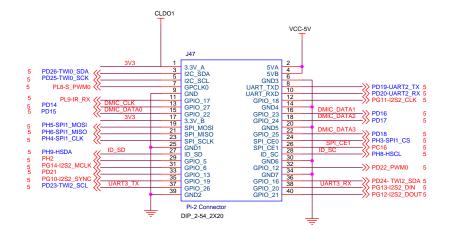




**SPDIF** VCC-5V CE17 4.7uF C0402 RC25 10R R0402 5 PH7-OWA\_OUT <<--CON-3-2\_00 PINE64 PINE-H64 Size Document Number
A3 SPDIF
Date: Thursday, March 07, 2019



## **Pi-2 Connector**





**EXT+ Connector** PH0\_UART0\_TX PWRON PH0\_UART0\_RX RESET GND GND1 DIP\_2\_54\_2x3PIN PINE64 PINE-H64 Size Document Number

A3 EXT+ Connector

Date: Thursday, March 07, 2019

