Demo Board For RV1126&RV1109

RV1126&1109 _IPC38_DEMO_MB_V1.21

RV1126_RV1109 Main difference		
	RV1126	RV1109
CPU	Quad A7	Dual A7
NPU	2.0Tops	1.2Tops
ISP	14M Pixel	5M Pixel

Reference Design Main Functions Introduction	
Power	4DCDC+3LDO
RAM	SPI FLASH
ROM	DDR3L/DDR3
Interface	SDMMC0/SDIO/MAC/MIPI_DSI/MIPI_CSI0/ I2S/USB/ADC

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	00.Cover Page				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	1 of 27

Index and Notes

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Note

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

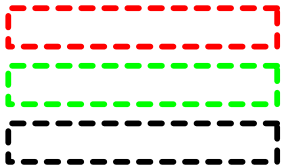
Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Graphic Description



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	01.Index and Notes				
Date:	Friday, February 05, 2021			Rev:	V1.21
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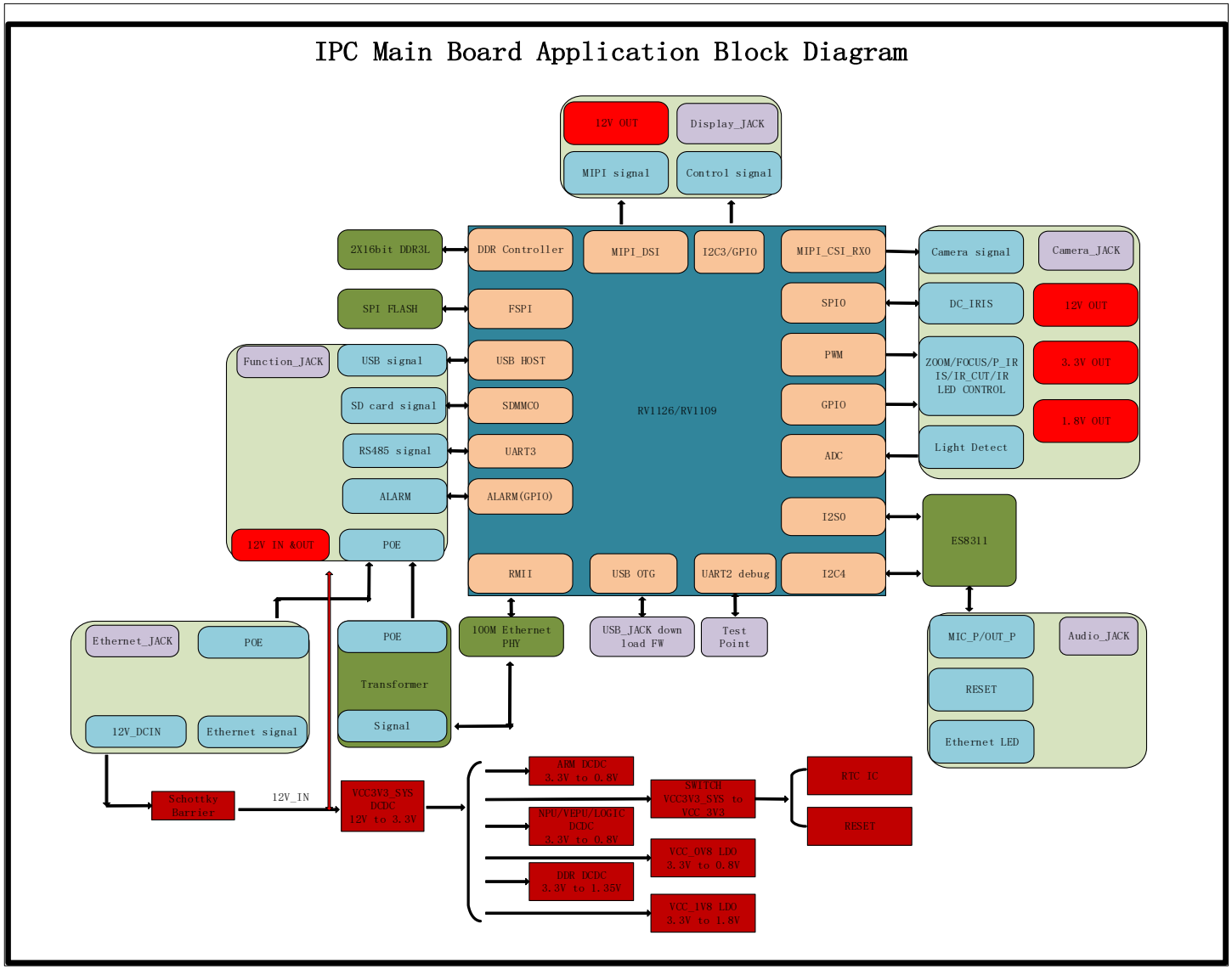
Revision History

Version	Date	Author	Change Note	Approved
V1.0	2020.05.11	Liyh	First edition	
V1.1	2020.06.18	LinXu		
V1.11	2020.07.24	LinXu	1.Change PCB decal of J6800; 2.R1103 is mount;	
V1.12	2020.08.31	LinXu	1.Add I2C0 pull-up resistor R1105/R1106; 2.Add R1000; 3.Add R1602/R1603/R1604; 4.Change U2002 to TCS9819-CM263 5.Add description of RESET; 6.Delete ED4200/ED4201; 7.R7000 connect to VCC3V3_MICBIAS; 8.Delete R7006; 9.Add R7008 and connection of Factory; 10.R7000 pin1 connect to VCC_3V3;	
V1.2	2020.11.13	LinXu	1.Increase R1107/C1107, modify the value of R1000/C1000; 2.Modify D2000 as a diode and increase current limiting resistor R2007; 3.Modify J4200 to 30pin, and adjust the signal sequence; 4.Delete J7000 and merge the audio signal with J4200; 5.Modify J6800 to 8pin; 6.Add ADCIN2 to KEY_SET connection; 7.Modify R1700/R1701 to 1k; 8.Remove resistor R6800;	
V1.21	2021.02.05	LinXu	1.Change U2002 from TCS9819-CM263 to TCS9819-CM293; 2.Change R2114 from 750K to 510K; 3.Change R2127 from 510K to 750K; 4.Change R2131 from 36K to 180K; 5.Change C4300 from 4.7uF to 10uF; 5.Modify part value of U2000/U2103; 6.Modify description of "Power Diagram and Sequence";	

Block Diagram



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Project:	RV1126&1109 IPC38 MB				
File:	03.Block Diagram				
Date:	Friday, February 05, 2021			Rev:	V1.21
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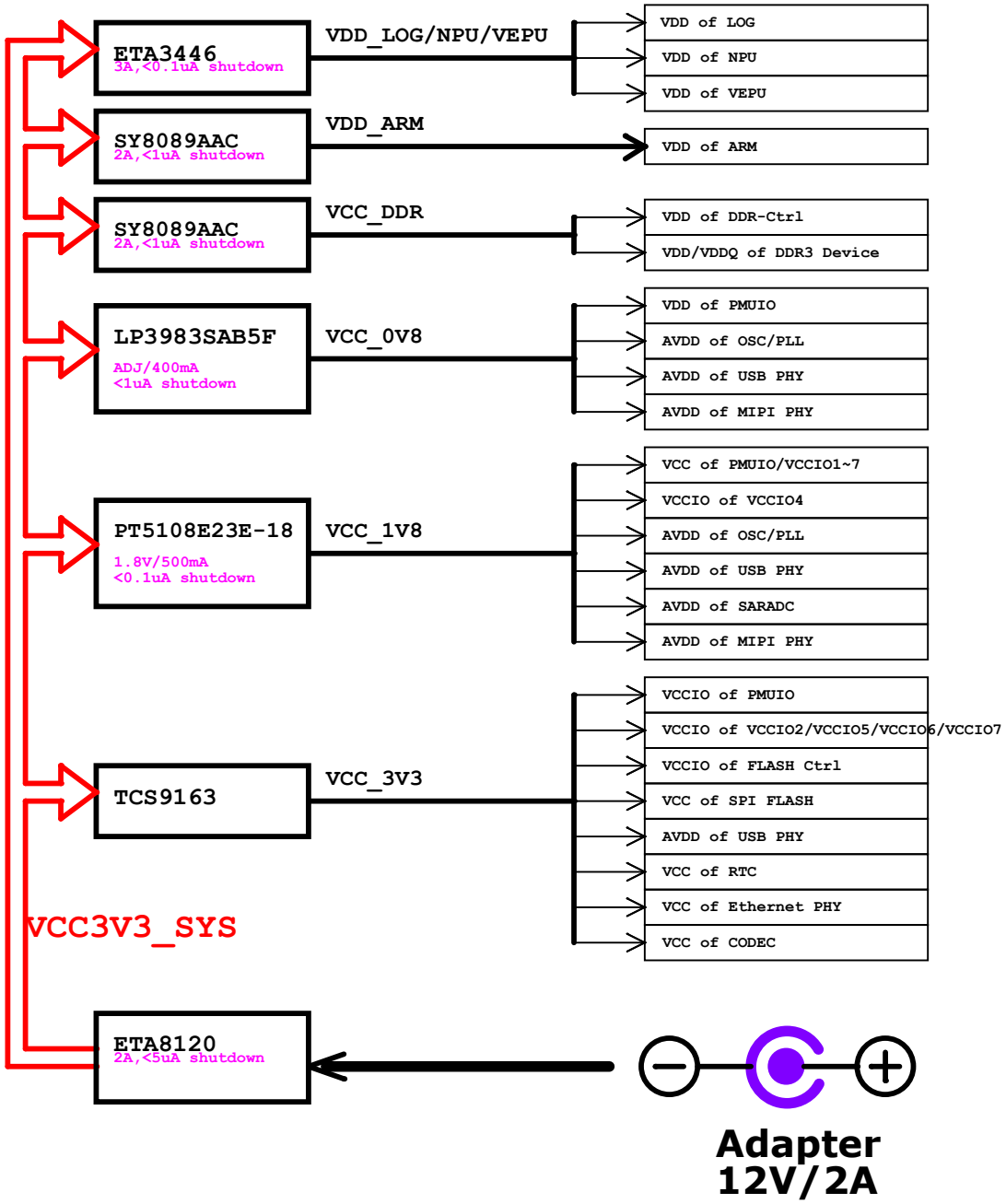
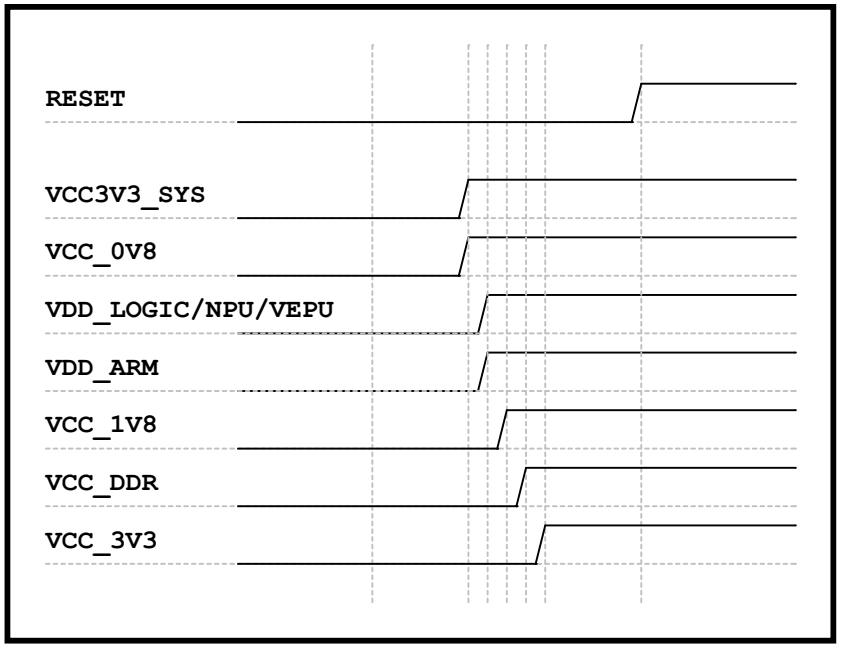
Power Diagram and Sequence



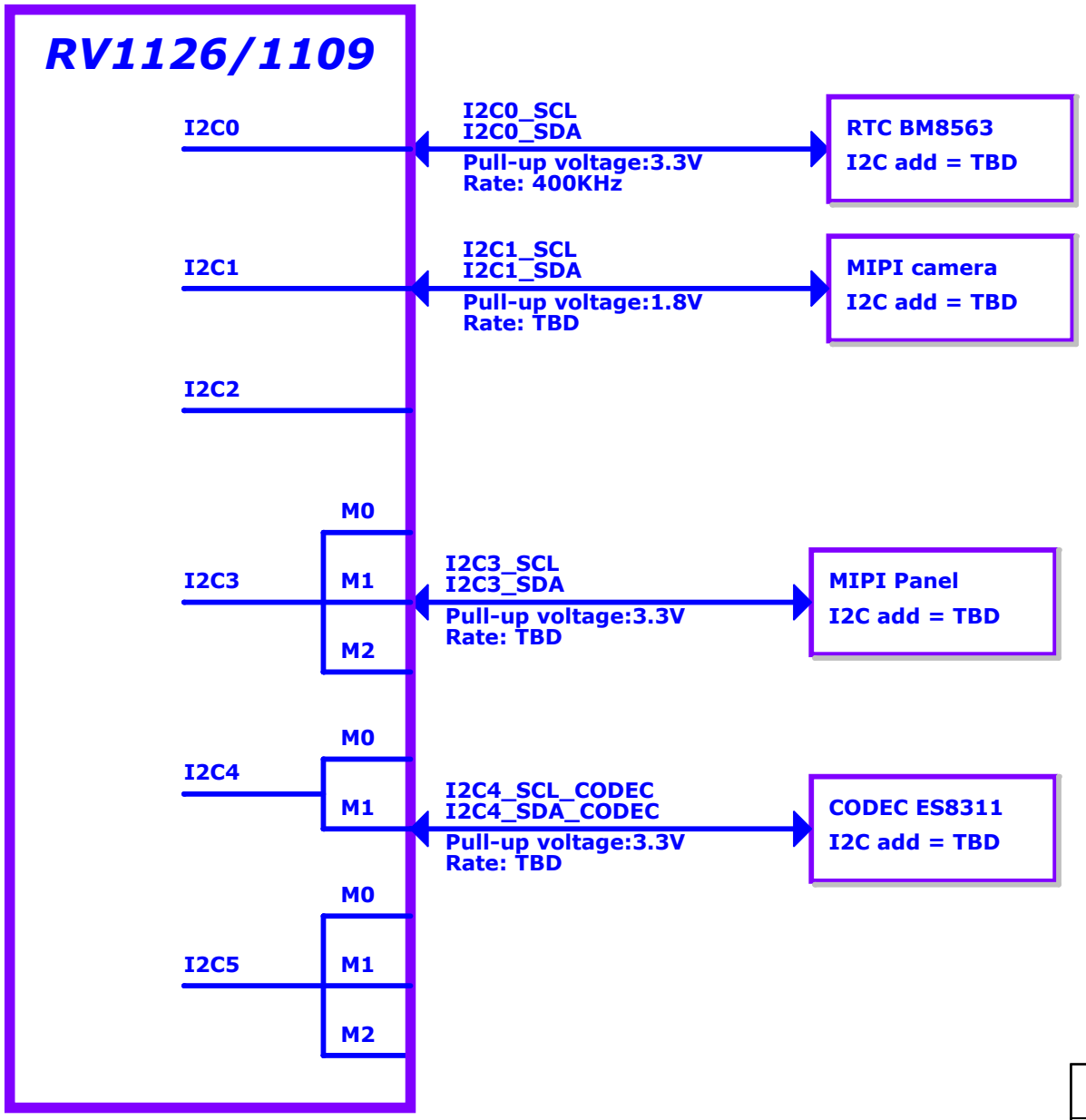
RV1126/RV1109 Power-on Sequence

Power Name	PMIC Channel	Time Slot	Default voltage	Supply Limit	Peak Current
VCC_0V8	LDO	Slot: 1	0.8V	0.4A	
VDD_LOGIC/NPU/VEPU	DC-DC BUCK	Slot: 2	0.825V	3A	2922mA
VDD_ARM	DC-DC BUCK	Slot: 2	0.824V	2A	542mA
VCC_1V8	LDO	Slot: 3	1.8V	0.5A	
VCC_DDR	DC-DC BUCK	Slot: 4	1.35V	2A	665mA
VCC_3V3	LDO	Slot: 5	3.3V	0.5A	
RESET	Finally send out the reset signal, depending on RESET IC				



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	04.Power Diagram and Sequence				
Date:	Friday, February 05, 2021			Rev:	V1.21
Designed by:	LinXu	Reviewed by:	<Checker>	Sheet:	5 of 27

I2C MAP



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Project:	RV1126&1109 IPC38 MB				
File:	05.I2C MAP				
Date:	Friday, February 05, 2021			Rev:	V1.2
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IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO0	***GPIO0A***	✓	✓	*VCC_3V3*		*3.3V*	
PMUIO1	***GPIO0BC***	✓	✓	*VCC_3V3*		*3.3V*	
VCCIO1	***GPIO0CD/GPIO1A***	✓	✓	*VCCIO_FLASH*		*1.8/3.3V*	*GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1 part voltage domain after power-on reset.It is pull-up for 1.8V*
VCCIO2	***GPIO1AB***	✓	✓	*VCC_3V3*		*3.3V*	
VCCIO3	***GPIO1BCD***	✓	✓	*NC*			
VCCIO4	***GPIO1D/GPIO2A***	✓	✓	*VCC_1V8*		*1.8V*	
VCCIO5	***GPIO2ABCD/GPIO3A***	✓	✓	*VCC_3V3*		*3.3V*	
VCCIO6	***GPIO3ABC***	✓	✓	*VCC_3V3*		*3.3V*	
VCCIO7	***GPIO3D/GPIO4A***	✓	✓	*VCC_3V3*		*3.3V*	

Power

U1000N
RV1126&RV1109
BGA409_14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

NPU_VDD_1	H11	VDD_NPU_VEPU_LOGIC
NPU_VDD_2	H12	
NPU_VDD_3	J10	
NPU_VDD_4	J11	
NPU_VDD_5	K10	
NPU_VDD_6	K11	
LOGIC_VDD_1	H9	VDD_NPU_VEPU_LOGIC
LOGIC_VDD_2	J9	
LOGIC_VDD_3	L10	
LOGIC_VDD_4	M11	
LOGIC_VDD_5	H13	
LOGIC_VDD_6	J13	
VEPU_VDD_1	L9	VDD_NPU_VEPU_LOGIC
VEPU_VDD_2	M9	
VEPU_VDD_3	N8	
VEPU_VDD_4	N9	
ARM_VDD_1	N12	VDD_ARM
ARM_VDD_2	P12	
ARM_VDD_3	P13	

Supply for VCCIO1~7 Power
VCCIO_VDD_1V8

VCCIO_VDD_1V8
H14 R1000 1 3.3R 5% 2 R0201 VCC_1V8
C1000 1nF X7R 25V C0201

VDD_NPU_VEPU_LOGIC — For NPU

C1001 100nF X5R 10V C0201	C1002 100nF X5R 10V C0201	C1003 100nF X5R 10V C0201	C1004 1uF X5R 6.3V C0402	C1005 1uF X5R 6.3V C0402	C1006 10uF X5R 4V C0402

VDD_NPU_VEPU_LOGIC — For LOGIC

C1007 100nF X5R 10V C0201	C1008 100nF X5R 10V C0201	C1009 1uF X5R 6.3V C0402	C1010 1uF X5R 6.3V C0402	C1011 10uF X5R 4V C0402

VDD_ARM

C1012 100nF X5R 10V C0201	C1013 100nF X5R 10V C0201	C1014 1uF X5R 6.3V C0402	C1015 10uF X5R 4V C0402

VDD_NPU_VEPU_LOGIC — For VEPU

C1016 100nF X5R 10V C0201	C1017 100nF X5R 10V C0201	C1018 1uF X5R 6.3V C0402	C1019 10uF X5R 4V C0402

GND

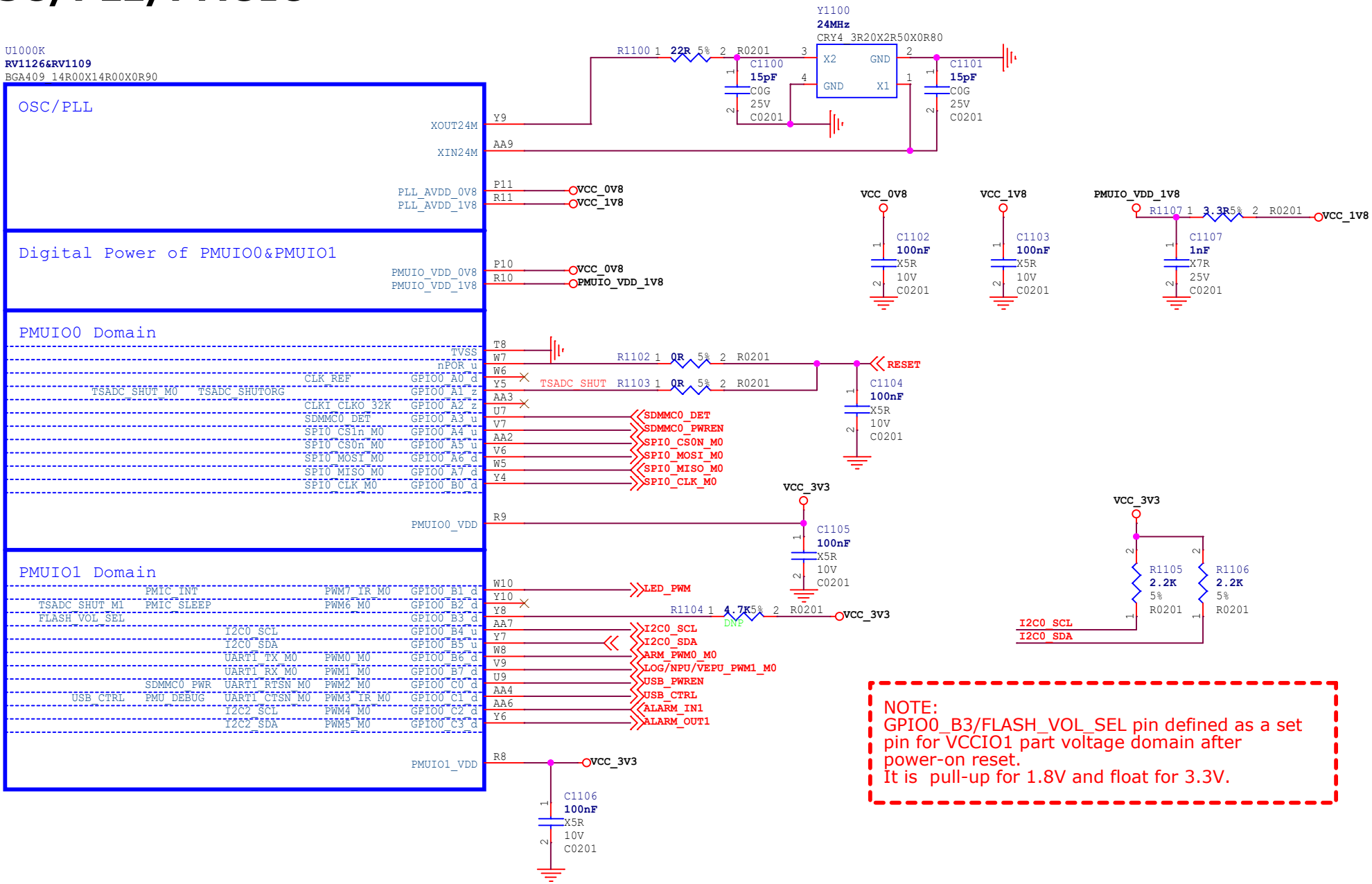
U1000O
RV1126&RV1109
BGA409_14R00X14R00X0R90

VSS/AVSS

A1	VSS_1	VSS_53	K9		
A21	AVSS_2	VSS_54	K12		
B12	VSS_3	VSS_55	K13		
C3	VSS_4	VSS_56	K14		
C5	VSS_5	VSS_57	L2		
C7	VSS_6	VSS_58	L5		
C10	VSS_7	VSS_59	L6		
C12	VSS_8	VSS_60	L11		
D9	VSS_9	VSS_61	L12		
D12	VSS_10	VSS_62	L13		
D18	AVSS_11	VSS_63	L14		
E4	VSS_12	VSS_64	L16		
E6	VSS_13	VSS_65	M3		
E8	VSS_14	VSS_66	M5		
E9	VSS_15	VSS_67	M7		
E10	VSS_16	VSS_68	M8		
E11	VSS_17	VSS_69	M10		
E12	VSS_18	VSS_70	M12		
F3	VSS_19	VSS_71	M13		
F5	VSS_20	VSS_72	M14		
F7	VSS_21	VSS_73	M16		
F8	VSS_22	VSS_74	N5		
F9	VSS_23	VSS_75	N6		
F10	VSS_24	VSS_76	N7		
F11	VSS_25	VSS_77	N10		
F12	VSS_26	VSS_78	N11		
F13	VSS_27	VSS_79	N13		
F14	AVSS_28	VSS_80	N14		
F15	AVSS_29	VSS_81	N16		
G2	VSS_30	VSS_82	P5		
G5	VSS_31	VSS_83	P7		
G6	VSS_32	VSS_84	P8		
G10	VSS_33	VSS_85	P9		
G11	VSS_34	VSS_86	P14		
G12	VSS_35	VSS_87	P16		
G13	VSS_36	VSS_88	R1		
G16	AVSS_37	VSS_89	R5		
G17	AVSS_38	VSS_90	R12		
H4	VSS_39	VSS_91	R13		
H5	VSS_40	VSS_92	R14		
H6	VSS_41	VSS_93	T6		
H7	VSS_42	VSS_94	T9		
H10	VSS_43	VSS_95	T10		
H15	VSS_44	VSS_96	T14		
J5	VSS_45	VSS_97	T17		
J6	VSS_46	VSS_98	V17		
J12	VSS_47	VSS_99	W9		
J14	VSS_48	VSS_100	W14		
J16	VSS_49	VSS_101	AA1		
K5	VSS_50	VSS_102	AA10		
K6	VSS_51	VSS_103	AA21		
K8	VSS_52				

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	10.RV1126&RV1109_Power/GND				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	8 of 27

OSC/PLL/PMUIO



NOTE:
GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1 part voltage domain after power-on reset.
It is pull-up for 1.8V and float for 3.3V.

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	11.RV1126&RV1109_OSC/PLL/PMUIO				
Date:	Friday, February 05, 2021			Rev:	V1.21
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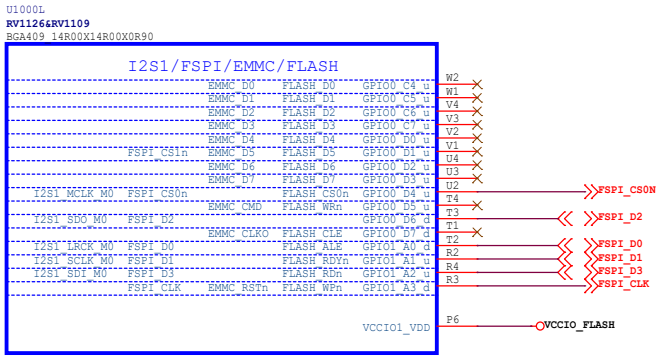
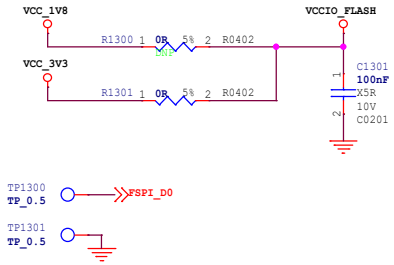
DDR Controller

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	12.RV1126&RV1109_DRAMController				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	10 of 27

EMMC/FLASH



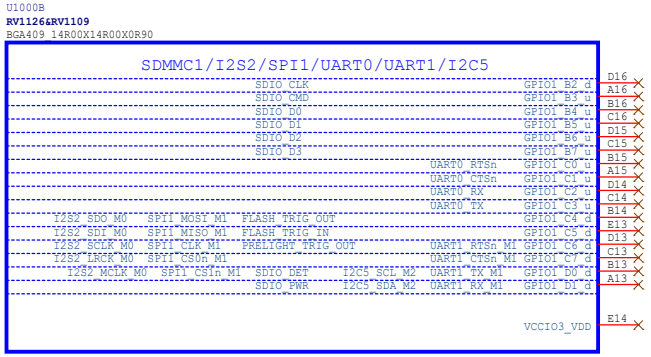


NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

Condition	VCCIO1 (VCCIO_FLASH)
FLASH_VOL_SEL=0	3.3V Default
FLASH_VOL_SEL=1	1.8V

SDMMC0/JTAG

SDMMC1/UART/I2S2



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	13.RV1126&RV1109_Flash/SD				
Date:	Friday, February 05, 2021			Rev:	V1.2
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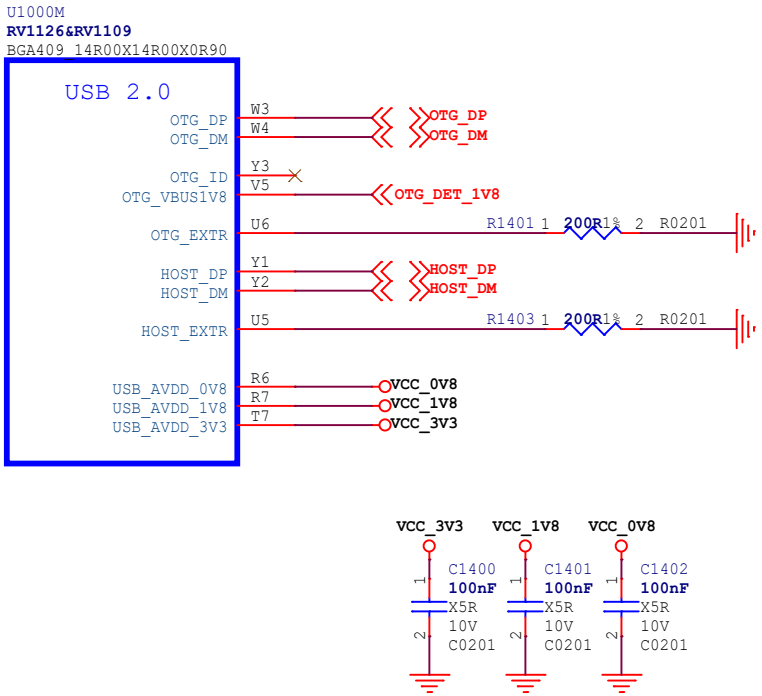
USB Controller



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	14.RV1126&RV1109_USB Controller				
Date:	Friday, February 05, 2021			Rev:	V1.2
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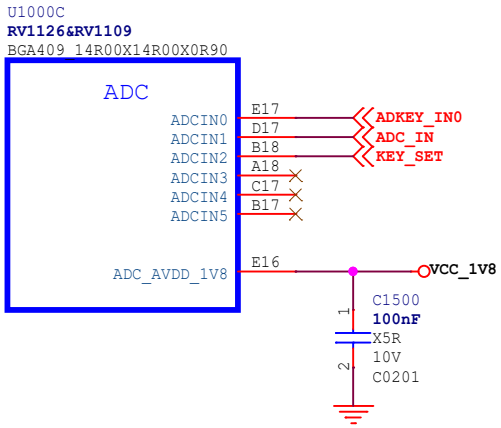
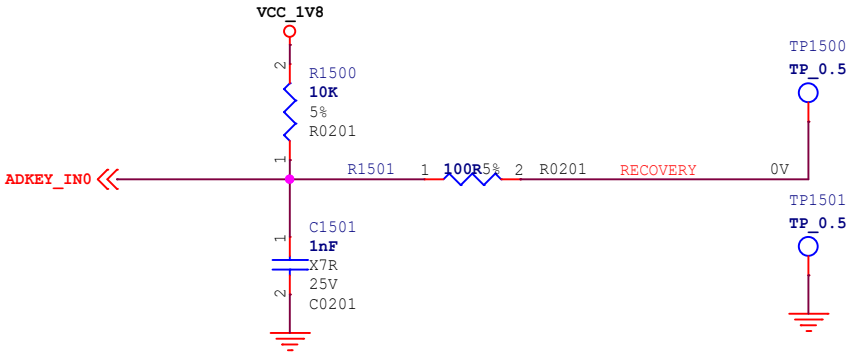
SARADC





Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	15.RV1126&RV1109_SARADC				
Date:	Friday, February 05, 2021			Rev:	V1.2
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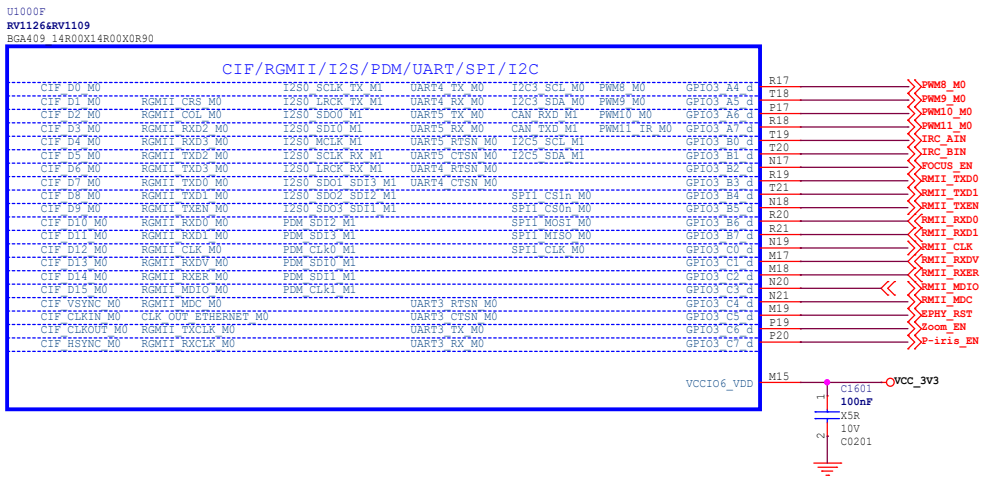
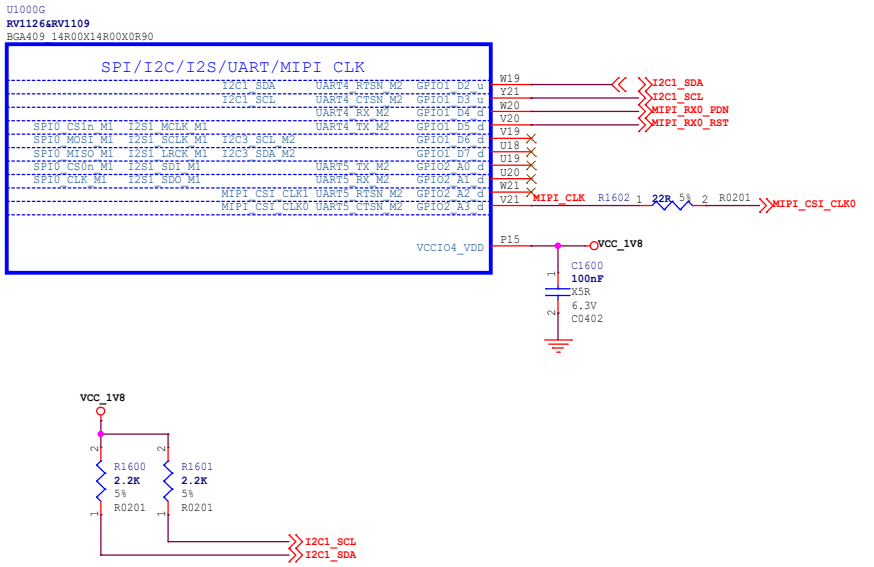
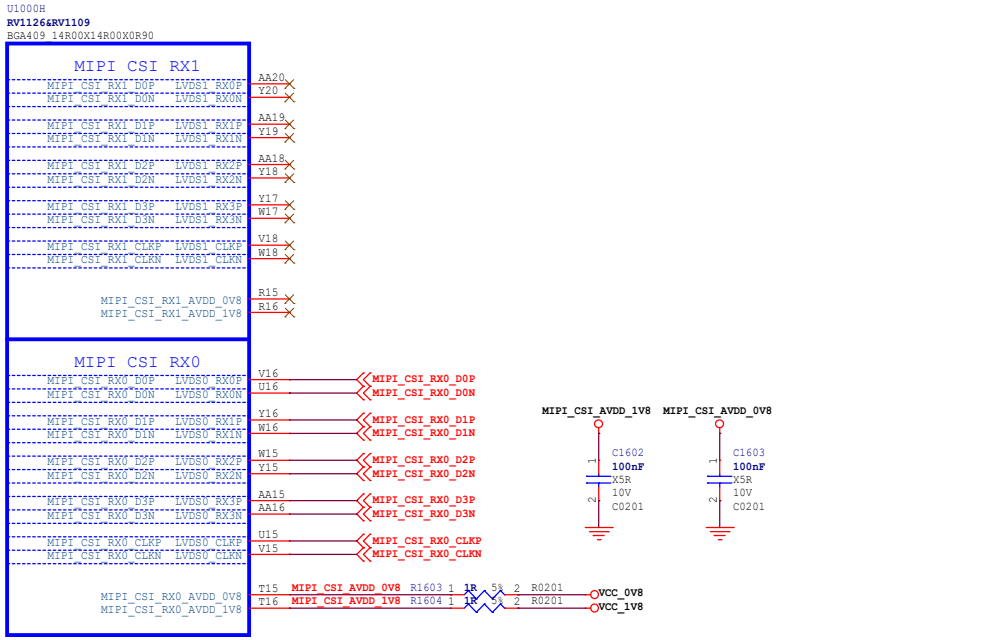
RGMII Interface



I2C/SPI/MIPI-CLK



MIPI-CSI Interface



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	16.RV1126&RV1109_VideoInput				
Date:	Friday, February 05, 2021			Rev:	V1.2
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LCDC/RGMII/PWM

U1000E
RV1126&RV1109
BGA409_14R00X14R00X0R90

LCDC/RGMII/CIF/UART/JTAG/I2S/SPI/I2C

		UART4_RTSN_M1		RGMII_TXD3_M1	CIF_D0_M1	LCDC_D0	GPIO2_A4_d
	I2C5_SCL_M0		UART4_CTSN_M1		RGMII_CRS_M1	CIF_D1_M1	LCDC_D1	GPIO2_A5_d
			UART4_TX_M1	PWM5_M1	RGMII_COL_M1	CIF_D2_M1	LCDC_D2	GPIO2_A6_d
		I2S2_SDO_M1	UART4_RX_M1	PWM4_M1	SPI0_CS0n_M2		LCDC_D3	GPIO2_A7_d
		I2S2_SDI_M1	UART5_TX_M1	PWM3_IR_M1	SPI0_MOSI_M2		LCDC_D4	GPIO2_B0_d
		I2S2_SCLK_M1	UART5_RX_M1	PWM2_M1	SPI0_MISO_M2		LCDC_D5	GPIO2_B1_d
		I2S2_LRCK_M1	UART5_RTSN_M1	PWM1_M1	SPI0_CLK_M2		LCDC_D6	GPIO2_B2_d
	I2C5_SDA_M0	I2S2_MCLK_M1	UART5_CTSN_M1	PWM0_M1	SPI0_CS1n_M2	CIF_D3_M1	LCDC_D7	GPIO2_B3_d
					RGMII_RXDV_M1	CIF_D4_M1	LCDC_D8	GPIO2_B4_d
					RGMII_RXD0_M1	CIF_D5_M1	LCDC_D9	GPIO2_B5_d
					RGMII_RXD1_M1	CIF_D6_M1	LCDC_D10	GPIO2_B6_d
					RGMII_CLK_M1	CIF_D7_M1	LCDC_D11	GPIO2_B7_d
					RGMII_RXER_M1	CIF_D8_M1	LCDC_D12	GPIO2_C0_d
					RGMII_MDIO_M1	CIF_D9_M1	LCDC_D13	GPIO2_C1_d
					RGMII_MDC_M1	CIF_D10_M1	LCDC_D14	GPIO2_C2_d
					RGMII_TXD0_M1	CIF_D11_M1	LCDC_D15	GPIO2_C3_d
					RGMII_TXD1_M1	CIF_D12_M1	LCDC_D16	GPIO2_C4_d
					CLK_OUT_ETHERNET_M1	CIF_D13_M1	LCDC_D17	GPIO2_C5_d
					RGMII_TXEN_M1	CIF_D14_M1	LCDC_D18	GPIO2_C6_d
		I2S1_MCLK_M2			RGMII_RXD2_M1	CIF_D15_M1	LCDC_D19	GPIO2_C7_d
		I2S1_SDO_M2			RGMII_RXD3_M1	CIF_VSYNC_M1	LCDC_D20	GPIO2_D0_d
		I2S1_SCLK_M2			RGMII_TXD2_M1	CIF_CLKOUT_M1	LCDC_D21	GPIO2_D1_d
		I2S1_LRCK_M2			RGMII_TXCLK_M1	CIF_CLKIN_M1	LCDC_D22	GPIO2_D2_d
		I2S1_SDI_M2			RGMII_RXCLK_M1	CIF_HSYNC_M1	LCDC_D23	GPIO2_D3_d
	I2C3_SCL_M1			PWM6_M1	SPI1_CS0n_M2		LCDC_DEN	GPIO2_D4_d
	I2C3_SDA_M1			PWM10_M1	SPI1_CLK_M2		LCDC_HSYNC	GPIO2_D5_d
			UART3_RTSN_M2	PWM9_M1	SPI1_MOSI_M2		LCDC_VSYNC	GPIO2_D6_d
			UART3_CTSN_M2	PWM8_M1	SPI1_MISO_M2		LCDC_CLK	GPIO2_D7_d
	I2C4_SCL_M0	CAN_RXD_M0	UART3_TX_M2	PWM7_IR_M1	SPI1_CS1n_M2			GPIO3_A0_u
	I2C4_SDA_M0	CAN_TXD_M0	UART3_RX_M2	PWM11_IR_M1				GPIO3_A1_u
	A7_JTAG_TCK_M1		UART2_TX_M1					GPIO3_A2_u
	A7_JTAG_TMS_M1		UART2_RX_M1					GPIO3_A3_u

J18 L17 M21 M20 L19 L20 K16 K17 K18 K19 K20 K21 J19 J21 J20 H20 H19 G21 G20 G19 H18 F21 F20 F19 J17 H17 C21 D21 E20 E19 G18 H16

LCD_IRQ
LCD_PWREN
RS485_CTL
I2C3_SCL
I2C3_SDA
LCD_RST
UART3_TX_485
UART3_RX_485
UART2_TX
UART2_RX

VCCIO5_VDD1 J15
VCCIO5_VDD2 K15
VCC_3V3

VCC_3V3
R1703 2.2K 5% R0201
R1704 2.2K 5% R0201
I2C3_SCL
I2C3_SDA

VCC_3V3
C1700 100nF X5R 10V C0201

MIPI-DSI Interface

U1000D
RV1126&RV1109
BGA409_14R00X14R00X0R90

MIPI DSI TX0

MIPI_DSI_TX0_D0P	A19	MIPI_DSI_D0P
MIPI_DSI_TX0_D0N	B19	MIPI_DSI_D0N
MIPI_DSI_TX0_D1P	A20	MIPI_DSI_D1P
MIPI_DSI_TX0_D1N	B20	MIPI_DSI_D1N
MIPI_DSI_TX0_D2P	B21	MIPI_DSI_D2P
MIPI_DSI_TX0_D2N	C20	MIPI_DSI_D2N
MIPI_DSI_TX0_D3P	D20	MIPI_DSI_D3P
MIPI_DSI_TX0_D3N	D19	MIPI_DSI_D3N
MIPI_DSI_TX0_CLKP	C19	MIPI_DSI_CLKP
MIPI_DSI_TX0_CLKN	C18	MIPI_DSI_CLKN
MIPI_DSI_TX0_AVDD_0V8	E18	VCC_0V8
MIPI_DSI_TX0_AVDD_1V8	G15	VCC_1V8

TP1700 TP_0.7
TP1701 TP_0.7
TP1702 TP_0.7
TP1703 TP_0.7

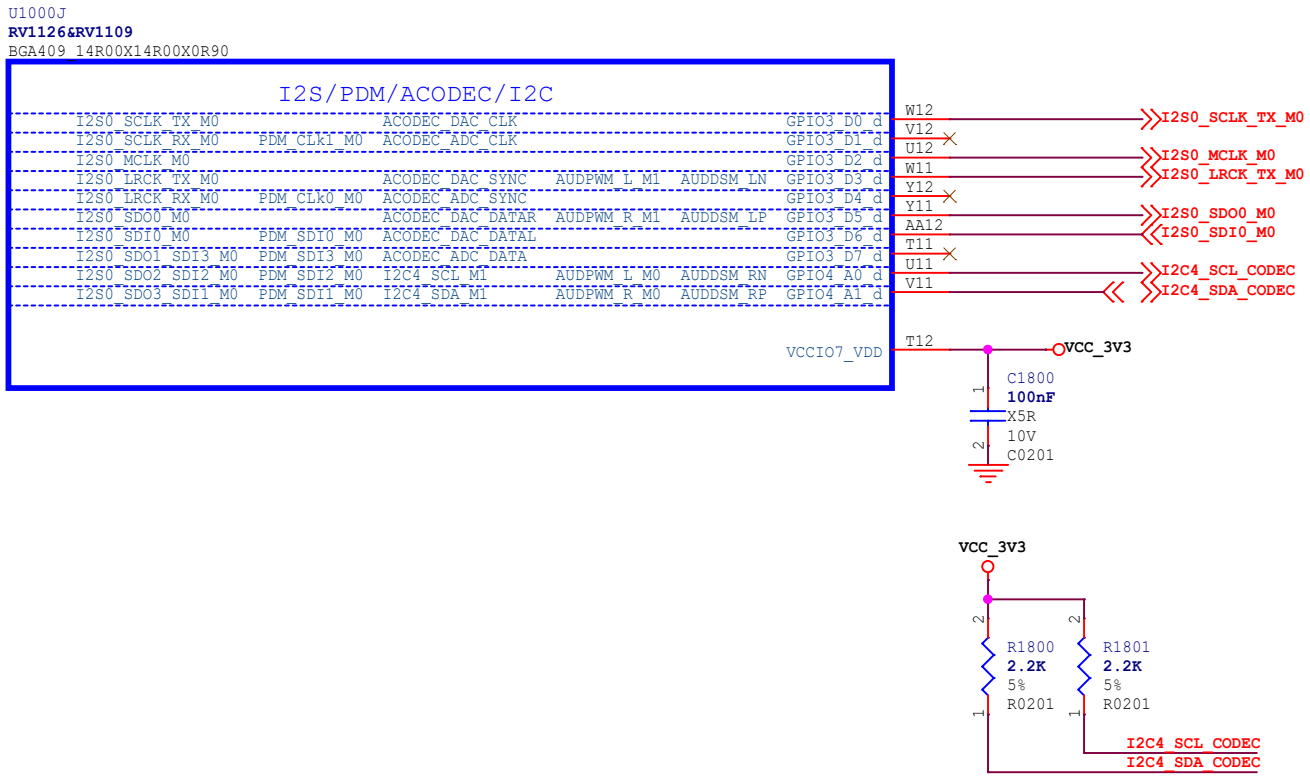
UART2_RX R1700 1K
UART2_TX R1701 1K
R0201
RX
TX
VCC_3V3

VCC_0V8
C1701 100nF X5R 10V C0201

VCC_1V8
C1702 100nF X5R 10V C0201

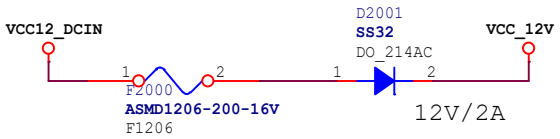
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	17.RV1126&RV1109_VideoOutput				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	15 of 27

Audio Interface

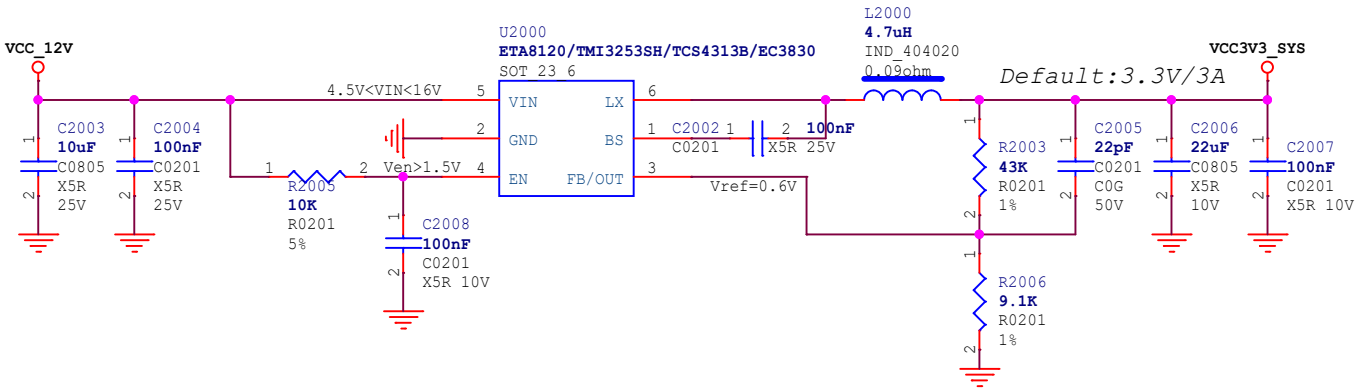


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	18.RV1126&RV1109_Audio				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	16 of 27

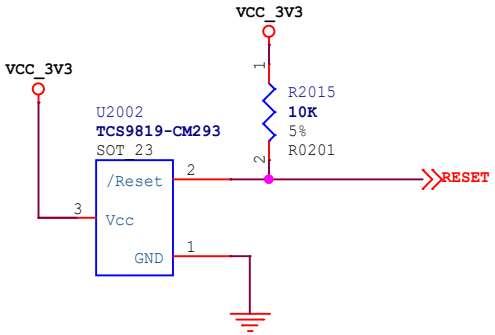
DC IN



VCC3V3_SYS

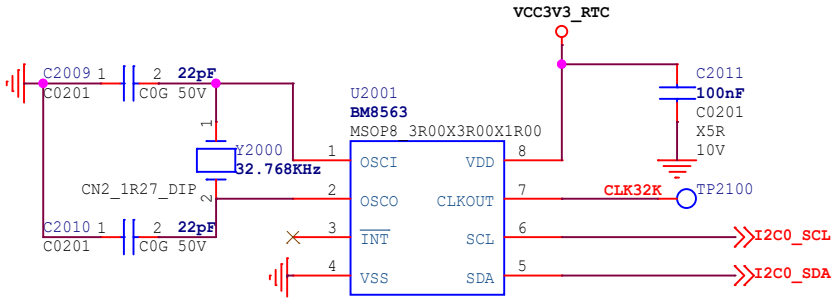


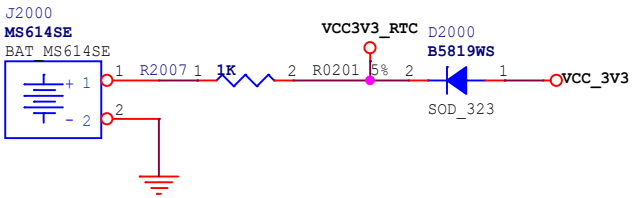
RESET



NOTE:
The Reset IC must select OD output,
otherwise the over-temperature protection
function cannot be enabled

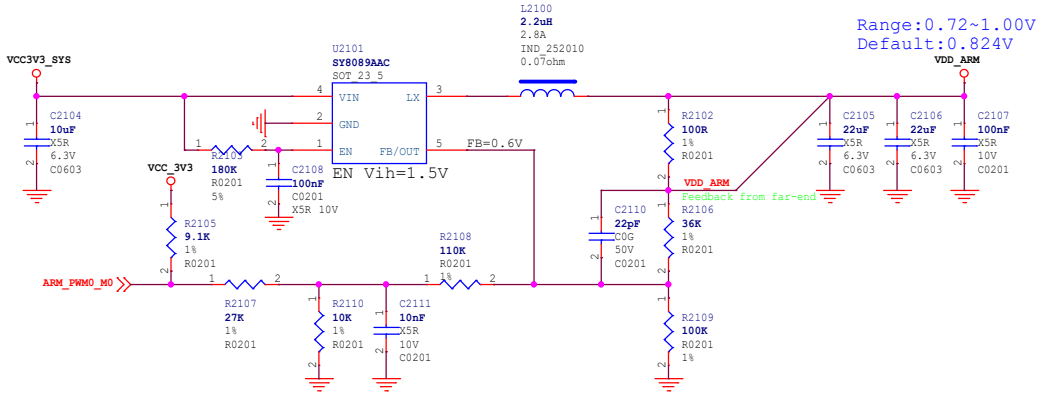
RTC CLOCK



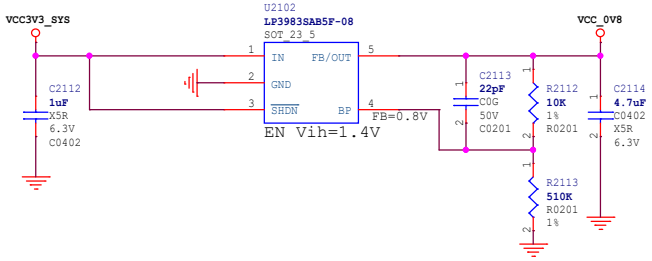


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	20.Power_DC IN				
Date:	Friday, February 05, 2021			Rev:	V1.21
Designed by:	LinXu	Reviewed by:	<Checker>	Sheet:	17 of 27

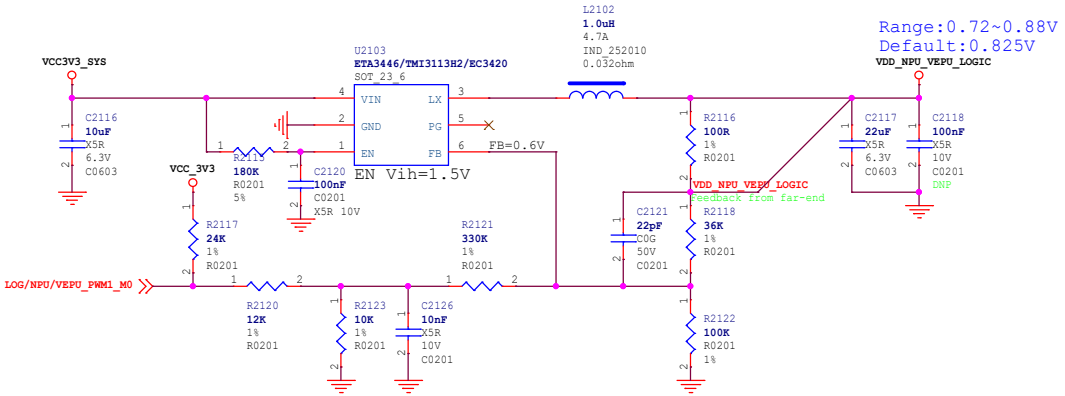
VDD_ARM



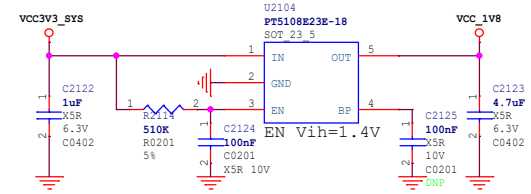
VCC_0V8



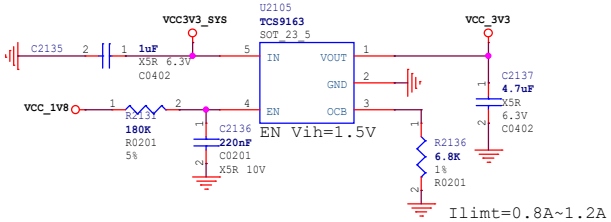
VDD_LOGIC/NPU/VEPU



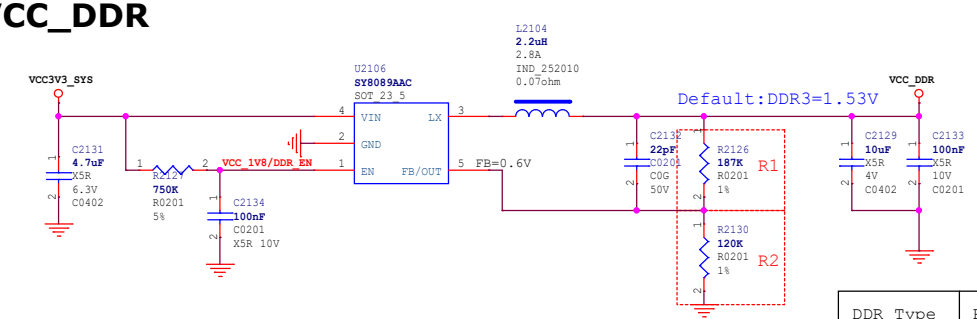
VCC_1V8



VCC_3V3



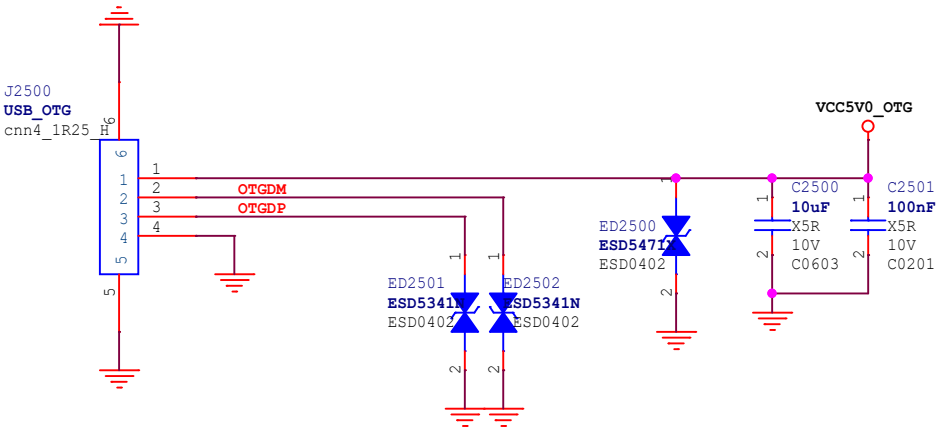
VCC_DDR

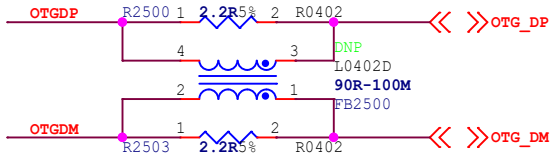


DDR Type	R1
DDR3	187K
DDR3L	150K

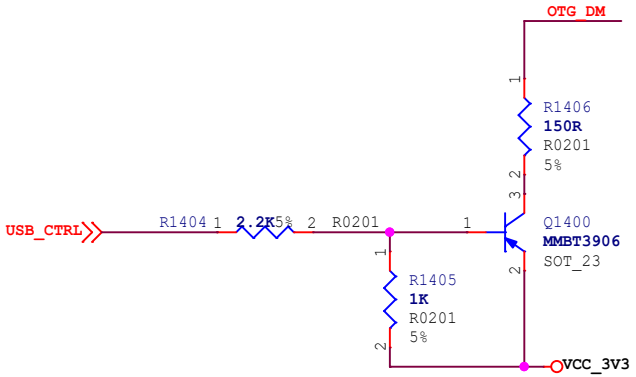
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	21.System Power				
Date:	Friday, February 05, 2021			Rev:	V1.21
Designed by:	LinXu	Reviewed by:	<Checker>	Sheet:	18 of 27

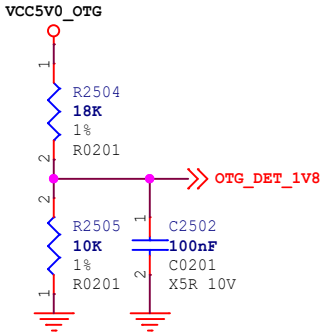
USB OTG





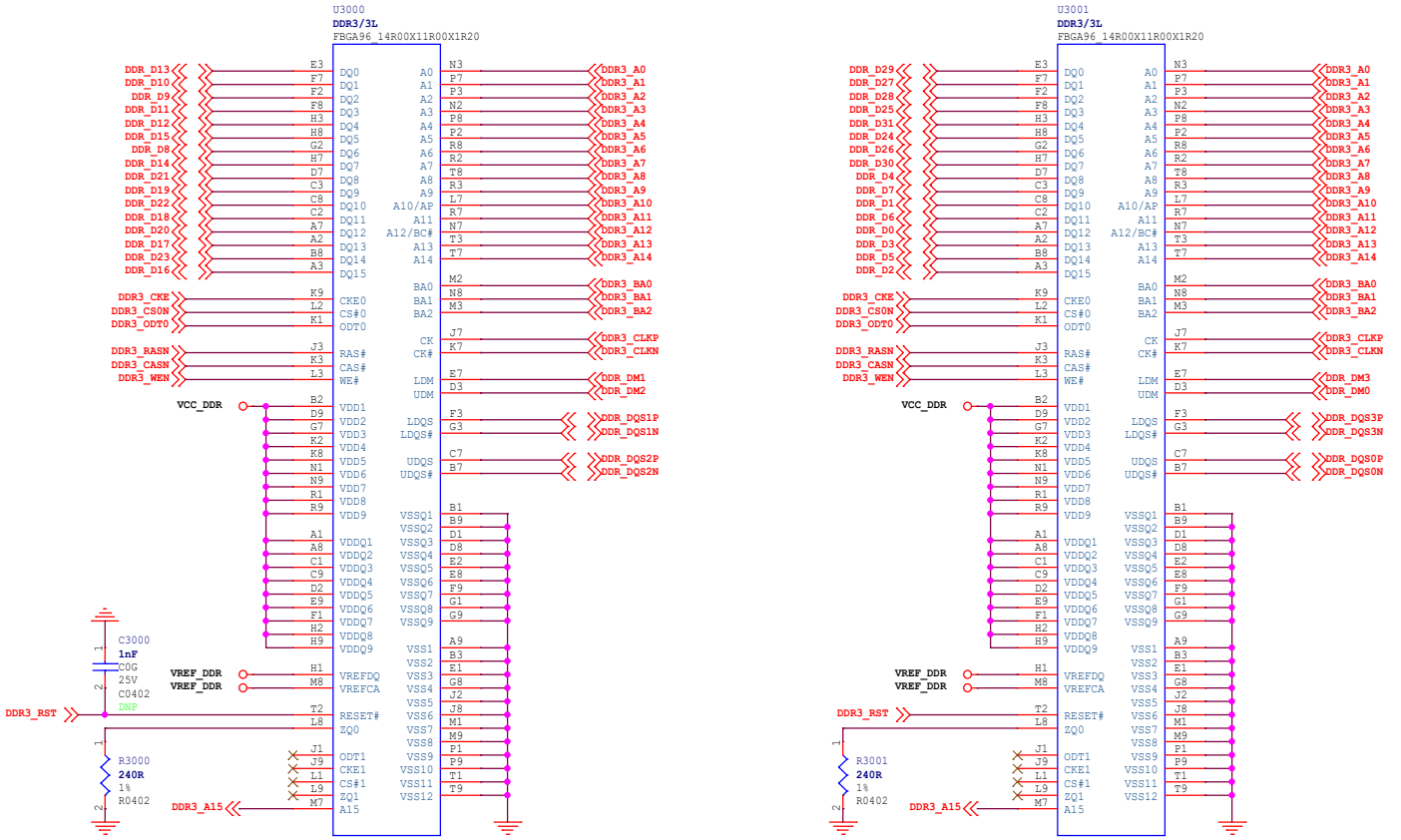
This circuit is used to improve usb compatibility.
Note:
These components are close to R2502 to avoid long branches.



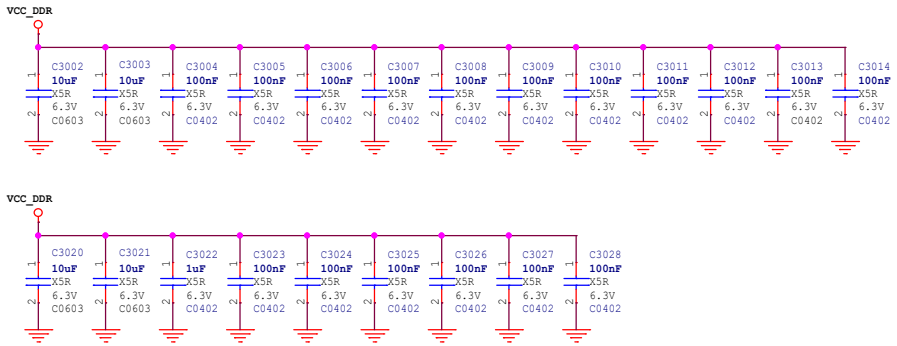


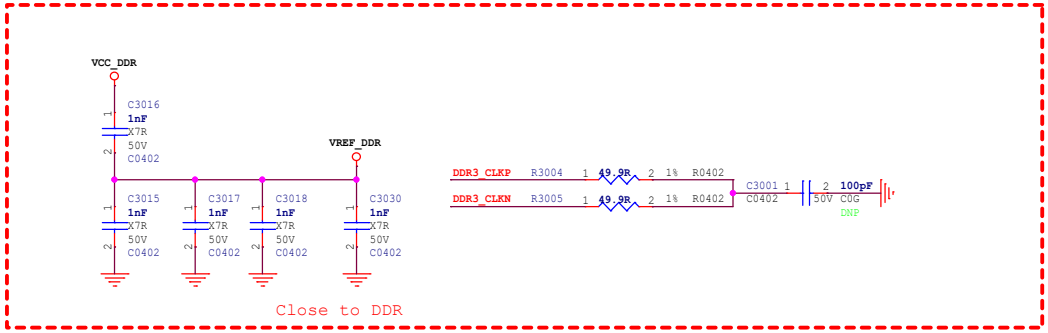
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	25.USB OTG				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	19 of 27

DDR3/DDR3L 2x16bit



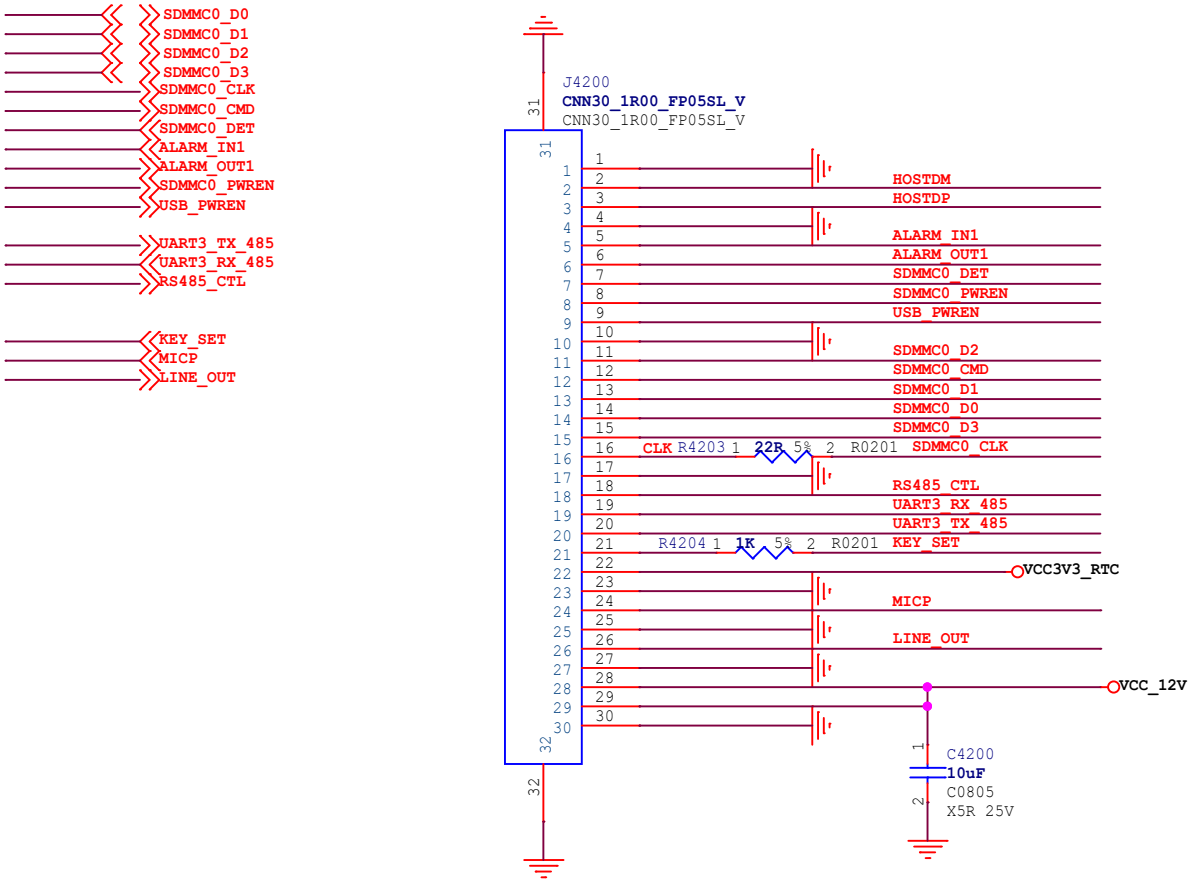
Note:All the Power filter capacitors should be placed close to the power pins of DDR3





Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	30.DRAM_DDR3/3L_96P_2X16bit				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	20 of 27

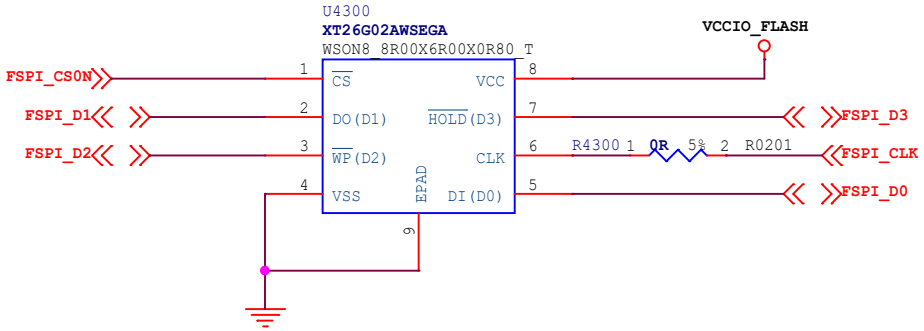
Extension port

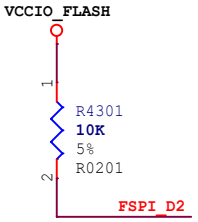


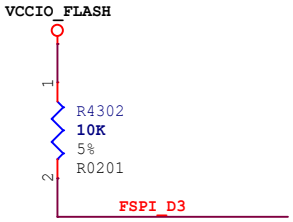
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	42.Flash-Micro-SD Card				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	21 of 27

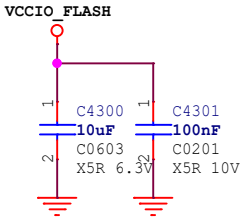
SPI Flash

NOTE:
Refer to the latest AVL for parts selection.



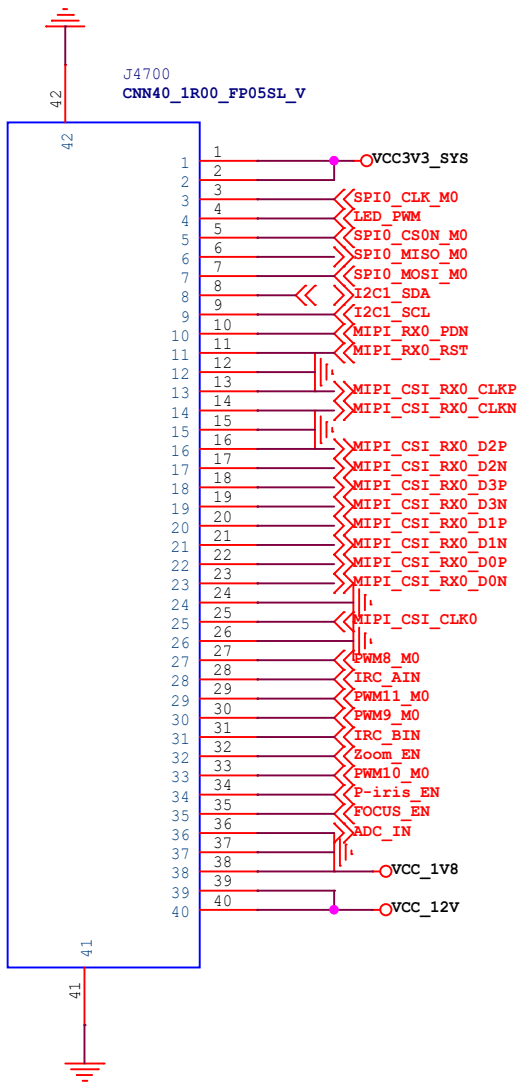


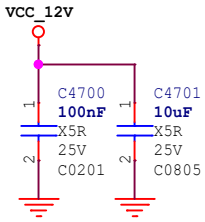


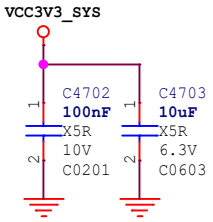


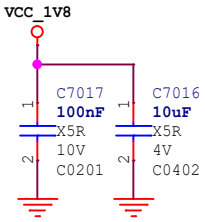
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	43.Flash-SPI Flash				
Date:	Friday, February 05, 2021			Rev:	V1.21
Designed by:	LinXu	Reviewed by:	<Checker>	Sheet:	22 of 27

MIPI CSI Interfae



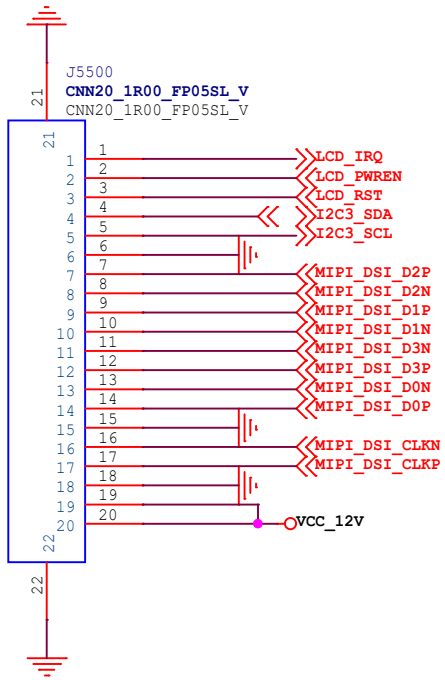


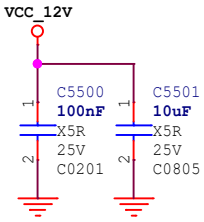




Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	47.VI-Camera_MIPI-CSI				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	23 of 27

MIPI DSI Interfae





Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	55.Vedio OUT				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	24 of 27

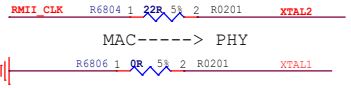
PHY

RMII_TXD0
RMII_TXD1
RMII_TXEN
RMII_RXDV
RMII_RXER
RMII_RXD0
RMII_RXD1
RMII_MDIO
RMII_MDC
RMII_CLK
EPHY_RST

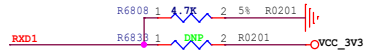
PHY Address/LED

RMII REF_CLK direction

Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode

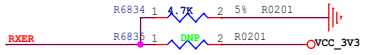


WOL/LED0 Selection



Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN

UTP / Fiber Selection

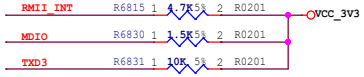


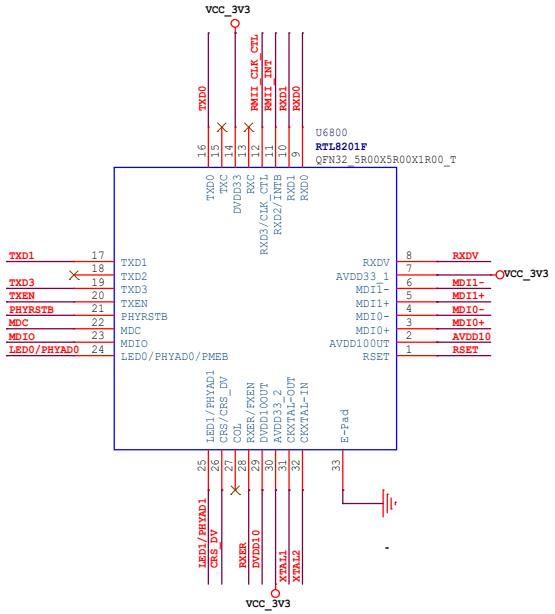
Pull Low for UTP Mode(default)
Pull High for Fiber Mode

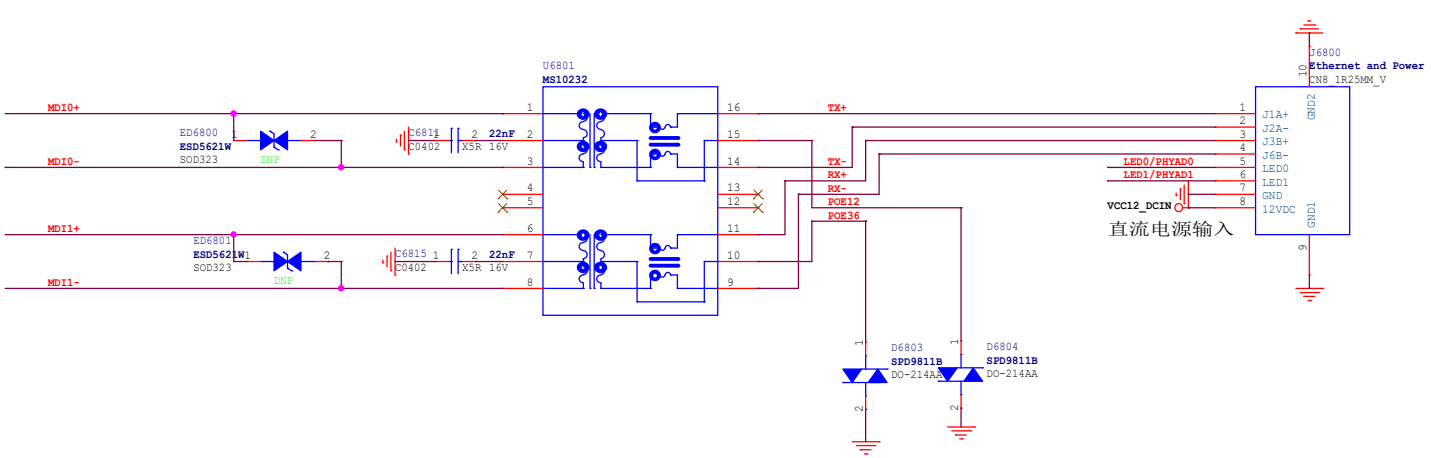
RMII_TXD0 — TXD0
RMII_TXD1 — TXD1
RMII_TXEN — TXEN
EPHY_RST — PHYRSTB
RMII_RXD0 — RXD0
RMII_RXD1 — RXD1
RMII_RXDV — CRS_DV
RMII_RXER — RXER
RMII_MDC — MDC
RMII_MDIO — MDIO

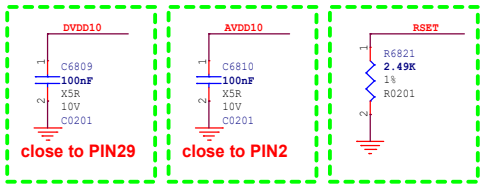
MII/RMII Selection

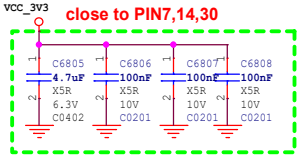
Pull High for RMII mode(default)



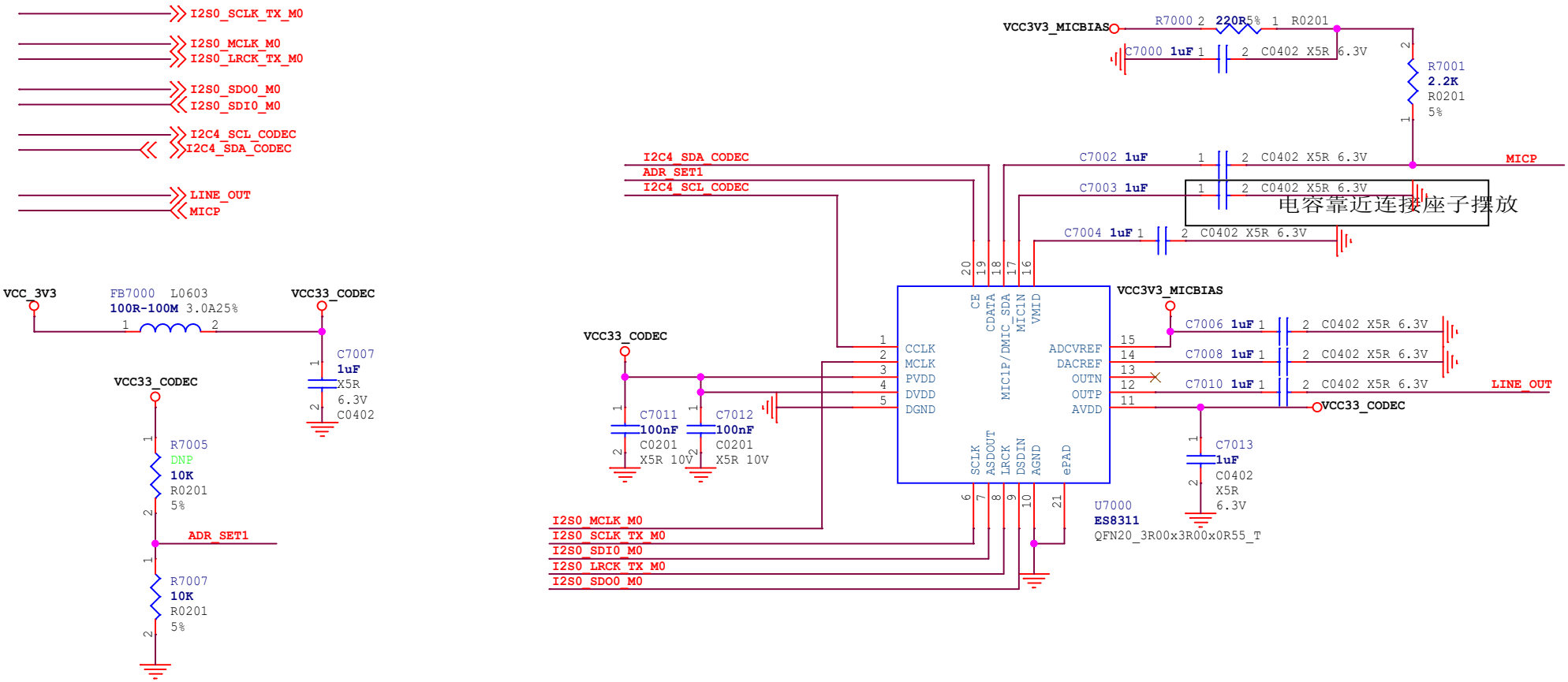




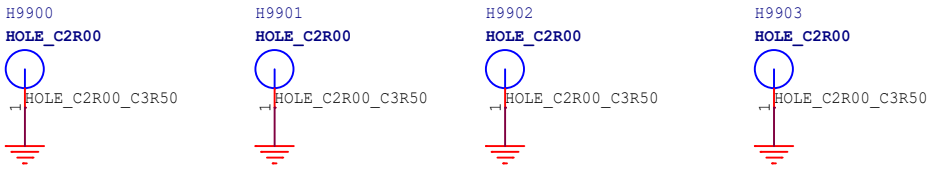




Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	68.Ethernet-EPHY_RMII				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	25 of 27



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	70.Audio Port				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	26 of 27



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126&1109 IPC38 MB				
File:	99.MARK/HOLE				
Date:	Friday, February 05, 2021			Rev:	V1.2
Designed by:	Linus.Lin	Reviewed by:	<Checker>	Sheet:	27 of 27