REVISION HISTORY

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Revision	Description	Date	Drawn	Checked
Ver 1.0	Initial Design	2017-10-24		
Ver 1.1	PCIe signal fix	2018-01-04		

PINE64	Desing name: Pine H64		
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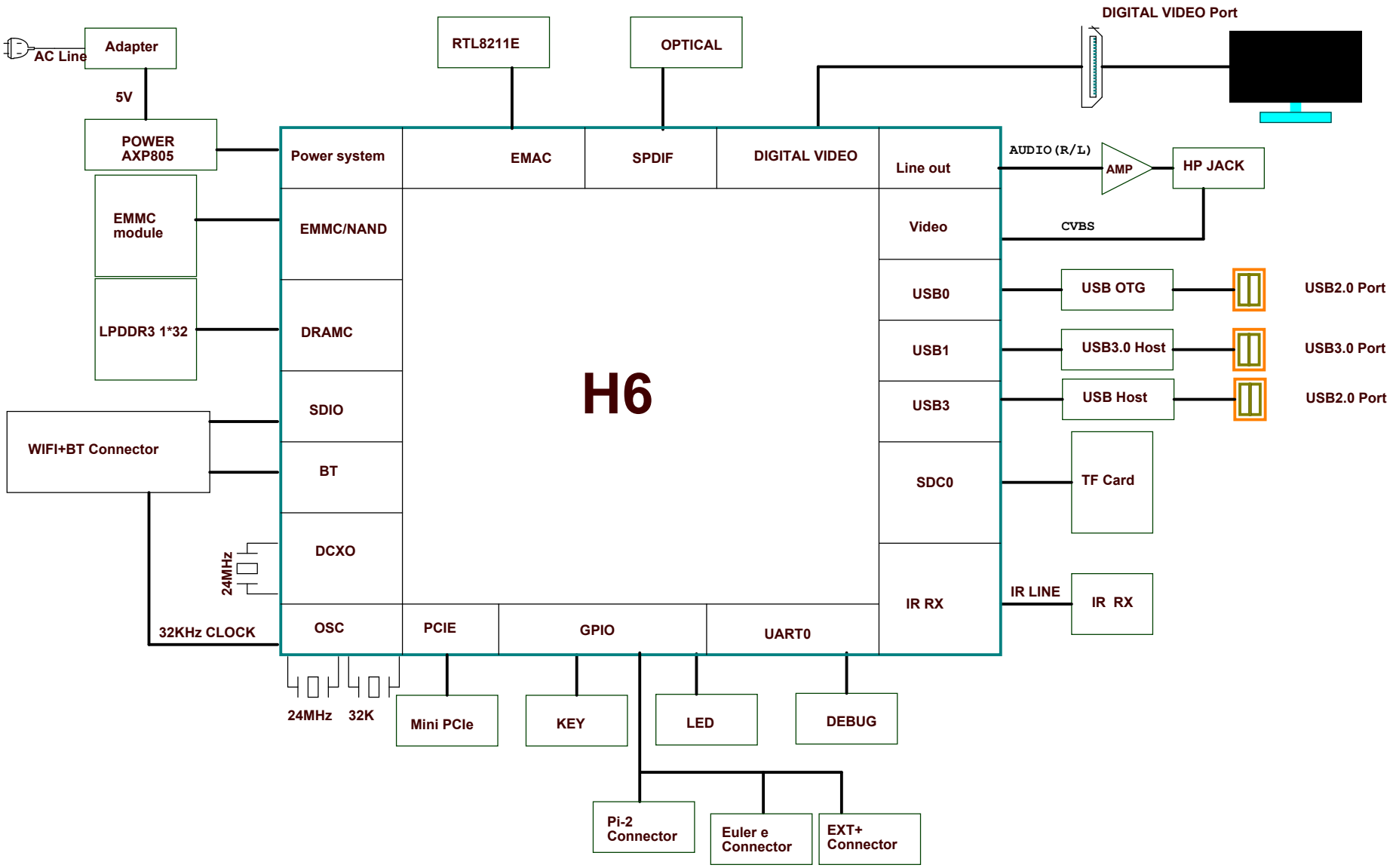
BLOCK



PINE64	Desing name	Pine H64
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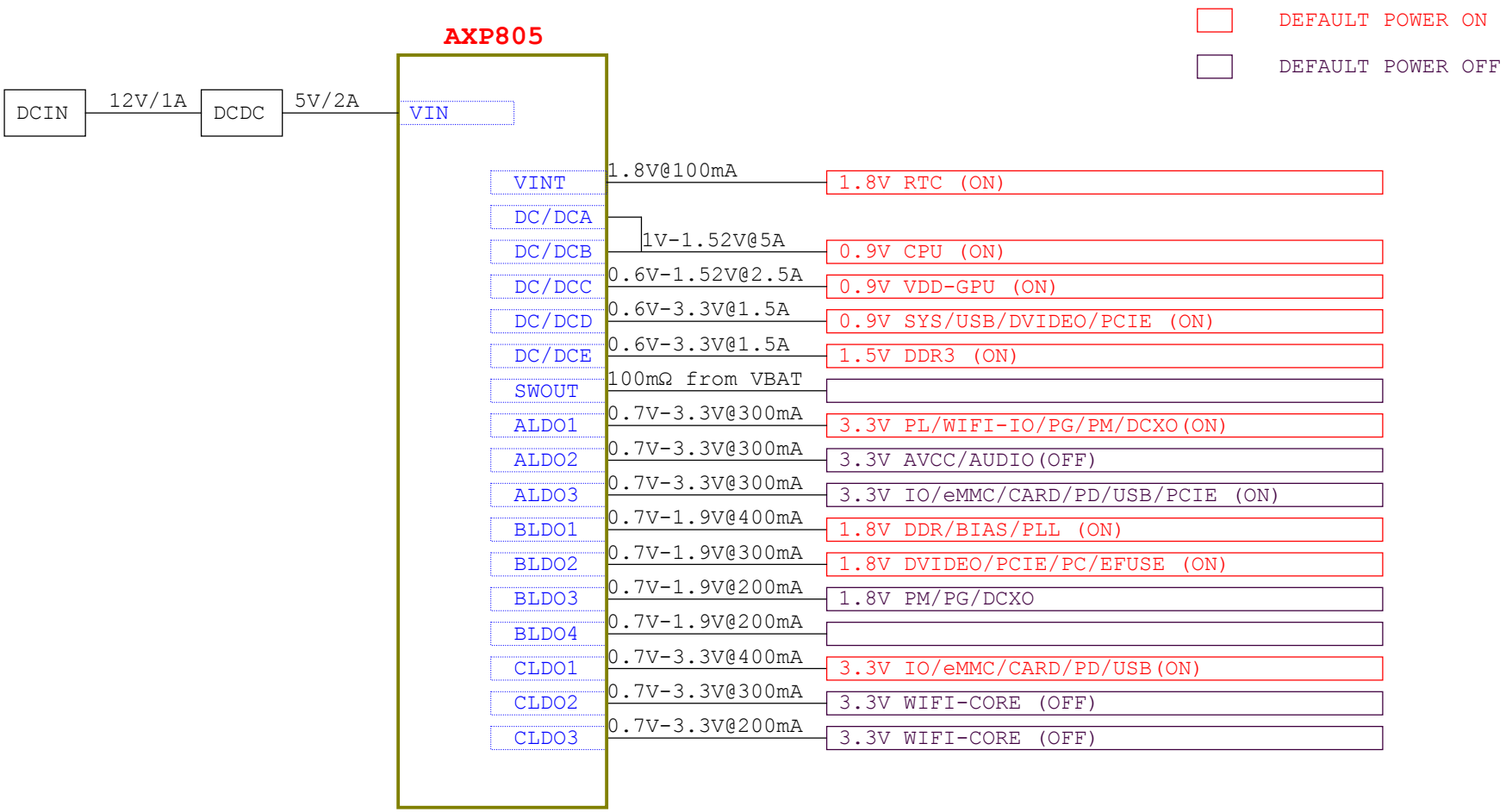
POWER TREE



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Pine H64 Port Assignmentver 1.0

Front:
- 2 x USB 2.0 type A port (top- OTG)
- 1x USB 3.0 type A port
- IR receiver (no need to staff IR connector, just reserved 3 pin connectors VCC, CIR_RX, GND)
- Head phone (with mic) jack
- 1x 90 degree angle small "Status" LED
- 2x push buttons – "RESET", "POWER"

Rear:
- 4K Digital Video Type-A port
- Gigabit Ethernet port
- +5V 3A 3.5mm OD/1.35mm ID barrel type DC power jack

Right side:
- eMMC module connector (top)
- microSD card slot (bottom)

Connectors on board:
- 2 pin RTC battery port
- miniPCIe connector (full length)
- 20 x 2 dual in line pins Pi-2 bus
- 17 x 2 dual in line pins port Euler 'e' bus
- 5 x 2 dual in line pins port EXT bus
- Wifi+BT port

GPIO Pins usage:
- PC0 - 16 — Used by eMMC module (SDC2)
- PD0 - 14 RGMII — Used by Ethernet RGMII
- PD14 - 18 — DMIC Ports
- PD19 - 22 — UART-2
- PD23 - 26 — UART-3
- PF0 - 5 — Used by TF Card (SDC0)
- PF6 — [Open to use]
- PG0 - 14 — Used by Wifi+BT(SDC1-SDIO,UART1,PCM2)
- PH0 - 4 — PCM0
- PH5 - 7 — OWA
- PH8 - 10 — Used by Digital Video
- PL0 - 10 — Used by system
- PM0 - 4 — [Open to use]

PIN	Define	CFG	Function
PC0	SPI0-CLK		eMMC
PC1	eMMC-DS		
PC2	SPI0-MOSI		
PC3	SPI0-MISO		
PC4	eMMC-CLK		
PC5	SPI0-CS		
PC6	eMMC-D0		
PC7	eMMC-D1		
PC8	eMMC-D2		
PC9	eMMC-D3		
PC10	eMMC-D4		
PC11	eMMC-D5		
PC12	eMMC-D6		
PC13	eMMC-D7		
PC14	eMMC-RST		
PC15	PCIe-RST		
PC16	GMAC-EN		

PIN	Define	CFG	Function
PF0	SDcard-D1		SDCard
PF1	SDcard-D0		
PF2	SDcard-CLK		
PF3	SDcard-CMD		
PF4	SDcard-D3		
PF5	SDcard-D2		
PF6	Pi2-PF6		

PIN	Define	CFG	Function
PG0	SDIO-CLK		Wifi/BT SDIO/UART module
PG1	SDIO-CMD		
PG2	SDIO-D0		
PG3	SDIO-D1		
PG4	SDIO-D2		
PG5	SDIO-D3		
PG6	UART1-TX		
PG7	UART1-RX		
PG8	UART1-RTS		
PG9	UART1-CTS		
PG10	I2S2-SYNC		
PG11	I2S2-CLK		
PG12	I2S2-DOUT		
PG13	I2S2-DIN		
PG14	PCIe-RST		

PIN	Define	CFG	Function
PD0	RGMII-RXD3		RGMII
PD1	RGMII-RXD2		
PD2	RGMII-RXD1		
PD3	RGMII-RXD0		
PD4	RGMII-RXCLK		
PD5	RGMII-RXCTL		
PD6	MAC-RST		
PD7	RGMII-TXD3		
PD8	RGMII-TXD2		
PD9	RGMII-TXD1		
PD10	RGMII-TXD0		
PD11	RGMII-TXCLK		
PD12	RGMII-TXCTL		
PD13	CLK125		
PD14	Pi2-PD14		

PIN	Define	CFG	Function
PH0	Euler-PH0		
PH1	Euler-PH1		
PH2	Euler-PH2		
PH3	Pi/Euler-PH3		
PH4	Pi2/Euler-PH4		
PH5	Pi2/Euler-PH5		
PH6	Pi2/Euler-PH6		
PH7	Euler-PH7(SPDIF)		
PH8	Pi2-PH8(ID_SC)		DIGITAL VIDEO
PH9	Pi2-PH9(ID_SD)		
PH10	DVIDEO-CEC		

PIN	Define	CFG	Function
PL0	Euler-PL0		
PL1	Euler-PL1		
PL2	Euler-PL2		
PL3	Euler-PL3		
PL4	Euler-PL4		
PL5	Euler-PL5		
PL6	Euler-PL6		
PL7	Euler-PL7		
PL8	Euler-PL8		
PL9	Euler-PL9(IR_RX)		
PL10	PCIe-WAKE		
PM0	Pi2-PM0		
PM1	Pi2-PM1		
PM2	Pi2-PM2		
PM3	Pi2-PM3		
PM4	Pi2-PM4		

PIN	Define	CFG	Function
PD15	Pi2-PD15		
PD16	Pi2-PD16		
PD17	Pi2-PD17		
PD18	Pi2-PD18		
PD19	Pi2-PD19(UART2_TX)		
PD20	Pi2-PD20(UART2_RX)		
PD21	Pi2-PD21		
PD22	Pi2-PD22(PWM0)		
PD23	Pi2-PD23		
PD24	Pi2-PD24		
PD25	Pi2-PD25(I2C0_CLK)		
PD26	Pi2-PD26(I2C0_DATA)		

EXT Connector

5V	1	2	HeartBeat LED
UBOOT	3	4	Reset Switch
Power Switch	5	6	GND
[PH0-UART0_TX]	7	8	[PH1-UART0_RX]
GND	9	10	KeyADC

Euler "e" Connector

3.3V	1	2	DC IN
N.C.	3	4	DC IN
N.C.	5	6	GND
[PL9-IR_RX]		7	8 5V
GND	9	10	[PH7-OWA_OUT] (SPDIF)
[PH4-I2S0_MCK/ SPI1_CLK]	11	12	[PH0-I2S0_SYNC]
[PH1-I2S0_BCK]	13	14	GND
[PH2-I2S0_DOUT]	15	16	[PH3-I2S0_DIN/ SPI1_CS]
3.3V	17	18	[PL8-S_PWM0]
[PL2-S_UART_TX]	19	20	GND
[PL3-S_UART_RX]	21	22	[PL4-S_JTAG_MS]
[PL0-S_TWI_SCK]	23	24	[PL1-S_TWI_SDA]
GND	25	26	[PL5-S_JTAG_CK]
[PL6-S_JTAG_DO]	27	28	[PL7-S_JTAG_DI]
[MIC2P]	29	30	[MIC2N]
[EAROUTP]	31	32	[EAROUTN]
[TVOUT]	33	34	GND

Pi-2 Connector

	3.3V	1	2	5V	
[PD26-TWI0_SDA]	GPIO 2 (I2C_SDA)	3	4	5V	
[PD25-TWI0_SCK]	GPIO 3 (I2C_SCL)	5	6	GND	
[PD22_PWM0]	GPIO 4 (GPCLK0)	7	8	GPIO 14 (UART_TXD)	[PD19-UART2_TX]
	GND	9	10	GPIO 15 (UART_RXD)	[PD20-UART2_RX]
[PD21]	GPIO 17	11	12	GPIO 18 (PCM_BCLK)	[PH1-I2S0_BCK]
[PD14/DMIC_CLK]	GPIO 27	13	14	GND	
[PD15/DMIC_DATA0]	GPIO 22	15	16	GPIO 23	[PD16/ DMIC_DATA1]
	3.3V	17	18	GPIO 24	[PD17/ DMIC_DATA2]
[PH5-SPI1_MOSI]	GPIO 10 (SPI_MOSI)	19	20	GND	
[PH6-SPI1_MISO]	GPIO 9 (SPI_MISO)	21	22	GPIO 25	[PD18/ DMIC_DATA3]
[PH4-SPI1_CLK]	GPIO 11 (SPI_SCLK)	23	24	GPIO 8 (SPI_CE0)	[PH3-SPI1_CS]
	GND	25	26	GPIO 7 (SPI_CE1)	[PF6]
[PH9-HSDA]	ID_SD		27 28	ID_SC	[PH8-HSCL]
[PM0]	GPIO 5	29	30	GND	
[PM1]	GPIO 6	31	32	GPIO 12	[PM2]
[PM3]	GPIO 13	33	34	GND	
[PH0-I2S0_SYNC]	GPIO 19(PCM_LRCK)	35	36	GPIO 16	[PM4]
[PD23- TWI2_SCL/UART3_TX]	GPIO 26	37	38	GPIO 20	[PD24- TWI2_SDA/UART3_RX]
	GND	39	40	GPIO 21 (PCM_ DO)	[PH2-I2S0_DOUT]

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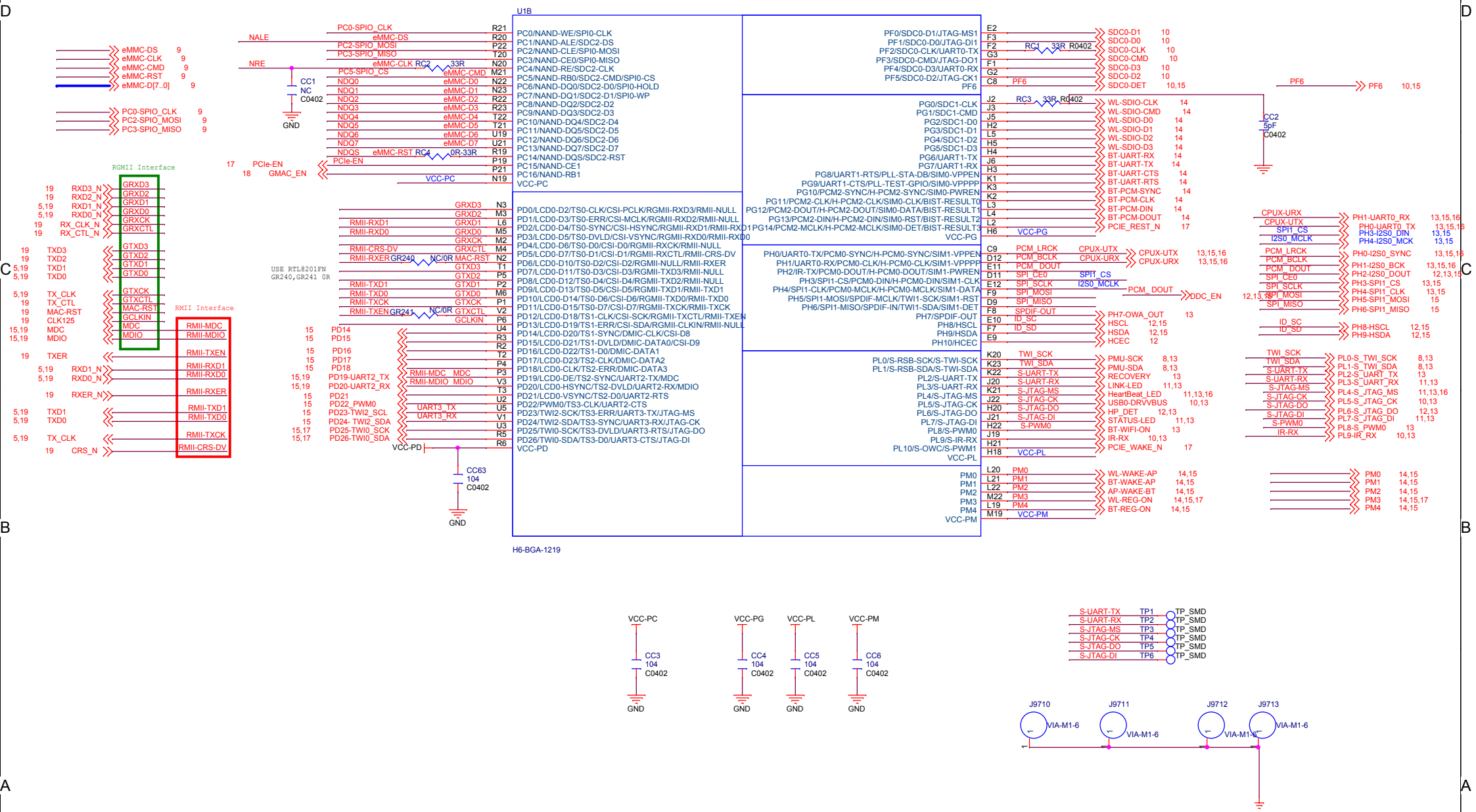
PC,PD, 部分IO口不具备中断功能
PF,PG,PH,PL,PM，部分IO口有中断功能



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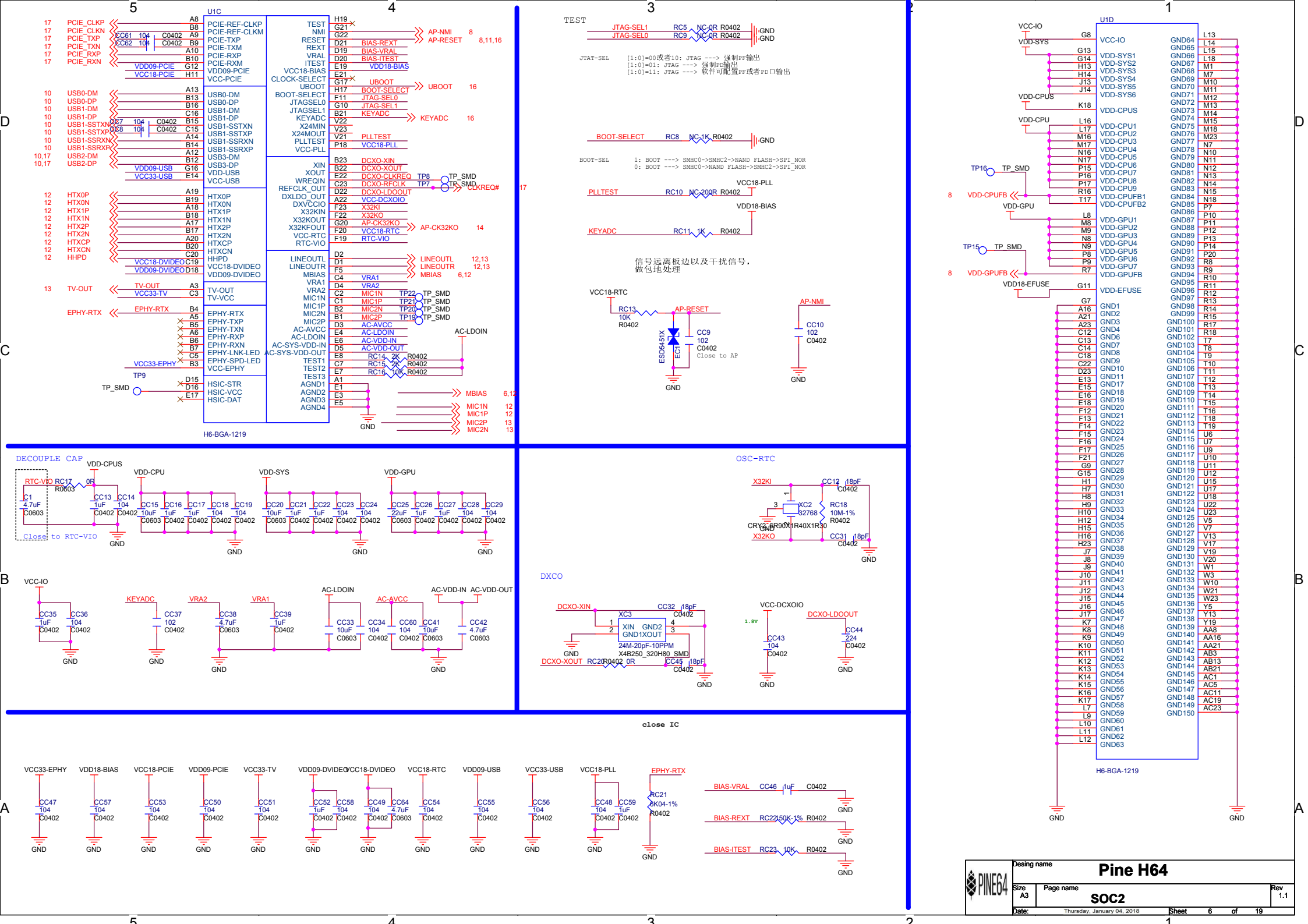
U1C
H6-BGA-1219
TEST
JTAG-SEL1
JTAG-SEL0
JTAT-SEL
[1:0]=00或者10: JTAG ---> 强制PF输出
[1:0]=01: JTAG ---> 强制PD输出
[1:0]=11: JTAG ---> 软件可配置PF或者PD口输出
BOOT-SELECT
BOOT-SEL
1: BOOT ---> SMHC0->SMHC2->NAND FLASH->SPI_NOR
0: BOOT ---> SMHC0->NAND FLASH->SMHC2->SPI_NOR
PLLTEST
KEYADC
信号远离板边以及干扰信号，
做包地处理
VCC18-RTC
AP-RESET
AP-NMI
ESD5451X
DECOUPLE CAP
VDD-CPUS
VDD-CPU
VDD-SYS
VDD-GPU
Close to RTC-VIO
OSC-RTC
X32KI
X32KO
DXCO
DCXO-XIN
DCXO-XOUT
24M-20pF-10PPM
X4B250_320H80_SMD
VCC-DCXOIO
DCXO-LDOOUT
close IC
VCC33-EPHY
VDD18-BIAS
VCC18-PCIE
VDD09-PCIE
VCC33-TV
VDD09-DVIDEO
VCC18-DVIDEO
VCC18-RTC
VDD09-USB
VCC33-USB
VCC18-PLL
EPHY-RTX
BIAS-VRAL
BIAS-REXT
BIAS-ITEST
U1D
H6-BGA-1219
Desing name
Pine H64
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SOC2
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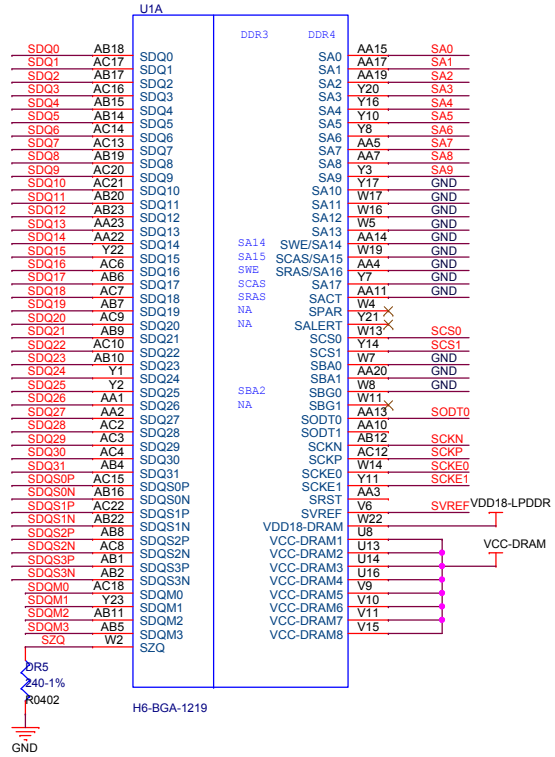
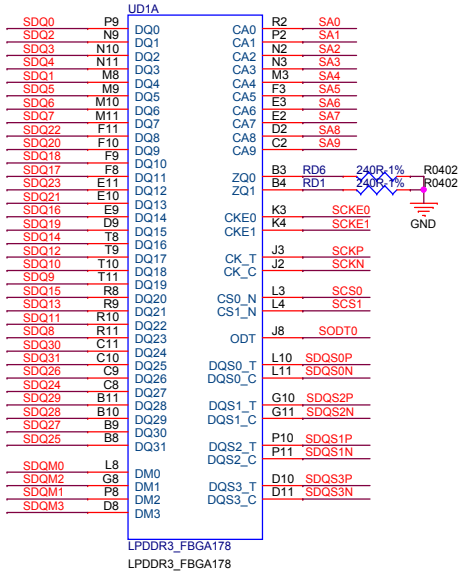
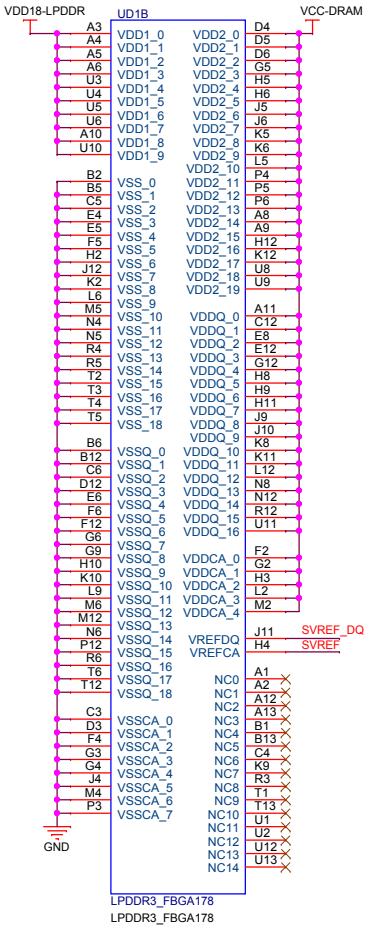
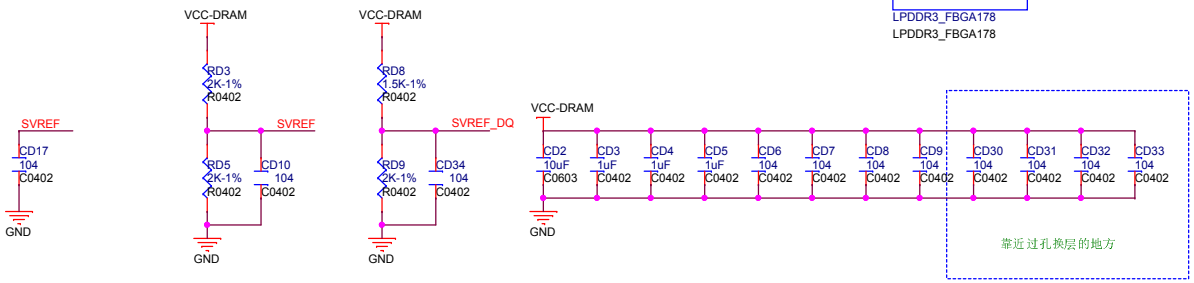
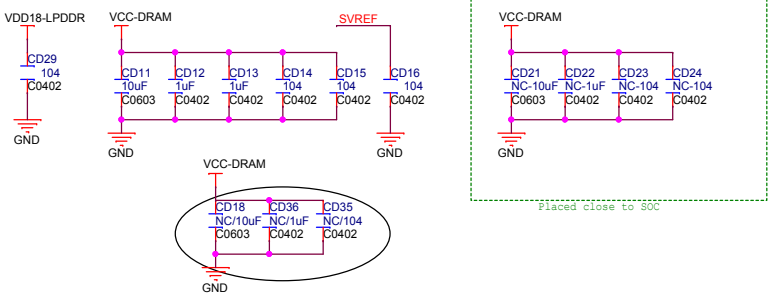
LPDDR3

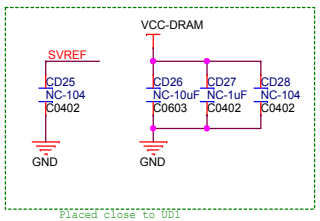


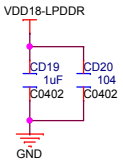


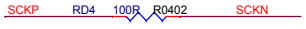












PINE64	Desing name	Pine H64	
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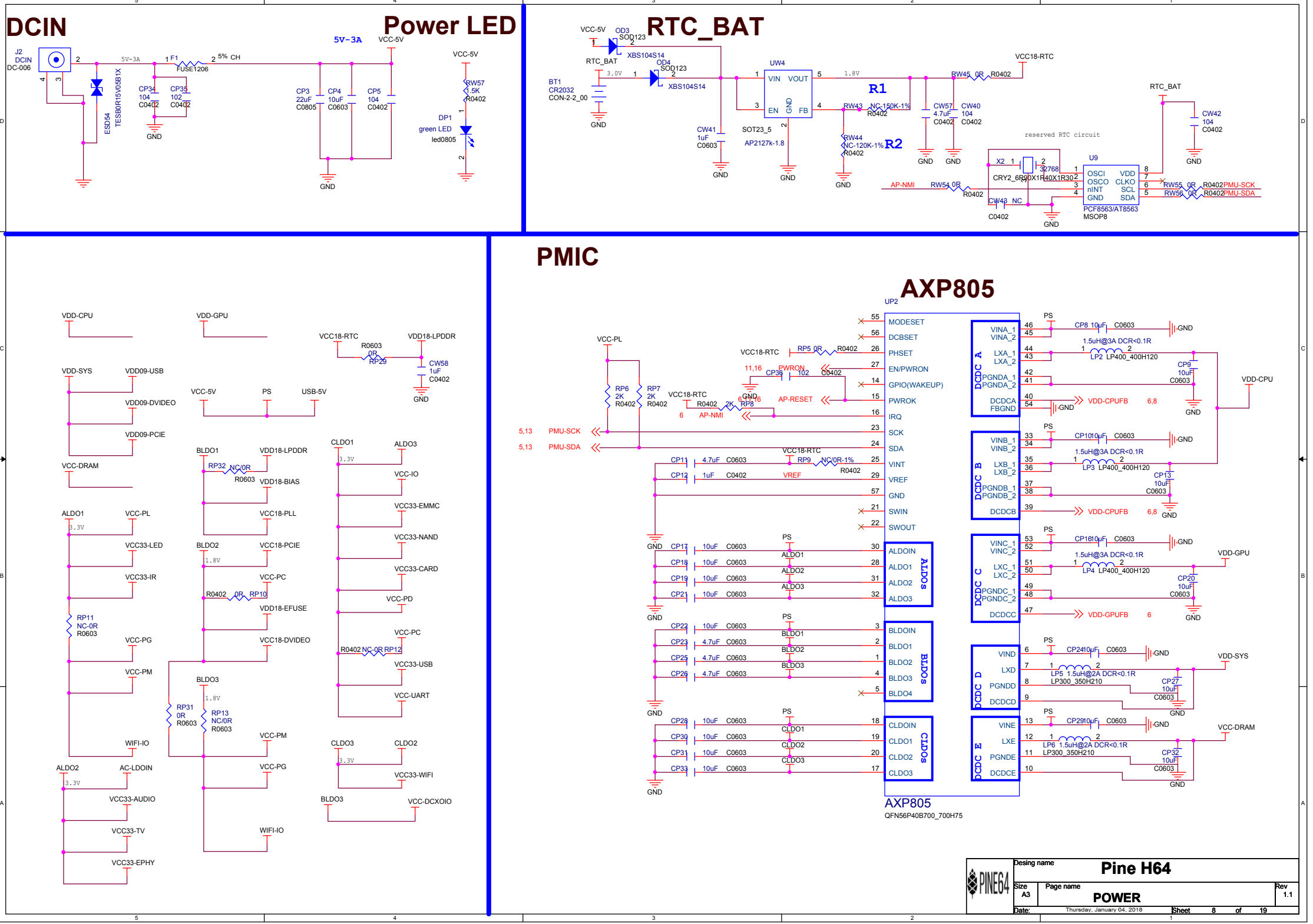
DCIN
Power LED
RTC_BAT
PMIC
AXP805
J2
DCIN
DC-006
5V-3A
F1
FUSE1206
5% CH
VCC-5V
CP34
104
C0402
CP35
102
C0402
GND
CP3
22uF
C0805
CP4
10uF
C0603
CP5
104
C0402
RW57
1.5K
R0402
DP1
green LED
led0805
ESD54
TESB0R15V05B1X
BT1
CR2032
CON-2-2_00
RTC_BAT
3.0V
XBS104S14
OD3
OD4
SOD123
UW4
VIN
VOUT
EN
GND
FB
SOT23_5
AP2127k-1.8
1.8V
R1
R2
RW43
NC-150K-1%
RW44
NC-120K-1%
R0402
CW41
1uF
C0603
CW57
4.7uF
C0402
CW40
104
C0402
VCC18-RTC
RW45 0R
reserved RTC circuit
X2
32768
CRY2_6R0X1R40X1R30
U9
OSCI
OSCO
nINT
GND
VDD
CLKO
SCL
SDA
PCF8563/AT8563
MSOP8
CW42
104
C0402
AP-NMI
RW54 0R
CW43 NC
RW55 0R
RW56 0R
R0402PMU-SCK
R0402PMU-SDA
VDD-CPU
VDD-GPU
VDD-SYS
VDD09-USB
VDD09-DVIDEO
VDD09-PCIE
VCC-DRAM
VCC-5V
PS
USB-5V
VCC18-RTC
R0603
0R
RP29
VDD18-LPDDR
CW58
1uF
C0402
BLDO1
RP32 NC/0R
R0603
VDD18-BIAS
VCC18-PLL
BLDO2
1.8V
VCC18-PCIE
VCC-PC
R0402 0R RP10
VDD18-EFUSE
VCC18-DVIDEO
BLDO3
1.8V
RP31
0R
R0603
RP13
NC/0R
R0603
VCC-PM
VCC-PG
WIFI-IO
CLDO1
3.3V
ALDO3
VCC-IO
VCC33-EMMC
VCC33-NAND
VCC33-CARD
VCC-PD
VCC-PC
R0402 NC-0R RP12
VCC33-USB
VCC-UART
CLDO3
CLDO2
VCC33-WIFI
VCC-DCXOIO
ALDO1
3.3V
VCC-PL
VCC33-LED
VCC33-IR
RP11
NC-0R
R0603
VCC-PG
VCC-PM
WIFI-IO
ALDO2
AC-LDOIN
VCC33-AUDIO
VCC33-TV
VCC33-EPHY
UP2
MODESET
DCBSET
PHSET
EN/PWRON
GPIO(WAKEUP)
PWROK
IRQ
SCK
SDA
VINT
VREF
GND
SWIN
SWOUT
PWRON
AP-RESET
PMU-SCK
PMU-SDA
RP5 0R
RP6
2K
R0402
RP7
2K
R0402
RP8
RP9
NC/0R-1%
CP36
102
C0402
CP11
4.7uF
C0603
CP12
1uF
C0402
ALDOIN
ALDO1
ALDO2
ALDO3
ALDOs
BLDOIN
BLDO1
BLDO2
BLDO3
BLDO4
BLDOs
CLDOIN
CLDO1
CLDO2
CLDO3
CLDOs
CP17
CP18
CP19
CP21
CP22
CP23
CP25
CP26
CP28
CP30
CP31
CP33
10uF
C0603
4.7uF
C0603
DCDC A
VINA_1
VINA_2
LXA_1
LXA_2
PGNDA_1
PGNDA_2
DCDCA
FBGND
CP8 10uF C0603
1.5uH@3A DCR<0.1R
LP2 LP400_400H120
CP9
10uF
C0603
VDD-CPUFB
6,8
DCDC B
VINB_1
VINB_2
LXB_1
LXB_2
PGNDB_1
PGNDB_2
DCDCB
CP10 10uF C0603
1.5uH@3A DCR<0.1R
LP3 LP400_400H120
CP13
10uF
C0603
DCDC C
VINC_1
VINC_2
LXC_1
LXC_2
PGNDC_1
PGNDC_2
DCDCC
CP16 10uF C0603
1.5uH@3A DCR<0.1R
LP4 LP400_400H120
CP20
10uF
C0603
VDD-GPUFB
DCDC D
VIND
LXD
PGNDD
DCDCD
CP24 10uF C0603
LP5 1.5uH@2A DCR<0.1R
LP300_350H210
CP27
10uF
C0603
VDD-SYS
DCDC E
VINE
LXE
PGNDE
DCDCE
CP29 10uF C0603
LP6 1.5uH@2A DCR<0.1R
LP300_350H210
CP32
10uF
C0603
VCC-DRAM
AXP805
QFN56P40B700_700H75
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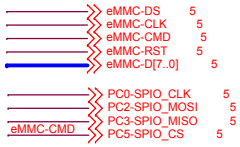
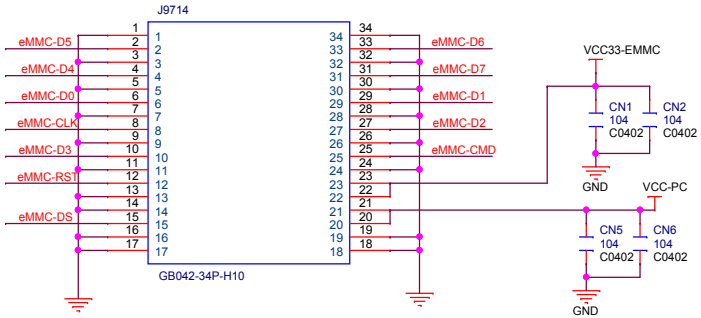
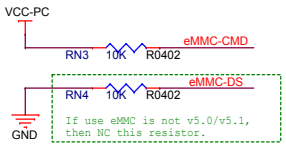
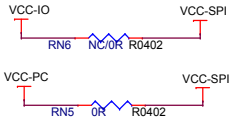
eMMC module/SIP Flash



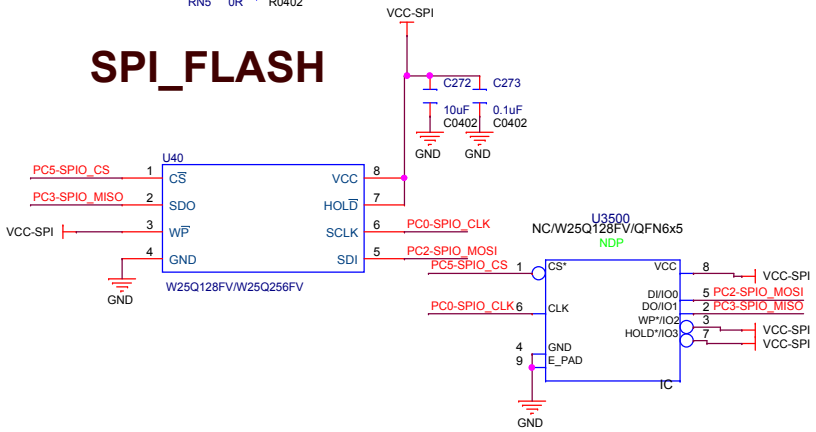




NOTE:Use spi IC voltage of 1V8 ADD RN5 0OHM,NC RN6.
Use spi IC voltage of 3V3 ADD RN6 0OHM,NC RN5.



SPI_FLASH



PINE64	Desing name	Pine H64	
	Size A3	Page name EMMC/SIP FLASH	Rev 1.1
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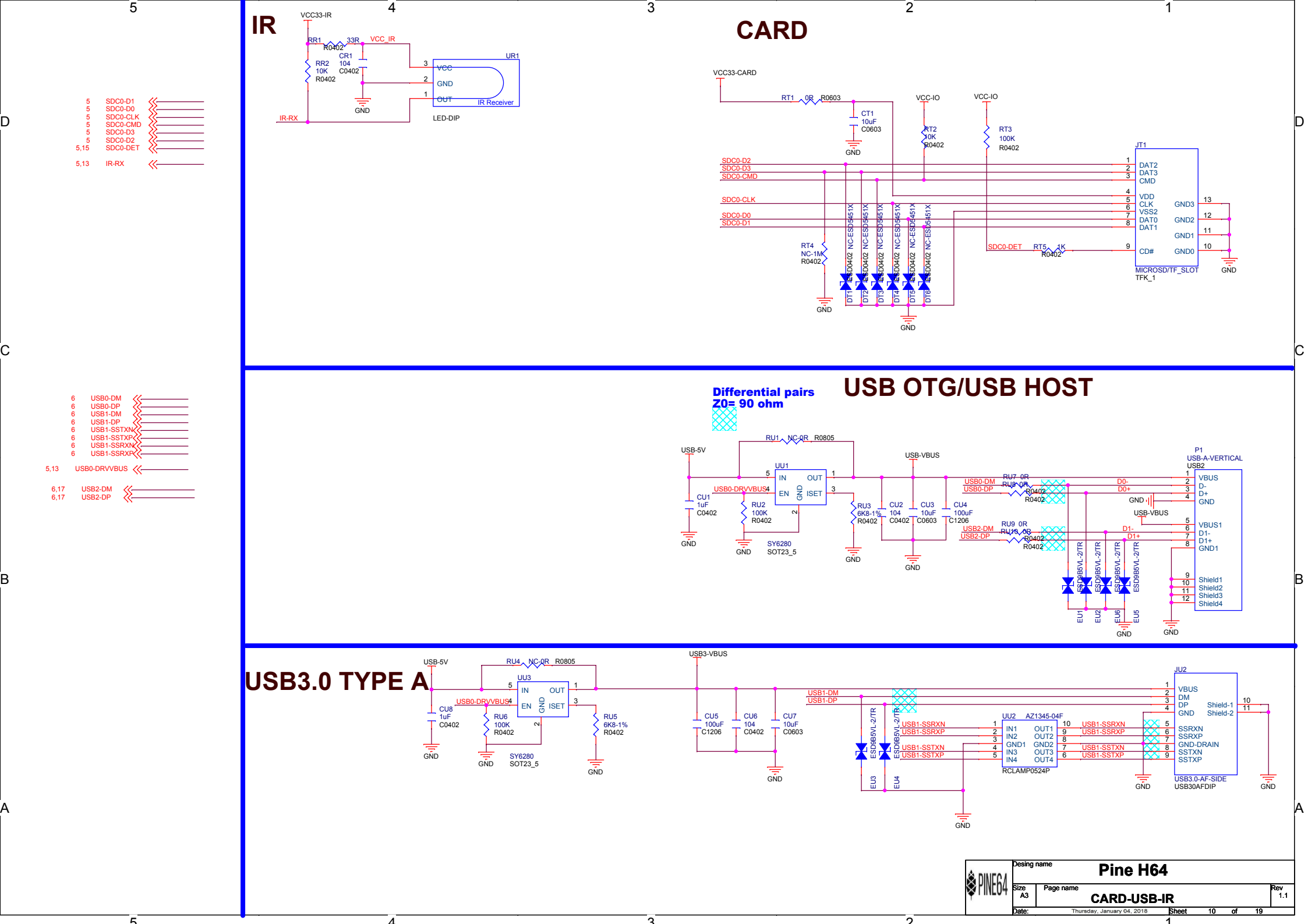
IR
CARD
USB OTG/USB HOST
Differential pairs
Z0= 90 ohm
USB3.0 TYPE A
5 SDC0-D1
5 SDC0-D0
5 SDC0-CLK
5 SDC0-CMD
5 SDC0-D3
5 SDC0-D2
5,15 SDC0-DET
5,13 IR-RX
6 USB0-DM
6 USB0-DP
6 USB1-DM
6 USB1-DP
6 USB1-SSTXN
6 USB1-SSTXP
6 USB1-SSRXN
6 USB1-SSRXP
5,13 USB0-DRVVBUS
6,17 USB2-DM
6,17 USB2-DP
VCC33-IR
RR1 33R R0402
VCC_IR
RR2 10K R0402
CR1 104 C0402
UR1
VCC
GND
OUT
IR Receiver
LED-DIP
IR-RX
VCC33-CARD
RT1 0R R0603
CT1 10uF C0603
VCC-IO
RT2 10K R0402
RT3 100K R0402
JT1
DAT2
DAT3
CMD
VDD
CLK
VSS2
DAT0
DAT1
CD#
GND3
GND2
GND1
GND0
MICROSD/TF_SLOT
TFK_1
RT4 NC-1M R0402
RT5 1K R0402
NC-ESD0402 NC-ESD5451X
DT1
DT2
DT3
DT4
DT5
DT6
RU1 NC-0R R0805
USB-5V
UU1
IN
OUT
EN
GND
ISET
CU1 1uF C0402
RU2 100K R0402
SY6280 SOT23_5
RU3 6K8-1% R0402
CU2 104 C0402
CU3 10uF C0603
CU4 100uF C1206
USB-VBUS
USB0-DM
USB0-DP
RU7 0R R0402
RU8 0R R0402
D0-
D0+
USB2-DM
USB2-DP
RU9 0R R0402
RU10 0R R0402
D1-
D1+
P1
USB-A-VERTICAL
USB2
VBUS
D-
D+
GND
VBUS1
D1-
D1+
GND1
Shield1
Shield2
Shield3
Shield4
ESD9B5VL-2/TR
EU1
EU2
EU5
EU6
RU4 NC-0R R0805
UU3
CU8 1uF C0402
RU6 100K R0402
RU5 6K8-1% R0402
USB3-VBUS
CU5 100uF C1206
CU6 104 C0402
CU7 10uF C0603
USB1-DM
USB1-DP
USB1-SSRXN
USB1-SSRXP
USB1-SSTXN
USB1-SSTXP
UU2 AZ1345-04F
IN1
IN2
GND1
IN3
IN4
OUT1
OUT2
GND2
OUT3
OUT4
RCLAMP0524P
EU3
EU4
JU2
VBUS
DM
DP
GND
Shield-1
Shield-2
SSRXN
SSRXP
GND-DRAIN
SSTXN
SSTXP
USB3.0-AF-SIDE
USB30AFDIP
PINE64
Desing name
Pine H64
Size A3
Page name
CARD-USB-IR
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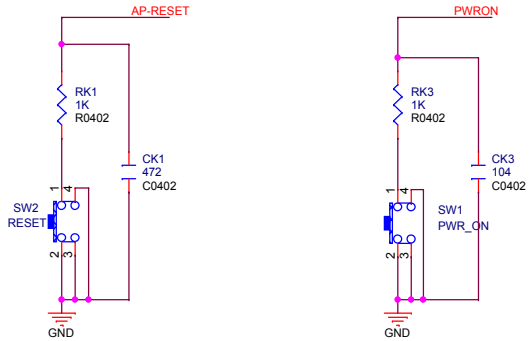
5,13,15,16 CPUX-UTX
5,13,15,16 CPUX-URX
5,13,16 HeartBeat_LED
5,13 STATUS-LED
5,13 LINK-LED

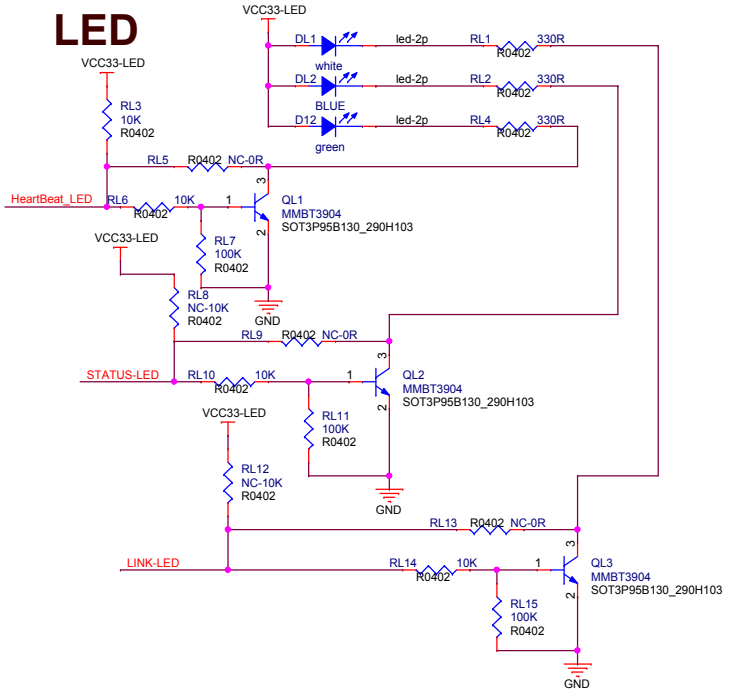
6,8,16 AP-RESET

8,16 PWRON

KEY



LED



PINE64	Desing name: **Pine H64**	
Size: A3	Page name: **KEY-LED-ETH-DEBUG**	Rev: 1.1
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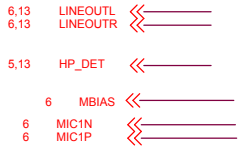
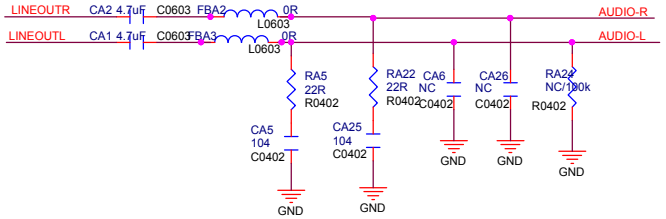
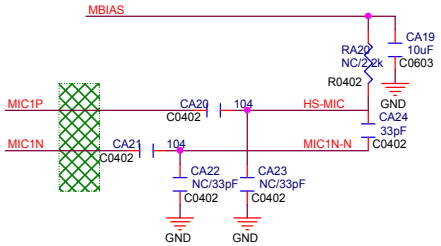
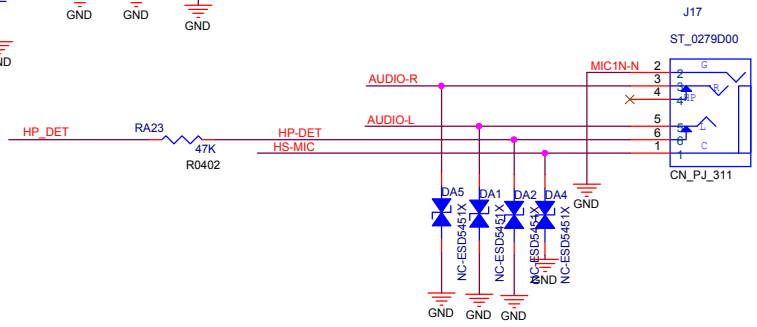
Audio

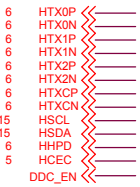


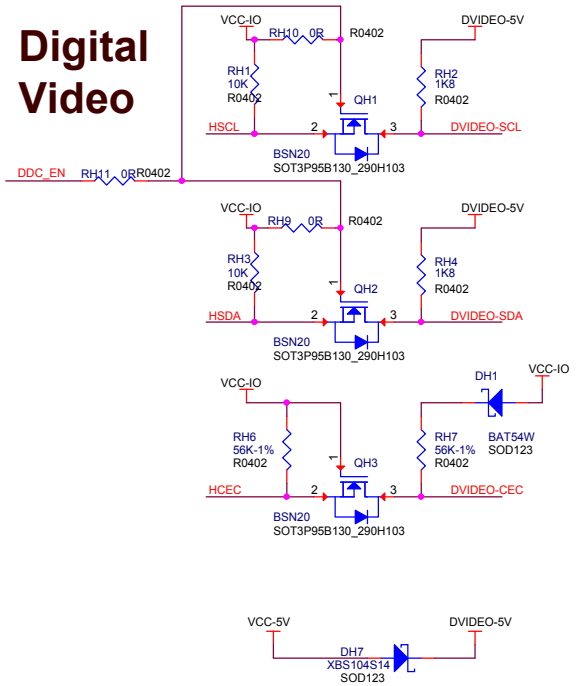


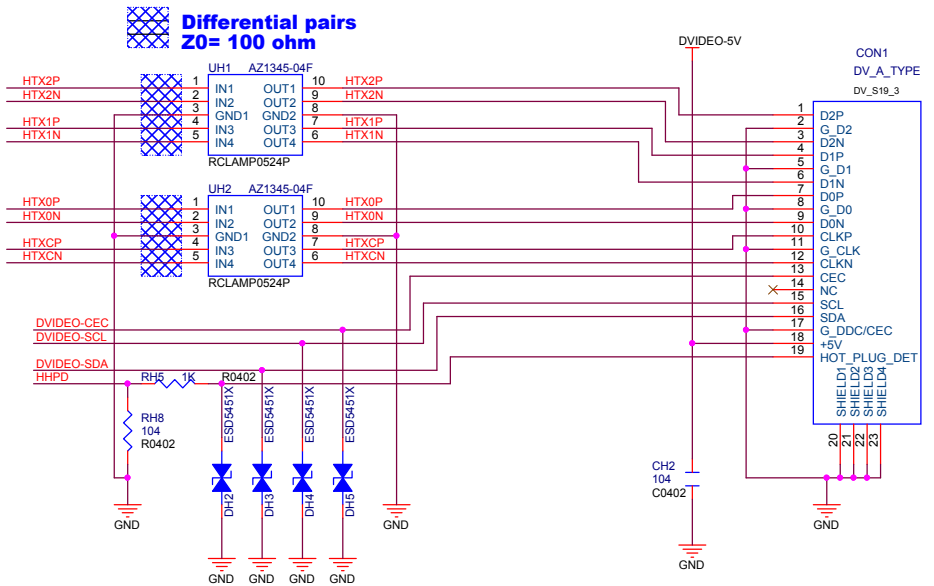




Digital Video







PINE64	Desing name	Pine H64	
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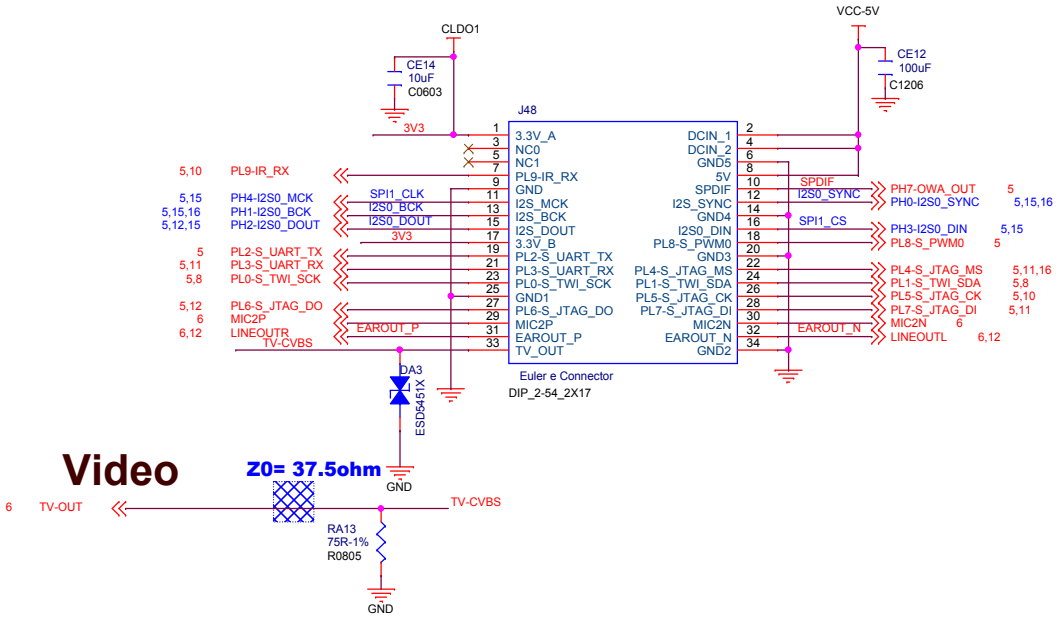
Euler e Connector



Video

Z0= 37.5ohm

6 TV-OUT

TV-CVBS

RA13
75R-1%
R0805

GND

PINE64	Desing name: Pine H64	
	Size: A3 — Page name: Euler“e”Connector	Rev: 1.1
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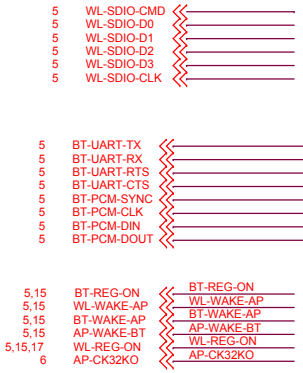
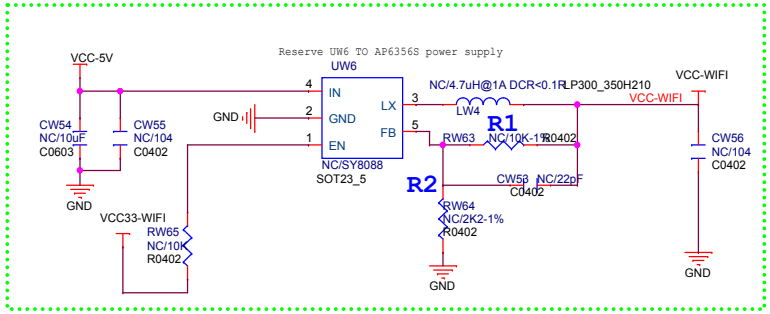
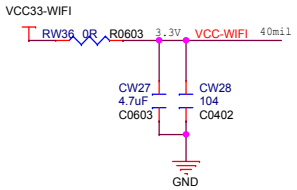
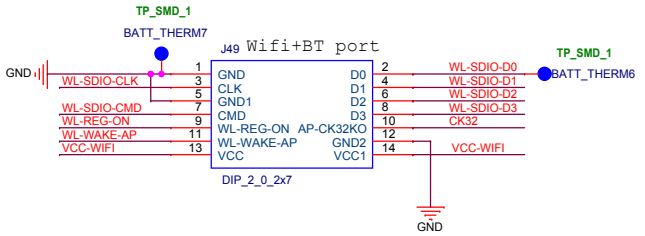
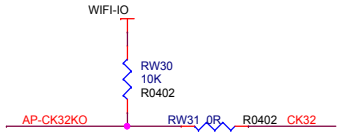
WIFI Connector

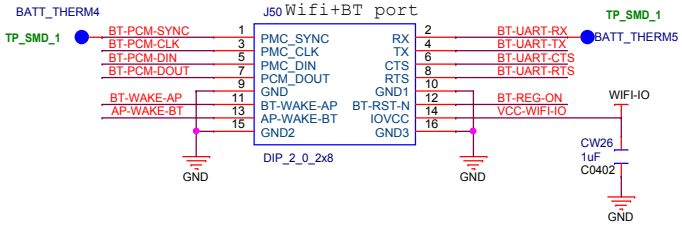












PINE64	Desing name	Pine H64	
	Size A3	Page name WIFI Connector	Rev 1.1
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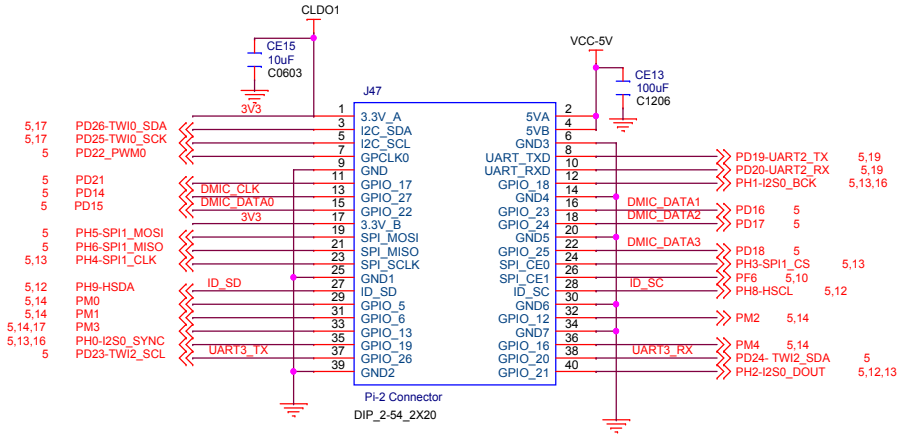
Pi-2 Connector



PINE64	Desing name	Pine H64	
	Size A3	Page name Pi-2 Connector	Rev 1.1
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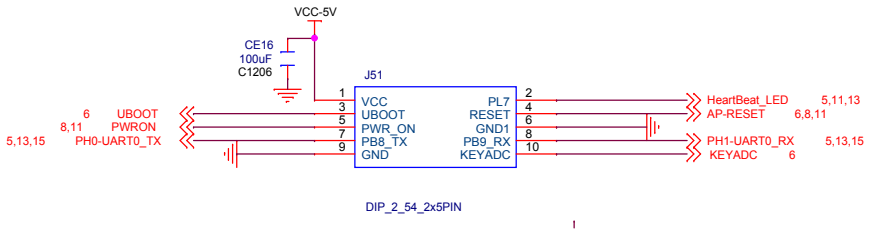
EXT+ Connector



Desing name	Pine H64	
Size A3	Page name EXT+ Connector	Rev 1.1
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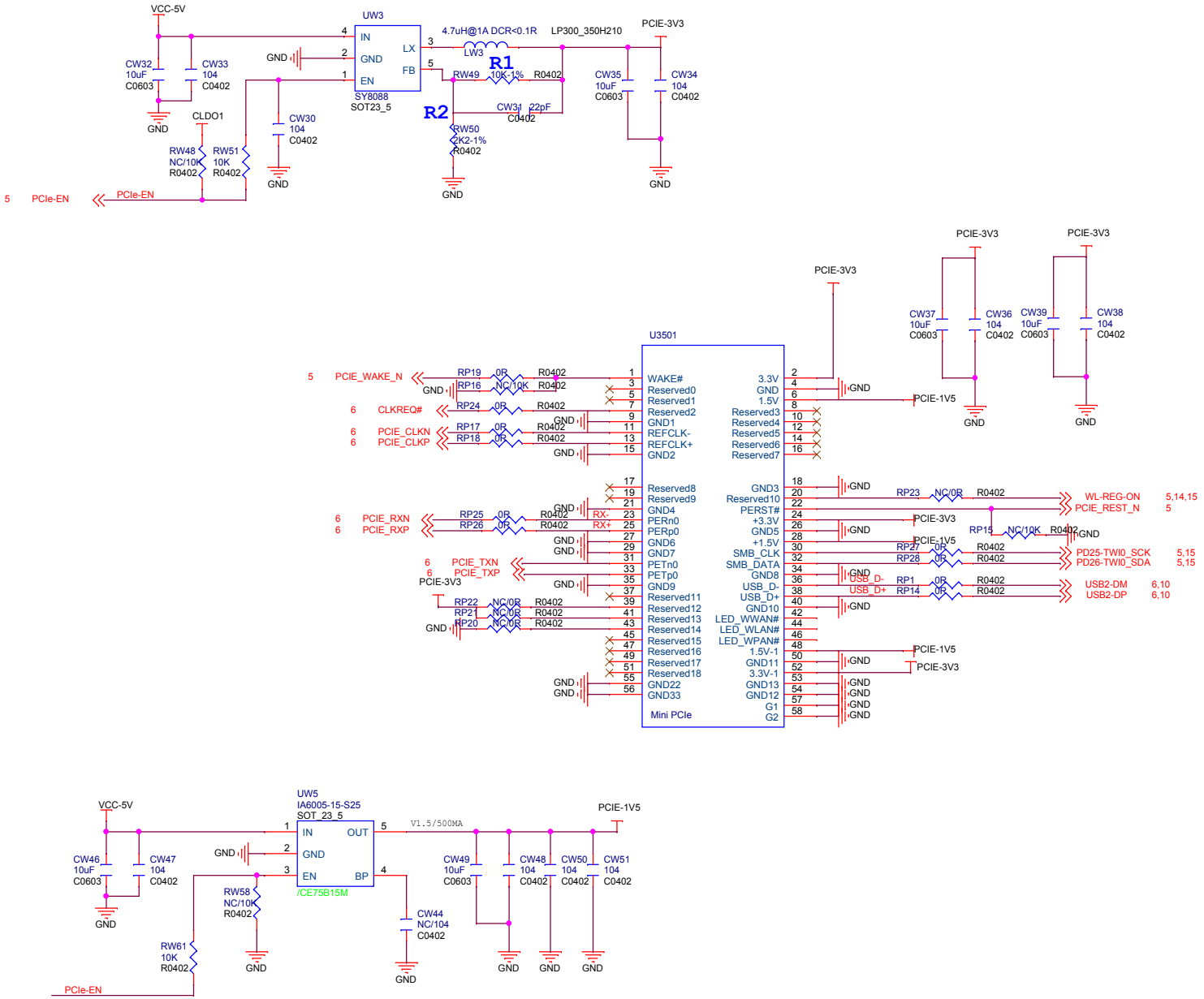
Mini PCIe



Desing name	Pine H64		
Size A3	Page name Mini PCIe		Rev 1.1
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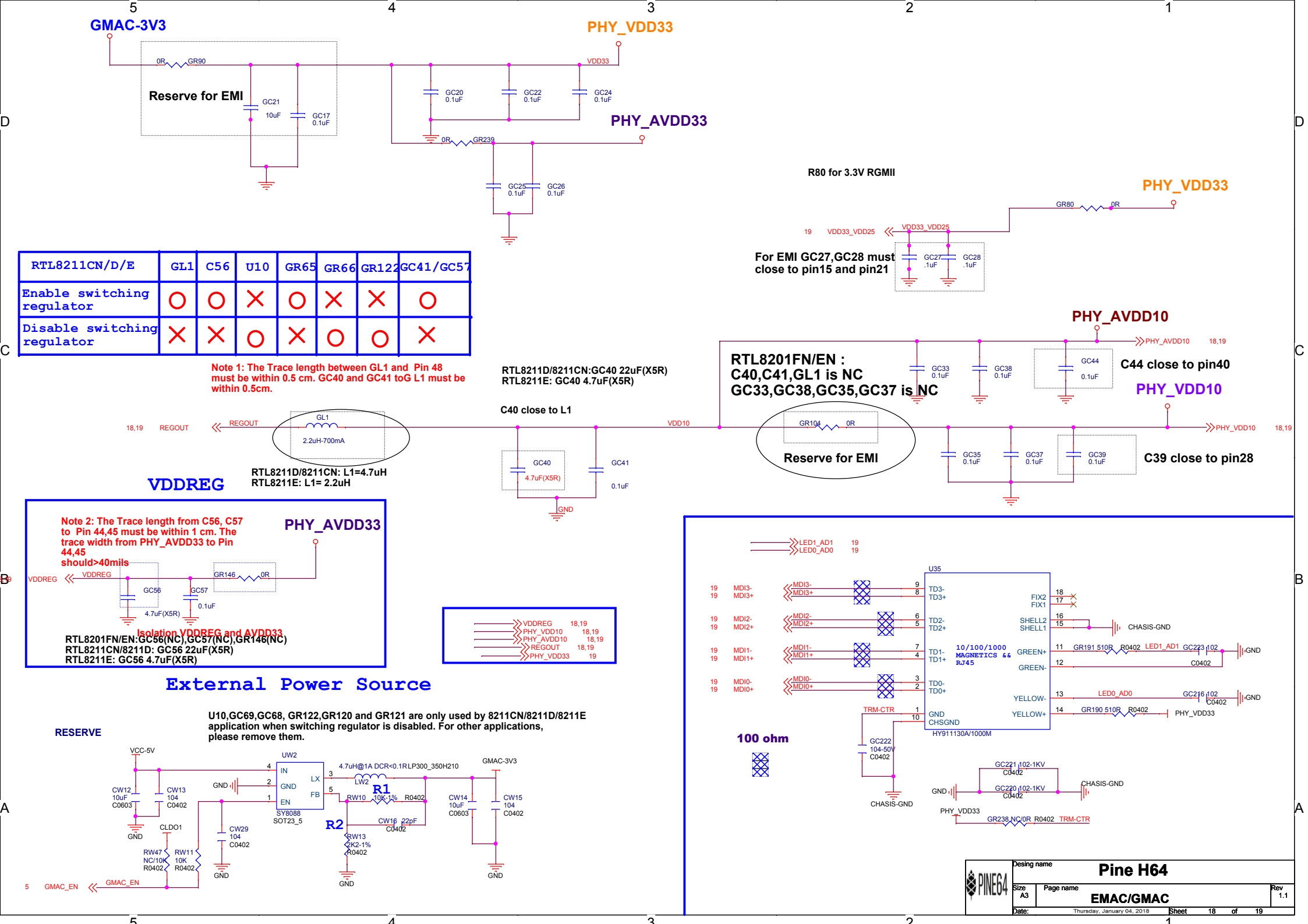

RTL8211CN/D/E	GL1	C56	U10	GR65	GR66	GR122	GC41/GC57
Enable switching regulator	O	O	X	O	X	X	O
Disable switching regulator	X	X	O	X	O	O	X

RTL8211CN/8211D/8211E/8201FN/8201EN

PME

PHY_VDD33

Note: PME Function
RTL8211D/8211E/ 8201FN only
RTL8201EN/8211CN Pin33 is NC

GR109 4.7K

PME >> PME

Interrupt

PHY_VDD33

GR127 for RTL8201EN INT function

CLK125/LED2_RXDLY — GR127 NC/0R — INT

GR106 4.7K

INT >> INT

External clock and Crystal

External clock source from OSC or Chipset.

XTAL1 — X5 (GND XIN / XOUT GND) — XTAL2

GC1 27pF — 25M-10PPM CRY-TSX3225 — GC2 27pF

Use external clock:
RTL8201FN/RTL8201EN/8211CN/8211D/8211E: GR105(0 ohm)

Enable/Disable SWREG

PHY_AVDD33

ENSWREG — GR65 0R — GR66 NC/0R

Connect ENSWREG to PHY_AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.

RTL8201FN /EN:
GR65 is Fiber Mode
GR66 is UTP Mode(default)

PHY Reset

GR57 NC0R/DD33_VDD25 >> VDD33_VDD25 18,19

GR58 0R PHY_VDD33 >> PHY_VDD33 18,19

GR55 4.7K

PHYRSTB — GR56 NC/0R PCIRST >> MAC-RST

GC54 0.01uF

RTL8211CN: GR58 (NC)
RTL8211D/8211E: GR57 (NC)
RTL8201FN /EN: GR58(NC)

For wake on LAN function, please mount GR55 GC54 and remove GR56

PHY_VDD33

MDC/MDIO

VDD33_VDD25 — GR125 NC/0 — GR128 0

MDIO — GR38 1.5K

MDIO >> MDIO
MDC >> MDC

RTL8201FN/EN/8211CN/8211D: GR128(NC)
RTL8211E:GR125(NC)

Configuration Setting

MII/RMII Setting only for RTL8201FN & RTL8201EN PHYAD2
Setting only for RTL8211E

PHY_VDD33

RTL8201FN USE RMII mode

GR46 4.7K — RX_CTL_PHYAD2 — GR47 NC/4.7K

RTL8201FN/RTL8201EN: RMII Signals:
Pull High for RMII mode — REF_CLK - Pin 22
Pull Low for MII mode — CRS_DV - Pin 36
RXD[1:0] - Pin 16, 14
TX_EN - Pin 27
TXD[1:0] - Pin 24, 23
RX_ER - Pin 39

PHY_VDD33

GR54 NC/4.7K — MDI3- — GR59 NC/4.7K

RTL8201FN: Pull High for LDO Enable
Pull Low for LDO disable

PHY_VDD33

LED1_AD1 18
LED0_AD0 18

GR88 NC/4.7K LED2_RXDLY_ENREG — GR87 NC/4.7K
GR69 NC/4.7K LED2_RXDLY — GR70 4.7K
GR71 4.7K LED1_AD1 — GR72 NC/4.7K
GR73 NC/4.7K LED0_AD0 — GR74 4.7K

RTL8211D/E: If use 2.5V RGMII please pull down (GR123)RXD0/SELRGV
RTL8211CN/8201EN:GR123,GR124 NC

GR123 NC/4.7K RXD0/SELRGV — GR124 4.7K
GR75 NC/4.7K RXD2/AN0 — GR76 4.7K
GR77 NC/4.7K RXD3/AN1 — GR78 4.7K — VDD33_VDD25 >> VDD33_VDD25 18,19
GR85 NC/4.7K RXD1/TXDLY — GR86 4.7K

GND

RTL8211CN/8211D/8211E:
GR76,GR78: Config for all capability
GR71,GR74: PHY Address=01 (8211D/8211CN)
GR46,GR71,R74: PHY Address=001 (8211E)
GR69,GR85: Without TX/RX Delay

RTL8201EN:
GR88:MII Interface
GR87:SNI Interface
GR71,GR74: PHY Address=01
Other resistors are NC

RTL8201FN:
R78 : REF_CLK Input
R77: REF_CLK Output
R69,R71,R74: PHY Address=001
Other resistors are NC

PHY_VDD33

VDD33

RSET/ENSWREG/CLK125 Co-layout

ENREG/RSET — GR112 NC/0R — ENSWREG

GR113 0R RSET

GR126 NC/4.7K

RTL8211D/E Pin39 is RSET (GR112,GR126 NC)
RTL8211CN Pin39 is ENSWREG (GR113,GR126 NC)
RTL8201FN/EN Pin39 is RXER (GR113 NC)

CLK125/LED2_RXDLY — GR114 NC/0R CLK125 >> CLK125 5,19

GC74 22pF

GR115 0R LED2_RXDLY

RTL8211D/E / RTL8201FN Pin32 is LED2_RXDLY (GR114 NC)
RTL8211CN Pin32 is CLK125 (GR115 NC)
RTL8201EN Pin32 is interrupt(GR114,GR115 NC)

Reserve for EMI.

LED2_RXDLY_ENREG — GR118 0R ENSWREG

GR119 NC/0R LED2_RXDLY

RTL8211CN Pin38 is LED2_RXDLY (GR118 NC)
RTL8211D/E Pin38 is ENSWREG (GR119 NC)
RTL8201FN/EN Pin 38 is Collision Pin(GR118 & GR119 NC)

RSET/CLK125 — GR116 0R CLK125 >> CLK125 5,19

GC73 22pF

GR117 NC/0R RSET

RTL8211D/E Pin46 is CLK125 (GR117 NC)
RTL8211CN Pin46 is RSET (GR116 NC)
RTL8201FN/EN Pin46 is RSET(GR116 NC)

Reserve for EMI.

PHY_AVDD33

PHY_VDD33

RTL8211D/E:GC45(NC)
RTL8211CN:GC45(NC)

GC45 NC/0.1uF

REGOUT — RSET/CLK125 — VDDREG — XTAL2 — XTAL1 — AVDD33_CEN — PHY_AVDD10 — ENREG/RSET — LED2_RXDLY_ENREG

U17

PGND REGOUT GND RSET/CLK125 VDDREG VDDREG CKXTAL2 CKXTAL1 AVDD33-1 AVDD10-1 ENREG/RSET DVDD33-1

MDI0+ 1 — MDI0- 2 — PHY_AVDD10 3 — MDI1+ 4 — MDI1- 5 — PHY_AVDD33 6 — MDI2+ 7 — MDI2- 8 — PHY_AVDD10 9 — MDI3+ 10 — MDI3- 11 — TXER 12

MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- AVDD33 MDI[2]+ MDI[2]- AVDD10-0 MDI[3]+ MDI[3]- NC

DVDD10-0 LED1/PHYAD1 LED0/PHYAD0 PME CLK125/LED2_RXDLY MDIO MDC PHYRSTB DVDD10 TXCTL TXD3 TXD2

RTL8211CN
RTL8211D/E
RTL8201EN/FN

RXCTL/PHYAD2 RXD0/SELRGV DVDD33 RXD1/TXDLY RXD2/AN0 RXD3/AN1 RXC INT DVDD33-0 TXC TXD0 TXD1

RX_CTL_PHYAD2 13 — RXD0/SELRGV 14 — VDD33 VDD25 15 — RXD1/TXDLY 16 — RXD2/AN0 17 — RXD3/AN1 18 — RX_CLK 19 — INT 20 — VDD33_VDD25 21 — TX_CLK 22 — TXD0 23 — TXD1 24

PHY_VDD10

RTL8201EN:GR79(NC)
RTL8201FN: GR79,GR84(NC)
RTL8211CN/8211D/8211E:GR84(NC)

GR79 0R

GR84 NC/4.7K

36 PHY_VDD10_CRS — 35 LED1_AD1 — 34 LED0_AD0 — 33 PME — 32 CLK125/LED2_RXDLY — 31 MDIO — 30 MDC — 29 PHYRSTB — 28 PHY_VDD10 — 27 TX_CTL — 26 TXD3 — 25 TXD2

PHY_AVDD33

AVDD33_CEN — GR83 0

GC47 1uF

GR83 Close to Pin41

RGMII/RMII

18 MDI3- >> MDI3+ 18
18 MDI2- >> MDI2+ 18
18 MDI1- >> MDI1+ 18
18 MDI0- >> MDI0+ 18

R35,36,37 Only for RTL8201FN/EN

PHY_VDD10_CRS — GR35 NC/0R — CRS_N >> CRS_N 5

LED2_RXDLY_ENREG

ENSWREG — GR37 0R — RXER_N >> RXER_N 5

Place filter network close to RX_CLK.
Reserved for EMI

RX_CLK — GR49 22R — RX_CLK_N

GC46 NC

RX_CTL_N 5
RX_CLK_N 5
RXD0_N 5
RXD1_N 5
RXD2_N 5
RXD3_N 5

RX_CTL_PHYAD2 — GR48 22R — RX_CTL_N
RXD0/SELRGV — GR50 22R — RXD0_N
RXD1/TXDLY — GR51 22R — RXD1_N
RXD2/AN0 — GR52 22R — RXD2_N
RXD3/AN1 — GR53 22R — RXD3_N

TX_CLK 5
TX_CTL 5
TXER 5
TXD0 5
TXD1 5
TXD2 5
TXD3 5

Close to PHY
Reserve for EMI

RSET

RSET — GR6 2.49K(1%)

Others

VDDREG 18
PHY_VDD10 18
PHY_AVDD10 18
REGOUT 18
PHY_VDD33 18,19

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	Size A3 / Page name	EMAC/GMAC — Rev 1.1
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