LABORATORY #3

THE UNIVERSAL LOGIC GATE

OBJECTIVE:

The objective of this experiment is to become familiar with the logic gates which are available to the digital designer. Performing this laboratory exercise will help the student become aware of the multiple uses of the NAND gate, acquaint the student with a method of implementing the six basic logic functions out of this universal gate, and provide the student an opportunity to write another clear and concise report.

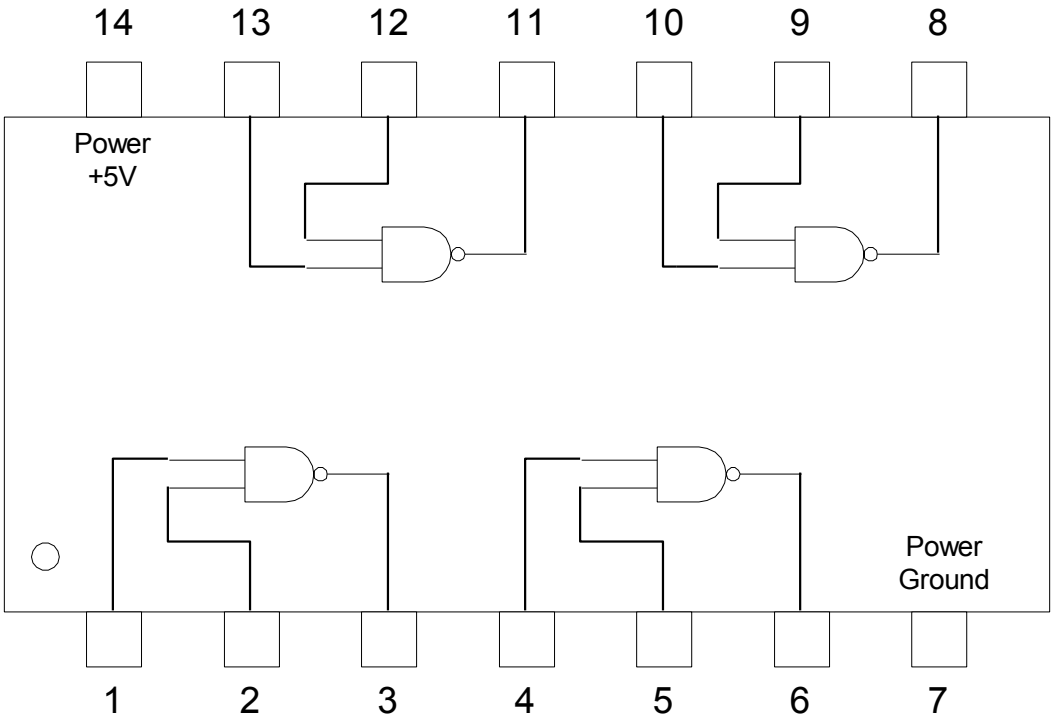
EQUIPMENT REQUIRED:

Global Specialties Design and Prototyping PB-505
Wire Leads
1 7400 TTL Integrated Circuit

PROCEDURE:

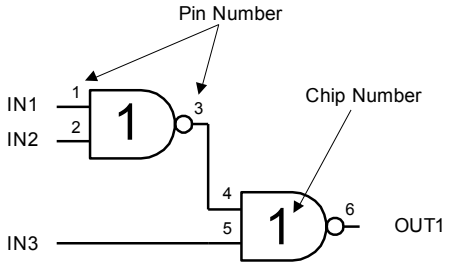
A. Pin Assignment for the 7400 TTL integrated circuit (IC)

Use the 7400 IC pin assignment diagram below and develop circuit *and* wiring diagrams which will implement the following logic circuits outlined in section B. This **MUST** be completed for pre-lab. Both sets of diagrams should be labeled with the actual connections that will be used, ie. S1, S0, Logic Monitor 0. The 7400 IC pin connections are outlined below.



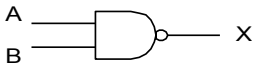
NOTE: It is **important** to have an accurate "wiring diagram" for all circuits implemented in this laboratory. Standard procedure is to number the "chips" (i.e., ICs) in an orderly fashion and to specify the pin connections on that particular chip. See the example below. It is **REQUIRED** that all lab circuits indicate the connections between all gate inputs and outputs by using numbering that corresponds to their IC pin numbers. In addition, each gate on a single IC is to possess the same number as that IC.

EXAMPLE:

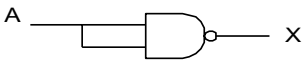


B. Logic functions based on NAND gates

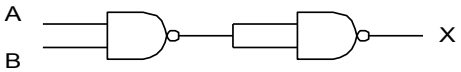
1)



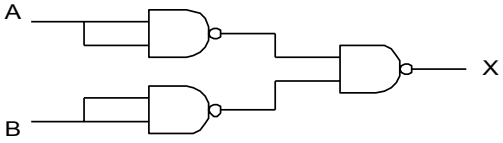
2)



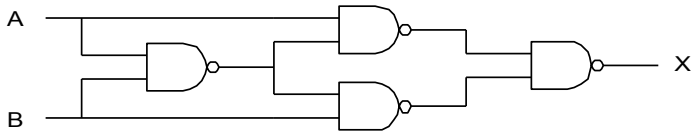
3)



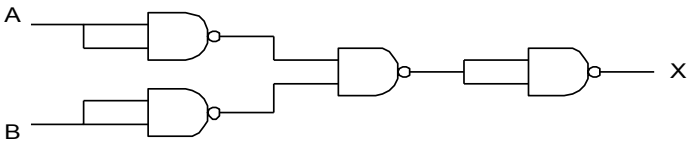
4)



5)



6)



C. Truth Tables

For prelab predict in the form of truth tables how these circuits will work. Use the same labels as those from the circuit and wiring diagrams, ie. S1, S0, Logic Monitor 0. Do not forget to include your predictions from between the gates in your truth tables. Label these with designations such as 'Chip 1, Pin 3'.

In lab, wire the circuits on the PB-505 and develop a truth table for each circuit again making sure to find the intermediate results from between the gates. *How do these compare with the ones you predicted in prelab?*

D. Using the NAND for other functions

Predict in your prelab what each circuit functions as, ie. AND, OR, NAND, NOR, EX, OR, NOT. To do this provide the truth tables for each of these logic functions in your prelab.

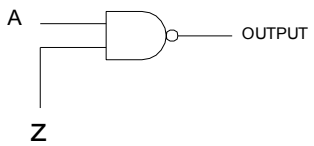
In lab, *state what each circuit is equivalent to and whether your predictions were correct.*

E. Floating inputs

Predict in your prelab (using a table formated the same as the one below) how you think the circuit below will act with the 'Z' input connected as follows:

i) Connected to +5 volts
ii) Floating (no connection at all)
iii) Connected to ground

Do not forget to label in your prelab what actual connections you plan to use. Also do not forget to label in your lab report what connections you actually used in lab. *In lab, state how the actual and predicted compared. What can be said about TTL for cases when an input is left unconnected?*



A	i	ii	iii
0			
1			