ECE 543: Introduction to Digital Systems

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Prelab #1: Introduction to the global specialties PB505

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Contents

1 Introduction

The objective of this lab is to become familiar with the lab equipment by testing the modules on the PB-505 Digital Lab. In addition, the lab will involve the construction of a circuit using the 7486 TTL IC.

2 Equipment Required

- Global Specialties Design and Prototyping PB-505
- Wire leads
- 7486 TTL Integrated Circuit(1)

3 Procedures

3.1 PB-505 Design

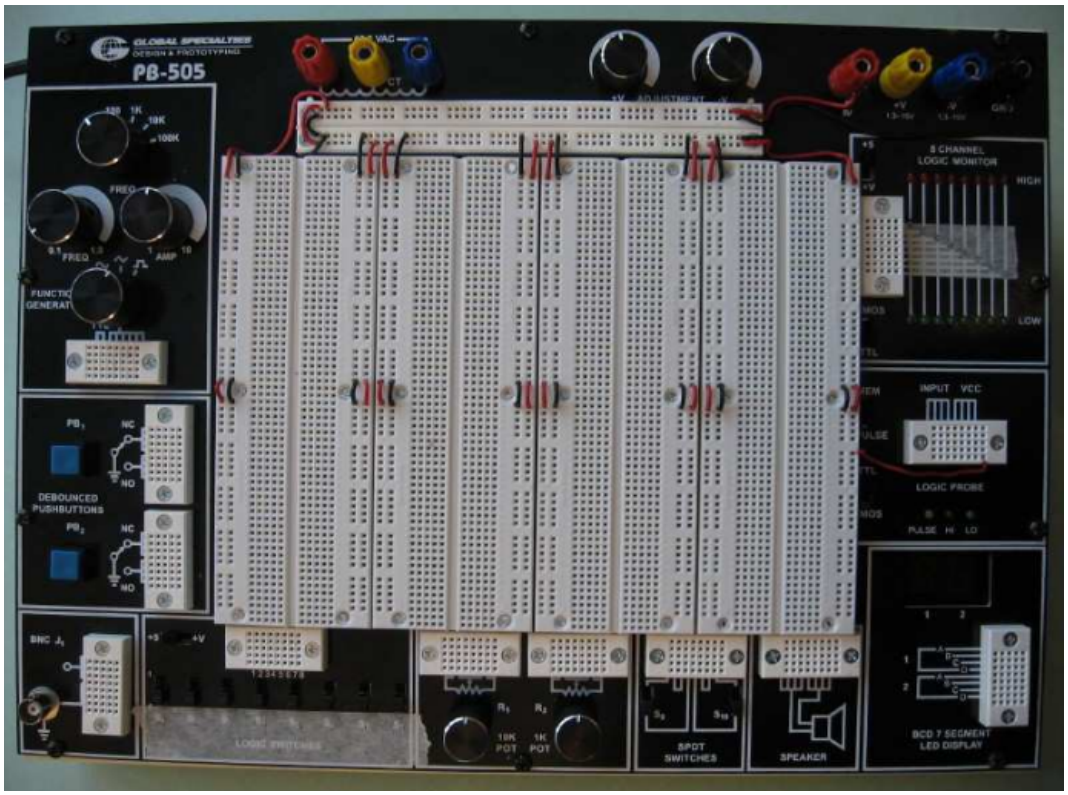
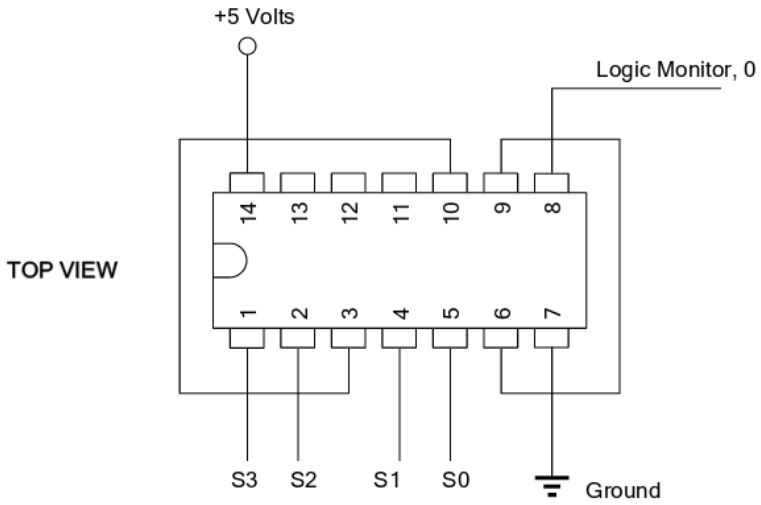


Figure 1: Global Specialties Design and Prototyping PB-505

The breadboard has internal connections. There are horizontal connections for each row of five sockets. There are vertical connections surrounding the horizontal rows. Those connected to the red wires hold VCC. Those connected to the black wires are ground. The board contains modules such as the Logic Monitor, Logic Probe, Wave Generator, Pushbuttons, Switches, and Speaker.

3.2 Circuit Diagrams

Voltage is attached to pin 14. Ground is attached to pin 7. S0 is connected to pin 5. S1 to pin 4. S2 to pin 2. S3 to pin 1. Pin 3 on the chip is connected to pin 10. Pin 6 on the chip is connected to pin 9. Pin 8 is the output.



3.3 IC Logic Diagrams

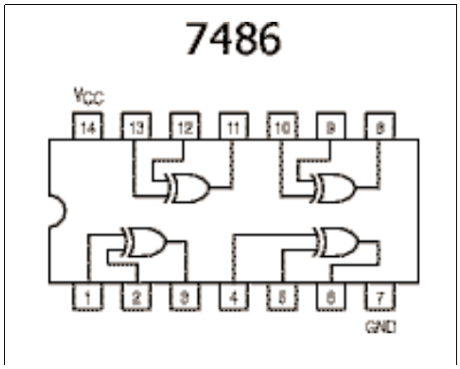


Figure 2: 7486 IC logic diagram

The IC takes pin 1 and pin 2 as inputs and outputs the XOR of the two pins to pin 3. The IC takes pin 4 and pin 5 as inputs and outputs the XOR of the two pins to pin 6. The IC takes as inputs pin 10 and pin 9 which are connected to pins 3 and 6 and outputs the XOR of the two pins to pin 8. Though our circuit does not use them the IC takes pin 12 and pin 13 as inputs and outputs the XOR of the two pins to pin 11.

3.4 IC Design

Features:

- Four 2-Input Exclusive OR Gates in a 14 Pin DIP package
- Outputs directly interface to CMOS, NMOS, and TTL
- Large operating voltage range
- wide operating conditions

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature	0 C to +70 C
Storage Temperature Range	-65 C to +150 C

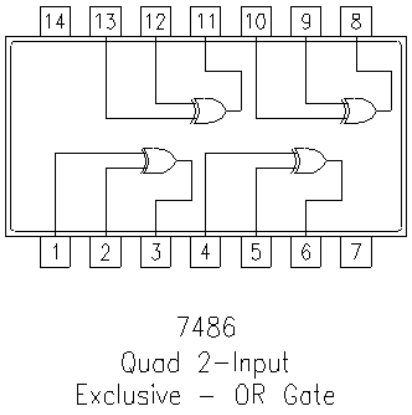


Figure 3: 7486 IC logic diagram

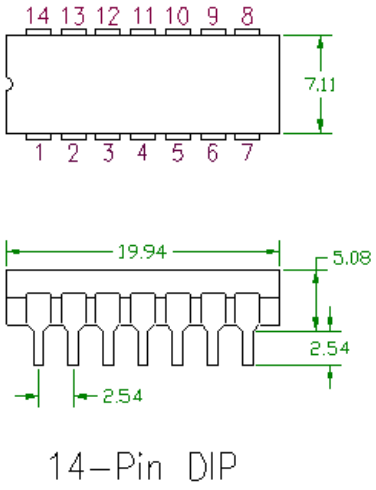


Figure 4: 7486 IC dimensions

3.5 Binary Table

Inputs				Intermediates		Output
S3	S2	S1	S0	Chip 1, Pin 3	Chip 1, Pin 6	Logic Monitor, 0
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	0	1	0	0	1	1
0	0	1	1	0	0	0
0	1	0	0	1	0	1
0	1	0	1	1	1	0
0	1	1	0	1	1	0
0	1	1	1	1	0	1
1	0	0	0	1	0	1
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	0	0

3.6 Work Done to Complete the Objective

Test the various modules on the PB-505 Digital Lab. Generate a circuit incorporating the 7486 TTL IC.

3.7 Predicted Results and Discussion

1. Logic switches should act as on and off switches for leads next to each switch.
2. Each push button should move GND from NC to NO.
3. The vertical rows meant for VCC should light the HIGH LED on the lamp monitor. The vertical rows meant for GND should light the LOW LEDs.
4. The logic probe should detect HIGH and LOW Voltages.
   (a) The probe should read LOW when connected to S7 and S7 is on. The probe should not detect any voltage when S7 is off.
   (b) The probe should read LOW when connected to NC and the push button is not pressed and not have a reading when the push button is pressed.
   (c) The PULSE light illuminates whenever voltage changes from 0 to low. When set to MEM it should remain illuminated until voltage hits 0.

4 References

Ronald J. Tocci et al. 2011. Digital Systems: Principles and Applications, 11th Ed.

"7486 - 7486 Quad EXCLUSIVE-OR Gate Datasheet". http://www.futurlec.com/74/IC7486.shtml Pearson/Prentice Hall.