CPE301 – SPRING 2019

Design Assignment 2B

Student Name: Meral Abu-Jaser

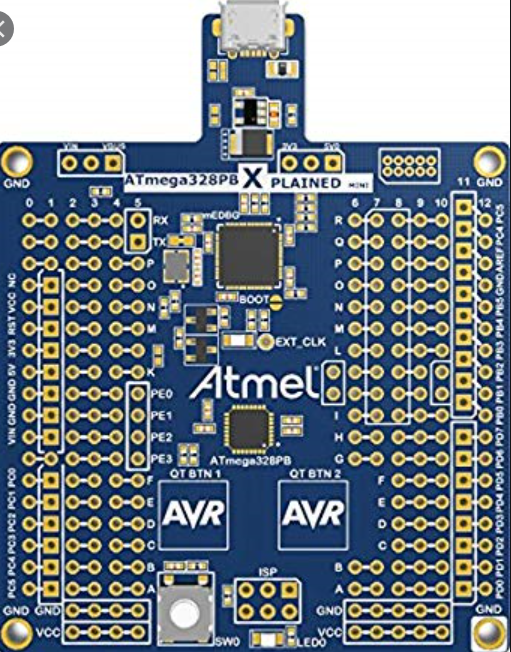
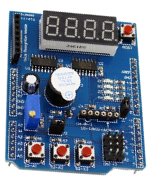
Student #: 5003137888

Student Email: abujaser@unlv.nevada.edu

Primary Github address: <https://github.com/MeralAbuJaser/Submission_da.git>

Directory: <https://github.com/MeralAbuJaser/Submission_da/tree/master/DB2B/DA2B>

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

Atmel Studio 7.0

-debugger

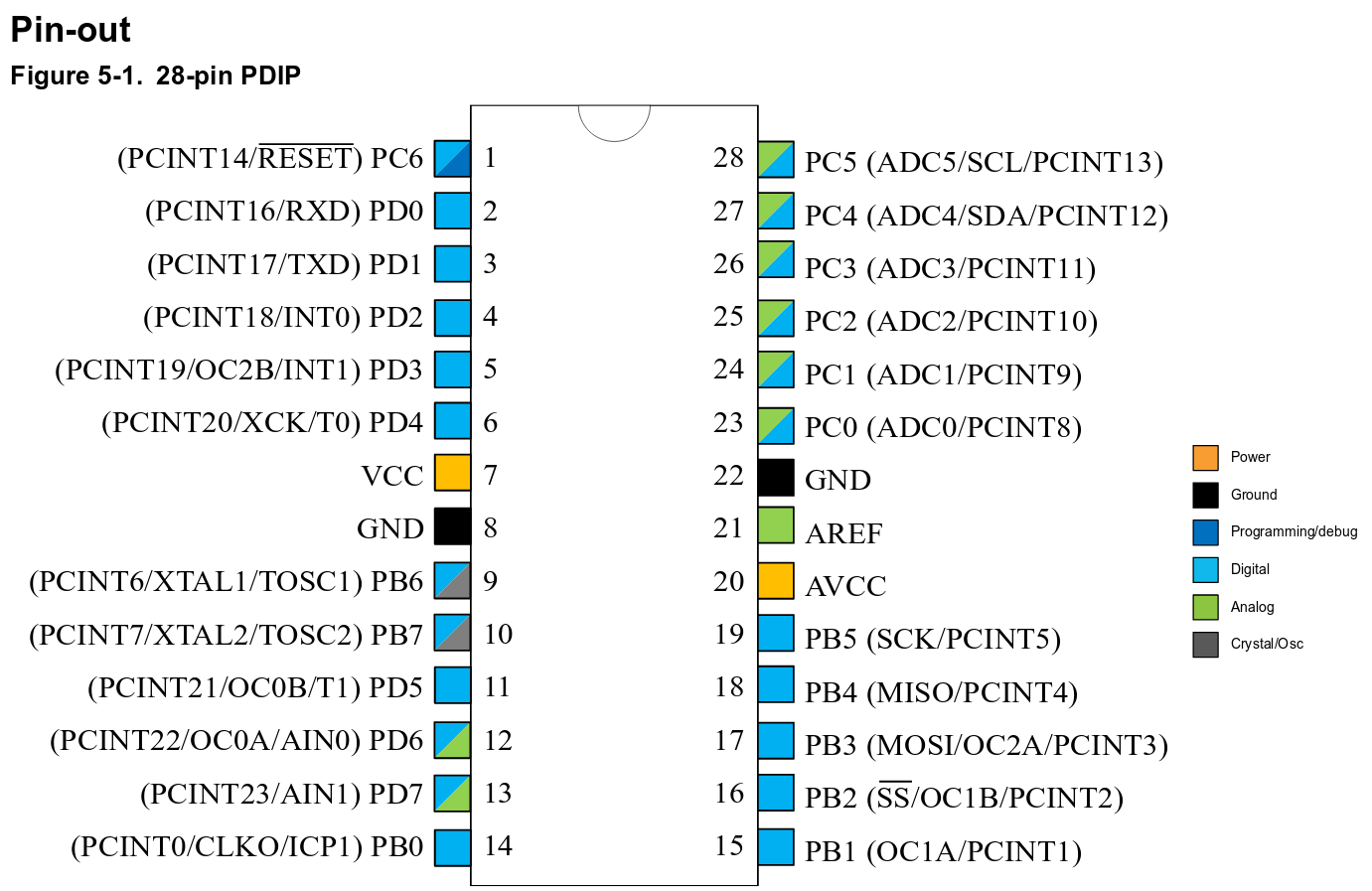
-simulator

-assembler

Atmega 328pb Sheild logic analizer

[](https://www.google.com/url?sa=i&url=https%3A%2F%2Fwww.artekit.eu%2Fproducts%2Fprototyping%2Fwires%2Fjumper-wires-male-male-flexible-pack-of-75%2F&psig=AOvVaw0O0cMWs7IBstavkEJVzMWY&ust=1584557125467000&source=images&cd=vfe&ved=0CAIQjRxqFwoTCJDZ7baVougCFQAAAAAdAAAAABAE)

male to male jumper

[](https://www.google.com/url?sa=i&url=https%3A%2F%2Ftoastedcornflakes.github.io%2Farticles%2Favr_getting_started.html&psig=AOvVaw2dpitmW3N7sA4UbkAQ2XaJ&ust=1584557063198000&source=images&cd=vfe&ved=0CAIQjRxqFwoTCPCLg5mVougCFQAAAAAdAAAAABAF)



using pins PC3, PB3, PB2

1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

C code

#define F\_CPU 16000000L

#include <avr/interrupt.h>

#include <avr/io.h>

#include <util/delay.h>

int main(void){

DDRB |= (1<<3); //DDRB.3 is output

PORTB &=~(1<<3); //PORTB.3 is output on low

EICRA = 0X02; //external interrupt on falling edge

EIMSK = (1<<INT0); //external interrupt INT0

sei ();

while(1){

PORTB |=(1<<3); //"LED ON"

\_delay\_ms(412); //delay 412ms

PORTB &=~(1<<3);//"LED OFF"

\_delay\_ms(337); //delay 337ms

}

return 1;

}

ISR (INT0\_vect){

DDRB &= ~(1<<3); //PORTB.3 output low DDRB.3

DDRB |= (1<<2); //PORT.2 output high

\_delay\_ms(2000); //delay 2s

PORTB &=~(1<<2); //PORTB.3 output High

DDRB &=~(1<<2); //PORTB.2 output LOW DDRB.2

DDRB |= (1<<3); //PORT.3 output high

}

Assembly code

.ORG 0

JMP LOOP

.ORG 0x02

JMP EX0\_ISR //initializing stack

LDI R22,HIGH(RAMEND) //

OUT SPH,R22 //

LDI R22,LOW(RAMEND) //

SBI DDRB, 2 //portb is set as output

CBI PORTB, 3 //portb.3 is set to low

LOOP:

LDI R22, 0X2 //falling edge triggered

STS EICRA, R22 //INT0 controller

SBI DDRB, 3

SBI PORTB, 3 //set to high

CALL DELAY2 //337.5ms delay

CBI PORTB, 3 //set to low

CALL DELAY1 //412.5ms delay

LDI R22, 1 << INT0 //falling edge triggered

OUT EIMSK, R22

SEI //enabling interrupts

JMP LOOP

EX0\_ISR:

CBI DDRB, 3

SBI DDRB, 2

CALL DELAY3 //delaying by 2s

CBI DDRB, 2 //outputting 0 to PB2

DELAY1://412.5ms delay loop

LDI R16, 230

LDI R17, 243

LDI R18, 32

AGAIN1:

DEC R16

BRNE AGAIN1

DEC R17

BRNE AGAIN1

DEC R18

BRNE AGAIN1

RET

DELAY2://337.5ms delay loop

LDI R16, 250

LDI R17, 237

LDI R18, 37

AGAIN2:

DEC R16

BRNE AGAIN2

DEC R17

BRNE AGAIN2

DEC R18

BRNE AGAIN2

RET

DELAY3://2 second deley loop

LDI R16, 164

LDI R17, 255

LDI R18, 255

AGAIN3:

DEC R16

BRNE AGAIN3

DEC R17

BRNE AGAIN3

DEC R18

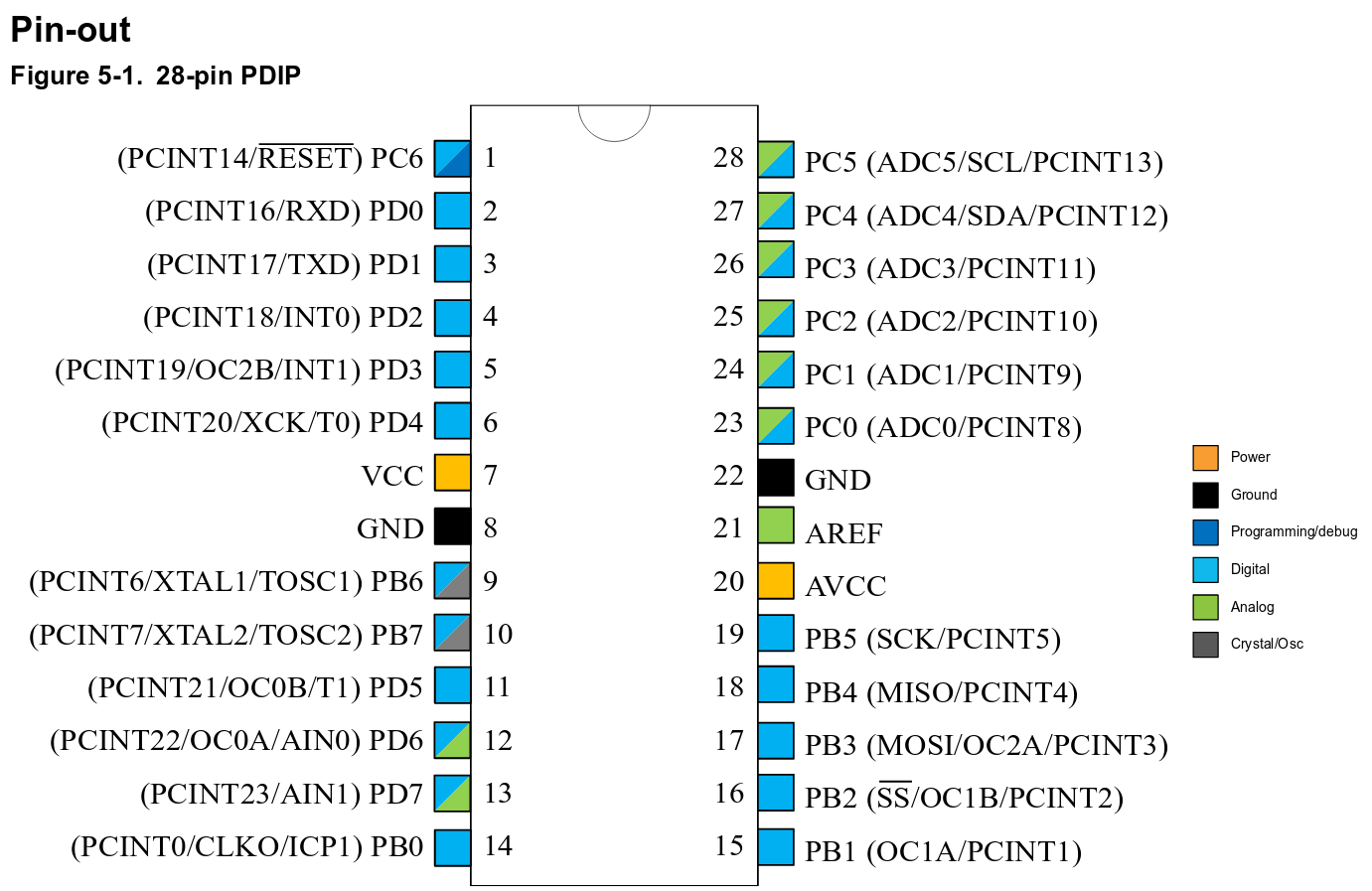
BRNE AGAIN3

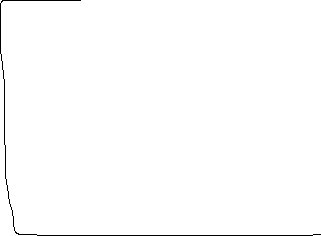
RET

1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**

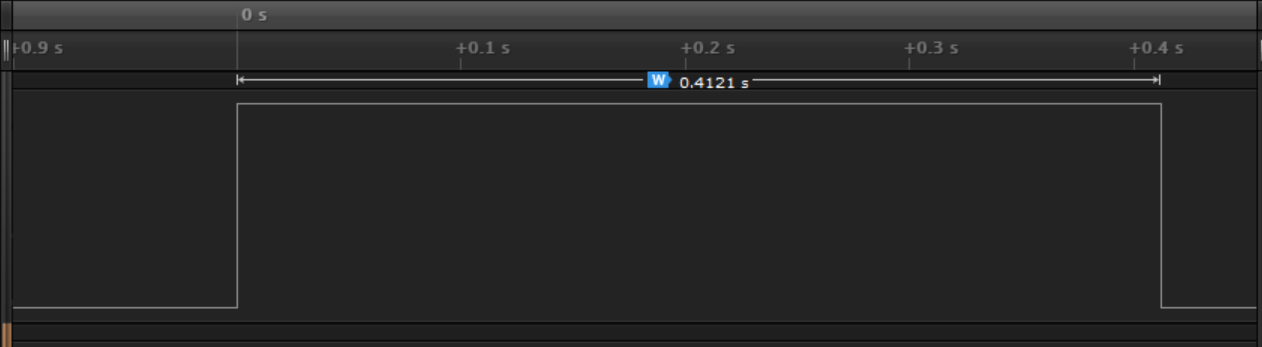
N/A

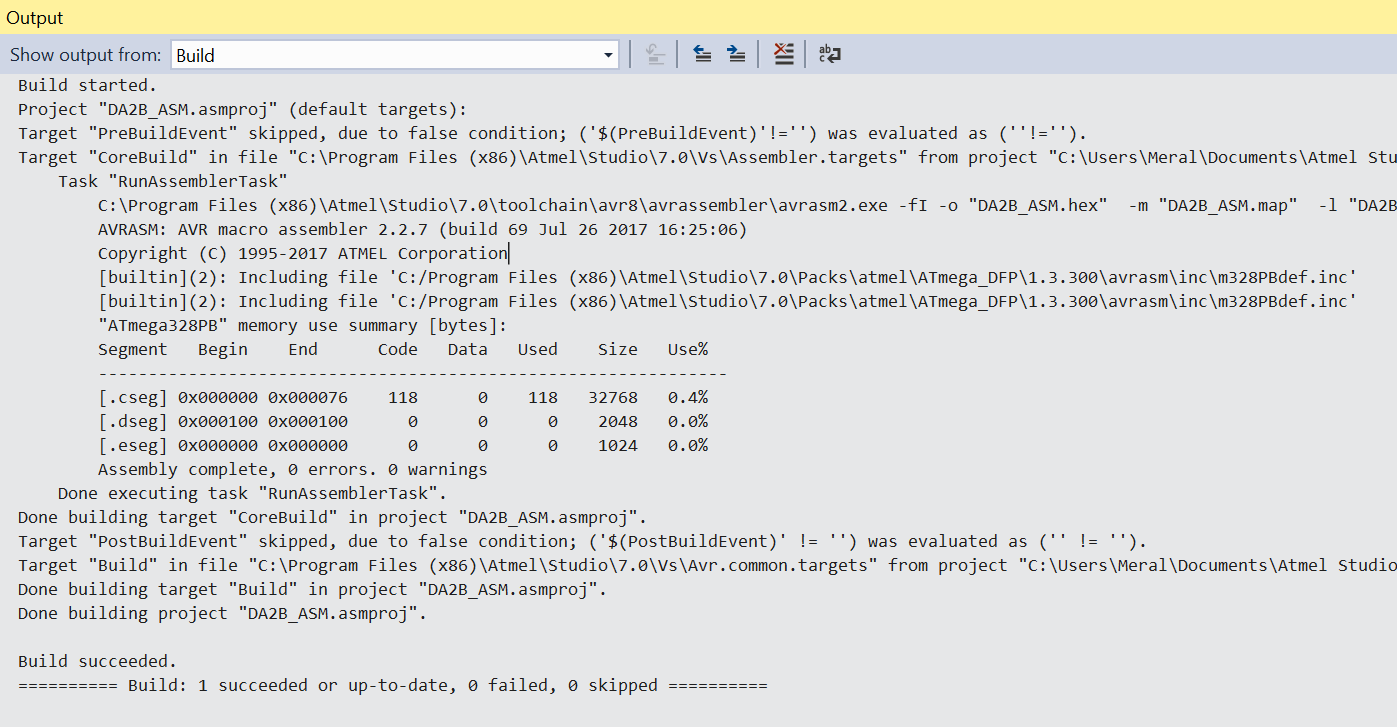
1. **SCHEMATICS**

[](https://www.google.com/url?sa=i&url=https%3A%2F%2Ftoastedcornflakes.github.io%2Farticles%2Favr_getting_started.html&psig=AOvVaw2dpitmW3N7sA4UbkAQ2XaJ&ust=1584557063198000&source=images&cd=vfe&ved=0CAIQjRxqFwoTCPCLg5mVougCFQAAAAAdAAAAABAF)



1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**





1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**

A circuit board on a table

Description automatically generatedA picture containing sitting, table, black, clock

Description automatically generatedA picture containing table, sitting

Description automatically generated

1. **VIDEO LINKS OF EACH DEMO**

<https://www.youtube.com/watch?v=phgdcTggWX8&t=0s>

1. **GITHUB LINK OF THIS DA**

<https://github.com/MeralAbuJaser/Submission_da/tree/master/DB2B/DA2B>

“This assignment submission is my own, original work”.