Computer Architecture Homework 4

Spring 2020, March

1 Boolean Algebra

Simplify the following expressions step by step (as simple as possible). Please write the answer in Sum Of Product (SOP) form.

1. $(A+B)(A+C)$

$= AA + AC + BA + BC$

$= A + AC + AB + BC$

$= A(1 + C + B) + BC$

$= A + BC$

2. $(A+\overline{B}+\overline{C})(A+\overline{B}C)$

$= A + (\overline{B}+\overline{C})\,\overline{B}C$

$= A + \overline{BC}\,\overline{B}\,C$

$= A + \overline{BC+B}\,C$

$= A + \overline{B}\,C$

3. $\overline{\overline{A+B\overline{C}} + D(\overline{E+\overline{F}})}$

$= \overline{\overline{A}\;\overline{B\overline{C}} + D\overline{E}F}$

$= \overline{\overline{A}\;\overline{B\overline{C}}}\;\overline{D\overline{E}F}$

$= (A + B\overline{C})\,(\overline{DF} + E)$

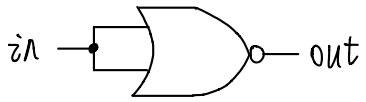
$= A\overline{DF} + AE + B\overline{C}\,\overline{DF} + B\overline{C}E$

$= A\overline{D} + AE + A\overline{F} + B\overline{C}\,\overline{D} + B\overline{C}E + B\overline{C}\,\overline{F}$

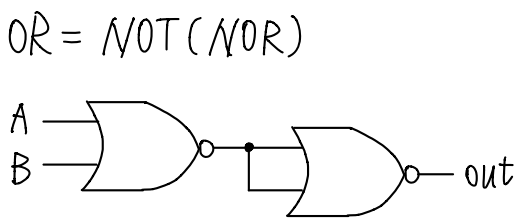
2 Logic Gates

1. Design Logic Gates

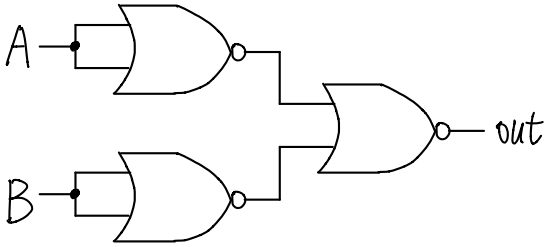
a. Create a NOT gate using only NOR gates.



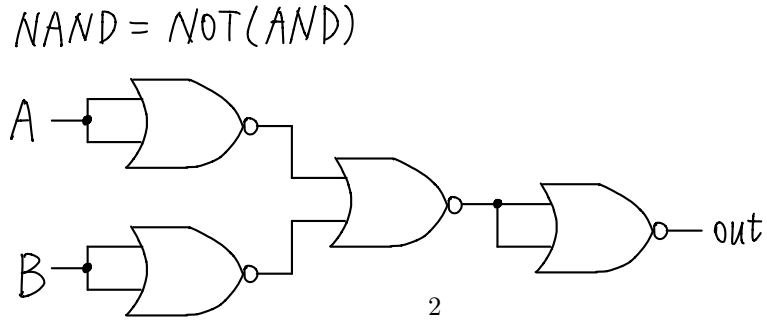
b. Create an OR gate using only NOR gates.



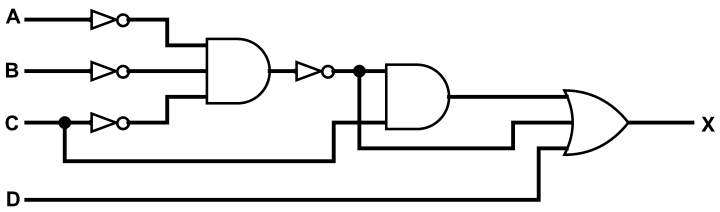
c. Create an AND gate using only NOR gates.



d. Create a NAND gate using only NOR gates.



2. The circuit shown below can be simplified. Please write the origin boolean expression of this circuit and simplify the expression step by step. Then draw the circuit according to the simplified boolean expression using the minimum number of two-input logic gates.



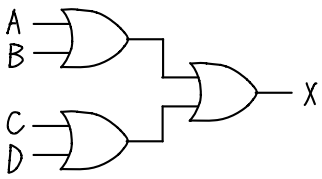
$$\overline{\overline{A}\,\overline{B}\,\overline{C}}\,C + \overline{\overline{A}\,\overline{B}\,\overline{C}} + D$$

$$= \overline{\overline{A}\,\overline{B}\,\overline{C}}\,(C+1) + D$$

$$= \overline{\overline{A}\,\overline{B}} + C + D$$

$$= A + B + C + D$$

$$= (A+B) + (C+D)$$

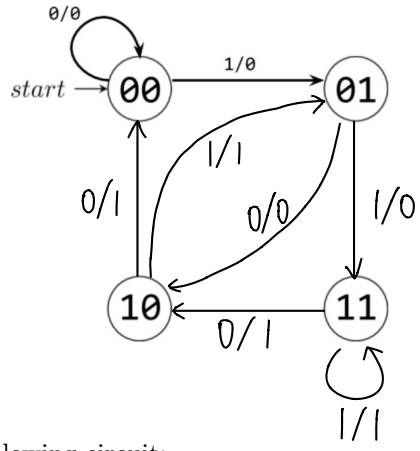


3 FSM and SDS

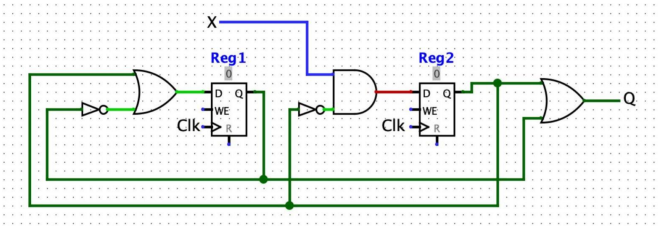
1. Write an FSM that takes in an n-bit binary number (starting with the MSB, ending with the LSB) and performs a **logical right shift by 2** on the input. For example, if our input is 0b01100, then our FSM should output 0b00011.

Input (MSB → LSB)	0	1	1	0	0
Output	0	0	0	1	1

Fill in the following FSM with the correct transitions and outputs. Format state changes as (input/output); we've done two for you. This is the **minimum** number of states; you may not add any more.



2. Consider the following circuit:



Assume the clock has a frequency of 50 MHz, all gates have a propagation delay of 6 ns, X changes 10ns after the rising edge of Clk, Reg1 and Reg2 have a CLK to Q time of 1 ns.

a. What is the **longest possible setup time** such that there are no setup time violations? Only giving a result will receive no point.

$T \geq \max(CLK \to q) + \max(CL\ Delay) + \text{Setup time}$

For reg 1: $\frac{1}{50\,MHz} \geq 6ns + 6ns + 1ns + \text{setup} \Rightarrow \text{setup time} \leq 7ns$

For reg 2: $\frac{1}{50\,MHz} \geq 6ns + 10ns + \text{setup} \Rightarrow \text{setup time} \leq 4ns$

$\Rightarrow$ So the longest setup time is 4 ns.

b. What is the **longest possible hold time** such that there are no hold time violations? Only giving a result will receive no point.

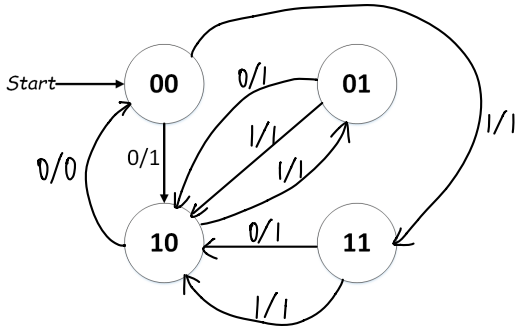
$\text{hold time} \leq \min(CLK \to q) + \min(CL\ Delay)$

For reg 1: $\text{hold time} \leq 1ns + 6ns = 7ns$

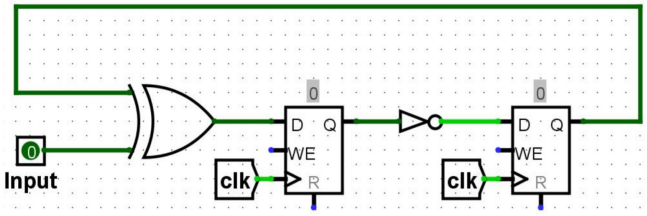
For reg 2: $\text{hold time} \leq 1ns + 6ns + 6ns = 13ns$

$\Rightarrow$ So the longest hold time is 7 ns.

c. Represent the circuit above using an equivalent FSM, where X is the input and Q is the output, with the state lables encoding Reg1Reg2 (e.g. "01" means Reg1=0 and Reg2=1). We did one transition already for you.



3. Assume **Input** comes from a register, and that there are no hold time violations. What's the fastest **frequency** you can run your clock for this circuit so that it executes correctly? Write your answer as a mathematical expression (you can also use $min()$, $max()$, $abs()$, and other simple operations if needed) using these variables: **X**=XOR delay, **N**=NOT delay, **C**=$\mathbf{t}_{clk-to-Q}$, **S**=$\mathbf{t}_{setup}$, **H**=$\mathbf{t}_{hold}$.



For the leftwise register,

$$T \geq C + X + S$$

For the rightwise register,

$$T \geq C + N + S$$

$$f_{max} = \frac{1}{\max(C+X+S,\ C+N+S)}$$

$$= \frac{1}{C + \max(X+N) + S}$$