Computer Architecture

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Exercise Sheet 1

Exercise sheet 1 – Computer History and Arithmetic

1. A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	41000	1
Data transfer	28000	2
Floating point	25000	2
Control transfer	6000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

2. Represent the following decimal numbers in both binary sign/magnitude and twos complement using 8 bits: +64; -28.

3. Represent the following twos complement values in decimal: 1100110; 1011101.

4. Consider the following operation on a binary word: Start with the least significant bit. Copy all bits that are 0 until the first bit is reached and copy that bit, too. Then take the complement of each bit thereafter. What is the result?

5. Consider the twos complement addition of two n-bit numbers:

$$z_{n-1}z_{n-2} \dots z_0 = x_{n-1}x_{n-2} \dots x_0 + y_{n-1}y_{n-2} \dots y_0$$

Assume that bitwise addition is performed with a carry bit c_i generated by the addition of x_i, y_i and c_{i-1}. Let v be a binary variable indicating overflow when $v = 1$.

The table below lists all possible combinations of the most significant bits (of *x* and *y*) and the carry bit resulting from addition of the second most significant bits.

Fill in the values in the table.

Input	x_{n-1}	0	0	0	0	1	1	1	1
	y_{n-1}	0	0	1	1	0	0	1	1
	c_{n-2}	0	1	0	1	0	1	0	1
Output	z_{n-1}								
	v								

6. Assume numbers are represented in 8-bit twos complement representation. Show the calculation of the following:

a) 6 + 12

b) -6 + 12

c) 6 - 12

d) -6 - 12

7. Is the following a valid alternative definition of overflow in twos complement arithmetic?

If the exclusive-OR of the carry bits into and out of the leftmost column is 1, then there is an overflow condition. Otherwise, there is not.