Computer Architecture

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Exercise Sheet 3

Exercise sheet 3 – Bus, Cache & Memory

1) Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.
   a) What is the maximum directly addressable memory capacity (in bytes)?
   b) Discuss the impact on the system speed if the microprocessor bus has
      i) a 32-bit local address bus and a 16-bit local data bus, or
      ii) a 16-bit local address bus and a 16-bit local data bus.
   c) How many bits are needed for the program counter and the instruction register?

2) Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.
   a) Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?
   b) Repeat assuming that half of the operands and instructions are one byte long.

3) The Intel 8088 microprocessor requires four processor clocks for a bus read operation. The valid data is on the bus for an amount of time that extends into the fourth processor clock cycle. Assume a processor clock rate of 4 MHz.
   a) What is the maximum data transfer rate?
   b) Repeat but assume the need to insert one wait state per byte transferred

4) A two-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.

5) A set-associative cache has a block size of four 16-bit words and a set size of 2. The cache can accommodate a total of 4096 words. The main memory size that is cacheable is 64K x 32 bits. Design the cache structure and show how the processor's addresses are interpreted.

6) Consider a memory system with the following parameters: T_c = 90 ns; $C_c = 10^{-3}$ \$/bit; T_m = 1100 ns; $C_m = 10^{-4}$ \$/bit
   a) What is the cost of 2 Mbyte of main memory?
   b) What is the cost of 2 Mbyte of main memory using cache memory technology?
   c) If the effective access time is 15% greater than the cache access time, what is the hit ratio H?

7) Consider a cache with a line size of 64 bytes. Assume that on average 30% of the lines in the cache are dirty. Each operation has on average 2 cache references, 15% of them are writes. A word consists of 8 bytes.
   a) Assume there is a 3% miss rate (0.97 hit ratio). Compute the amount of main memory traffic, in terms of bytes per instruction for both write-through and write-back policies. Memory is read into cache one line at a time. However, for write back, a single word can be written from cache to main memory.
   b) Repeat part a for a 5% rate.
   c) Repeat part a for a 7% rate.
   d) What conclusion can you draw from these results?

8) Consider a dynamic RAM that must be given a refresh cycle 32 times per ms. Each refresh operation requires 75 ns; a memory cycle requires 250 ns. What percentage of the memory's total operating time must be given to refreshes?

9) Draw a diagram to show how a memory module consisting of 256K 8-Bit words could be organized. Note that for 256K 8-bit words, an 18-Bit address is needed and is supplied to the module from some external source.

10) For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory?