

An Extensible Framework for Evaluation of Arithmetic Hardware

Zifan Wang
Supervisor: Dr. James Davis

Imperial College London

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- Started as a specialised evaluation system for high-radix online arithmetic units
 - At-speed
 - Precision Checking

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- Started as a specialised evaluation system for high-radix online arithmetic units
 - At-speed
 - Precision Checking
- Digital designers all use their own testbenches

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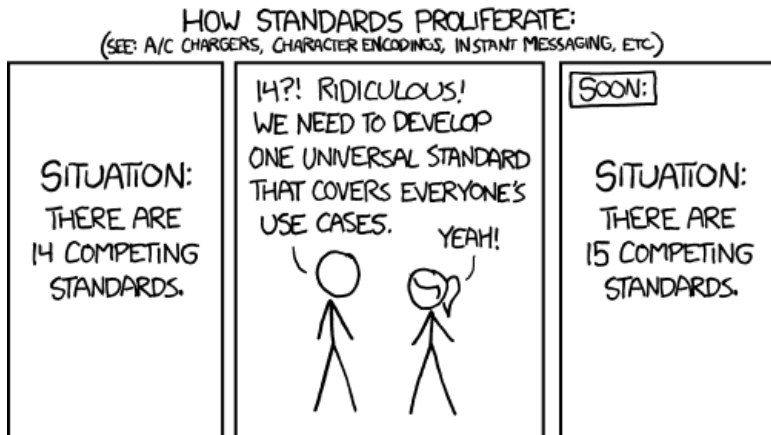
Demo

Evaluation

Evaluation

Backup Slides

- Started as a specialised evaluation system for high-radix online arithmetic units
 - At-speed
 - Precision Checking
- Digital designers all use their own testbenches
- Propose an extensible framework



Purpose

- Design and Implement an evaluation framework
 - High maximum frequency

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- Design and Implement an evaluation framework
 - High maximum frequency
 - Controllable frequency

Purpose

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- Design and Implement an evaluation framework
 - High maximum frequency
 - Controllable frequency
 - Provide information regarding precision of output

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- Design and Implement an evaluation framework
 - High maximum frequency
 - Controllable frequency
 - Provide information regarding precision of output
 - Flexible, customisable

Purpose

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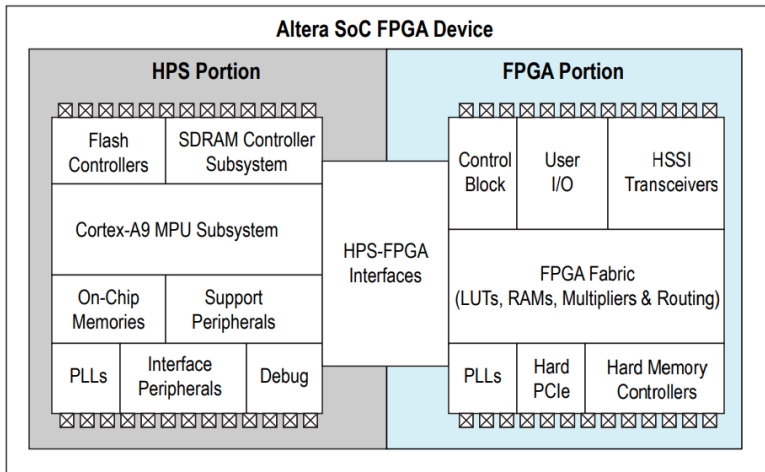
Evaluation

Backup Slides

- Design and Implement an evaluation framework
 - High maximum frequency
 - Controllable frequency
 - Provide information regarding precision of output
 - Flexible, customisable
 - User-friendly

Hardware Choice

Cyclone V SX SoC Development Board



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System Architecture

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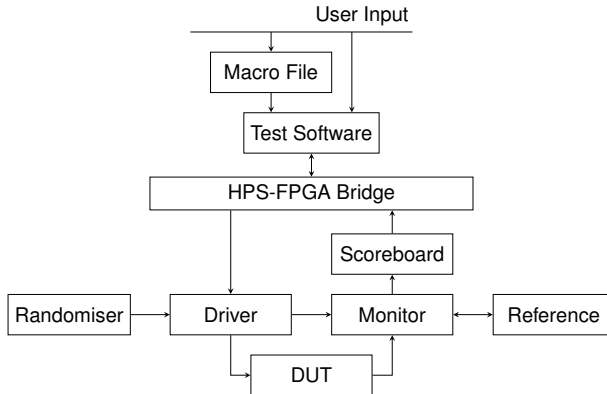
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- Inspired by UVM agent
- Modular, thus extensible



Monitor Structure

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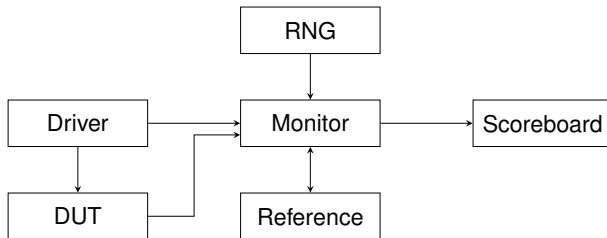
Demo

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Backup Slides

- Lazy Monitor
 - Randomly select data points to check



Monitor Structure

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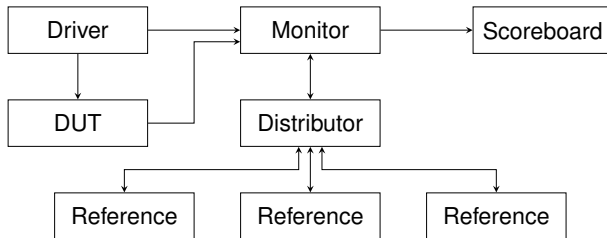
Demo

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Backup Slides

- Parallel Monitor
 - Checks all data points in parallel



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- Maximum frequency
 - TimeQuest: 394.01MHz
 - Hardware test: Stable at 400MHz; breaks at 425MHz
 - Can be pushed further, but stopped for time

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- Maximum frequency
 - TimeQuest: 394.01MHz
 - Hardware test: Stable at 400MHz; breaks at 425MHz
 - Can be pushed further, but stopped for time
- User-friendliness
 - Performed an OOTB Testing
 - No previous knowledge on Qsys or the framework
 - Obtained results in 2 hours

Results

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- Flexibility

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Item	Reconfigurability
WIDTH	≤ 32 bits
NUM_SUB_MON	≥ 2
f_{dut}	$\leq 400\text{MHz}$
DUT I/O	2 in 1 out
DUT delay	All values
bitset/bitclr	All values
manual	All values
time	All values

- Auto mode filtering limited to bit-wise manipulation
- No access to all precision data
- 32-bit limit to many things

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- Shows the configuration process
- Shows software interaction

Limitations

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- Limited customisability of current implementation
- Tedious and error-prone
- Could be overcome with 2 improvements
- Unified software system + Verilog preprocessor
- Set up a more powerful HPS-FPGA communication system
- Not limits to the extensibility of the framework

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Thank you

Questions?

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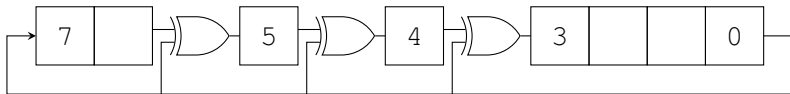
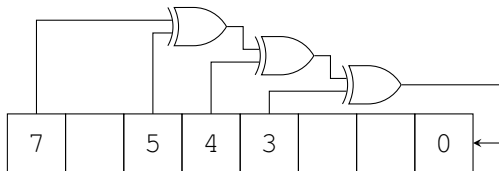
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Randomiser Structure

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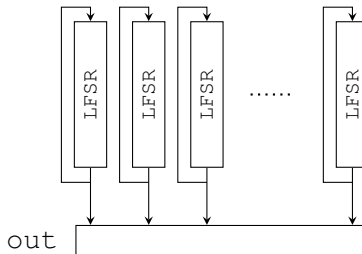
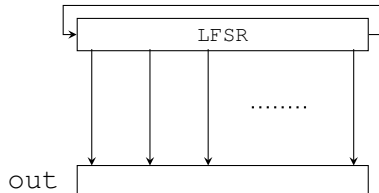
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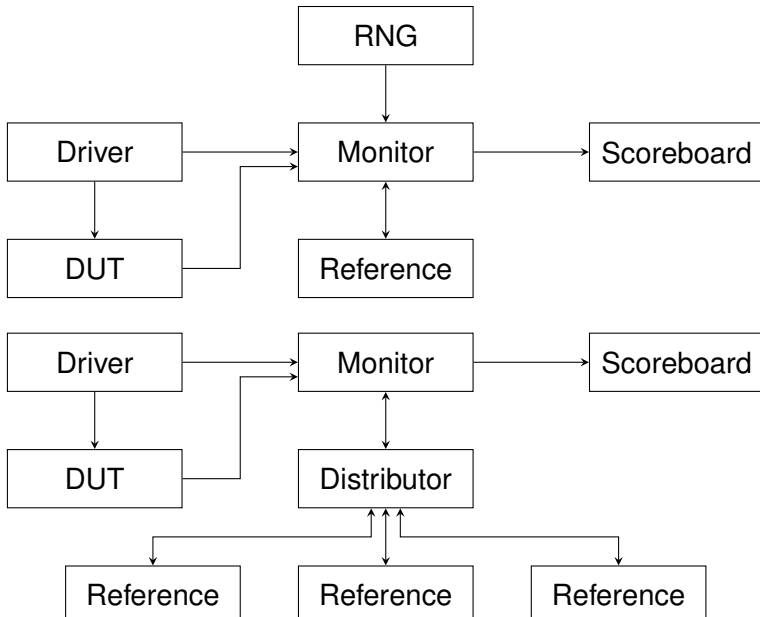
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Monitor Structure



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