High-radix On-line Arithmetic Verification System

Final Year Project 1800478: Interim Report

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I. Introduction

This project is a part of a larger project investigating the effect of using high-radix number systems with on-line arithmetic operators. The overarching aim would involve implementing such a system on FPGA and quantifying its performance improvements. This aim would be achieved through two vertically split individual projects. One would design and verify the arithmetic operator modules, while the other would design a system from the top-level to test and evaluate these operators. This project deals with the system-level issues.

II. Project Specification

At the end of the project, the system should be able to perform the following: 1.Takes in the arithmetic modules designed by the sister project as its input; 2.Generate and run tests on these modules; 3.Vary the frequency and voltage of the FPGA; 4.Evaluate its performance.

A. Project Interfacing

Numbering system I/O

B. Hardware Choice

The system itself will be built on a Cyclone V board. Its SoC has integrated an HPS (Hard processor system) and an FPGA.

C. Deliverables

The initial deliverable for the engineering side involves running a simple program on the FPGA through the HPS with the FPGA frequency being controllable. After this, the next critical step would be making sure the modules under test will be the point of failure and not the testbench. This would include some research on ways in improving the speed of feeding inputs to the arithmetic units, and checking its outputs. Once this could be confirmed, we can start adding a selection of different functionalities.

1.Running standard benchmarks; 2.Running key algorithms or their components; 3.Experiment with other power efficiency improving techniques, such as undervolting; 4.Add support for different radix arithmetic; 5.Allow graceful failures for the testbench in case of unintended behaviour for the arithmetic modules; 6.Add an interactive UI to control the voltage and frequency at run time and examine the DUT's behaviour;

Depending on the time situation, more or less items on this list may be fulfilled.

III. Background

IV. Implementation Plan

Compared to existing research, the combination of high-radix and online is relatively novel, and to optimising it on a system level for popular FPGA accelerations such as neural networks would be innovative as well. With respect to the testbench, figuring out a system to obtain the optimal point of operation of the FPGA, in terms of its voltage and frequency, would also require some advanced research.

A. Risks

A major risk of this project is related to its schedule and the existence of an initial blocking task. While most of the later sections of the project can be selectively added or removed from the scope relatively easily, the initial setup of the testbench will always remain critical to any further improvements. It is thus vital that the bare minimum system gets done early. To ensure this happens, it will be placed in the highest priority before its completion, and any blocking issue should be discussed with the supervisor if it could not be resolved after significant effort.

The other major risk has to do with the progress of the sister project. The purpose of the testbench is to verify and stress the arithmetic designs. If these designs would not be available near the end of this project, it would be difficult to empirically prove the capabilities of the testbench and its surrounding system. It is not impossible, as there are still substitutions for them. For functional purposes, standard off-the-shelf adders and multipliers could be used in lieu. For other purposes, it is possible to have a model done before the actual design starts in the paired project. While this would allow this project to progress easier, it would be extra work for the other project, which is ultimately up to the decision of the other student. In all, it would be nice to have a solid arithmetic module completely to run in this testbench, but without one, the system can still be built and completed, albeit generating less useful data towards the overall aim of the project.

V. Evaluation Plan

VI. Ethical, Legal, and Safety Plan

VII. Conclusion

APPENDIX A
FORMULAE

$$1 + 1 = 2$$

APPENDIX B
DATA

Sum	1	2	3	4
1	2	3	4	5
2	3	4	5	6

APPENDIX C
ILLUSTRATIONS

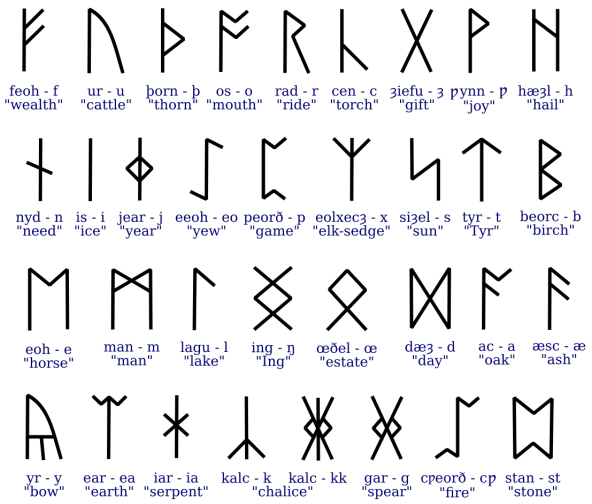

Fig. 1. Placeholder

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