

Imperial College London

Department of Electrical and Electronic Engineering

Final Year Project Report (DRAFT)



Project Title: **A High-radix Online Arithmetic Verification System**

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Course: **EEE4**

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Abstract

Nice abstract

1 Introduction

2 Background

3 Requirements Capture

4 Analysis and Design

5 Implementation

5.1 Randomiser

5.1.1 Fibonacci vs Galois

5.1.2 Vertical vs Horizontal

5.2 Driver

5.2.1 Dual Driver System

5.2.2 Delay Tester

I built a delay tester to find out the delay of the DUT. With a 3-bit counter as shown in the timing diagram, it can measure this delay for up to 8 clock cycles.

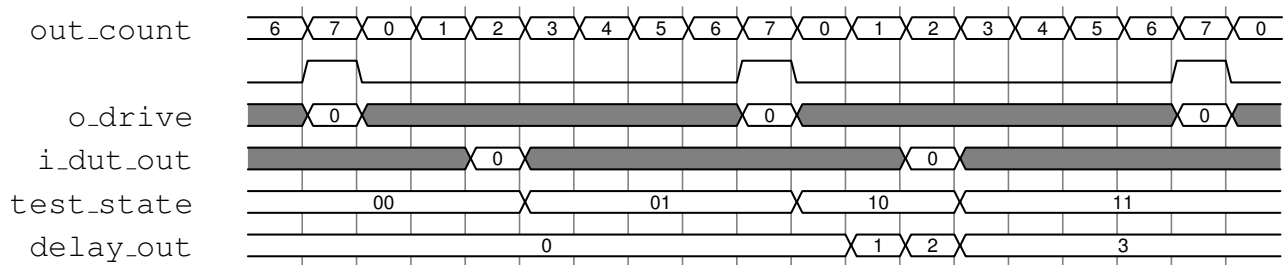


Figure 1: 3-bit Delay Tester FSM

Testing with 0 is safe since LSFR will never output 0.

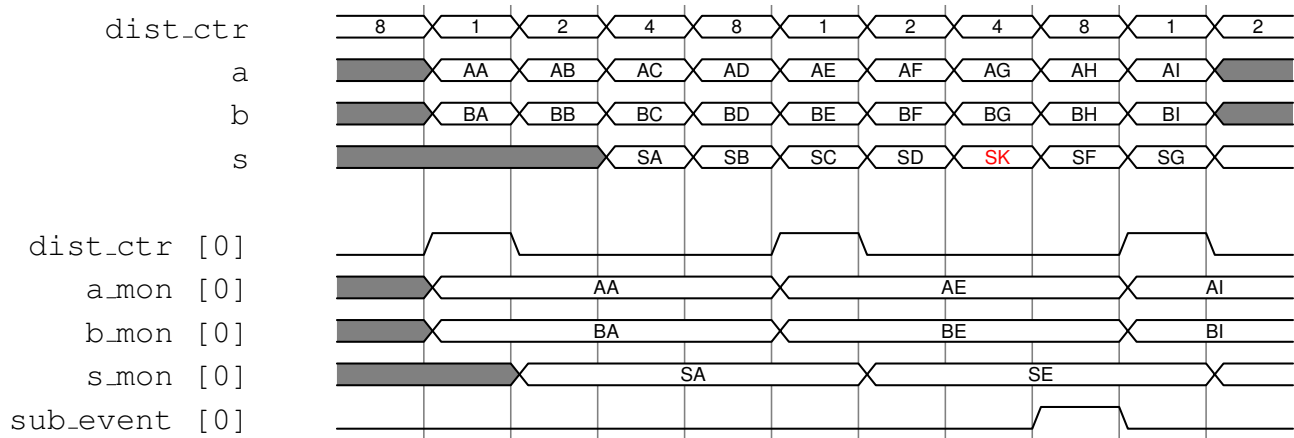


Figure 2: Distributed Monitoring System

5.3 Monitor

5.3.1 Sub Monitors

5.4 Scoreboard

6 Testing

7 Results

8 Evaluation

9 Conclusion

10 Further Work

11 User Guide

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