Imperial College London

Department of Electrical and Electronic Engineering

Final Year Project Report (DRAFT)

Project Title:	**A High-radix Online Arithmetic Verification System**
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Nice abstract

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5.1 Randomiser

With relatively low effort, random testing can provide significant coverage and discover relatively subtle errors [7]. LFSRs are a reliable way of generating pseudorandom numbers quickly with low cost [10].

5.1.1 LFSR Configurations

To compare, we can examine an 8-bit LFSR with taps on bit [7,5,4,3].

Fibonacci – Classical option, easier to write and scale in hardware.

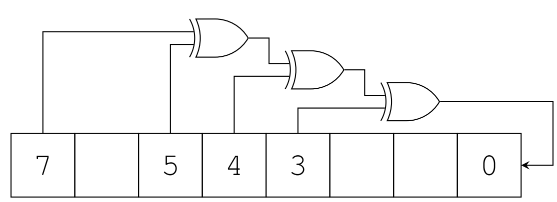

Figure 1: Fibonacci Configuration

Galois – Harder to write if variable length is desired, but faster in hardware.

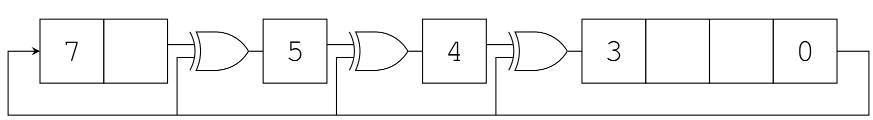

Figure 2: Galois Configuration

Others – Other LFSR configurations such as Xorshift [15] exists, but they are much slower in hardware.

5.1.2 Randomiser Structure

Horizontal – Easy to build, easy to test with.

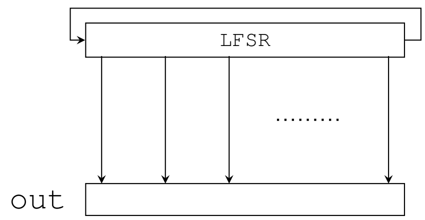

Figure 3: Horizontal Structure

Vertical – Nice randomness, more scalable, need to seed all the LFSRs differently.

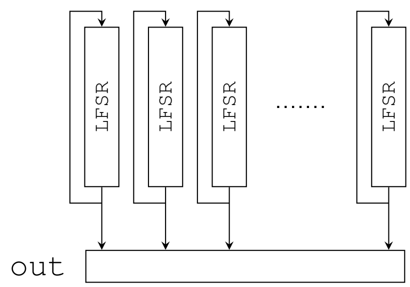

Figure 4: Vertical Structure

5.2 Driver

5.2.1 Dual Driver System

One driver focusses on fast stress tests, The other allows handwritten tests to coexist with random tests. They can be switched in software.

5.3 Monitor

5.4 Scoreboard

6 Software Design Choices

6.1 Code Structure

7 Hardware Implementation

7.1 Project Hierarchy

7.2 Randomiser

7.3 Driver

7.3.1 Delay Tester

I built a delay tester to find out the delay of the DUT. With a 3-bit counter as shown in the timing diagram, it can measure this delay for up to 8 clock cycles.

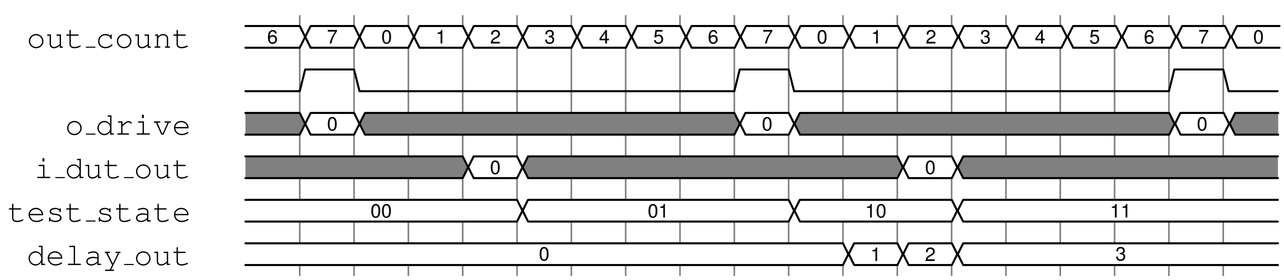

Figure 5: 3-bit Delay Tester FSM

Testing with 0 is safe since LFSR will never output 0.

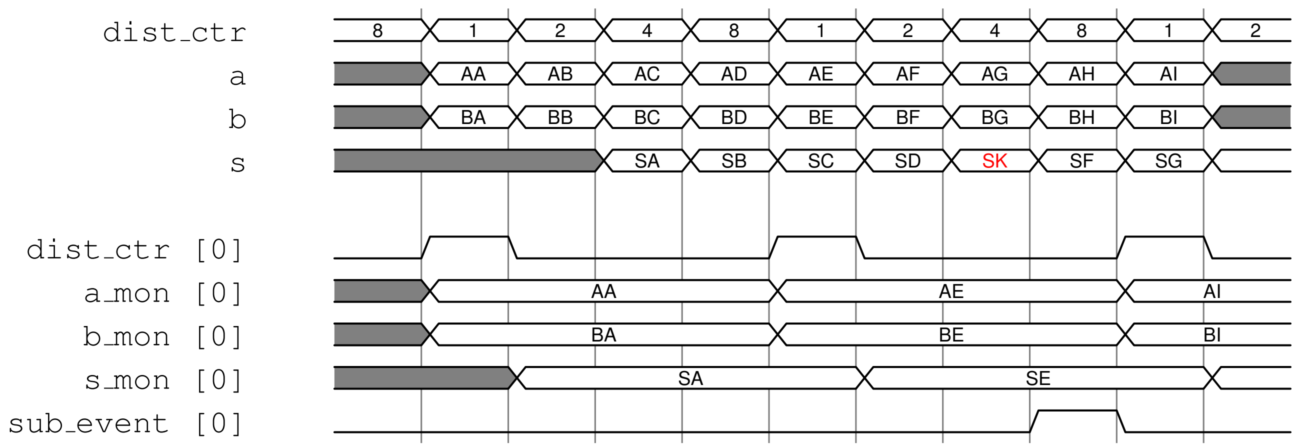

Figure 6: Distributed Monitoring System

7.3.2 Switching system

7.4 Monitor

7.4.1 Sub Monitors

7.5 Scoreboard

8 Software Implementation

9 System Integration

9.1 Qsys

10 Testing

11 Results

12 Evaluation

13 Conclusion

14 Further Work

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