

# A High-radix Online Arithmetic Verification System

Final Year Project 1800478: Interim Report

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# 1 Introduction

With the right number representation system, it is possible to perform arithmetic operations MSD first. Consequently, these online arithmetic operators are attractive for hardware implementation in both serial and parallel forms. When computing digits serially, they can be chained such that subsequent operations begin before the preceding ones complete. Parallel implementations tend to be most sensitive to failure in their LSDs, making them more friendly to overclocking than their LSD first counterparts, for which the opposite is true.

In the past, online operators have typically been implemented in binary. Although Radix-2 modules are the simplest to design and has the shortest cycle time per digit, it has the highest online delay and requires the largest number of cycles to complete calculations [14]. As such, the choice of binary is not absolute. In this project, I will explore high-radix online operators, investigating their suitability for FPGA implementation and examining the resultant tradeoffs between performance, area and power.

## 2 Background Research

### 2.1 Online Arithmetic

Traditional arithmetic operators have two common characteristics. Firstly, their order of operation may be different depending on the operation itself. A traditional adder, parallel or serial, generates its answers from the LSD to the MSD. A traditional divider design, on the other hand, generates its answer from the MSD to the LSD [1] [10].

Due to this inconsistency, arithmetic operators may be forced to compute word-by-word, waiting for all digits to finish in the previous operator before the next can start [17]. Therefore, if a divider follows an adder, the divider has to wait until the adder has completed its computation before it can begin its own.

The other commonality of traditional designs is that their precisions are specified at design-time. Once built, a 32-bit adder always adds 32 bits together, adding 16-bit numbers usually involves masking the unused bits. A possible way of making it less inefficient would be using SIMD instructions [3], combining smaller operations into a larger one that fits the hardware. This, however, has the tradeoff of being harder to program, and the applications must have sufficient parallelism to exploit.

Online arithmetic does not suffer from the first issue as it performs all arithmetic operations from MSD first [5] [6]. Furthermore, pipelining can be used with online serial arithmetic operators. Thus the output digit of an earlier operation can be fed into the next operator before the earlier one completes its computation.

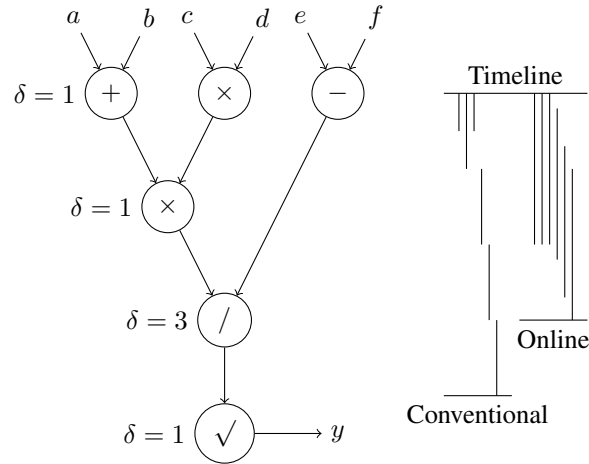


Figure 1: Computing  $y = \sqrt{(a+b)cd/(e-f)}$  with serial online operators [5]

As illustrated in figure 1, while each individual operation may take longer than its conventional counterpart, online arithmetic can provide a speedup if the operators are chained in serial. In addition to the tradeoff in time, individual online arithmetic operators also uses more memory. To perform all computation from the MSD to the LSD, the use of a redundant number system is compulsory. However, this redundancy also has its advantage in making the operators scalable. The time required per digit can be made independent of the length of the operands [15].

A recently proposed architecture allows the precision of online arithmetic to be controlled at runtime [17]. Traditionally, this runtime control was restricted due to the parallel adders present in the multipliers and dividers. This architecture reuses a

fixed-precision adder and stores residues in on-chip RAM. As such, a single piece of hardware can be used to calculate to any precision, limited only by the size of the on-chip RAM.

The way online arithmetic alleviates the second problem of fixed precision falls out directly from its MSD-first nature. Suppose the output of a conventional ripple adder is sampled before it has completed its operation. In this case, the lower digits would have been completed, but the carry would not have reached the higher ones. This means the error on the result would be significant, as the top bits were still undetermined [11]. However, if the output of a parallel online adder is sampled before its completion, the lower bits would be the undetermined ones. This means the error of the operation would be small. With overclocking, online arithmetic operators fail gracefully, losing their precision gradually from the lowest bits first. Thus, it allows for a runtime tradeoff between precision and frequency [12].

## 2.2 High-radix Arithmetic

Conventional designs of arithmetic operators use binary representations. This was chosen four decades ago to maximise numerical accuracy per bit of data. However, using a high-radix representation system could still yield better numerical accuracy while reducing area cost for FPGAs. For example, a hexadecimal floating-point adder was shown to have a 30% smaller area-time product than its binary counterpart, while still delivering equal worst-case and better average-case numerical accuracy [2].

However, the savings are not without trade-offs. This trade-off can become unfavourable if the specification requires much I/O and little computation [16]. This is because the overhead of radix conversion would be significant. It is also unwise to use high-radix representations when the numbers are unusually small, thus making the savings offered by the high-radices negligible [2].

## 2.3 High-radix Online Arithmetic

Using high-radix number representations for online arithmetic is a relatively novel concept. While there has been some research with similar premises [8] [9], We take a more direct approach with this project by implementing custom operators made for high-radix online arithmetic on an FPGA. This will provide empirical results on the method, and will hopefully reveal practical insights along the way.

Furthermore, benchmarking this exotic arithmetic system with popular FPGA applications such as neural networks would be interesting, as there is not much precedence for it.

# 3 Project Specification

## 3.1 Project Organisation

This project is a part of a larger project investigating the effect of using high-radix number representation with online arithmetic operators. The overarching aim involves implementing such a system on an FPGA and quantifying its performance improvements. This is achieved through two individual projects, vertically split from the enveloping project. One shall design and verify the arithmetic operator modules, while the other shall design a system from the top-level to test and evaluate these operators. This project deals with the system-level issues.

As this project progresses in parallel with the designing of the operator modules, it is necessary to decouple the two projects so that, being individual projects, they can be evaluated individually. The success of one project should not be restricted by the status of the other. To this end, the goal of the system-level design is more focussed on its functionalities and robustness. This relationship and its effect on the evaluation will be examined further in the evaluation chapter of this report.

To ensure the two products will work together once they are both complete, a common interface needs to be agreed upon. The interface will be done using Qsys. Its reasoning falls off directly from the use of the hardware; as such it will be explained in the corresponding section.

## 3.2 Deliverables

At the end of the project, the system should be able to perform the following:

1. Connect to the arithmetic modules as its input;
2. Generate and run tests on these modules;
3. Vary the frequency and voltage of the FPGA;
4. Evaluate its performance.

### 3.3 Hardware Choice

The system itself will be built on a Cyclone V SX SoC Development Board from Intel [26].

The 5CSXFC6D6F31C6N SoC has an Arm Cortex-A9 MPCore accompanied by Intel's 28nm FPGA fabric [19]. The FPGA is necessary for implementing the hardware design and obtaining empirical results for the project.

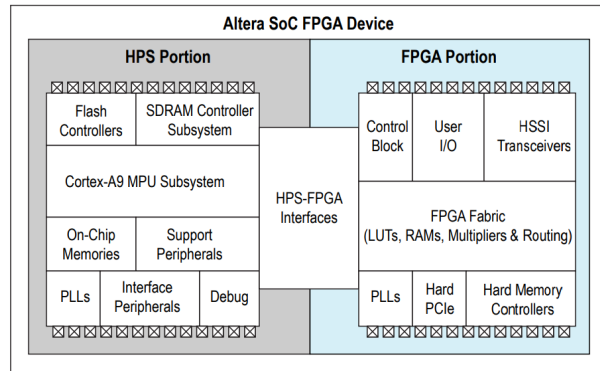


Figure 2: Structure of the System-on-Chip

While an FPGA without an embedded CPU will be enough for this project to work, having an Hard Processor System (HPS) on the same chip is useful as the test software can run on it. The HPS is a separate piece of hardware that distinguishes itself from a soft processor, such as the Nios II, a processor programmed onto the FPGA itself. With this additional capacity, a better user interface can thus be constructed with more detailed, on-the-fly control of the FPGA. This means setting up the testbench will only require programming the design into the FPGA, followed by running the test script on the HPS. The product will thus be self-contained. It will be more accessible as no additional setup is required for the user.

It should be noted that Xilinx offers similar boards as well. Its Zynq SoC family has a very comparable structure as they too integrate the software programmability of an Arm processor with the hardware possibility of an FPGA. For example, similar to the Cyclone V SX, Zynq-7000S features an Arm Cortex-A9 coupled with a Xilinx 28nm FPGA [30]. As such, a board like the ZedBoard [31] could be just as viable for this project.

As there are very few significant functional differences between the two brands, I shall initially explore with the Intel board, simply for its availability and my familiarity with their development tools. Due to the architectural differences between the logic elements between Xilinx and Altera FPGAs [13], the performances on the two boards are not necessarily identical. Once the project has progressed to a point where the system design is mature and tested, the Xilinx alternative can be explored as an extension.

### 3.4 Software Choice

The software choice follows closely with the hardware choice in this project. To develop for Intel FPGAs, Quartus has to be used. The version picked is arbitrary as there are not many functional differences between the versions that will be critical to the project. As Quartus Prime 16.0 is the version installed in the computers in the department, I will use the same version simply for convenience. This naturally means the hardware system will be built with the system integration tool that comes with Quartus – Qsys.

The Qsys software is designed to be used for integrating different hardware modules into a system. As such, it will be used as the interface for the two parallel projects.

While an HLS language could be used, in this design it suffers from a few problems and does not offer enough benefits to justify its use. Usually HLS is preferred for developing complex algorithms, because compilers can optimise them into RTL much better than humans. However, the resulting RTL would be unreadable, making directly controlling or debugging at the hardware level nearly impossible. The interfaces require detailed control of the actual hardware and the rest of the testbench has a lot of control path work and direct manipulation on the data bits. It is therefore not worth it to use HLS and as such, this design will be written in Verilog.

Other than the hardware design tools, there is some freedom of choice on the HPS side of the project. The test will be built with Python, which will be running on an Ubuntu system that is installed on the HPS. This choice is made as there are previous unrelated projects on the same development board, which means a lot of time can be saved on tedious setup works such as getting an operating system booting.

## 4 Engineering Background

### 4.1 Testbench Architecture

The design of the verification system is the major engineering challenge of this project. While there have been many similar performance analyses done on hybrid SoCs before, each of them used their own, usually ad hoc, testbench design [11]. As such, most testbenches are not designed to be scalable or portable, serving only what they are built for. In this project, I shall use a generic structure inspired by that of an agent in Universal Verification Methodology (UVM).

Before UVM, integrated circuit designs were verified with methodologies developed independently by stimulator vendors such as Cadence, Mentor Graphics, and Synopsys. In an effort to unify for greater efficiency, the standards organisation of the Electronic Design Automation (EDA) industry, Accellera, established UVM with support from multiple vendors. It provided a common structure for verification, with class libraries that made building and running a testbench a significantly smoother experience. The agent is a container in UVM that emulates and verifies DUTs [18]. While this project is in no position to achieve what UVM has done, I do hope that this testbench would have an easily modifiable structure that will make the process of testing similar future designs slightly simpler.

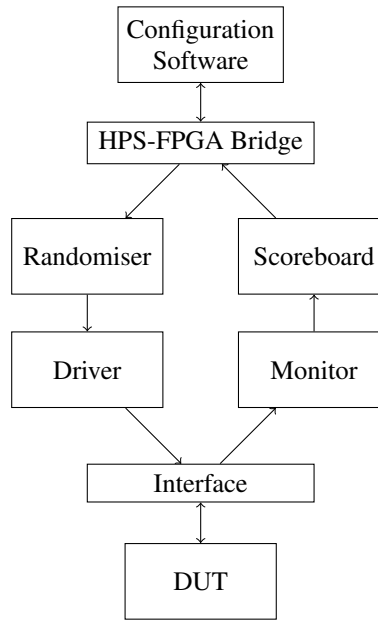


Figure 3: Block diagram of the proposed testbench

Configuration is first done from software running on the HPS, which sends the test specifications to the randomiser. The randomiser will provide a stream of random data that will be converted to meaningful test inputs by the driver. The test output will be watched by the monitor, reporting any interesting event to the scoreboard, which keeps track of them. The scoreboard feeds the information back to the software on-demand. The interface is used to decouple the control logic from the DUT, allowing the frequency of the DUT to be finely controlled.

### 4.2 Data Transfer Rate

In order to stress the DUT, the verification system must perform at a much higher frequency than the expected frequency of the DUT. Assuming the DUT is to run at 300MHz, to fully explore the effect of overclocking, the testbench must be able to run at double the frequency or higher. This gives a target frequency of 800MHz. Assuming a data width of 32-bit, the target data transfer rate is then estimated to be 25.6Gbps.

#### 4.2.1 HPS-FPGA Bridge

As the testing is to be controlled by the HPS, the HPS-FPGA bridge will be the immediate bottleneck if the test data is to flow from HPS to FPGA. While the HPS can easily generate test data with a piece of software, there is a large amount of overhead as data crosses from one architecture to another. This overhead exists in the form of both decreased bandwidth and increased delay. Thus, it is not sensible for the HPS to send out data during runtime.

#### 4.2.2 Off-chip DDR SDRAM

Another thought may be to first populate the off-chip DDR SDRAM on the FPGA side, then feed that data to the DUT during test. This is already much faster than passing the data directly from HPS. The 1GB, 32-bit wide DDR3 on the FPGA side is rated at 400MHz. With double rate transfer, this gives a maximum transfer rate of 25.6Gbps.

Although using the off-chip RAM may theoretically achieve the targets, it still has its disadvantages. Firstly, the process of filling up the memory takes time. Thus, the testing would be broken up into bursts, with time in between for checking results and filling in new data. The complexity of the SDRAM interface also requires an SDRAM controller to be used to manage SDRAM refresh cycles, address multiplexing and interface timing. These all add up to significant access latency. While it could be overcome with burst and pipelined accesses, it would further complicate the SDRAM controller. A controller is provided by Intel [21], but it would consume a non-negligible amount of the limited FPGA resources while adding unnecessary complexities to the design. Customising or building a new SDRAM controller to fit this project is possible, but needlessly time-consuming.

#### 4.2.3 On-chip Memory

The on-chip memory is much faster and simpler to use. In comparison, this memory is implemented on the FPGA itself, and thus needs no external connections for accesses. It has higher throughput and lower latency than the SDRAM. The memory transactions can also be pipelined, giving one transaction per clock cycle. With an on-chip FIFO accessed in dual-port mode, the write operations at one end and the read operations at the other end can happen simultaneously. This feature is useful as tests are prepared and fed into the DUT, or when test results are collected and fed to the monitor.

On-chip memory is not without its drawbacks. It is volatile like SDRAM and very limited in capacity. SDRAMs can have store about 1GB, while on-chip memory could only hold a few MB [20]. Volatility is not exactly of concern in this project, but its small capacity means not much test data can be held before it needs more fed in.

#### 4.2.4 Distributed RAM / Registers

On-chip memory has a minimum latency of 1 clock cycle as the R/W access gets processed. If a even faster memory is desired, we can use LUTs or registers to store them. This option would eliminate the latency but takes up much more FPGA resources. The capacity is even more limited as LUTs are usually used for logic. There will be a significant amount of data generated during testing, and the testbench should be as lightweight as possible to allow flexibility in the DUTs. As such, distributed RAM will not be used in this project for data transfer.

### 4.3 Runtime Test Data Generation

To exploit the benefits of on-chip memory, a way of generating test data at runtime needs to be designed. As arithmetic operators have a vast set of valid inputs, it is necessary to have cost effective test generation.

A good choice here is to use random testing. With relatively minimum effort, random testing can provide significant coverage and discover relatively subtle errors [4]. The main drawback of random testing is the possible lack of coverage on extreme cases, and the usual solution is to provide handwritten tests to complement random testing. However, as the main goal of this testbench is gauging the performance of the module, and not necessarily verifying the correctness of it, this could be ignored during stress testing. If logic correctness testing is later required, these special tests could be written and run separately with a relaxed timing restriction.

LFSRs are a reliable way of generating pseudo random numbers fast with minimum cost [7]. They will thus form the starting point of data generation. While it is possible for data generated to be invalid as inputs to the DUT, this should not be the case for most benchmarks in this project. Even if so, they can be dealt with at the monitor.

With this, the software would only need to configure the randomiser, and test data no longer needs to pass through the HPS-FPGA bridge.

### 4.4 Clock Domains

Another concern in the system design is of the different clock domains that must exist on the FPGA. At a minimum, there needs to be two clock domains, one surrounds the DUT and another supports the rest of the control logic around the DUT. These clock frequencies can be generated and distributed with PLLs, which are provided as IP Cores in the Quartus software [22]. Data crossing clock domains will be fed through FIFOs to prevent loss.

The proposed structure will have the main bulk of the control logic running on a separate clock domain as the DUT. Only an interface with FIFOs and minimum logic will be running in synchronous with the DUT. Therefore, the test controls can be running at a slower frequency without bottlenecking the system, allowing the DUT to be stressed further.

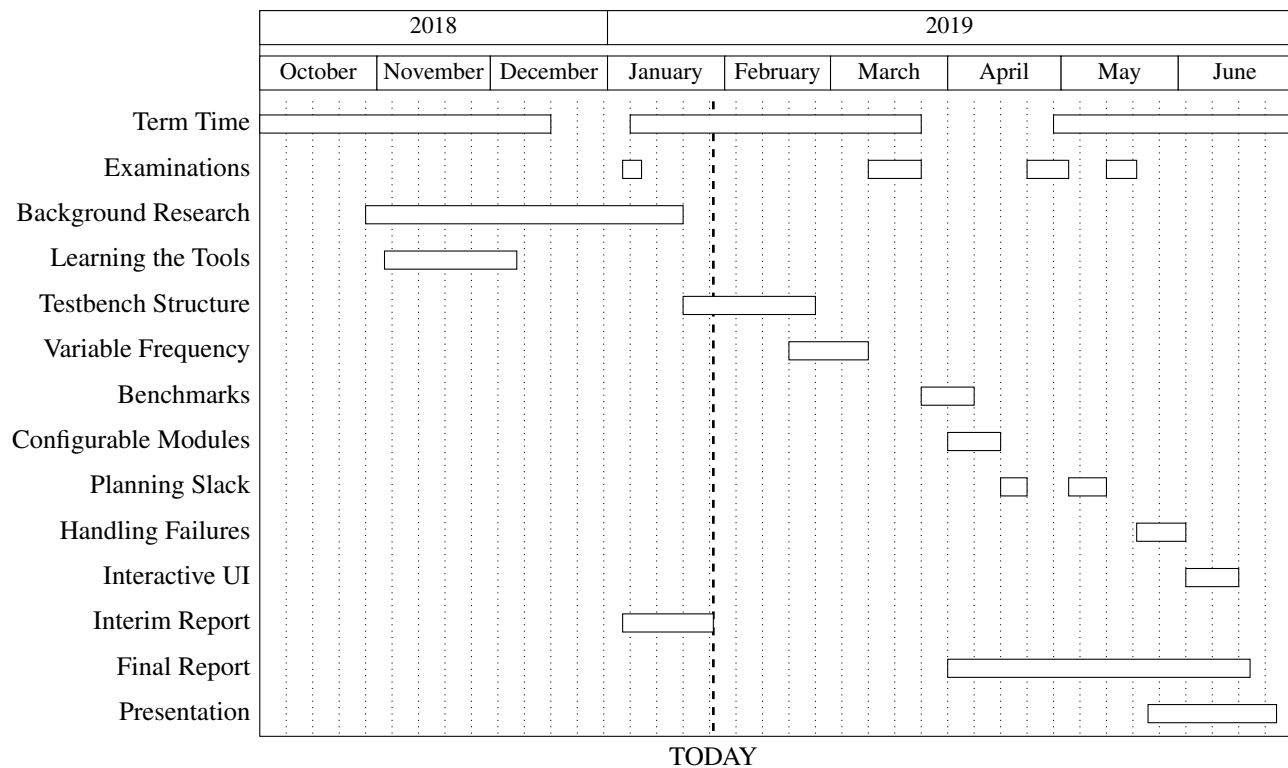


Figure 4: Project Timeline

## 4.5 Result Analysis

If the monitor detects an interesting event such as an error, it will sent out a message to the scoreboard. The scoreboard has counters tracking these events, and update them back to the software periodically.

The software can run statistics to provide further insights to the user.

## 5 Implementation Plan

### 5.1 Milestones

The project is divided into three main phases. The initial one is of research and learning. This is to lay the foundation to the project, and is represented by task 2 and 3 in the timeline. The second phase is building the core product of the project. This includes task 4, 5 and 6 in the timeline. The final phase is enhancing the product, represented by task 7, 8, and 9.

### 5.2 Timeline

In order to track the progress and success of the project, the difficulties of the deliverables need to be analysed first. Figure 4 provides a visualisation of the project timeline. Some slack is included into the plan to reduce risk and give potential for extension.

#### 5.2.1 Term Time and Examinations

Time available for the project varies greatly throughout the year. The greatest factors would be the term time and the examinations. The time needed for revision has been marked in the chart. These times will have minimum progress to the project.

During term time, there would be coursework deadlines, which would also negatively affect the time that could be allocated to this project. One coursework module was selected for Autumn and three was picked for Summer. As such, it is expected that the progress would be somewhat slower during Autumn but significantly slower during Spring. To make up for the time lost, a part of Christmas were used and a few weeks from Easter will also be committed towards the project.

The list of tasks were then laid out onto the timeline. This is done according to its expected difficulty and the expected availability to work on these tasks.

### **5.2.2 Background Research**

To fill in the background knowledge required to work on this project, the first months were spent on reading textbooks and papers. The research is to provide context and motivation to the project. It also provided an overview of the field of research and some understanding towards the current state-of-art. Most importantly, it offered the necessary knowledge needed for this project. The result of this research is summarised back in chapter III.

### **5.2.3 Learning the Tools**

Due to the lack of experience in programming hybrid SoCs and the lack of knowledge in the current state-of-art digital arithmetic designs, a significant portion of the effort was spend on researching and learning the skills necessary to carry out the project. This involved building a small testing system on the board. Details regarding this testing system can be found in the Work to Date section.

### **5.2.4 Testbench Structure**

Once comfortable with the tools, The main design of the testbench can start. This task would be the foundation of this project, as it would provide a basis for all following features. A skeletal testbench should be complete and functional at the end of this task. This means the an operator module matching the correct specifications can be loaded into the testbench, and compute some non-trivial tests.

### **5.2.5 Variable Frequency**

As the project seeks to quantify the performance across a range of frequencies, the most important feature of the system would be the ability to vary this parameter. This would be done by controlling the PLLs with the HPS [22]. Once implemented, tests will be run to explore and confirm the maximum frequency the testbench would remain reliable. If it does not meet the planned target, the testbench may need to be redesigned, and this project would be under some risk.

While most of the later sections of the project can be selectively added or removed from the scope relatively easily, this initial setup of the testbench structure will always remain critical to any further improvements. It is thus vital that the bare minimum system gets done early. To ensure this happens, this task and the testbench structure will be placed in the highest priority before its completion, and any blocking issue should be discussed with the supervisor if it could not be resolved after reasonable effort.

### **5.2.6 Benchmarks**

With a promising base, more intricate tests and benchmarks can be designed. These would aim to reflect the system's performance running meaningful compute tasks. The systems enveloping the arithmetic modules could be stressed with popular algorithms to evaluate real-life obtainable speed up. In addition to better tests, this task also aims to obtain better data from these tests. The minimum result required here would be numerical information on power consumption, FPGA resources required, and the data throughput.

The last three tasks forms the core of this project. In other words, all three tasks must be completed for a minimum functional product. The following tasks would be mostly considered as useful extensions. While not as vital as the core tasks, the following tasks greatly improves the quality of life and usability, and thus are equally critical to the success of the final product.

### **5.2.7 Configurable Modules**

So far, only modules of a specific I/O width and numerical representation could be tested. It might be interesting to explore arithmetic modules with other configurations. To allow the testbench be used for further experiments or future projects, it is helpful to have a configurable testbench. Qsys components can be configured with the Hardware Component Definition File [23]. The plan is to build the testbench as a Qsys component, then use Qsys Component Editor as an interface for configuration.



### 5.2.8 Handling Failures

Another improvement to the testbench is related to how it handles failures in the module. It would be much more insightful for the user, if a more insightful failure message is provided in addition to just a simple failure rate. This could include examples of failed output against expected output, or statistical data describing the pattern of failures. This additional logic during run-time may degrade performance of the testbench, so it would be useful for the verbosity of this information to be configurable by the user.

### 5.2.9 Interactive UI

If time allows for even greater user experience enhancements, an real-time interactive graphical user interface could be constructed for the final demonstration. This would visualise the reduction of the module's precision as the user increases the clock rate. However, this would take significant time and effort, and this task will be re-evaluated when the project progresses to the stage. An time-saving yet functional alternative would be a command-line interface with a well-documented user guide.

### 5.2.10 Reports and Presentation

The reports and the presentation are the most visible in all deliverables of this entire process. As such, while not directly contributing to the progress of the project, they are still vital to its success. The reports will be written alongside with the engineering process. At the end, around a week of time will be spent solely on completing and polishing up the final report. This should allow ample time for a well-organised submission.

The week after the final report will be used for the presentation. This would involve preparing a slide deck, a demo, and a script.

## 5.3 Work to Date

Before any engineering work is done towards the final product, a small module was built to learn the environment. This module should be simple yet covers enough grounds to provide as much learning during the process as possible without taking up too much actual development time towards the product. As the greatest unfamiliarity is with the interaction across the HPS-FPGA bridge, a simple hardware accelerated adder was made for this training.

### 5.3.1 FPGA Side

Programming the FPGA to communicate with the HPS is no trivial task. Luckily, there exist a golden system reference design [29] for the board in use for this project. Unfortunately, support for certain versions of Quartus are missing from the GSRD download database, including the one used for this project, 16.0. While the design could be opened with a different version of the software, it would cause a series of conflicts usually related to using IP Cores that have changed over the iterations. To circumvent this issue cleanly, GSRD version 14.1 was downloaded and compiled on a separate install of Quartus II 14.1. This allowed the reference design to be studied in detail, and the sections required for this project to be rebuilt with Quartus Prime 16.0.

From the perspective of the FPGA, The HPS exposes three bridges for connections [24]. As this is a relatively simple task, the lightweight bridge is used. Module `altera_hps` exposes the master of this bridge as `h2flw_axi_master`. Next, the actual hardware adder needs to be built and integrated as a hardware module in Qsys with a matching interface. A simple adder can produce its result after one clock cycle. This greatly simplifies the logic required for the Avalon slave interface. The logic for the control and data signals are then written according to the interface specifications [28]. Following the naming conventions for the signals allows Qsys Component Editor to automatically detect the Avalon slave from this module at analysis. This saves the troubles of editing the `_hw.tcl` file. To experiment with module configuration, the adder is designed with variable width.

The adder is then instantiated and connected to the rest of the system with two clicks in Qsys. From there, Qsys can generate the HDL for the entire system, which is then compiled to a bitstream file. With the bitstream ready, the work now shifts to the HPS.

### 5.3.2 HPS Side

The HPS runs Ubuntu and a bash script has been written to load the bitstream onto the FPGA. Next, A program is written in Python to test the hardware design from the HPS. The interfaces are mapped onto the physical memory, thus they can be accessed by opening `/dev/mem`. Checking against the specifications [24], the lightweight master is at `0xFF20_0000`. Qsys allocates the memory spaces of modules relatively, so when it reports that the adder has been placed at `0x0010_0000`, it is

physically at 0xFF30\_0000. The adder is designed to have its two inputs at 0x00 and 0x10 and its output at 0x20, which has been assigned by Qsys relatively to 0xFF30\_0000.

With the memory mapping understood, the script can be designed to closely mirror this relative relationship between the modules using classes. For example, this allows the adder to still define its output at 0x20 in the adder class, and then initialised with an AXI module bringing it to the correct physical address. This parallel between software and hardware should be helpful as the product gets more complex.

For testing, 1000 add operations are executed separately with and without the hardware acceleration of the FPGA. While called hardware acceleration, it is not expected for the FPGA to have a higher performance than the HPS in this testing case. The CPU is reasonably efficient in calculating additions, while to calculate on the FPGA has a large overhead cost as the data transfers across the bridge back and forth.

## 6 Evaluation Plan

### 6.1 Metrics

One natural way of measuring the success of the project is to look at the actual progress and comparing it to the plan given in the implementation plan. It should be noted that no plan is perfect, so some deviation is allowed. However, if there is significant delay from the implementation plan, there must be justifications given.

The next few measures looks at the performance of the final product. First, the maximum stress of that the testbench and provide without failing can be used as a success measure. A testbench with a higher maximum frequency can reveal a wider picture in the performance of the DUT. This would hopefully allow more insights to be gained regarding the DUT, or it could mean that the testbench can be used for future designs that may be faster than the current one. As the main quantitative metric, this would be a vital indicator of the project's success.

The Robustness of the testbench is also vital to the product's performance. The testbench should be free from errors within a reasonable operating range. If the testbench becomes unreliable with some minor changes to the system, the data that can be obtained would be very limited. The failure of the DUT can no longer be confirmed, as the error may be in the testbench instead of the DUT.

The ease of use of the testbench could be another evaluation point. On the hardware side, the verification system can be packaged into a Qsys module. Given the DUT is also a module with an agreed interface, they could be easily connected in Qsys for testing. For example, the DUT may be written in VHDL for its deterministic nature, but the testbench maybe written in Verilog for its simplicity, but as both can be synthesised into a module, they would still be compatible in Qsys. On the software side, a user-friendly interface could be built. A usable command line interface maybe good enough, but a simple graphic interface could make the tests much more visual and interesting.

The interface could also provide information on the failure in the DUT. A better testbench would provide more insightful details when the DUT fails. This would make debugging or evaluating the design much simpler. Along with the GUI, this project has many optional extensions that would be discussed further in the corresponding section. After the main goal of the project being met, the number of optional functions implemented would become a good measure of the progress of the project.

Since the project is of the verification system, the results from the benchmarks should not be used for evaluation of this project.

A noteworthy point in evaluation is regarding the progress of the sister project. The purpose of the testbench is to verify and stress the arithmetic designs. If these designs would not be available near the end of this project, it would be difficult to empirically prove the capabilities of the testbench and its surrounding system. It is not impossible, as there are still substitutions for them. For functional purposes, standard off-the-shelf arithmetic modules could be used in-lieu. For other purposes, it is possible to have a model done before the actual design starts in the paired project. While this would allow this project to progress easier, it would be extra work for the other project, which is ultimately up to the decision of the other student. In all, it would be nice to have a solid arithmetic module completely to run in this testbench, but without one, the system can still be built and completed, albeit generating less useful data towards the overall aim of the project.

## 7 Ethical, Legal and Safety Plan

### 7.1 Ethical Considerations

Checking against the ethical issue list provided by Imperial College Research Ethics Committee [25], this project does not

- damage participants' mental or physical health;

- jeopardise the safety or liberty of the researchers;
- use any private information;
- involve sensitive subject matter or methods;
- risk any conflict of interest between the researchers and the College.

This project is thus free from significant ethical concerns.

## **7.2 Legal Considerations**

Intel Quartus Prime software offers a variety of IP cores. These are encrypted module designs that would be integrated into the verification system of the project [27]. This project would integrate some of these IP cores so that some of the basic circuit building blocks would not need to be redesigned.

While it would be possible to complete this project with a free license, Imperial has academic licenses for the software allowing for faster compilation time.

## **7.3 Safety Considerations**

As the project is done mainly on a computer with minimum physical aspects, there is no major safety concern. For the minor concerns associated with the project, the physical development board will be handled with care, and the desk works will be interleaved with breaks.

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