An Extensible Framework for Evaluation of Arithmetic Hardware

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Motivation

- Started as a specialised evaluation system for high-radix online arithmetic units
  - At-speed
  - Precision Checking

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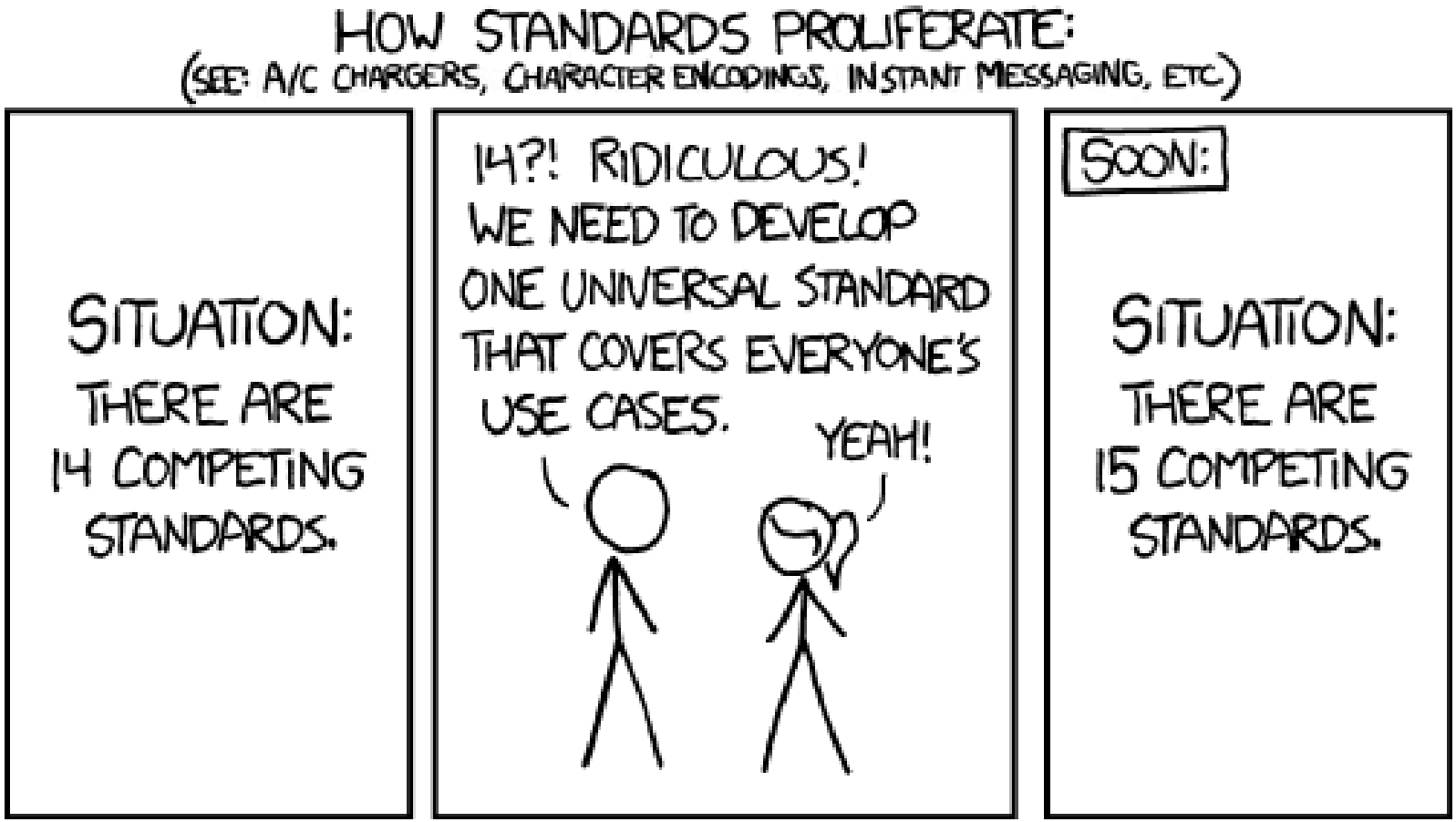
  - At-speed
  - Precision Checking
- Digital designers all use their own testbenches
- Propose an extensible framework

Motivation



xkcd.com/927

Purpose

- Design and Implement an evaluation framework
  - High maximum frequency

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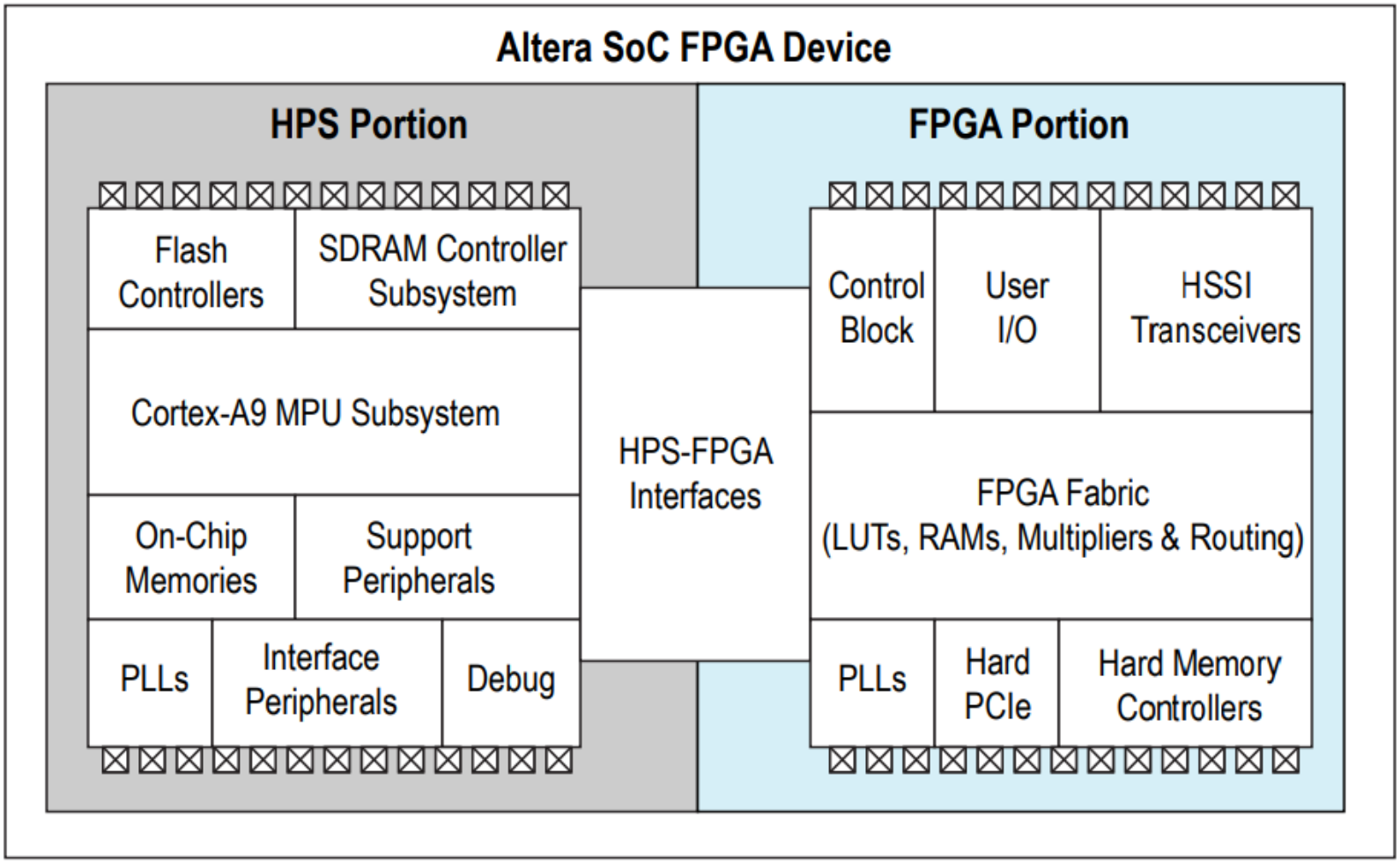
  - Flexible, customisable
  - User-friendly

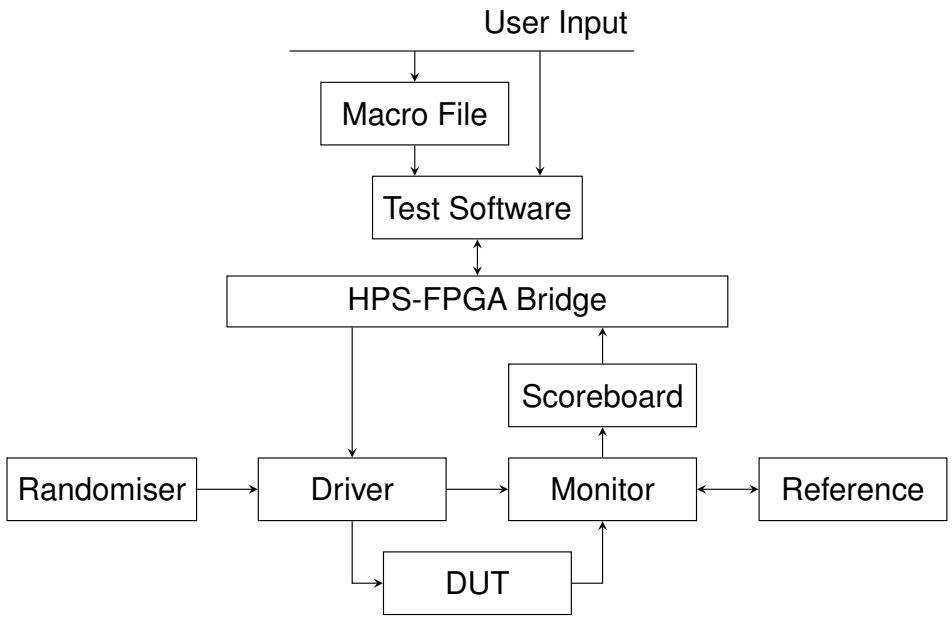
Hardware Choice

Cyclone V SX SoC Development Board

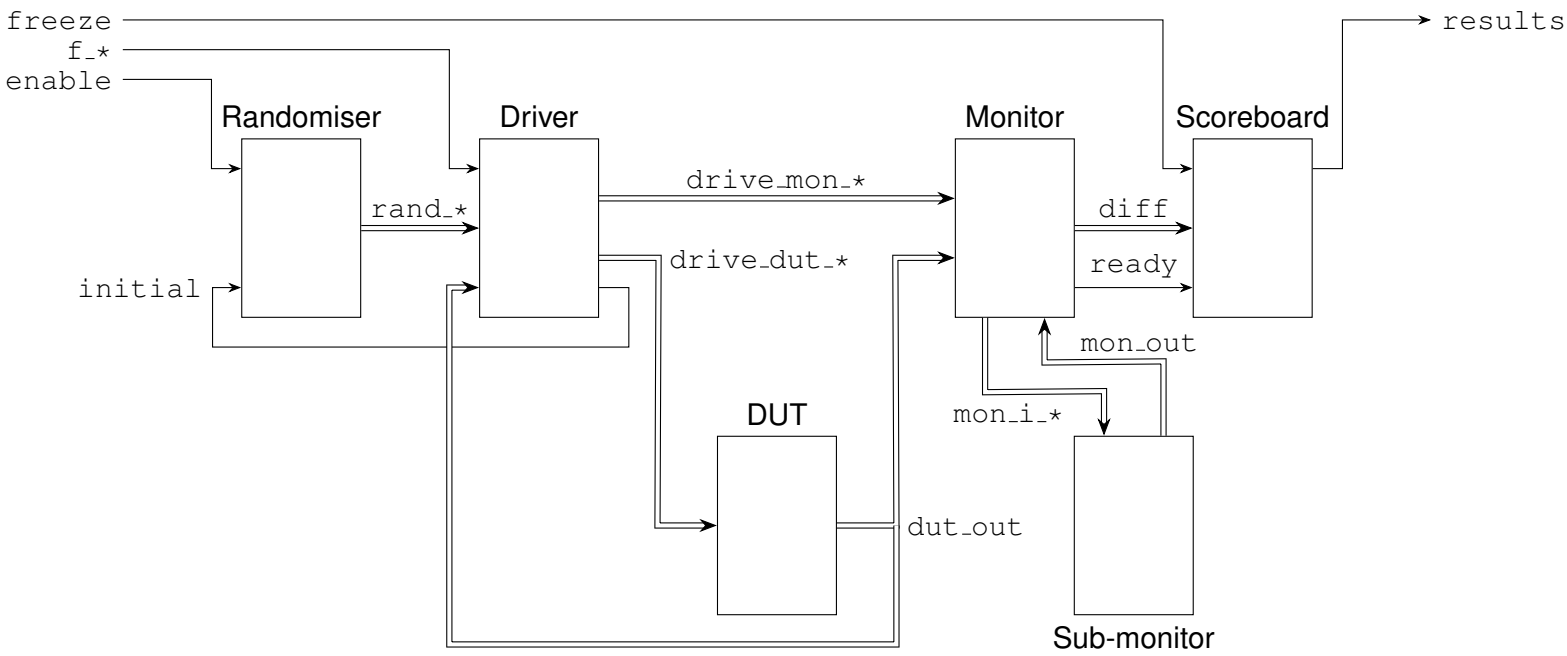


System Architecture

- Inspired by UVM agent
- Modular, thus extensible



Hardware


freeze
f_*
enable
initial
Randomiser
rand_*
Driver
drive_mon_*
drive_dut_*
Monitor
diff
ready
Scoreboard
results
mon_out
mon_i_*
DUT
dut_out
Sub-monitor

Software

Results

- Flexible
- Robust
- User-friendly

Demo

- Shows the configuration process
- Shows software interaction

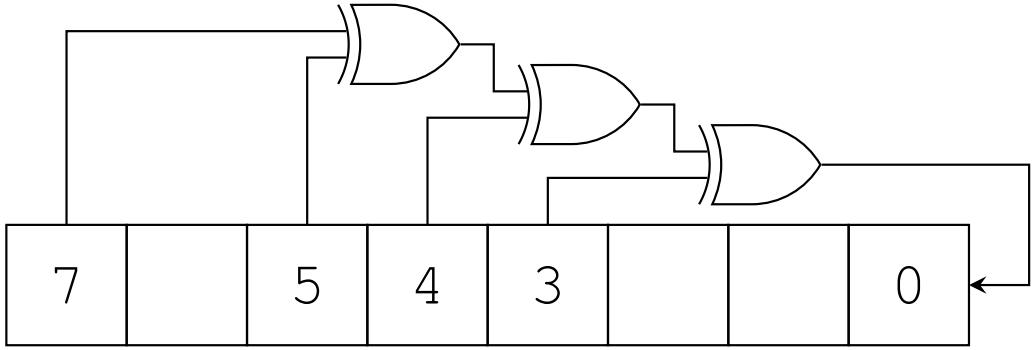
Limitations

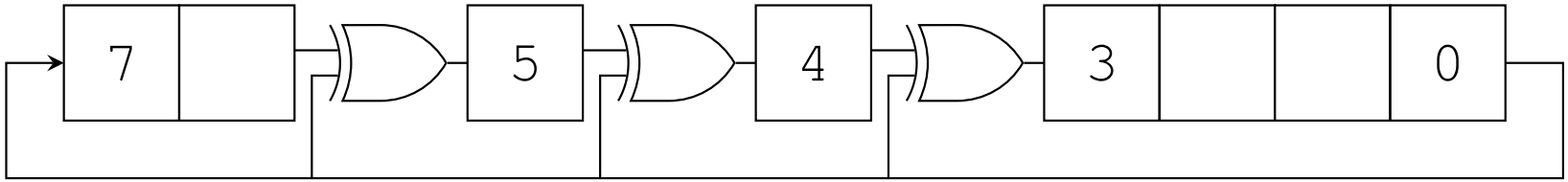
- Limited customisability of current implementation
- Tedious and error-prone
- Could be overcame with 2 improvements
- Unified software system + Verilog preprocessor
- Set up a more powerful HPS-FPGA communication system
- Not limits to the extensibility of the framework

Thank you

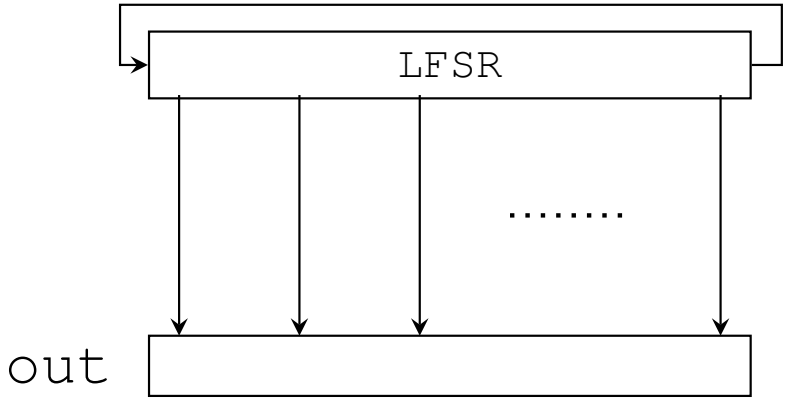
Questions?

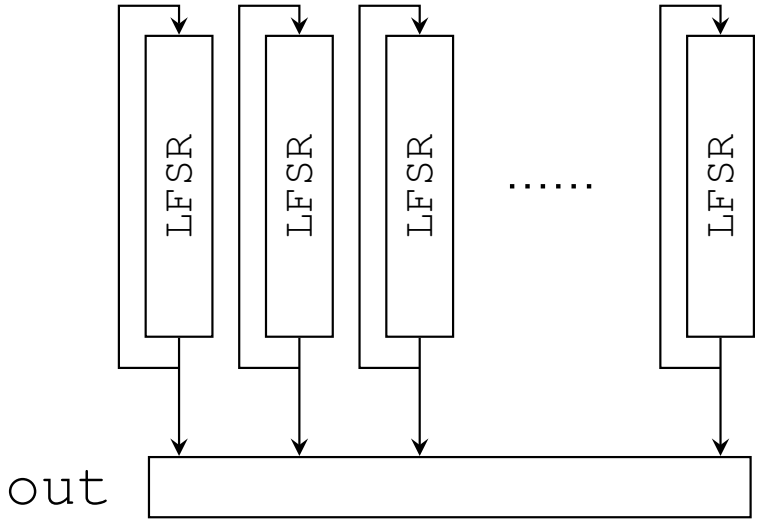
LFSRs





Randomiser Structure





Monitor Structure