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Background

D&I

Hardwa

Softwar

Results

Evaluation

Backup Slides

An Extensible Framework for Evaluation of Arithmetic Hardware

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Imperial College London

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Background Motivation

Design & Implementation

System Hardware Software

Results

Results Demo

Evaluation Evaluation

Backup Slides

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Backgrou

Del

System

Softwar

Results

Evaluati

Evaluation

Backup Slides

Motivation

- Started as a specialised evaluation system for high-radix online arithmetic units
 - At-speed
 - Precision Checking

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Backgrou

Del

System Hardwa

Softwar

Results

Evaluation

Backup Slides

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- Started as a specialised evaluation system for high-radix online arithmetic units
 - At-speed
 - Precision Checking
- Digital designers all use their own testbenches

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Motivation

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System

Softwar

Results Demo

Evaluation Evaluation

Backup Slides

Motivation

- Started as a specialised evaluation system for high-radix online arithmetic units
 - At-speed
 - Precision Checking
- Digital designers all use their own testbenches
- Propose an extensible framework

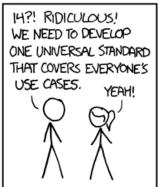
Motivation

Motivation

Besults

HOW STANDARDS PROLIFERATE: (SEE: A/C CHARGERS, CHARACTER ENCODINGS, INSTANT MESSAGING, ETC.)

SITUATION: THERE ARE 14 COMPETING STANDARDS.



500N:

SITUATION: THERE ARE 15 COMPETING STANDARDS.

xkcd.com/927

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Purpose

Backgrou Motivation

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Results

Evaluation

Backup Slides

- Design and Implement an evaluation framework
 - High maximum frequency

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System Hardwa

Result

Results Demo

Evaluation

Backup Slides

Purpose

- Design and Implement an evaluation framework
 - High maximum frequency
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 - Provide information regarding precision of output

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Purpose

- Design and Implement an evaluation framework
 - High maximum frequency
 - Controllable frequency
 - Provide information regarding precision of output
 - Flexible, customisable

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Purpose

Backgroun

Motivation

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Hardwa

Result

Demo Evaluation

Evaluation Evaluation

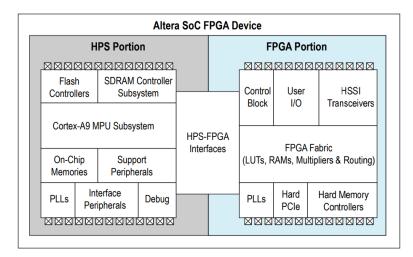
Backup Slide

- Design and Implement an evaluation framework
 - High maximum frequency
 - Controllable frequency
 - Provide information regarding precision of output
 - Flexible, customisable
 - User-friendly

Backup Slide

Hardware Choice

Cyclone V SX SoC Development Board



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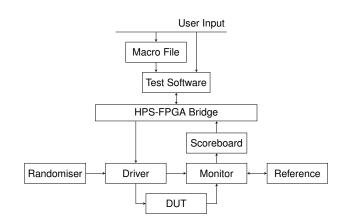
Results

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System Architecture

- Inspired by UVM agent
- · Modular, thus extensible



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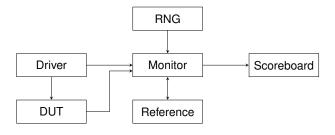
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Evaluation Evaluation

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Monitor Structure

- Lazy Monitor
 - Randomly select data points to check



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Results

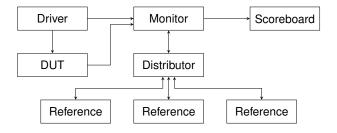
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Monitor Structure

- Parallel Monitor
 - Checks all data points in parallel



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Software

Software

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Software

Results

Results

Demo

Evaluation

Backup Slides

Results

- Maximum frequency
 - TimeQuest: 394.01MHz
 - Hardware test: Stable at 400MHz; breaks at 425MHz
 - Can be pushed further, but stopped for time

Results

Background Motivation

Motivation

System

Software

Results

Demo

Evaluation Evaluation

Backup Slide

Maximum frequency

TimeQuest: 394.01MHz

- Hardware test: Stable at 400MHz; breaks at 425MHz
- Can be pushed further, but stopped for time
- User-friendliness
 - Performed an OOTB Testing
 - No previous knowledge on Qsys or the framework
 - Obtained results in 2 hours

Background Motivation

Motivation

System Hardwar

Result

Results

Evaluation

Evaluation

Backup Slide

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- Flexibility

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Results

Demo

Evaluation

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Flexibility

Item	Reconfigurability
WIDTH	≤32 bits
NUM_SUB_MON	≥2
f _{dut}	≤400MHz
DUT I/O	2 in 1 out
DUT delay	All values
bitset/bitclr	All values
manual	All values
time	All values

- Auto mode filtering limited to bit-wise manipulation
- No access to all precision data
- 32-bit limit to many things

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Result

Demo

Evaluation

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- Shows the configuration process
- Shows software interaction

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Results
Demo

Evaluation Evaluation

Backup Slides

Limitations

- Limited customisability of current implementation
- Tedious and error-prone
- Could be overcame with 2 improvements
- Unified software system + Verilog preprocessor
- Set up a more powerful HPS-FPGA communication system
- Not limits to the extensibility of the framework

Questions?

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Evaluation

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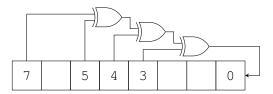
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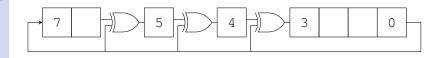
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LFSRs





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System

Software

Results

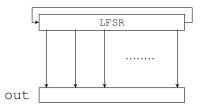
Demo

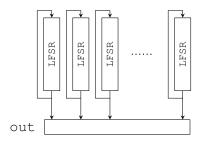
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Randomiser Structure







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Monitor Structure

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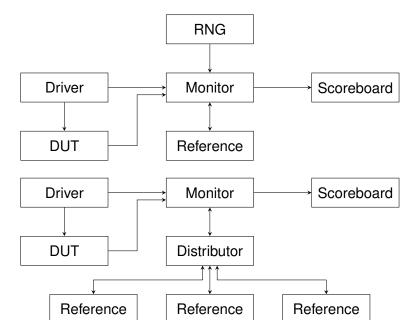
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Software

Results
Demo

Evaluation Evaluation

Backup Slides



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System Hardware Software

Results

Results

Evaluati

Evaluation

Backup Slides

Hardware

