Stockholm
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MERLIN NIKHIL

OBJECTIVE

Aspiring developer with a strong foundation in cloud technologies, particularly Azure, I bring a robust background of three years hands-on industry experience, specializing in hardware logic design. Possessing an open mind to both personal and collaborative ideas, I am driven by self-motivation and a keen aptitude for problem-solving. Eager to channel my coding enthusiasm into dynamic projects within a collaborative software engineering environment.

SKILLS

- Python OOP
- Django
- Flask
- MySQL
- MongoDB
- REST APIs
- Git & GitHub
- Verilog
- System Verilog
- UVM
- Agile
- Azure

EDUCATION & CREDENTIALS

Advanced IT Course: System Developer Python and IT Security | Lexicon IT Proffs
Stockholm, Sweden (oct 2023-Feb 2024)

- **Introduction:** Agile methodologies, Scrum, UI/UX design principles, Trello, Git & GitHub, Linux.
- **Web Programming:** HTML, CSS, Bootstrap, JavaScript.
- **Python:** Object-Oriented Programming (OOP), Django, Flask, REST APIs.
- **Databases:** MySQL & MongoDB.
- **IT-Security:** Ethical Hacking & Penetration Testing: MITM attacks, Server-side attacks, Client-Side attacks, Spoofing, Backdooring, Darknet, Exploits, Password Cracking, Bettercap, Beef, XSS & XSRF, Spoofing, Social Engineering, Burp Suite, Metasploit, Nmap.
- **Cloud Technology Stack:** Azure, DevOps, Docker, Replit.

MTech-VLSI Design | Sathyabama University
Chennai, India (2011–2013)

Master's degree in VLSI Design, specializing in the intricacies of Very Large-Scale Integration. Developed expertise in the design and implementation of integrated circuits, honing skills crucial for the modern semiconductor industry.

BTech - Electronics and Communication Engineering | Vimal Jyothi Engineering College
Kannur, India (2007-2011)

Bachelor degree in Electronics and Communication Engineering, gaining a strong foundation in the principles of electronic systems and communication technologies. Developed practical skills through coursework and projects, fostering a solid understanding of the core concepts in the field.

EXPERIENCE

FPGA DESIGN ENGINEER | AESTER INDIA PVT. LTD
Dec 2018 - Nov 2021

Analyzed technical challenges in project requirements, proposed solutions for manager approval, authored Verilog hardware logic code, verified modules through simulation and FPGA implementation, and communicated daily project progress updates while addressing challenges with the project manager.

Environments: RTL & FPGA Design, Xilinx ISE, Xilinx Vivado, Spartan FPGA Board

ASSISTANT PROFESSOR, ELECTRONICS AND COMMUNICATION | CMS COLLEGE OF ENGINEERING AND TECHNOLOGY
Jun 2013 - Sep 2014

Guided and assisted a class of 68 students in their academic journey, maintaining accurate attendance records, student reports, and class reports to track and assess student progress and performance.

CAREER BREAK | Personal and Family Responsibilities
Dec 2021-Sept 2023

Following the COVID-19 pandemic, it became necessary for me to take on increased responsibilities for my family and children, which were further compounded by multiple relocations. Now, I am excited to re-enter the professional sphere with renewed focus and dedication.

CAREER BREAK | Maternity and Child Care
Oct 2014-nov 2018

Took a career break to focus on the important and rewarding responsibility of raising and caring for my two children. This period involved managing and prioritizing various tasks, including childcare, early childhood education, and creating a supportive home environment.

LANGUAGE

English – Professional knowledge in spoken and written form
Malayalam – Mother tongue

REFERENCES

Good references given upon request.