4-to-1 Multiplexer

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Detailed Description:

We needed to implement an inverter using 0.18 micrometer CMOS technology and 0.5 micrometer CMOS technology, assuming matched design once and minimum area once. The spice netlist of the inverters is as follows. All the inverters designs are added as well as both the transient and DC analysis (they are all commented so that when one is needed for analysis, the comment would be removed, and it would be used). Each inverter has Vdd set to the voltage specified in the project description, 1 PMOS, 1NMOS (both using the models required by the project), capacitor (with the required value in the project description), a pulse Vin for transient analysis, DC Vin for DC analysis, and both DC and transient analysis. Note that each analysis is done separately, so for example, when the transient analysis is needed, both DC analysis and DC Vin are commented.

In the 4-to-1 multiplexer spice netlist, there is the Vdd which is 1.8 volts, 2 load lines (pulses), 4 inputs (pulses), inverter for each input and each load line, PUN, PDN, capacitor (0.2 pf), resistor(1k ohm), the transient analysis to see the inputs, load lines, and output, and finally, the measuring of the average power dissipated using .meas command. The test case we used covered all possibilities by making the frequencies of inputs halved. For example, frequency of I1 is half that of I0, frequency of I2 is half that of I1, frequency of I3 is half that of I2, frequency of I4 is half that of I3, frequency of I5 is half that of I4, frequency of S0 is half that of I5, and frequency of S1 is half that of S0.

Note that I0 is on when S0 is 0 and S1 is 0, I1 is on when S0 is 1 and S1 is 0, I2 is on when S0 is 0 and S1 is 1, and I3 is on when S0 is 1 and S1 is 1.

All the sizes of the transistors will be in the next section.

1. 0.18 technology Inverter:

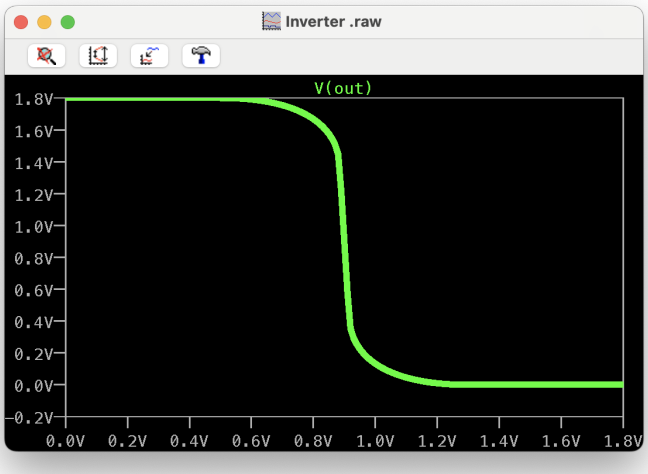
a. Matching Design:

i. Size of transistors:

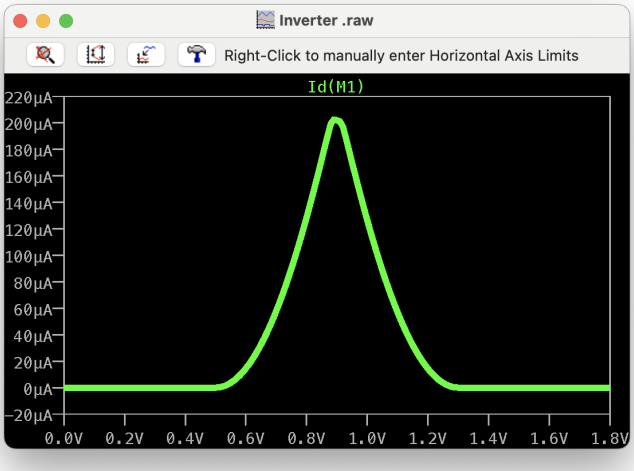
1. PMOS: width = 4.14 micrometer, length = 0.18 micrometer (width was approximated to be divisible by 0.18)
2. NMOS: width = 0.9 micrometer, length = 0.18 micrometer

ii. Results:

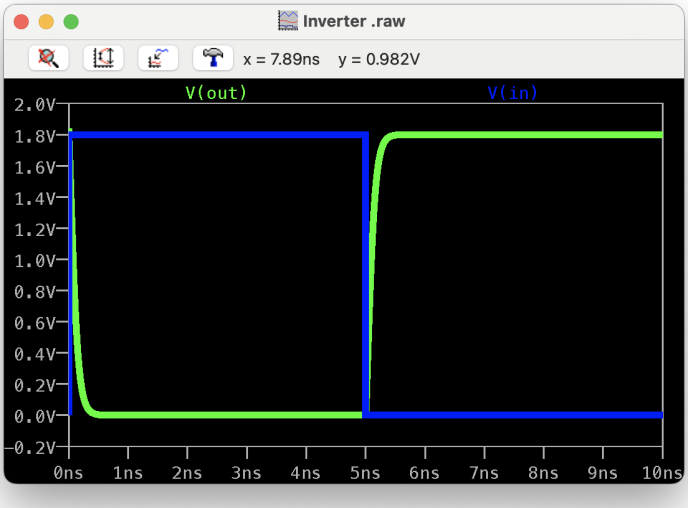
1. VTC:



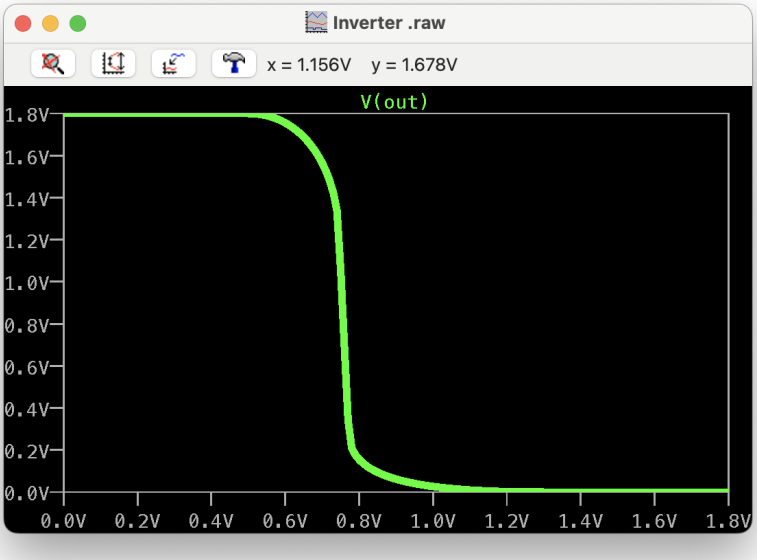
2. Supply current:



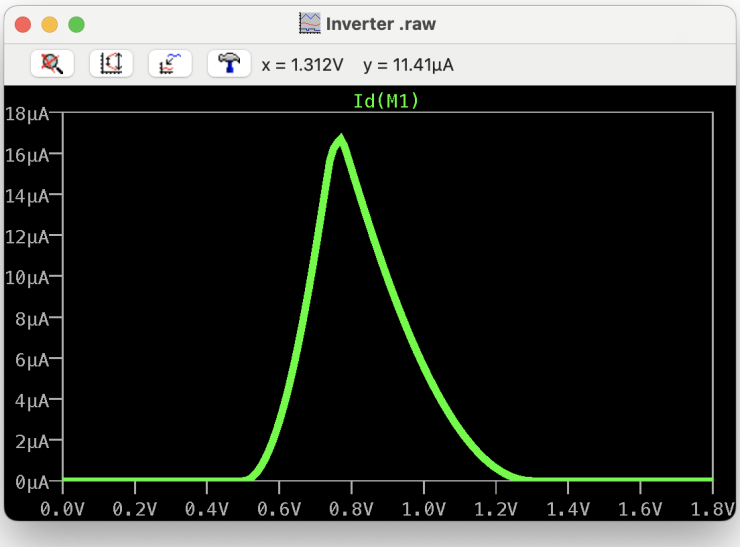
3. Transient simulation:



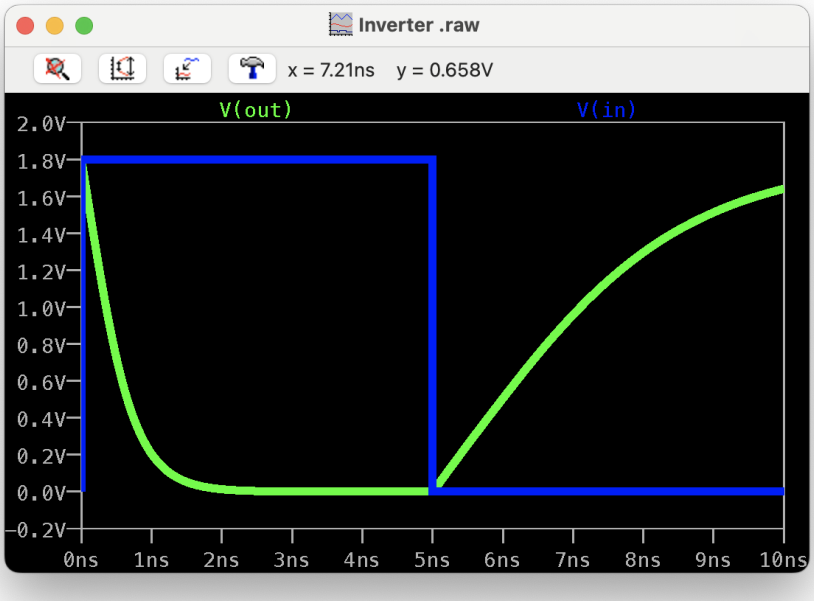
b. Minimum Area:
   i. Size of transistors:
      1. PMOS: width = 0.18 micrometer, length = 0.18 micrometer
      2. NMOS: width = 0.18 micrometer, length = 0.18 micrometer
   ii. Results:
      1. VTC:



2. Supply current:



3. Transient simulation:



2. 0.5 technology Inverter:

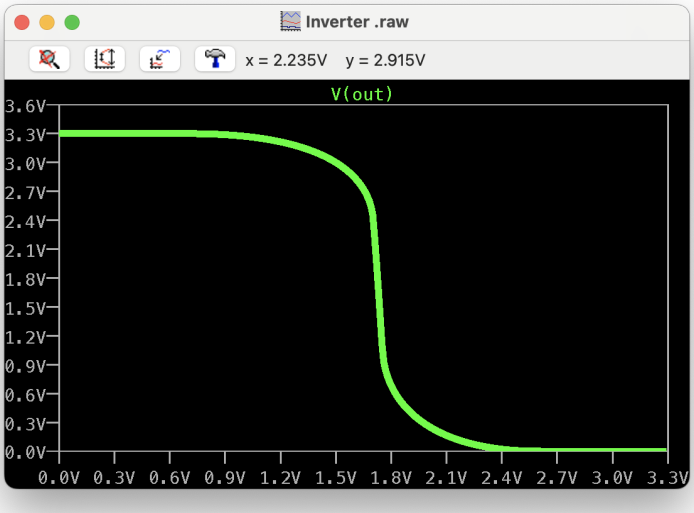
a. Matching Design:

i. Size of transistors:

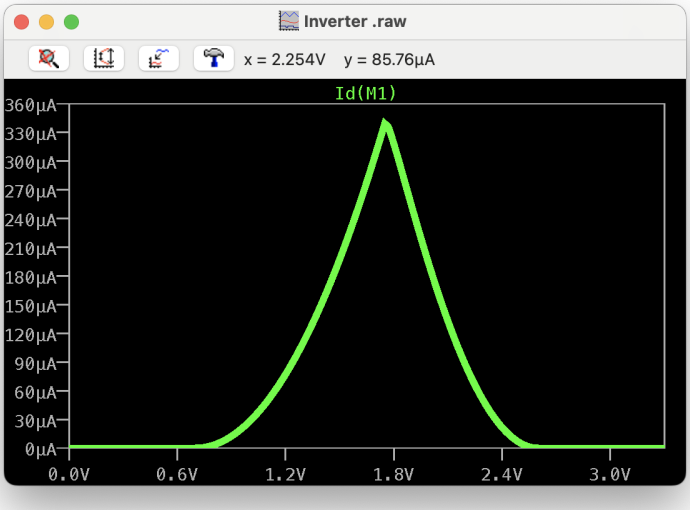
1. PMOS: width = 5 micrometer, length = 0.5 micrometer
2. NMOS: width = 1.25 micrometer, length = 0.5 micrometer

ii. Results:

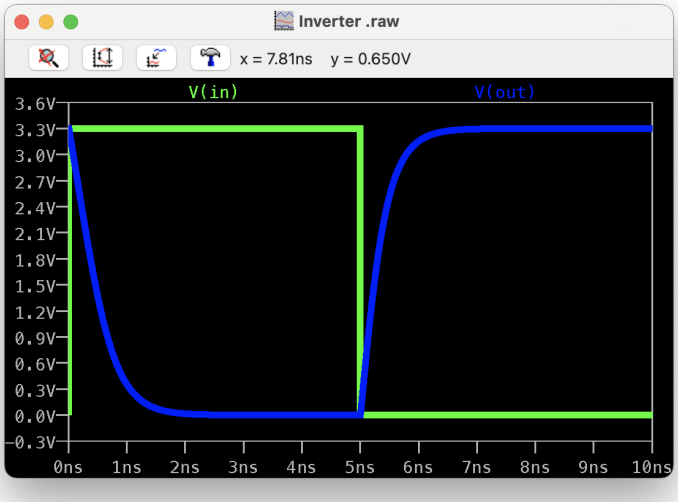
1. VTC:



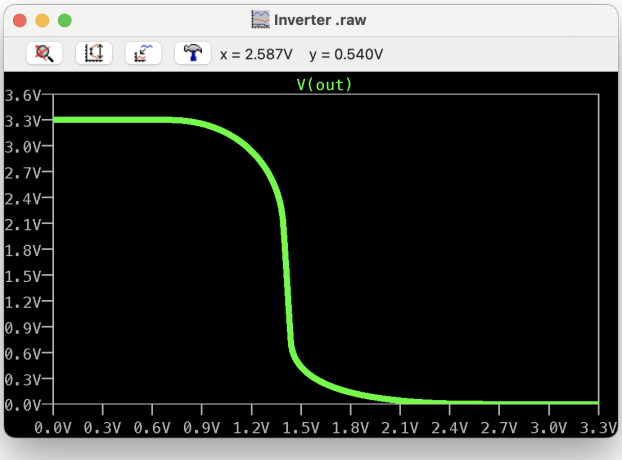
2. Supply current:



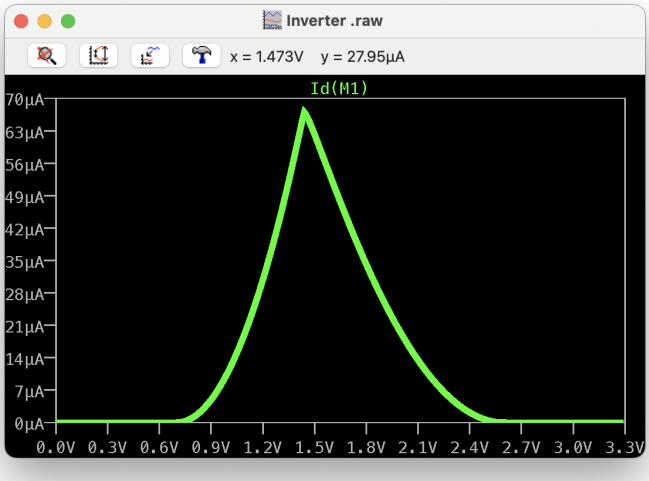
3. Transient simulation:



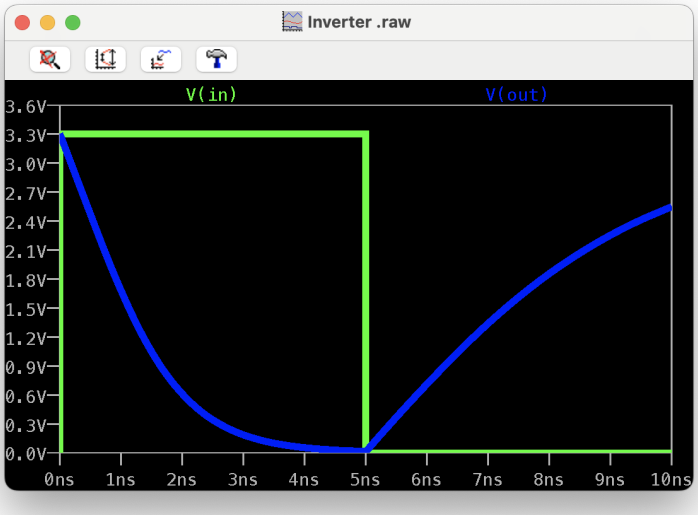
b. Minimum Area:
   i. Size of transistors:
      1. PMOS: width = 0.5 micrometer, length = 0.5 micrometer
      2. NMOS: width = 0.5 micrometer, length = 0.5 micrometer
   ii. Results:
      1. VTC:



2. Supply current:



3. Transient simulation:

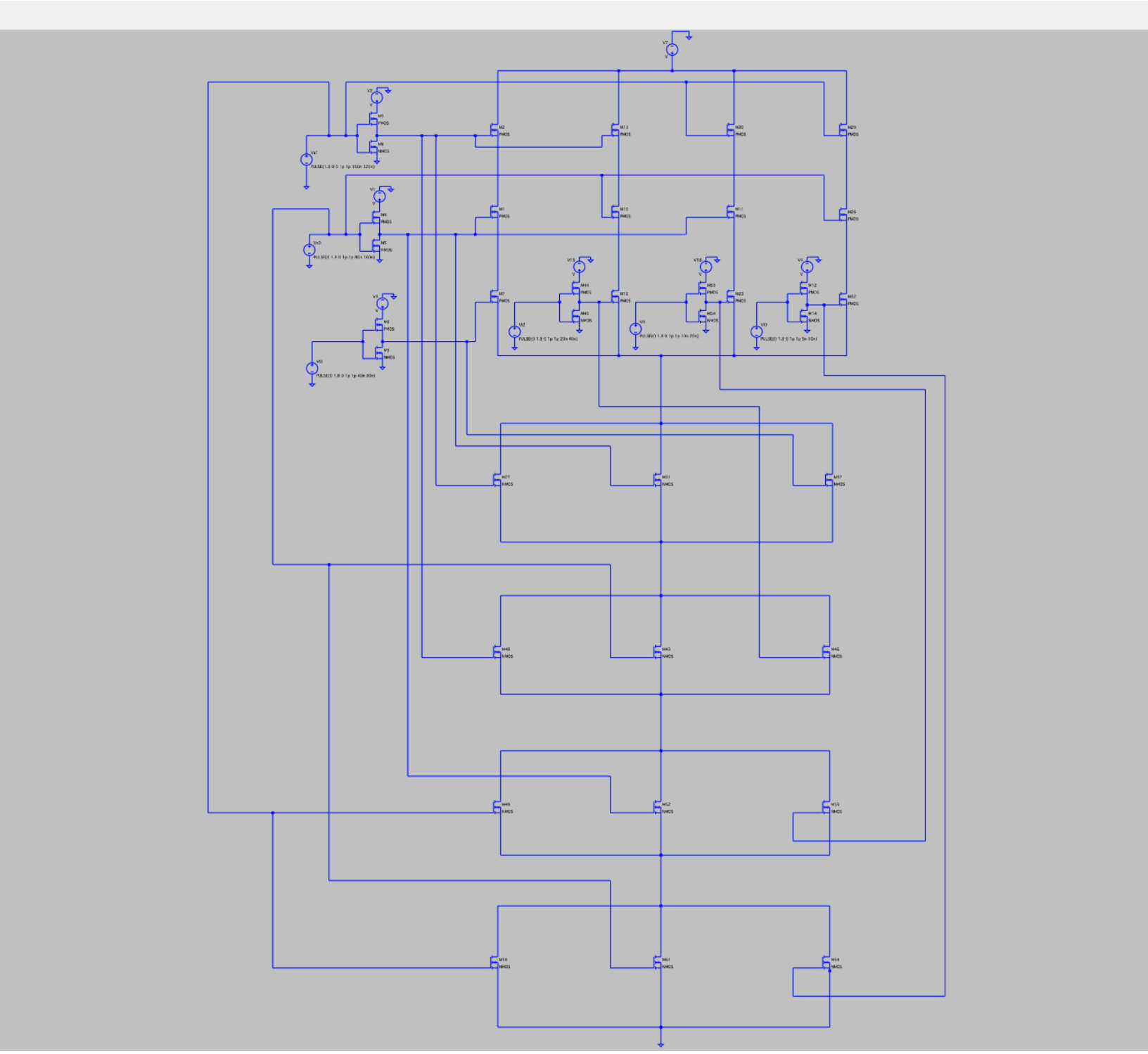


3. 4-to-1 multiplexer:

a. Number of transistors and size: For the 4-to-1 multiplexer: 24 transistors were used, along with 12 transistors for the inverters. Therefore, a total of 36 transistors were used.
Size of transistors in inverter:
PMOS: width = 1.8 micrometer, length = 0.18 micrometer

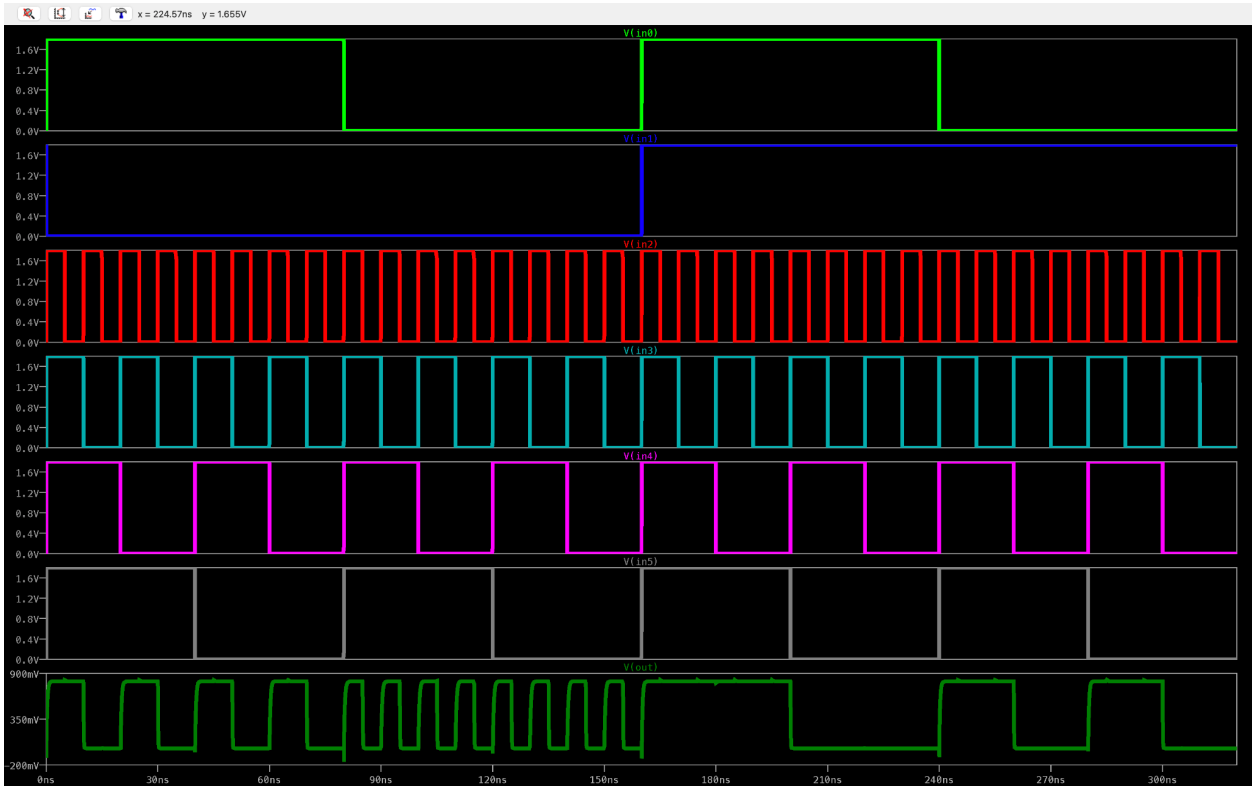
NMOS: width = 0.9 micrometer, length = 0.18 micrometer
Size of transistors in the 4-to-1 multiplexer:
PMOS: width = 5.4 micrometer, length = 0.18 micrometer
NMOS: width = 3.6 micrometer, length = 0.18 micrometer

b. Schematic:



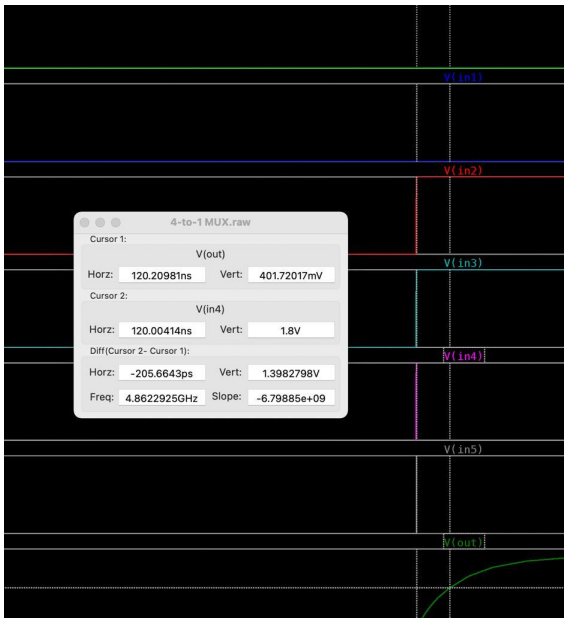
4. Test case: This test case covers achieves 100% functional coverage

a. Plots for inputs and outputs:

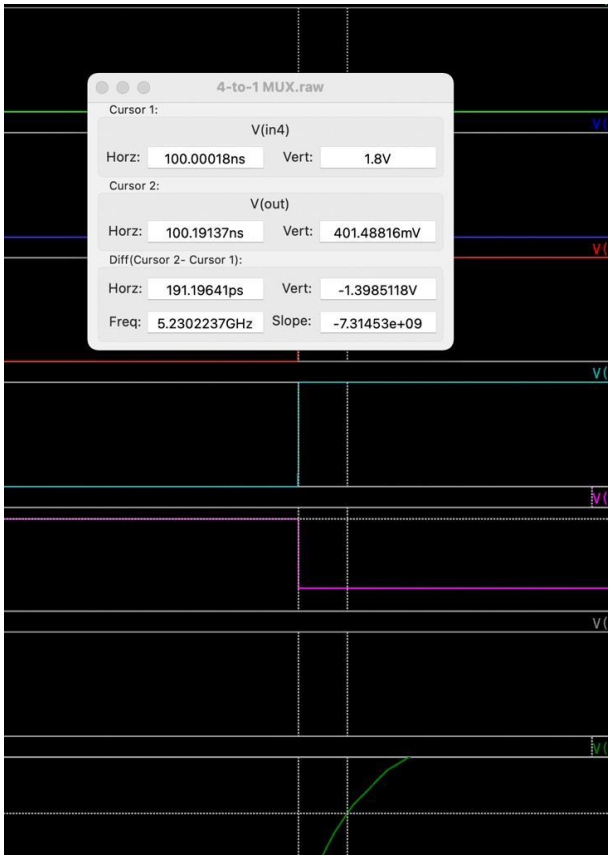


b. Propagation delay time: By using the plot of input and output and adjusting the cursor to get the delay, we have found out that:

i. T_{pLH}: 205.6643 ps (note in the screenshot it appears negative because of the cursors)



ii. T_{pHL}: 191.19641 ps



c. Power dissipation:
The first value is the average power dissipated in the 4-to-1 multiplexer, and the second value is the average power dissipated through the resistor only.

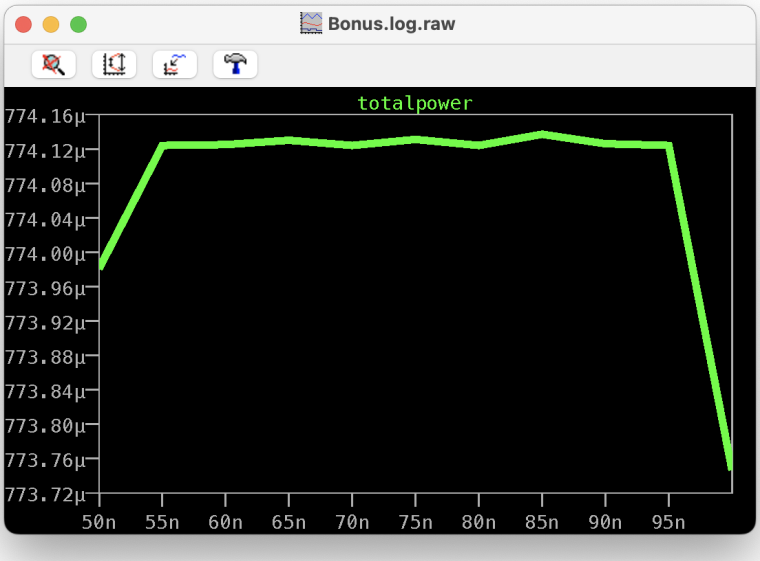
```
power: AVG(v(n001)*abs(i(vdd)))=0.000740133 FROM 0 TO 3.2e-07
power_dis: AVG(v(out)*(i(r1)))=0.000313217 FROM 0 TO 3.2e-07
```

5. Bonus Feature:

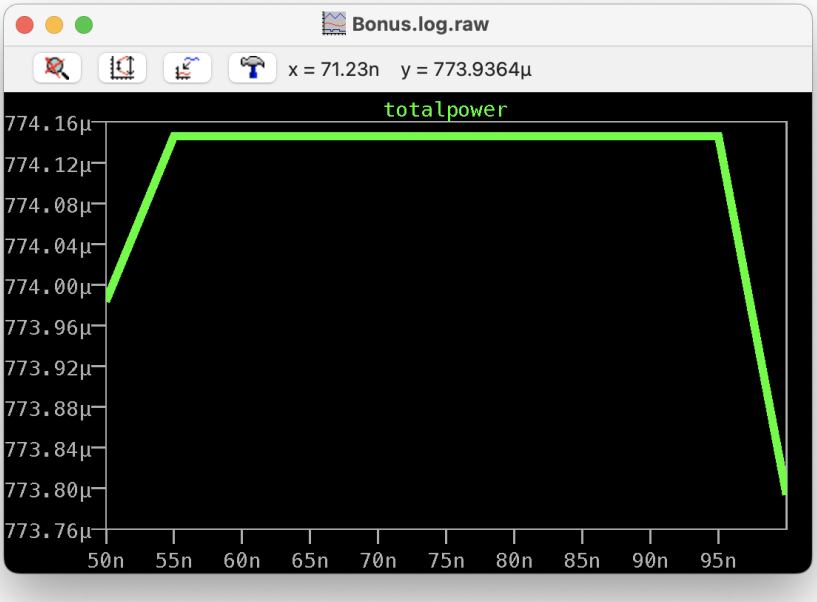
The instruction used was: .step param pWidth 50n 100n 5n.
This instruction sweeps the input from 50n to 100n with step 5n.

Explanation: At the beginning, the equivalence capacitance of the transistors gets charged. Due to the small pulse width (100n), there is not enough time for the capacitor to discharge; thus, it draws less power from the circuit, and the power dissipation will decrease.

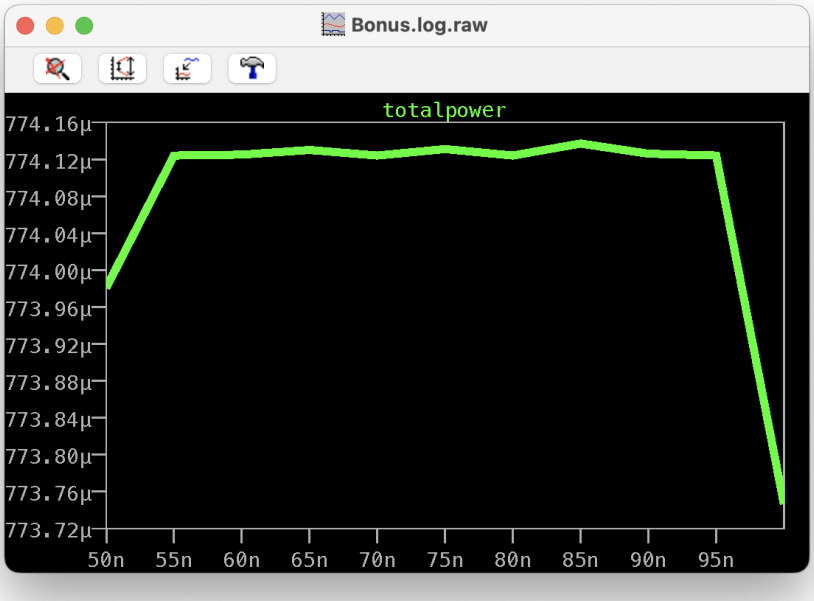
I0 swept:



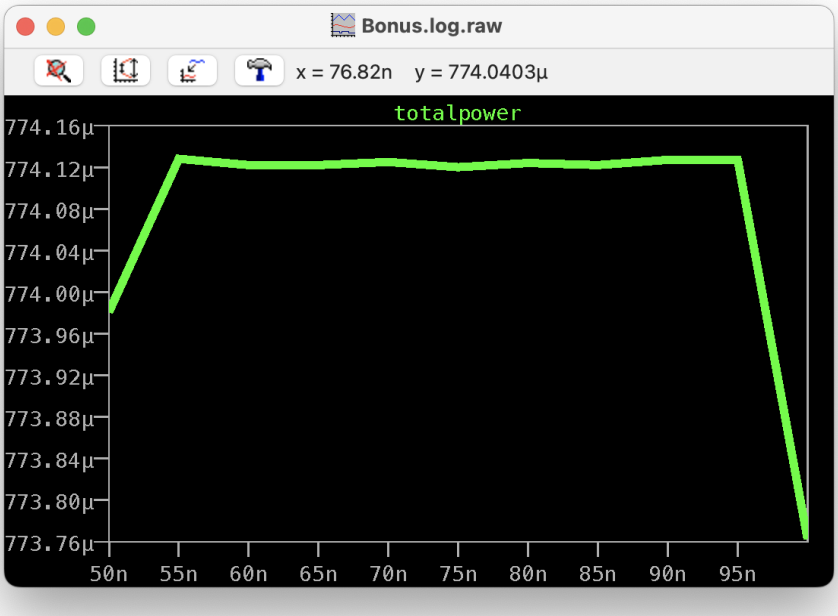
I1 swept:



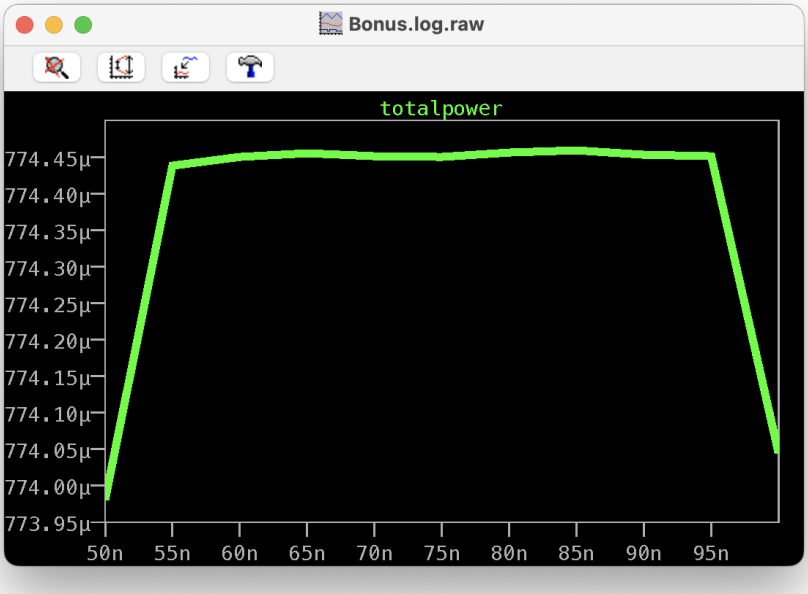
I2 swept:



I3 swept:



S0 swept:



S1 swept:

Contribution:

Merna Abdelbadie:

1. I implemented the inverter and the 4-to-1 multiplexer by calculating the areas of each transistor in both technologies (0.18 and 0.5), as well as writing the spice netlist.
2. I have done the plots needed for the project; this includes the VTC, along with the supply current and transient simulation for the inverters. Also, the plots for all inputs and output of the test case for the 4-to-1 multiplexer.
3. I have calculated the power dissipation.
4. I have implemented the bonus feature and its explanation.

Farah Fathy:

1. I calculated the propagation delay time (T_{pLH} & T_{pHL})
2. I designed the CMOS inverter and the PUN & PDN of the 4-to-1 multiplexer and implemented its schematic in LTSpice.